# Design, Analysis and Implementation of Multiphase Synchronous Buck DC-DC Converter for Transportable Processor

by

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**(ABSTRACT)**

As laptop mobile users expect more application features and long battery life, the processor current has to increase to response the demanding while the voltage has to decease to save the power loss. Therefore, it is necessary for a system designer to improve the efficiency of the voltage regulator converter (VRC) for the processor. Laptop processor architecture is more complicated than desktop because of different mode operations and their transitions. The laptop processor runs at different voltage levels for each operation mode to save the battery life. Therefore, the VRC needs to supply the correct and stable voltage to the processor. In this thesis, an analysis of power loss is derived to estimate the efficiency and switching frequency, three widely current sensing methods are discussed, two methods to compensate for the thermal resistance in loss less current sense methods are proposed, the tolerance of load line base on the component's tolerance in the converter is analyzed, the equation to estimate the output capacitance is derived, and the small signal analysis of multiphase synchronous buck converter with the droop current loop is derived.

A hardware prototype was implemented base on 4-phase synchronous buck topology to provide high efficiency and lower cost solution. The results of load line meets the Intel specification in different modes of operation, provides the best transient responses, and meets the specification during the load transient. The control loop lab measurement is also matched with the analysis and simulation.

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## Table of Content


Chapter 1 Introduction ..... 1

1.1 VRC Topology for Laptop Microprocessor ..... 3
1.2 System Overview ..... 8
1.3 Thesis Outline ..... 11
Chapter 2 System Design ..... 12

2.1 Selection of Power Stage Components ..... 12
2.1.1 Upper MOSFET Loss Analysis ..... 13
2.1.2 Lower MOSFET Loss Analysis ..... 15
2.1.3 Driver Loss ..... 16
2.1.4 Shoot Through ..... 16
2.1.5 Dead Time Diode Conduction Loss ..... 18
2.2 Optimization of Switching Frequency ..... 19
2.3 Selection of Current Sensing Methods ..... 21
2.3.1 Resistor Method ..... 21
2.3.2 DCR Method ..... 22
2.3.3 $R_{DSON}$ Method ..... 23
2.4 Thermal Compensation Methods for Loss-Less Current Sensing ..... 25
2.5 Transient Effects by DCR Sensing Method ..... 30
2.6 Load Line Tolerance Analysis ..... 31
2.7 Output Capacitor ..... 36
2.7.1 Output Capacitor Calculation ..... 36
2.7.2 Bulk Output Capacitor Selection ..... 38
2.7.3 Output Capacitor Versus Bandwidth ..... 40
2.8 Inductor Design ..... 41
Chapter 3 Control Loop Design ..... 43

3.1 DC Model ..... 43
3.2 Open Loop AC Model ..... 44
3.3 Multiphase Close Loop Model ..... 46
3.4 Compensator Design: ..... 50
3.5 Simulation Model ..... 55
Chapter 4 Experiment Results ..... 56

4.1 Application Circuit Component Value ..... 56
4.2 Load Line and Efficiency ..... 57
4.2.1 Active Mode ..... 57
4.2.2 Deep Sleep Mode ..... 59
4.2.3 Deeper Sleep Mode ..... 60
4.2.4 Efficiency versus Frequency in Active Mode ..... 61
4.2.5 Efficiency versus MOSFET ..... 62
4.2.6 Efficiency by Number of Phase ..... 63
4.3 Output Capacitor Options ..... 64
4.3.1 Option 1 ..... 65

4.3.1.1 Transient Response ..... 65
4.3.1.2 Mode Transition ..... 67
4.3.1.3 Loop Measurement Comparison ..... 69
4.3.2 Option 2 ..... 71
4.3.2.1 Transient Response ..... 71
4.3.2.2 Mode Transition ..... 73
4.3.2.3 Loop Measurement Comparison ..... 74
4.3.3 Option 3 ..... 76
4.3.3.1 Transient Response ..... 76
4.3.3.2 Mode Transition ..... 77
4.3.3.3 Control Loop Comparison ..... 78
4.4 Ceramic Capacitor Trade Off ..... 80
4.5 Time Constant Mismatch Effect Transient ..... 83
Chapter 5 Conclusion and Future Work ..... 85

## Table of Figures


Figure 1.1 Laptop Top Level Architecture ..... 2
Figure 1.2 Conventional Buck Converter ..... 4
Figure 1.3 Synchronous Buck Converter and Gate Signal Waveforms ..... 5
Figure 1.4 2-Phase Multiphase Synchronous Buck Converter ..... 6
Figure 1.5 3-phase Inductor Current Cancellation ..... 7
Figure 1.6 3-phase Input Capacitor Current ..... 7
Figure 1.7 Comparison of Traditional and IMPV Processor Voltage ..... 9
Figure 2.1 Synchronous Buck Converter ..... 12
Figure 2.2 Typical Turn on of Upper MOSFET ..... 13
Figure 2.3 Simplify Model Internal Driver and Upper MOSFET ..... 14
Figure 2.4 Switching Waveform of Lower MOSFET ..... 16
Figure 2.5 Shoot Through Waveform ..... 17
Figure 2.6 Shoot-through Model ..... 17
Figure 2.7 Power Loss Break Down of 1-phase ..... 20
Figure 2.8 Efficiency of 20A at Different Switching Frequency ..... 20
Figure 2.9 Resistor Current Sense Method ..... 21
Figure 2.10 Inductor DCR Current Sense Method ..... 22
Figure 2.11 Capacitor voltage is shown to be proportional to inductor current ..... 23
Figure 2.12 IRF7832 Normalized On-Resistance vs Temperature ..... 24
Figure 2.13 $R_{DSON}$ Current Sense ..... 24
Figure 2.14 DCR Sense Method Implementation ..... 25
Figure 2.15 Panasonic Linearity PTC ..... 26
Figure 2.16 Droop Circuitry Implementation ..... 27
Figure 2.17 Resistance Ratio vs Temperature of Panasonic NTC Thermistor ..... 28
Figure 2.18 Normalize Resistance NTC Thermistor of $\beta$ is 4000K ..... 29
Figure 2.19 Linear NTC Network ..... 30
Figure 2.20 DCR Time Constant Mismatch During Transient ..... 30
Figure 2.21 Load Line Specification ..... 31
Figure 2.22 Load Line Analysis at $40^{o}C$ ..... 35
Figure 2.23 Load Line Analysis at $105^{o}C$ ..... 35
Figure 2.24 Processor Voltage Specification During Transient ..... 36
Figure 2.25 Simplify DC Converter During Load Transit From High to Low ..... 38
Figure 2.26 Practical Capacitor Model ..... 39
Figure 2.27 Zoom In of Rising Processor Load Current ..... 39
Figure 2.28 Typical Bulk Capacitor Impedance ..... 41
Figure 3.1 Synchronous Buck Converter with Parasitic Components ..... 43
Figure 3.2 Average DC Transformer Model ..... 44
Figure 3.3 Small Signal Model ..... 45
Figure 3.4 Simplified Multiphase Synchronous Buck with Droop Current ..... 47
Figure 3.5 Block Diagram of Multiphase Buck Converter ..... 48
Figure 3.6 Close Loop Block Diagram of Multiphase Buck ..... 49
Figure 3.7 Gain Plot of Open Loop Duty to Output and Duty to Inductor Current ..... 51
Figure 3.8 Phase Plot of Open Loop Duty to Output and Duty to Inductor Current ..... 52
Figure 3.9 Gain Plot of Current and Voltage Loops ..... 52

Figure 3.10 Phase Plot of Current and Voltage Loop ..... 53
Figure 3.11 Gain of Converter Loop with Load Variation ..... 54
Figure 3.12 Phase of Converter Loop with Load Variation ..... 54
Figure 3.13 Simplis Simulation Model ..... 55
Figure 3.14 Gain and Phase Plot of Simulation Model ..... 55
Figure 4.1 Compensation Network ..... 57
Figure 4.2 Load Line in Active Mode ..... 58
Figure 4.3 Efficiency in Active Mode ..... 58
Figure 4.4 Load Line in Deep Sleep Mode ..... 59
Figure 4.5 Efficiency in Deep Sleep Mode ..... 60
Figure 4.6 Load Line in Deeper Sleep Mode ..... 61
Figure 4.7 Efficiency in Deeper Sleep Mode ..... 61
Figure 4.8 Efficiency vs. Frequency at 19V ..... 62
Figure 4.9 MOSFET Efficiency Comparison ..... 63
Figure 4.10 Efficiency vs. Number of Phase ..... 64
Figure 4.11 Transient Response of Option 1 ..... 65
Figure 4.12 Zoom In of Load Current Rising Edge of Option 1 ..... 65
Figure 4.13 Zoom In of Load Current Falling Edge of Option 1 ..... 66
Figure 4.14 Geyserville Transition of Option 1 ..... 68
Figure 4.15 C4 Transition of Option 1 ..... 68
Figure 4.16 Gain and Phase of Overall System Loop Measurement of Option 1 ..... 69
Figure 4.17 Gain Plot of Analysis Model of Option 1 ..... 70
Figure 4.18 Phase Plot of Analysis Model of Option 1 ..... 70
Figure 4.19 Gain and Phase Plot of Simulation of Option 1 ..... 71
Figure 4.20 Transient Response of Option 2 ..... 71
Figure 4.21 Zoom In of Load Current Rising Edge of Option 2 ..... 72
Figure 4.22 Zoom In of Load Current Rising Edge of Option 2 ..... 72
Figure 4.23 Geyserville Transition of Option 2 ..... 73
Figure 4.24 C4 Transition of Option 2 ..... 73
Figure 4.25 Gain and Phase of Overall System Loop Measurement of Option 2 ..... 74
Figure 4.26 Gain Plot of Analysis Model of Option 2 ..... 74
Figure 4.27 Phase Plot of Analysis of Option 2 ..... 75
Figure 4.28 Gain and Phase Plot of Simulation of Option 2 ..... 75
Figure 4.29 Transient of Option 3 ..... 76
Figure 4.30 Zoom In Rising Edge Transient of Option 3 ..... 76
Figure 4.31 Zoom In Falling Edge Transient of Option 3 ..... 77
Figure 4.32 Gyserville Transition of Option 3 ..... 77
Figure 4.33 C4 Transition of Option 3 ..... 78
Figure 4.34 Gain and Phase of Overall System Loop Measurement of Option 3 ..... 78
Figure 4.35 Gain Plot of Analysis Model of Option 3 ..... 79
Figure 4.36 Phase Plot of Analysis Model of Option 3 ..... 79
Figure 4.37 Gain and Phase Plot of Simulation of Option 3 ..... 80
Figure 4.38 Transient Response of 5 x 2R5TPD680M5 ..... 81
Figure 4.39 Zoom in Rising Edge of Transient Response of 5 x 2R5TPD680M5 ..... 81
Figure 4.40 Transient Response of 5 x 2R5TPD680M5 and 20 x 22uF Ceramic ..... 82
Figure 4.41 Transient Response of 5 x 2R5TPD680M5 and 20 x 22uF Ceramic ..... 82

Figure 4.42 RC Time Constant Same as L/R..... 83
Figure 4.43 RC Time Constant Greater than 15% of L/R ..... 84
Figure 4.44 RC Time Constant Less than 15% of L/R..... 84
Figure 5.1 One and Two Stages Efficiency Solutions Comparison..... 88

## Chapter 1 Introduction

Today, with convenience and satisfactory performance, laptop computers are gaining more popularity than their desktop counterpart, and thus there is an increasing need of efficient processing for the amount of power from battery or ac adaptor to the processor. As laptop computers continue improving their performance, the power dissipation also increases which can cause complex thermal management problems in laptop. Although the power of laptop processor is specified in low power range, it can generate a lot of heat dissipation. At a result, laptops can burn mobile user's thigh and reduce the battery life if system designer is not careful in designing and optimizing the VRC for processor. The microprocessor is the heart of any computer, whether it is a desktop, server or laptop. Today, the market for laptop computers is divided into the Portability segment and the Mobility segment. The Mobility segment offers users who want extra freedom from ac adapter and runs from low power processor to extend the battery life. The Mobility segment includes thin and light notebook, mini and sub-notebook. Thin and light notebook such as Intel Centrino$^{TM}$ combines the highest processor performance with the system designs that emphasize mobility. This category of notebooks is weighing less than 5.5lbs and less than 1 inch of thickness. The Portability segment offers users who want the best performance, along with desktop-like features such as larger screens, full size keyboards and intensive multimedia applications such as video, gaming, music and so on. The users are willing to compromise on weight and battery life in exchange for features and performance. This category laptop intends to use ac adapter most of time and occasionally move the laptops from location to location. Figure 1.1 shows a top level of

laptop architecture. This thesis focuses on design, analysis and implementation of a VRC for processor in Portability segment.

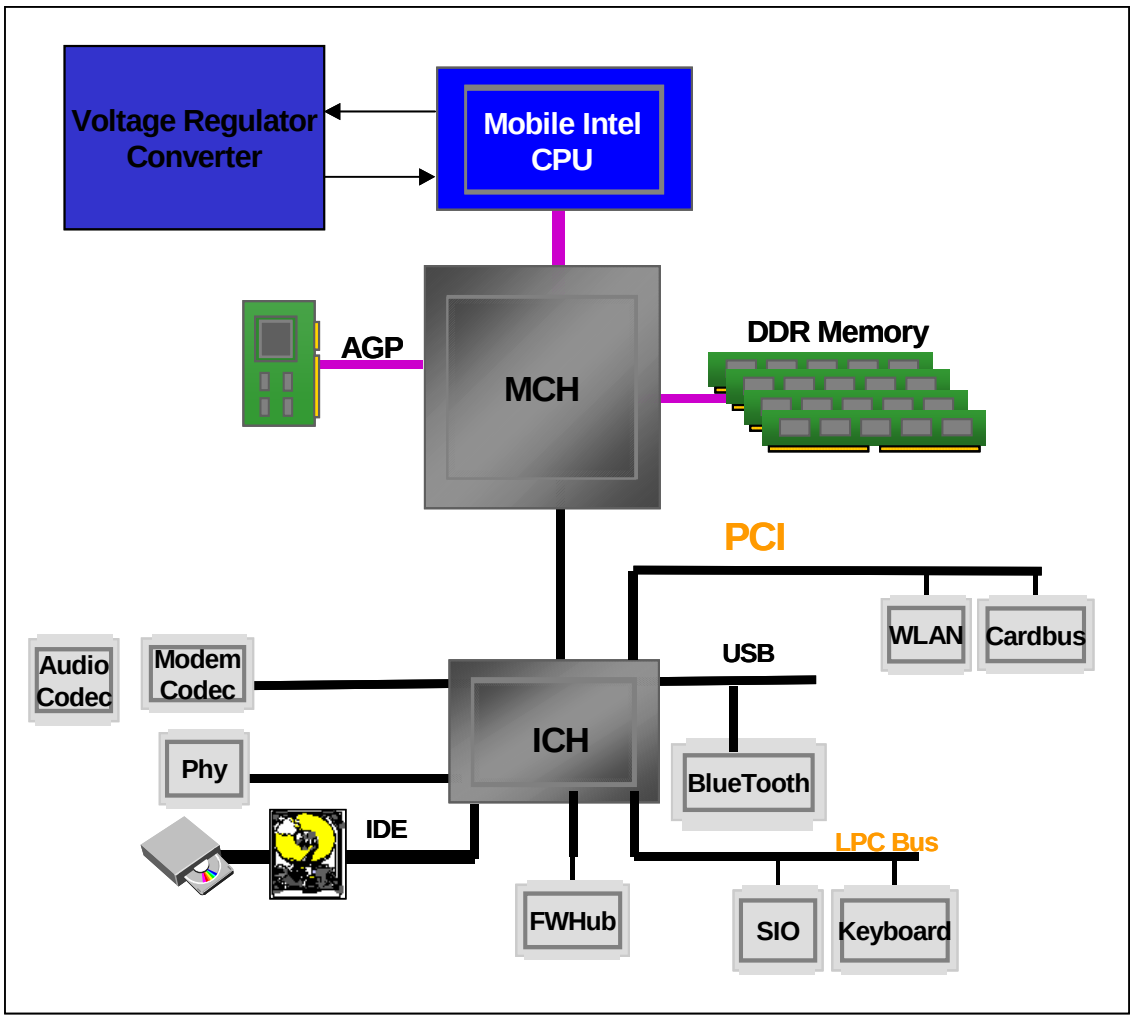



Figure 1.1 Laptop Top Level Architecture

In recent years, there has been numerous works of voltage regulator for computer processors [1-4]. However, these works have been focused on optimizing the voltage regulator to achieve adaptive voltage position (AVP) during the load transient. The initial output voltage drop during the load transient was not carefully planned to meet the specifications. In this thesis, the design and analysis of VRC to meet both static and transient load line voltage tolerance specifications are discussed. An insight of overall

system loop, which combines the voltage and active droop current loops, is analyzed to determine the system stability and verified by experimental results. The compensation network is also optimized to meet both load transient and reference voltage change. The minimum output capacitance along with equivalent series resistance of the VRC is derived to meet the load line specifications during the load transient and to provide low cost solution.

### 1.1 VRC Topology for Laptop Microprocessor

In general, the source to power the laptops is either from battery or ac adapter. Other types of power source, such as fuel cell and solid states [5], are still in research and development stage. Intel expects a full charged laptop to be last 8 hours without ac adapter by 2006. Presently, fuel cell in combination with Lithium-Polymer provides the highest potential to replace the rechargeable battery because of lifetime usage of the fuel cell. The rechargeable battery, such as Lithium Ion, typically includes two cells in parallel and then stacking up to four times (2P4S). The voltage of battery varies from 10.8V(2P3S) to 14.4V(2P4S). The voltage of ac adapter, which is called brick in industry, converts from 120V ac to 19V to 21V dc. Currently, the supply voltage to microprocessor is in the range of 0.8V to 1.6V. According to the Intel roadmap, the voltage will be reduced by 0.6 faction of each generation of processor. To convert voltage either from battery or ac adapter, buck converter topology has been widely used for microprocessors in the industry because it reduces the overall system cost and shortens the design cycle to meet the market window time. The majority of VRC for laptop processor today are using synchronous rectification instead of conventional buck.

Figure 1.2 shows power stage of the conventional buck converter. The metal oxide semiconductor field effect transistor (MOSFET) $S_1$ is to transfer the energy from input to output. After $S_1$ is off, the diode $D_1$ conducts so that the energy of inductor can be discharged. The output voltage is regulated by a control loop to determine the on time of $S_1$. The disadvantage of conventional buck converter is the significant power loss during the diode $D_1$ conduction period, which is the product of the forward voltage drop and its current.

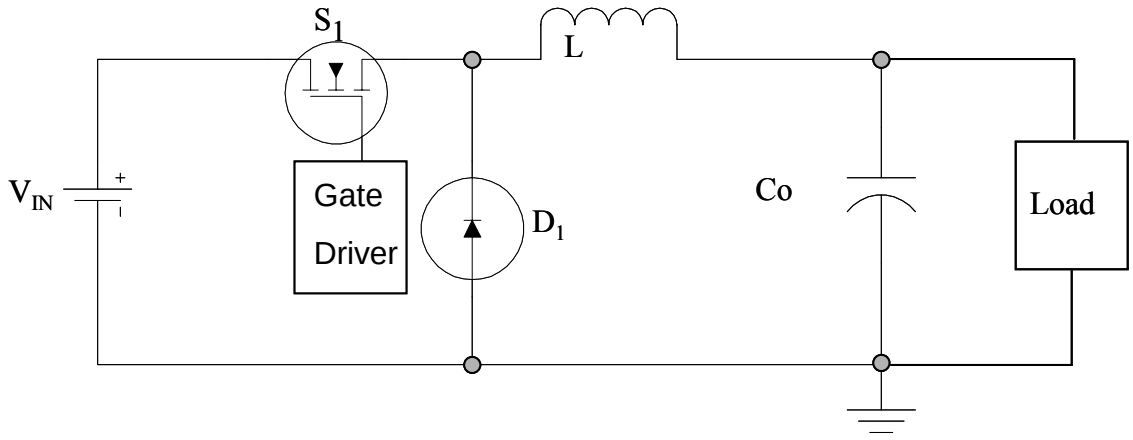



Figure 1.2 Conventional Buck Converter

As shown in Figure 1.3, by replacing the diode with MOSFET $S_2$, the conventional buck is converted to synchronous buck topology. The ideal gate signal waveforms of $S_1$ and $S_2$ are also shown in Figure 1.3. The dead-times between $S_1$ and $S_2$ are used to prevent the shoot-through. During the dead time, the inductor current continues flowing through internal body diode of $S_2$. When the gate signal of $S_2$ is high, the inductor current flows through $S_2$. Synchronous buck topology provides better efficiency than standard buck

converter because the on-resistance $R_{DSON}$ of $S_2$ is in the milliohm range during $S_2$ on time interval.

With technology progressing, laptop buyers expect the use of audio, video and other applications increases. Therefore, the mobile processing power has become more important than ever. As mention earlier, the laptop processor demands more current as the performances compete to its desktop rivalry. To handle such high current processors, the industry had adopted the multiphase synchronous buck topology. Figure 1.4 shows an example of two-phase synchronous buck converter.

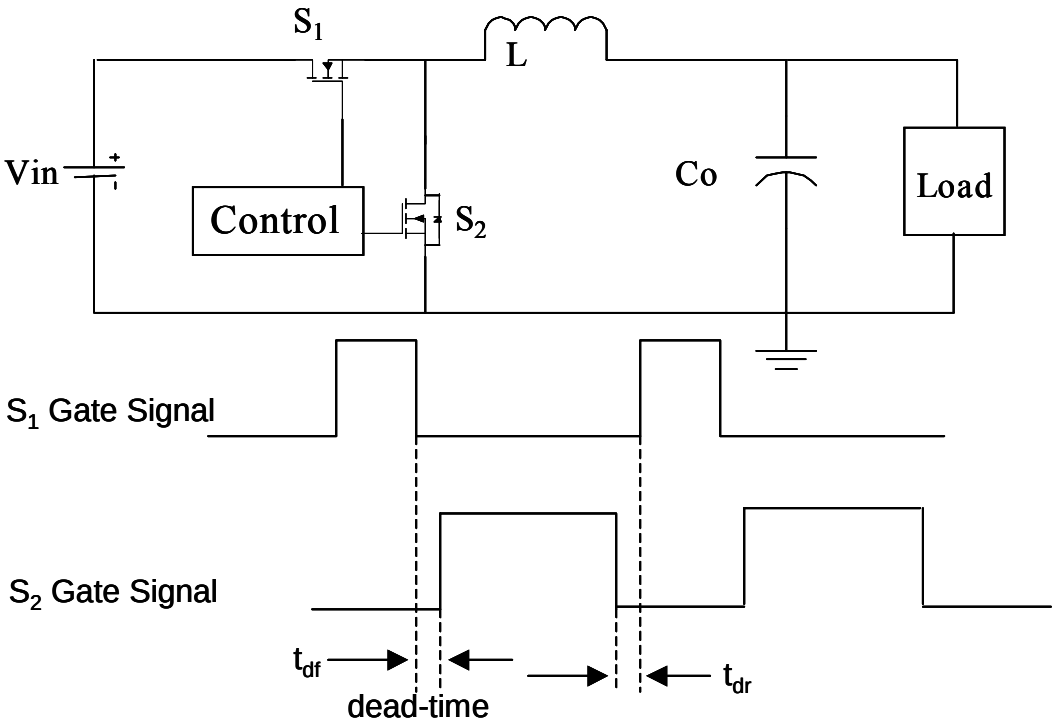



Figure 1.3 Synchronous Buck Converter and Gate Signal Waveforms

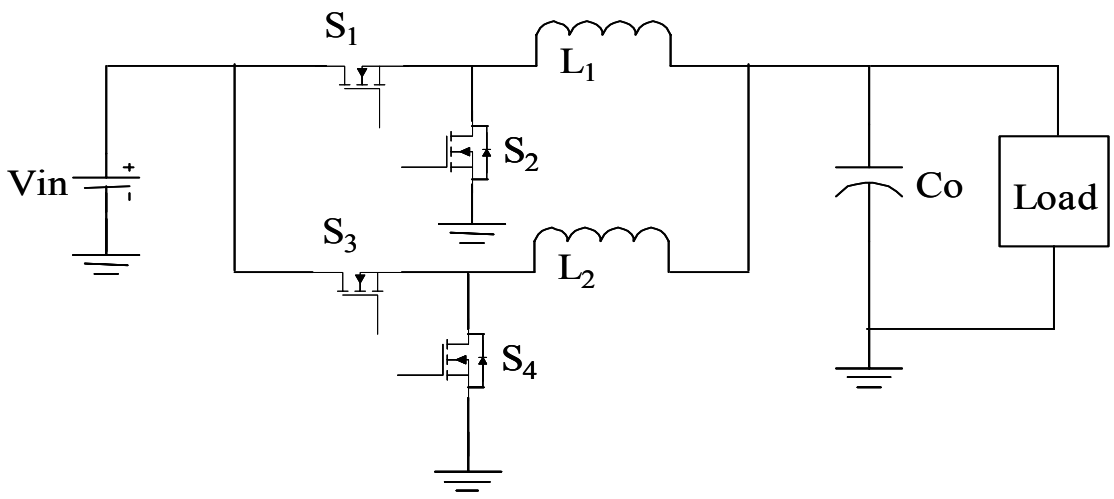



Figure 1.4 2-Phase Multiphase Synchronous Buck Converter

Multiphase buck converter architecture use interleaved timing to multiply ripple frequency to reduce the input and output currents. Figure 1.5 shows an example of 3-phase ripple cancellation of inductor current. The total ripple of inductor current has smaller magnitude and three times ripple frequency than individual channel. The advantages of output inductor current ripple cancellation result in lower cost of output capacitors, few components and reduced the power dissipation. Equation 1.1.1 shows the formula of inductor current for individual phase.

$$Ipp = \frac{(V_{IN} - V_{CC}) \cdot V_{CC}}{L \cdot fs \cdot V_{IN}} \qquad (1.1.1)$$

Where, $V_{IN}$ and $V_{CC}$ are the input and output voltages, respectively. L is inductor value per phase; and $f_S$ is switching frequency per phase. Reference [6] shows an equation and graphical to calculate the total output current ripple.

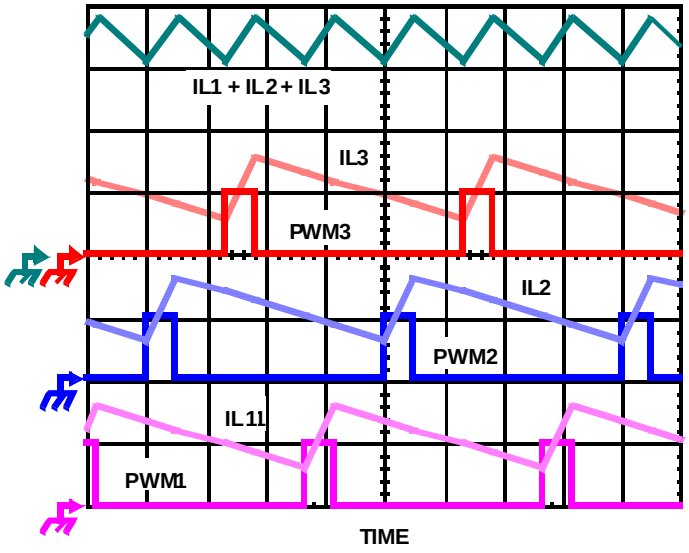



Figure 1.5 3-phase Inductor Current Cancellation

Another benefit of multiphase buck converter is the reduced input ripple current by increases the input ripple current frequency. This benefit results in smaller input capacitor and lowers overall system cost, and thus saving the board area. Figure 1.6 shows input current reduction for 3-phase converter.

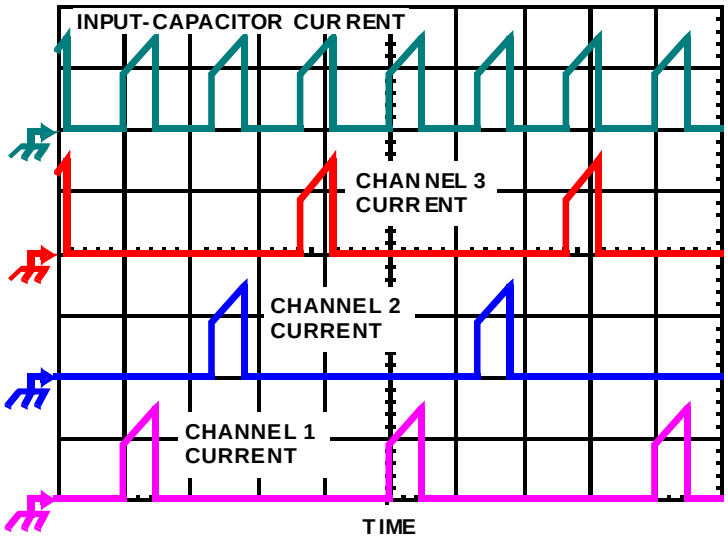



Figure 1.6 3-phase Input Capacitor Current

Equations 1.1.2a and 1.1.2b show the calculation formula of root mean square (RMS) current per phase. Equation 1.1.4 shows the total RMS input current. Reference [6] shows graphical solution to determine the input capacitor RMS current base on the load current, duty cycle and number of phase.

$$RMS = \sqrt{\frac{1}{T}\int_0^T f^2(t)dt} \qquad (1.1.2a)$$

$$I_{RMS} \approx I\sqrt{D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta I}{I}\right)^2} \qquad (1.1.2b)$$

$$I_{RMS} \approx I\sqrt{D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta I}{I}\right)^2}\cdot\sqrt{N\Phi} \qquad (1.1.3)$$

Reference [7] is proposed the multiphase coupled-buck converter, which increases the duty cycle to improve the efficiency. The industry has not adopted this topology because of the complexity of magnetic components. Recently, a 2-stage synchronous buck converter was introduced for higher efficiency [8-9]. This solution is briefly explored and compared the efficiency with one stage solution. The results efficiency data are shown in the Chapter 5.

**1.2 System Overview**

During any mode operation of laptop, a VRC needs to supply the correct voltage and current to the processor. Most laptops now use Voltage Identification (VID) programmable voltage to allow the processor to program the reference voltage of dc/dc converter. Because of converter tolerance and varying current drawn from processor, Intel specifies the tolerance for the processor voltage. In 1999, Intel introduced the first Intel Mobile Voltage Position Technology (IMVP) on Pentium III processor. The advantage of IMVP is to reduce the processor power by dynamically adjust the processor

voltage base on the processor activity states since processor power is proportional to the square of the processor voltage.

Another feature of IMVP is to reduce the output capacitors, which has the highest potential cost in dc/dc converter that reduce the overall of system cost. Figure 1.7 shows the difference between traditional processor voltage regulator and IMPV voltage regulator.

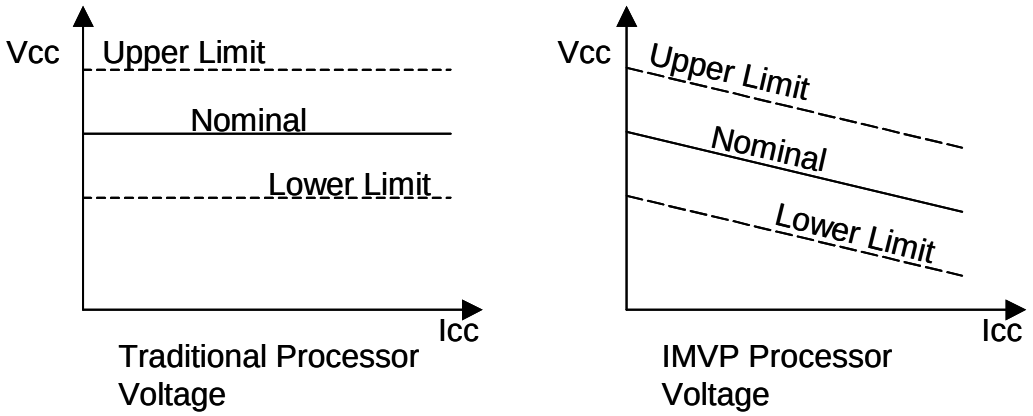



Figure 1.7 Comparison of Traditional and IMPV Processor Voltage

A numerical example below demonstrates the benefit of IMVP on reducing processor power over the traditional voltage regulator.

$$P_T = \frac{(V_T)^2}{R} \qquad (1.2.1a)$$

$$P_{IMPV} = \frac{(V_{IMPV})^2}{R} \qquad (1.2.1b)$$

$$P_{IMPV} = P_T \cdot \frac{(V_{IMPV})^2}{(V_T)^2} \qquad (1.2.1c)$$

Where $P_T$ is traditional power, $V_T$ is traditional voltage, $P_{IMPV}$ IMPV power, $V_{IMPV}$ is IMPV voltage and R is processor load.

Let us consider a numerical example:

For $P_T$ = 100W when $V_T$ = 1.4V with $V_{IMPV}$ = 1.3V, $P_{IMPV}$ = 86.2W.

Percentage of IMPV processor save = ($P_T$ - $V_{IMPV}$)/ $P_T$ = 13.8%

Today, the Intel Mobile Pentium processor supports the Enhanced Intel SpeedStep™ Technology. This feature allows the processor to change the voltage and clock frequency between two performance modes. The two modes are the Maximum Performance mode, which runs at highest CPU frequency and high VID, and the Battery Optimization Performance mode that runs at lowest CPU frequency mode and lower VID. To further improve the battery life, Intel includes Deep Sleep and Deeper Sleep modes in the Mobile Pentium processor. Deeper Sleep mode operates at very low voltage when at low power state.

General Design Specification of Intel Mobile Pentium Processor:

- Input Voltage, $V_{IN}$: 12V to 19V
- VID: 1.325V
- Deep Sleep Voltage: -1.7% of VID
- Deeper Sleep Voltage: 0.8V
- Maximum Output Current: 80A
- Maximum Deep Sleep Current: 24A
- Maximum Deeper Sleep Current: 6A
- Load Line Tolerance: +/-25mV (5mV ripple voltage)
- Load Line Slope: 1.3m Ohm/A

### 1.3 Thesis Outline

This thesis focuses on the design, analysis, and implementation of multiphase synchronous buck converter for the high-end laptops that is desktop-like features.

Chapter II describes different factors that affect the overall efficiency, optimize the switching frequency, methods of current sense, time constant mismatch in direct current resistor (DCR) current sense method, thermal compensate for loss less current sense methods, stack up analysis of load line and calculation of the minimum capacitors to reduce the cost.

Chapter III describes the dc analysis, open loop small signal analysis and close loop small signal analysis of multiphase synchronous buck converter. The system voltage loop, current loop and reference to output transfer functions are derived. The compensation network is also optimized to provide the best result.

Chapter IV shows load line and efficiency in Active, Deep Sleep and Deeper Sleep modes, efficiency at different switching frequencies and efficiency of different number of phases. Three options of output capacitors are evaluated. The converter loop gain and phase margin are compare between laboratory measurement and analysis. The effect of mismatch time constant of DCR method during the transient is presented.

Chapter V draws the conclusion of this work, discusses the possible of the future work and comparison the efficiency between one and two stage at high current laptop.

## Chapter 2 System Design

### 2.1 Selection of Power Stage Components

With recent advancement in power MOSFET technology, the process of selecting the optimum MOSFET can be lengthy time. The MOSFETs have to meets all the system requirements and provide the lowest cost. The factors of system effect the decision of MOSFET base on:

a. Maximum processor current $I_{CC}$, nominal processor voltage $V_{CC}$ at High Frequency Mode HFM. Those will effect the power dissipation.

b. Switching frequency $f_S$ contributes the power dissipation when turn on, off and on time.

c. Maximum allowable temperature on the case of MOSFET in enclose environment of laptop.

d. Figure of Merit (FOM) of $R_{DSON}$ and gate charge.

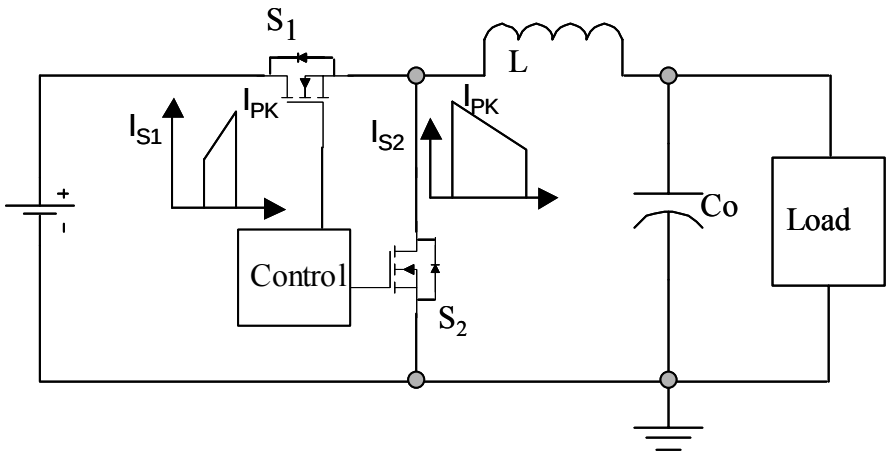



Figure 2.1 Synchronous Buck Converter

Figure 2.1 is shown synchronous buck converter again for convenient.

### 2.1.1 Upper MOSFET Loss Analysis

The power losses of upper MOSFET $S_1$ include switching, conduction and reverse recovery loss of bottom MOSFET $S_2$. Since the on-time $t_{on}$ of $S_1$ is relatively short (7.4% when $V_{IN}$ is 19V), this leads to small conduction loss. Therefore, the majority of power loss of $S_1$ comes from switching loss.

a. Conduction Loss:

From Figure 2.1, the power loss of conduction can be estimate:

$$P_C = (I_{RMS})^2 \cdot R_{DSON} \cdot t_{on} \qquad (2.1.1)$$

b. Switching Loss:

Figure 2.2 shows typical turn-on waveforms of the upper MOSFET. The turn-off waveforms are qualitatively similar with the charge axis reversed.

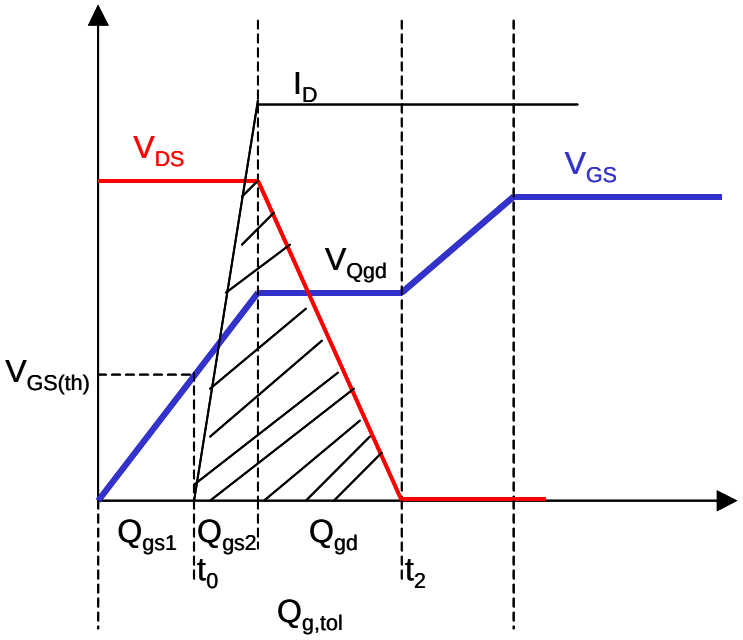



Figure 2.2 Typical Turn on of Upper MOSFET

For simple analysis, the energy of loss during turn on or off can be estimate by the area of current and voltage of $S_1$. Therefore, the average power loss of switching can be calculated:

$$Won = \frac{1}{2} \cdot V_{DS} \cdot I_D \cdot (t_2 - t_0) \qquad (2.1.2)$$

$$Psw = Won \cdot fs = \frac{V_{IN} \cdot I_{PK}}{2} \cdot fs \cdot \frac{(Q_{gs2} + Q_{gd})}{Ig} \qquad (2.1.3)$$

$I_g$ is gate driver current that charges the gate-to-source and gate-to-drain capacitances of $S_1$. Figure 2.3 shows a typical representation internal of driver and $S_1$. $R_{pu}$ and $R_{pd}$ are representing the pull up and pull down resistor of driver during rising and falling of $S_1$, respectively. $R_{pcb}$ is resistance of print circuit board, and $R_g$ is the internal gate resistance of $S_1$. $C_{gs}$, $C_{gd}$ and $C_{ds}$ are gate-to-source capacitance, gate-to-drain miller capacitance, and output capacitance of $S_1$, respectively.

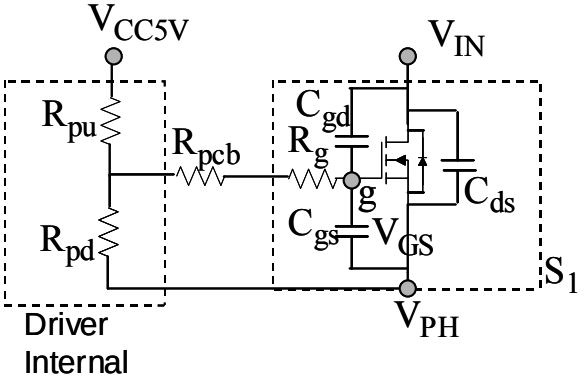



Figure 2.3 Simplify Model Internal Driver and Upper MOSFET

$I_g$ can be derived by using Ohm's law with an approximating $V_{Qgd}$ at node g. $V_{Qgd}$ can be easily found from MOSFET's datasheet on the graph of gate charge versus gate to source voltage. $I_{g\_rise}$ and $I_{g\_fall}$ are the currents during turn-on and turn-off periods.

$$I_{g\_rise} = \frac{V_{CC5V} - V_{Qgd}}{R_{pu} + R_{pcb} + R_g} \qquad 2.1.4a$$

$$I_{g\_fall} = \frac{V_{Qgd}}{R_{pu} + R_{pcb} + R_g} \qquad 2.1.4b$$

The total switching power loss can be found as below:

$$P_{SW} = \frac{V_{IN} \cdot I_{PK}}{2} \cdot f_s \cdot (Q_{gs2} + Q_{gd}) \cdot \left( \frac{1}{I_{g\_rise}} + \frac{1}{I_{g\_fall}} \right) \qquad (2.1.5)$$

c. Reverse Recovery Loss:

Because of the inductor current flows through body diode of $S_2$ during dead time, some amount of minority charge stores in the diode. When the upper MOSFET $S_1$ turns on, $S_1$ will carry extra current to remove most of the diode stored minority charge. This extra current can induce the switching loss of $S_1$. The power loss of reverse recovery of body diode can be estimated:

$$P_{rr} = V_{IN} \cdot Q_{rr} \cdot f_s \qquad (2.1.6)$$

Where $Q_{rr}$ is recovery charge of bottom MOSFET $S_2$. $Q_{rr}$ can be found in the MOSFET's datasheet.

d. MOSFET Output Capacitor Loss:

The power loss of MOSFET output capacitor can be calculated:

$$P_{Coss} = \frac{V_{IN}^2 \cdot C_{oss} \cdot f_s}{2} \qquad (2.1.7)$$

Where $C_{oss}$ can be found in the MOSFET's datasheet.

### 2.1.2 Lower MOSFET Loss Analysis

The conduction loss is the most contributing factor of the total power loss for synchronous MOSFET $S_2$. The switching loss of $S_2$ is negligible because it has almost zero-voltage switching during turn-on and turn-off due to the conduction of its body diode. The conduction loss of $S_2$ can be estimated:

$$P_C = (I_{RMS})^2 \cdot R_{DS(ON)} \cdot t_{off} \qquad (2.1.8)$$

Figure 2.4 shows typical turn-on switching waveforms of $S_2$ to show why the switching loss is negligible.

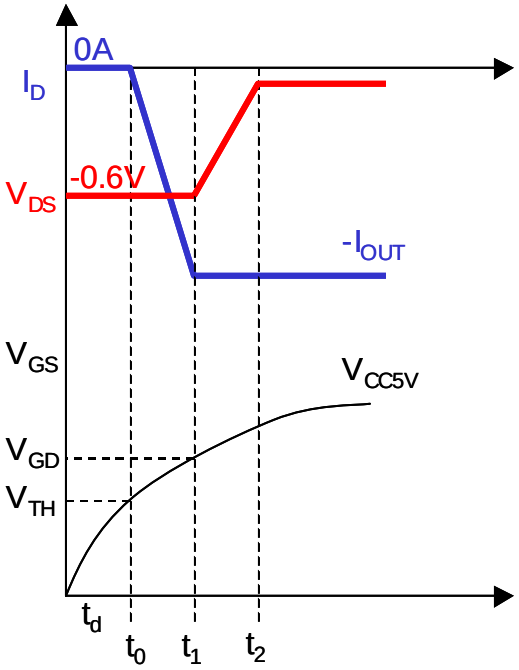



Figure 2.4 Switching Waveform of Lower MOSFET

The switching power loss of lower MOSFET can be calculated in similar method as upper MOSFET.

### 2.1.3 Driver Loss

From Figure 2.2, the driver power loss of upper or lower MOSFET can be estimate:

$$P_G = \frac{1}{Ts} \cdot \int_0^{Ts} V_{GS} \cdot Ig \cdot dt = fs \cdot V_{GS} \cdot \int_0^{Ts} Ig \cdot dt \qquad (2.1.9)$$

$$P_G = fs \cdot V_{GS} \cdot Q_{g,\,tol} \qquad (2.1.10)$$

### 2.1.4 Shoot Through

Shoot-through is another factor that system engineer has to pay attention when choosing the MOSFETs. It reduces the overall system efficiency and reliability. The symptoms of

shoot-through can be seen in higher temperature of the MOSFETs especially $S_1$ and more parasitic ringing at the phase node. Figure 2.5 shows an example of shoot-through during $S_1$ turning on and $S_2$ turning off.

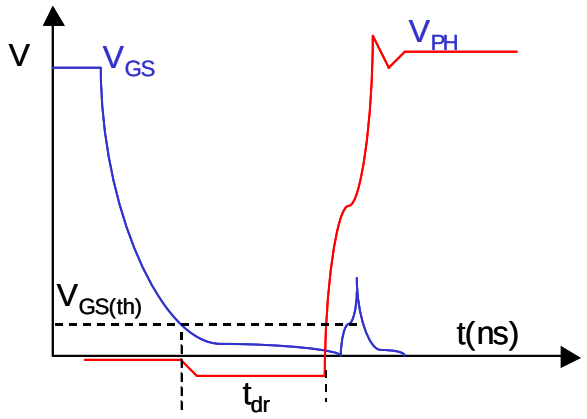



Figure 2.5 Shoot Through Waveform

If $V_{GS}$ of $S_2$ is above the $V_{GS(th)}$ threshold during the rising edge of phase node, $S_2$ will turn on and creates a short path within milliohm resistance range from $V_{IN}$ to ground. As a result, this shoot-through current diminishes the system efficiency and creates the thermal issue for $S_1$ and $S_2$. In Figure 2.6, $S_2$ is replaced with an equivalent circuit to assist understanding the shoot-through and to calculate the $V_{GS}$ during $S_1$ turn-on. $R_{pd}$ is pull-down resistor of gate driver when $S_2$ is off. By writing the node equation at g and solve the differential equation, $V_{gs}$ can be found as below:

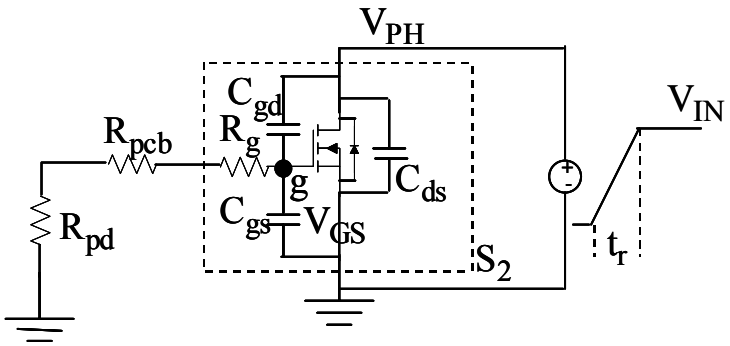



Figure 2.6 Shoot-through Model

$$C_{gd}\frac{d(V_{PH}-V_{GS})}{dt}=C_{gs}\frac{dV_{GS}}{dt}+\frac{V_{GS}}{Rt} \qquad (2.1.11)$$

$$V_{GS}=Rt\cdot Cgd\cdot\frac{Vin}{tr}\cdot\left(1-e^{\frac{-tr}{Rt\cdot(Cgd+Cgs)}}\right) \qquad (2.1.12)$$

$R_t$ is total resistance of $R_{pd}$, $R_{pcb}$ and $R_g$. Equation 2.1.12 is valid during the $t_r$. In the real application, $t_r$ is much less than $R_t*(C_{gd}+C_{gs})$. Therefore, equation 2.1.12 can be simplified:

$$V_{GS}=Cgd\cdot\frac{Vin}{(Cgd+Cgs)} \qquad (2.1.13)$$

To prevent the shoot-through, $V_{GS}$ in equation 2.1.13 has to be less than $V_{GS(th)}$. In reference [10], the author discussed a few options that prevent the shoot-through. Slow down the rise time of upper MOSFET is not practical solution because this method creates higher switching loss for upper MOSFET.

### 2.1.5 Dead Time Diode Conduction Loss

Diode conduction time is when both upper and lower MOSFET are turned off. The diode can be either lower MOSFET body diode or Shottky diode. Schottky diode can be used to improve the efficiency. The disadvantage of using Schottky diode is added more cost to the system. The power loss during the dead time can be found:

$$P_D=V_F\cdot I_{CC}\cdot f_S\cdot(t_{dr}+t_{df}) \qquad 2.1.14$$

The dead time, $t_{dr}$ or $t_{df}$, depends on how the driver controls the MOSFET gate drives. The driver includes either fixed amount of delay or adaptive shoot-through circuitry that monitors the gate to source voltage of one gate signal to make sure that it is below the threshold before turning on other gate signal to avoid the shoot-through. Another part of

delay is the time that takes the gate to source voltage reach to the MOSFET's threshold. This time can be calculated from Figure 2.2 as below:

$$t_0 = \frac{Qgs1}{Ig} \qquad 2.1.15$$

**2.2 Optimization of Switching Frequency**

Switching frequency in the VRC for laptop processor is a very critical factor that needs more attention from designer. Switching frequency affects the battery life, thermal design and overall cost. To simplify the analysis to determine the suitable frequency, the total power loss per phase can be estimated in equation 2.2.1.

$$Ploss = Pcond + Psw + Prr + Pg + Potr \qquad (2.2.1)$$

$P_{cond}$ is total conduction power loss of $S_1$, $S_2$ and DCR loss of inductor. $P_{sw}$ is the switching loss of $S_1$. Prr is the reverse recovery loss of $S_2$. Pg is gate driver loss for both $S_1$ and $S_2$. Potr is power loss of output capacitor of $S_1$ and body diode of $S_2$ dead time. Other power losses such as equivalent series resistance (ESR) of input and output capacitors, core loss of inductor and PCB resistance have been neglected. Figure 2.7 shows the calculation of power loss break down at different switching frequency for two parallel of IRF7821 for upper and two parallel of IRF7832 for lower MOSFET at 20A output current. Conduction loss $P_{cond}$ is independent of switching frequency. Other power losses are increased proportional to the switching frequency.

Equation 2.2.1 can also be use to determine the efficiency over the switching frequency, Figure 2.8. Since the thermal and battery life constrain in the laptop, the switching frequency is limited. To extend the battery life of laptop, the industry usually targets for 85% efficiency from dc/dc converter for processor. To have 85% efficiency, the switching frequency cannot exceed 350kHz. To have fast transient response and less

output capacitors, lower switching frequency is not a practical option. Because of those factors, industry has been using switching frequency between 200kHz to 300kHz.

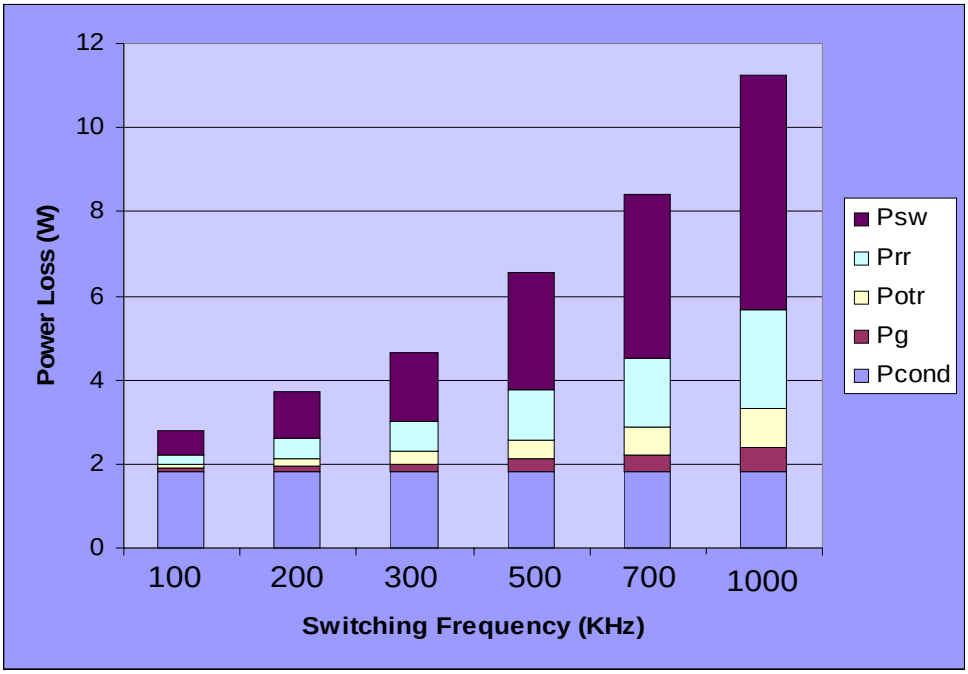



Figure 2.7 Power Loss Break Down of 1-phase

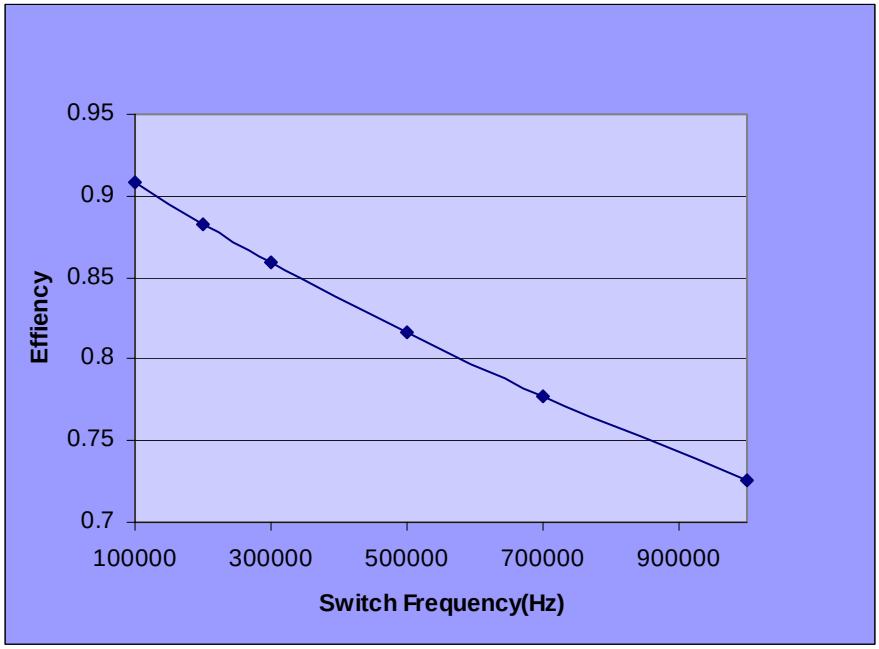



Figure 2.8 Efficiency of 20A at Different Switching Frequency

## 2.3 Selection of Current Sensing Methods

There are numerous methods that can be used to sense the output current for current balance and over current protection in multiphase. Three widely used methods in computer industry are $R_{DSON,}$ DCR and Resistor in series with output inductor.

### 2.3.1 Resistor Method

This method is traditional and still being used in many laptops. The advantage of this method is that it provides the highest tolerance accuracy. With technology today, the tolerance of resistor can be down to 0.5% to 1% and the resistance can be found in 1mΩ range. The tighter tolerance, the higher cost of component will be. The disadvantage is that it lowers the system efficiency. For 20A load and 1mΩ device, the power loss per phase can be found:

$$P = I^2 \cdot R = 20^2 \cdot 0.001 = 0.4 \text{ W} \qquad (2.3.1)$$

The efficiency will be lower by 1.67% for 4-phase synchronous buck converter at 95.68W. Figure 2.9 shows the connection configuration.

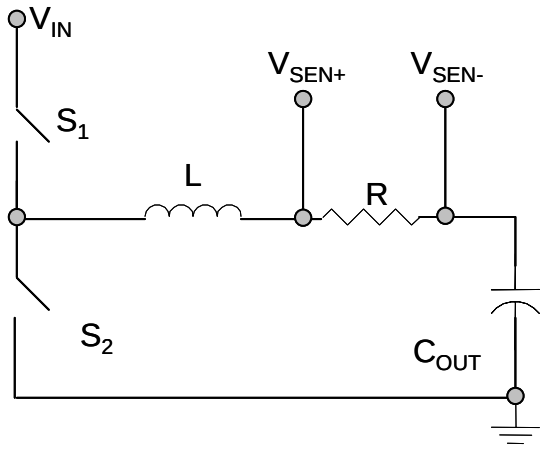



Figure 2.9 Resistor Current Sense Method

### 2.3.2 DCR Method

Inductor DCR current sensing method is fundamentally similar to resistor sense method by using the winding resistance of inductor as sensing element. Figure 2.10 shows current sensing method. The advantages of this method are no additional cost to the system and less power loss. The accuracy of this method depends on DCR tolerance of inductor. Today, the tolerance of DCR varies from 5% to 10% while the tolerance of inductor varies from 10% to 20%, respectively. Because the copper wire is the source of the DCR, the resistance of copper increases with the temperature by 0.39%/$^{o}$C.

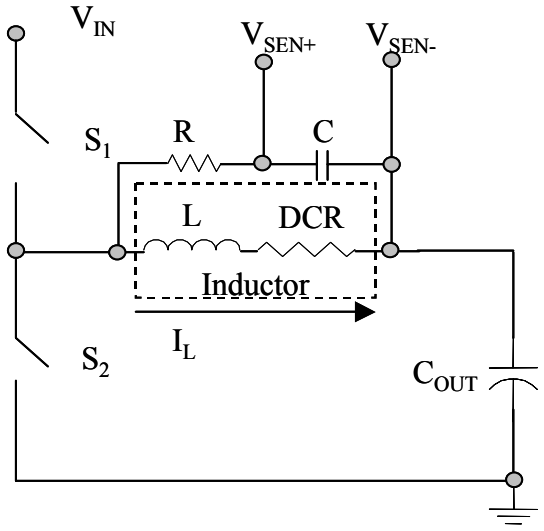



Figure 2.10 Inductor DCR Current Sense Method

Figure 2.11 shows the voltage, current of inductor and voltage cross capacitor $V_C$ during on and off time. The capacitor voltage is proportional to current flow through inductor.

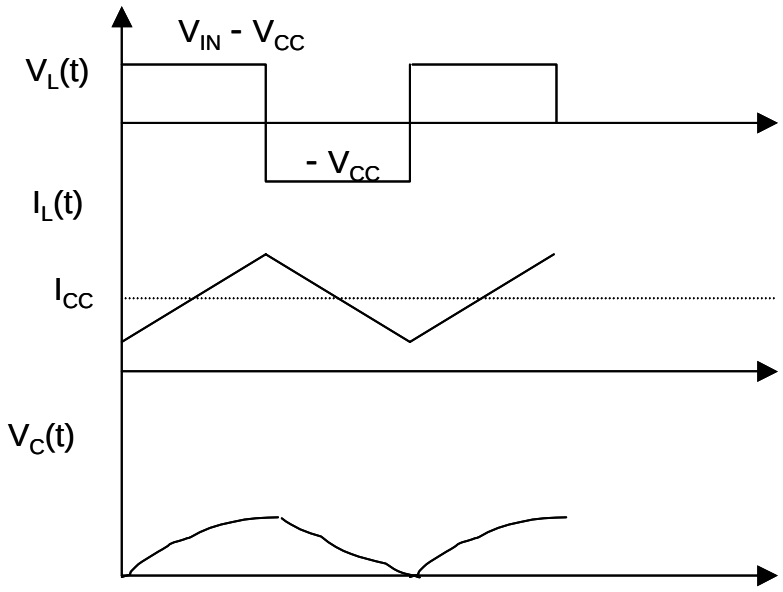



Figure 2.11 Capacitor voltage is shown to be proportional to inductor current

From Figure 2.10, voltage of capacitor can be found:

$$V_L(s) = I_L \cdot (s \cdot L + DCR) \qquad (2.3.2)$$

$$Vc(s) = I_L \cdot DCR \frac{\left(\frac{s \cdot L}{DCR} + 1\right)}{(s \cdot C \cdot R + 1)} \qquad (2.3.3)$$

If R-C network components are selected such that the RC time constant matches the L/DCR time constant then the voltage of capacitor is proportional to the voltage drop cross the DCR.

### 2.3.3 $R_{DSON}$ Method

Another popular loss-less current sensing method is to use the lower MOSFET $R_{DSON}$ since the MOSFET behaves as resistance during its on time. This method results in the least accuracy. The accuracy depends on the characteristic of MOSFET $R_{DSON}$ initial tolerance at room temperature and temperature coefficient. The temperature coefficient is typical 0.4%/$^{o}$C, which is close to DCR temperature coefficient, that can be obtained

from drain-to-source on resistance versus junction temperature in the MOSFET datasheet as shown in Figure 2.12.

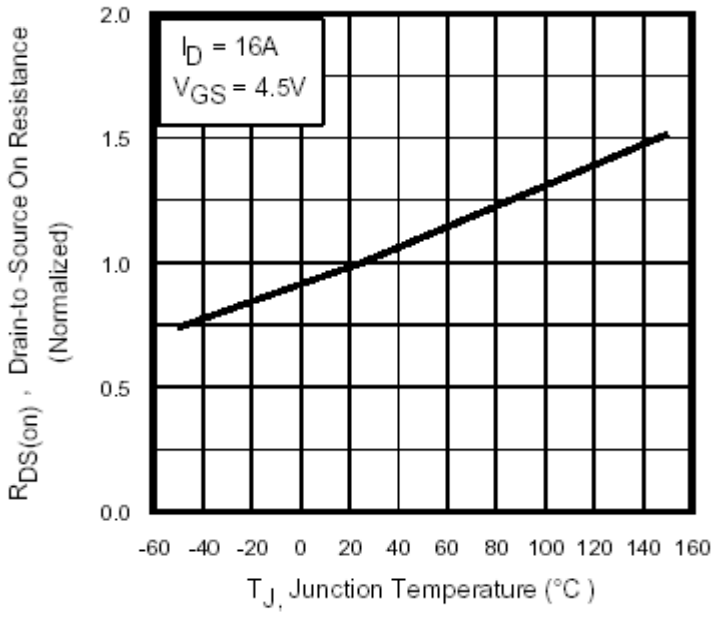



Figure 2.12 IRF7832 Normalized On-Resistance vs Temperature

The MOSFET manufacturers usually specify the typical and maximum values of on resistance. The initial tolerance of on resistance at room temperature varies with the technology of the process and typical greater than 20%. Figure 2.13 shows the circuit of using on resistance $S_2$ to sense the current.

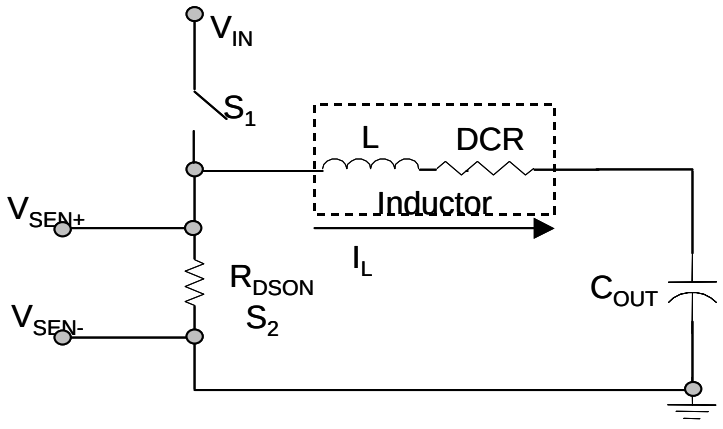



Figure 2.13 $R_{DSON}$ Current Sense

## 2.4 Thermal Compensation Methods for Loss-Less Current Sensing

As DCR or $R_{DSON}$ increases with temperature, the voltage cross of DCR or $R_{DSON}$ will increase at the same time. This results in an error current between the current sense information and load current. The sense current is used to adjust the output voltage level. Eventually, the processor voltage could be out of the minimum and maximum window specifications. Figure 2.14 shows how the load current can be sensed. The sample and hold circuitry of controller reproduces a current which is proportional to output current. Assume the time constants are matched between L/DCR and RC, the capacitor voltage $V_C$ is replicated cross the sense resistor $R_{SEN}$. The current through the sense resistor is proportional to the inductor current. Equation 2.4.1 shows the relation between the inductor and the sense current, $I_{SEN}$.

$$R_{SEN} \cdot I_{SEN} = I_L \cdot DCR \qquad 2.4.1$$

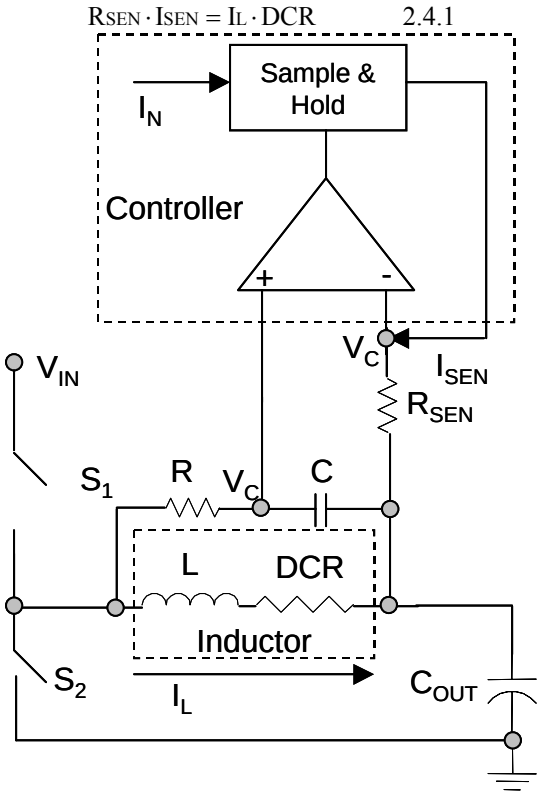



Figure 2.14 DCR Sense Method Implementation

This sample and hold circuitry can also be used to sense for $R_{DSON}$ or resistor sense methods. To compensate the DCR or $R_{DSON}$ increase with temperature, a thermistor, or thermally sensitivity resistor, can be used instead of the standard resistor in $R_{SEN}$. There are two basic types of thermistor, Positive Temperature Coefficient (PTC) and Negative Temperature Coefficient (NTC). A PTC device will increase resistance with an increase in temperature; an NTC device will decrease resistance with an increase in temperature [11-12].

Again, the DCR of inductor increases by 0.39%/$^{o}$C. Equation 2.4.1 proves that to have $I_{SEN}$ proportional to $I_L$ with insensitively to the temperature, $R_{SEN}$ has to increase by 0.39%/$^{o}$C. A PTC will achieve this purpose. The Temperature Coeffience Resistance (TCR) of PTC depends on the PTC materials. The TCR has the tolerance that varies from 1% to 10%. Figure 2.15 shows the PTC resistance of Panasonic varies with temperature. To have best coupling temperature between the inductor and PTC, the PTC has to be placed close to the inductor on the board. The cost of PTC is as high as twice of NTC. The NTC typically costs about 5 cents in high volume.

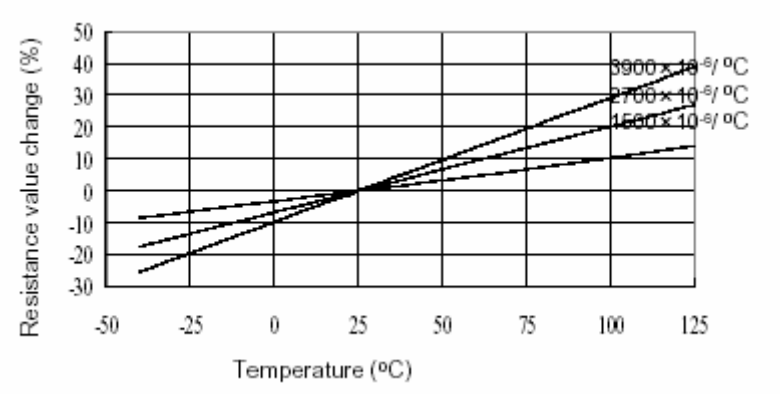



Figure 2.15 Panasonic Linearity PTC

In IMPV processor, the processor voltage decreases to save the power as load increase, which is called droop voltage in industry. Figure 2.16 shows a circuit to implement the droop voltage [6]. Inside the controller, the droop current $I_{DROOP}$ can be mirrored from $I_{SEN}$. Therefore, $I_{DROOP}$ is the same as $I_{SEN.}$ The droop current is forced to flow into the node at negative of error amplifier and creates a voltage drop across the feedback resistor $R_{FB}$. The resulting steady state value of processor voltage droop is:

$$V_{DROOP} = I_{SEN} \cdot R_{FB} \qquad (2.4.2)$$

By substitute equation 2.4.1 into 2.4.2, one has:

$$V_{DROOP} = \frac{I_L \cdot DCR}{R_{SEN}} \cdot R_{FB} \qquad (2.4.3)$$

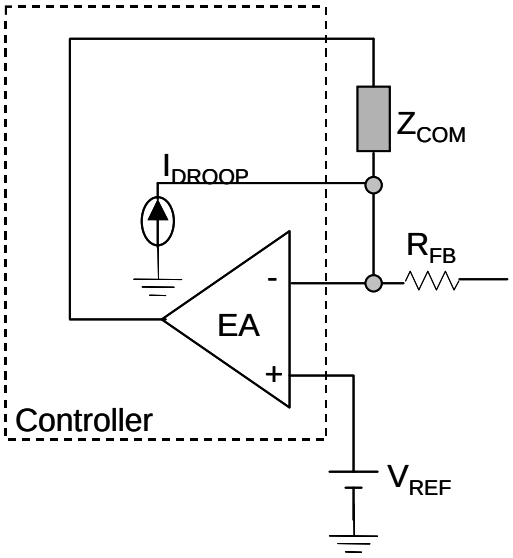



Figure 2.16 Droop Circuitry Implementation

Another method of compensating the thermal increase of DCR or $R_{DSON}$ is to use NTC resistor for $R_{FB}$. This method will reduce the system cost. $R_{SEN}$ can be as standard resistor in this method. If a NTC resistor in $R_{FB}$ position decreases with the same rate of temperature coefficient as DCR or $R_{DSON}$, then the processor voltage will stay in the tolerance window.

Equation 2.4.4,[11], describes the relationship of NTC resistance at any temperature. It can be found in most of NTC thermistor literature.

$$R_T = R_O \cdot e^{\left(\beta \cdot \left(\frac{1}{T} - \frac{1}{T_O}\right)\right)} \qquad 2.4.4$$

$R_O$ is the resistance at a specified reference temperature $T_O$ which is expressed in Kevin. The usual reference temperature is 25°C. $R_T$ is the resistance at an absolute temperature T that is also expressed in Kevin. β is the material constant which is the slope of thermistor R-T characteristic over the specified temperature range. Most NTC thermistor manufactures provide a table of resistance at different temperature or resistance ratio curve versus temperature of each material. For example, Figure 2.17 shows the resistance ratio versus temperature at different β of Panasonic NTC thermistor.

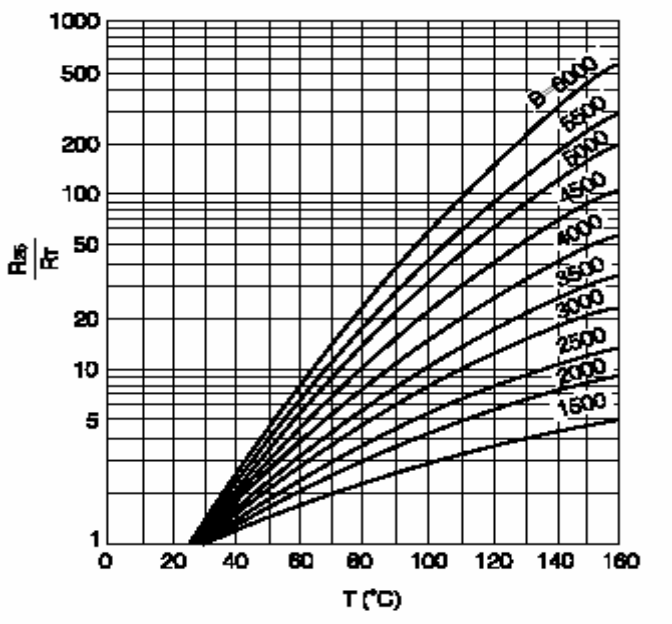



Figure 2.17 Resistance Ratio vs Temperature of Panasonic NTC Thermistor

Figure 2.18 shows the normalize resistance versus temperature with β = 4000K. The resistance of NTC decreases with a nonlinear rate, which is not matching with the linear change of DCR or $R_{DSON}$.

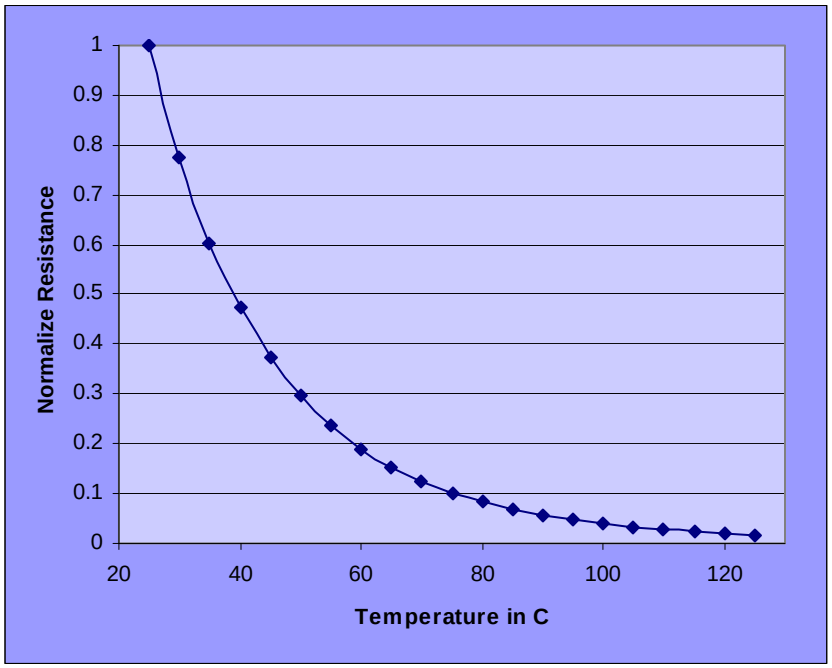



Figure 2.18 Normalize Resistance NTC Thermistor of β is 4000K

Figure 2.19 shows a combination resistor network of NTC thermistor and standard resistors to create the resistance decreasing linearly over the temperature. If this NTC network replaces the $R_{FB}$ resistor, this network circuit will achieve same purpose of PTC. This circuit has been widely used in industry to save the system cost. NTC has to place near the inductor for DCR method or near the MOSFET for $R_{DSON}$ method for tracking the temperature rise of inductor or MOSFET.

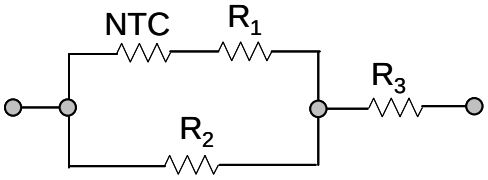



Figure 2.19 Linear NTC Network

## 2.5 Transient Effects by DCR Sensing Method

The equation of voltage capacitor in DCR current sense method is repeated here for convenient.

$$Vc(s) = I_L \cdot DCR \frac{\left(\frac{s \cdot L}{DCR} + 1\right)}{(s \cdot C \cdot R + 1)} \qquad (2.5.1)$$

If the time constant of L/DCR is not matched with the RC time constant, the $I_{DROOP}$ will send wrong current information during the transient. If L/DCR is higher than RC, the processor voltage will be lower. Likewise, the processor voltage will be higher when RC time constant is higher than L/DCR. Figure 2.20 shows effect of mismatch time constant during the transient.

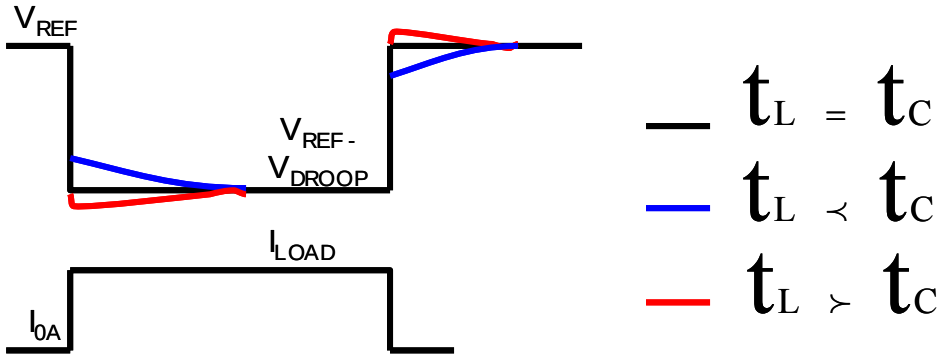



Figure 2.20 DCR Time Constant Mismatch During Transient

Equation 2.6.2 shows the processor voltage in time domain [13].

$$V_{CC}(t) = V_{REF} - I_L \cdot R_{DROOP} \cdot \left[ 1 - \frac{\left(\frac{\omega_C}{\omega_Z} - 1\right)}{\left(\frac{\omega_C}{\omega_P} - 1\right)} \cdot e^{-\omega_C \cdot t} - \frac{\left(\frac{\omega_P}{\omega_Z} - 1\right)}{\left(\frac{\omega_P}{\omega_C} - 1\right)} \cdot e^{-\omega_P \cdot t} \right] \quad 2.5.2$$

$$\omega_P = \frac{1}{RC} \quad 2.5.3a$$

$$\omega_Z = \frac{DCR}{L} \quad 2.5.3b$$

$$\omega_C = \frac{1}{f_C} \quad 2.5.3c$$

$f_C$ is the cross-over frequency of dc/dc converter. $\omega_P$ is much less than $\omega_C$. Therefore, the settling time is determined by $\omega_P$.

**2.6 Load Line Tolerance Analysis**

Figure 2.21 shows the load line specification. If the processor voltage is below the minimum specification, the processor could be lock out. If the processor voltage is above the maximum specification, the processor will consume more power and may short its lifetime.

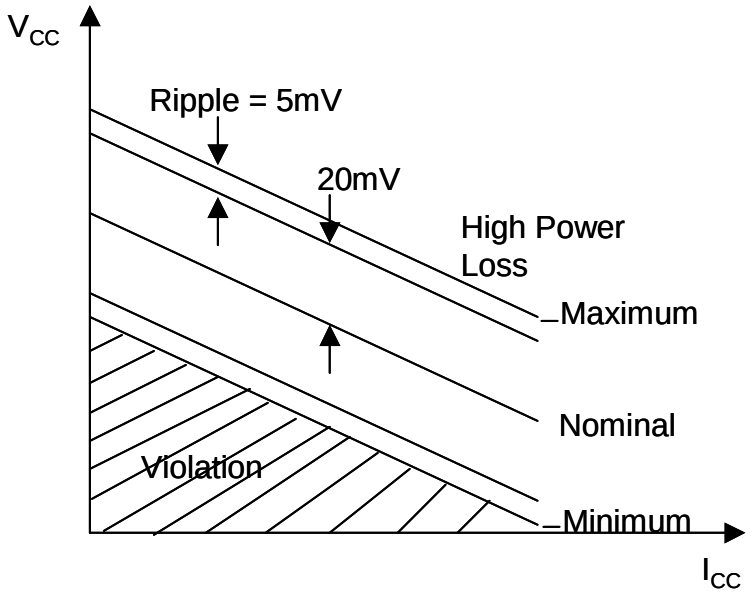



Figure 2.21 Load Line Specification

The reference voltage $V_{REF}$ of controller is typically the output of the Digital Analog Converter (DAC). The accuracy of DAC voltage is the most influencing factor in the load line. The tolerance of DAC typically varies from +/- 0.5% to +/-1%. For example, the tolerance of 1.3V of DAC is +/- 6.5mV and +/-13mV for +/- 0.5% and +/-1%, respectively. The higher DAC tolerance is the more accuracy is required from other factors that affect the load line. The lower DAC tolerance results in lower yield of controller in wafer, therefore the cost of controller will increase. Because the processor voltage decreases as load current increase, the accuracy of current sense circuits in multiphase is also very important. The current sense method also affects the load line accuracy. Because of inductor current sensing is loss less, low cost and provides reasonable current information accuracy, it is selected for the following analysis. The other factors contributing the load line error are no load set point accuracy, external 1% resistors, etc…

Table 2.6.1 shows the tolerance of all the parameters that affects the load line error in Tol column. The tolerances of inductor DCR, PTC and current sense circuitry are mainly effect the current sense information. The table also includes the tolerance of output inductor, resistor and capacitor to calculate the effect of undershoot or overshoot voltage during the transient into the load line. In order to generate the nominal, minimum and maximum load lines, the table needs to program of load line specifications, number of phase, component value and its tolerance…etc that are in light and bright green color rows. The rows with plum color are calculated from the inputs rows.

The results of load line in this thesis are based on 4-phase operation and average current mode. The tolerance of minimum and maximum load lines are obtained by using the

root-sum-square (RSS) methods. The tolerance of load line is obtained by calculating the deviation from the nominal output voltage to the three sigma of standard deviation the different of the nominal to the output voltage which corresponds to the tolerance of one parameter while other tolerance of parameters are equal to zero.

| Description of parameter | Tol | Sym | Minimum | Nominal | Maximum |
|---|---|---|---|---|---|
| Number of phases in multi-phase buck converter. | | $N_\Phi$ | | 4 | |
| Low load operating current. | | $I_{MIN}$ | | 0 | |
| Full load operating current. | | $I_{MAX}$ | | 80 | |
| Reference voltage setting. | | VID | | 1.325 | |
| Output voltage of unloaded converter (specification limits). | | $V_{CORE,NL}$ | 1.275 | 1.300 | 1.325 |
| Output voltage of fully-loaded converter (specification limits). | | $V_{CORE,FL}$ | 1.171 | 1.196 | 1.221 |
| Nominal switching frequency | | Fsw | | 300E+03 | |
| Nominal duty cycle, low load | | d,LL | | 9.29% | |
| Nominal duty cycle, full load | | d,FL | | 8.54% | |
| Offset direction | | | | - | |
| Offset-generating voltage | 2% | $V_{OS,SET}$ | 1.960 | 2.00 | 2.040 |
| PTC Reference Characteristic Temperature | | $T_{PTC,REF}$ | | 25 | |
| Chosen PTC at Room Temperature | 5% | $R_{PTC}$ | 779.00 | 820.00 | 861.00 |
| Positive Temperature Coefficient of PTC(%/°C) | 5% | $\alpha_{PTC}$ | 0.314% | 0.330% | 0.347% |
| Inductor Reference Characteristic Temperature | | $T_{L,REF}$ | | 20 | |
| Initial Inductor DCR (T=20°C) | 10% | $R_{DC}$ | 1.62E-03 | 1.70E-03 | 1.79E-03 |
| Initial Suggested Feedback Resistance | | | | 1.89E+03 | |
| Chosen Feedback resistance | 1% | $R_{FB}$ | 1.89E+03 | 1.91E+03 | 1.93E+03 |
| Suggested resistor between OFS and GND | | | | 318.3E+03 | |
| Chosen resistor between OFS and GND | 1% | $R_{OFS}$ | 312.84E+03 | 316E+03 | 319.16E+03 |
| Ambient temperature | | $T_{A,L}$ | | 40 | |
| Hot inductor temperature | | | | 105 | |
| Inductance - low load (0A @ T=20°C) | 20% | $L_{LL}$ | 480.00E-09 | 600E-09 | 720.00E-09 |
| Inductance - full load (20A @ T=20°C) | 20% | $L_{FL}$ | 430.40E-09 | 538E-09 | 645.60E-09 |
| Suggested time-constant network resistor | | | | 29E+03 | |
| Resistor in time-constant network | 1% | $R_\tau$ | 32.08E+03 | 32.4E+03 | 32.72E+03 |
| Thermal coupling coefficient between Inductor and PTC | | | | 75% | |
| Thermal coupling coefficient between Inductor and Sense Cap | | | | 75% | |

| | | | | | |
|---|---|---|---|---|---|
| Inductor DCR temperature coefficient | | $\alpha_L$ | | 0.390% | |
| DCR at cold (T=40°C) | | $R_{DC(COLD)}$ | | 1.833E-03 | |
| DCR at hot (T=105°C) | | $R_{DC(HOT)}$ | | 2.26E-03 | |
| Temperature of PTC - Hot | | | | 89 | |
| Temperature of sense cap - Hot | | | | 89 | |
| Capacitor in time-constant network - Cold | 10% | $C_{\tau,COLD}$ | 9.00E-09 | 10.00E-09 | 11.00E-09 |
| Capacitor in time-constant network - Hot | 10% | $C_{\tau,HOT}$ | 8.37E-09 | 9.30E-09 | 10.23E-09 |
| PTC Sense Resistor - Cold (T=40°C) | | | | 861E+00 | |
| PTC Sense Resistor - Hot (T=88.75°C) | | | | 992.51E+00 | |
| Tau mismatch - cold, low load | | | | 1.0% | |
| Tau mismatch - hot, low load | | | | -13.7% | |
| Tau mismatch - cold, full load | | | | -10% | |
| Tau mismatch - hot, full load | | | | -27% | |
| Current measurement offset - cold, low load | | | | 859.45E-03 | |
| Current measurement offset - hot, low load | | | | 1.01E+00 | |
| Current measurement offset - cold, full load | | | | 1.02E+00 | |
| Current measurement offset - hot, full load | | | | 1.25E+00 | |
| Reference voltage output of DAC. | 0.6% | $V_{REF}$ | 1.317E+00 | 1.325E+00 | 1.333E+00 |
| Current-sense gain | 8.0% | $F_{DROOP}$ | 1.2E+00 | 1.30E+00 | 1.40E+00 |
| Offset voltage | | | | -12.1E-03 | |
| Low-load droop current cold (includes time-constant mismatch) | | | | 6.0E-06 | |
| Low-load droop current hot | | | | 3.0E-06 | |
| Full-load droop current cold | | | | 58.2E-06 | |
| Full-load droop current hot | | | | 63.0E-06 | |

Table 2.6.1 Load Line Accuracy

Figure 2.22 and Figure 2.23 show the results of load line analysis in cold and hot temperature, respectively. The cold temperature is chosen to be 40°C, which is ambient temperature in laptop. The hot temperature is chosen to be 105°C such that the highest temperature of motherboard is allowed in laptop environment. The results of load lines slope in cold temperature tend to decrease less as the current increase because the DCR is less increase. While the load line slope in hot temperature is opposite. In both case, the load lines are met with the specification.

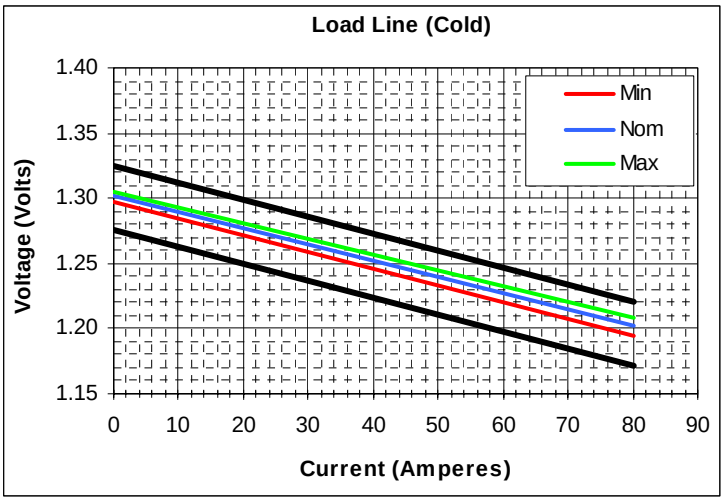



Figure 2.22 Load Line Analysis at 40°C

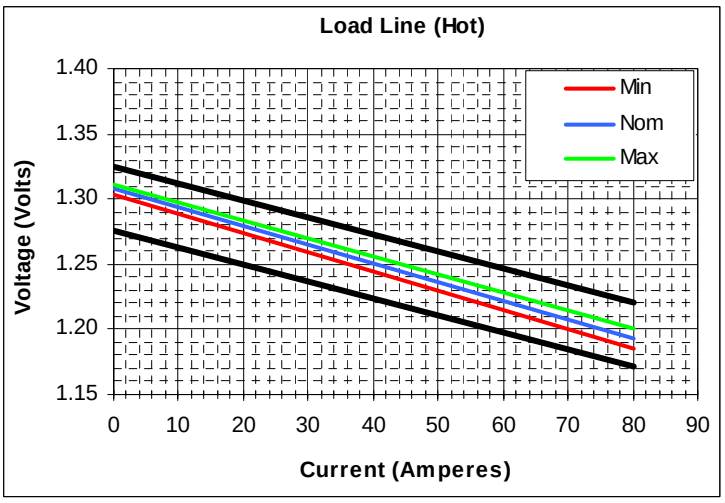



Figure 2.23 Load Line Analysis at 105°C

## 2.7 Output Capacitor

### 2.7.1 Output Capacitor Calculation

Output capacitance is another important factor, which may reduce the system cost in multiphase converter. If the output capacitance is not enough, the processor voltage will violate the specifications during the transient. The amount of output capacitors is based on the parameters of maximum load step, the slew rate of load step and the maximum allowable output voltage deviation under transient. Figure 2.24 shows the specification of the processor voltage during the transient when the load is removed.

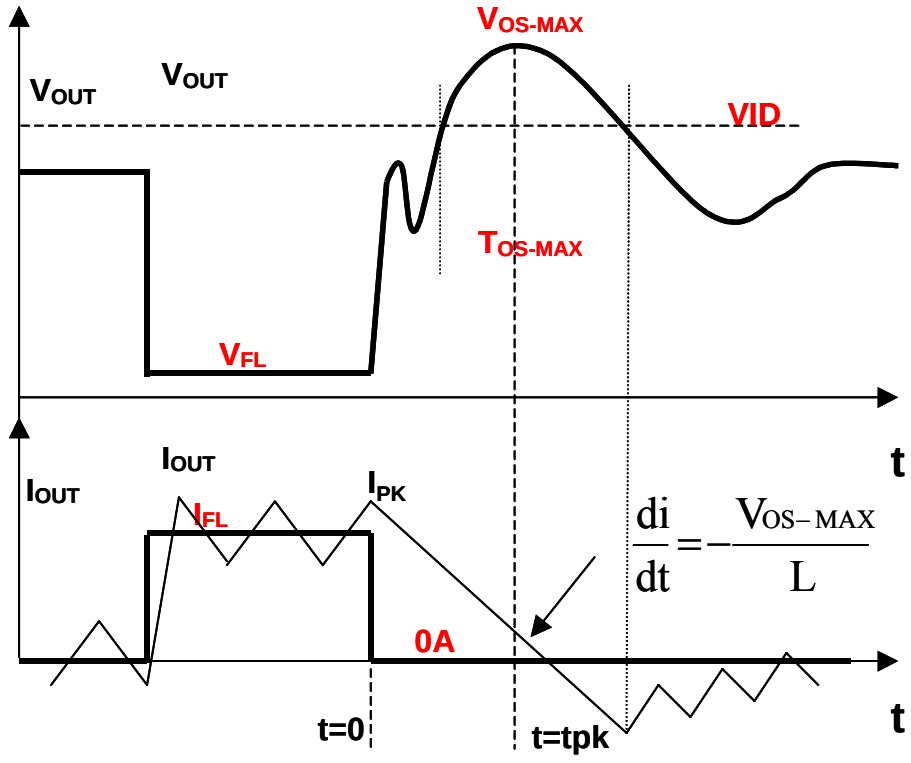



Figure 2.24 Processor Voltage Specification During Transient

$V_{OS\text{-}MAX}$, 50mV above the VID, is the maximum allowable output voltage during the transient. $T_{OS\text{-}MAX}$ is maximum time allow when output voltage above the VID. The minimum of output capacitor is calculated during the load current transit from full load to

light load. At $T_0$ the output voltage increases which cause the voltage of output error amplifier decreases below the valley of saw-tooth voltage, therefore there is no PWM signal for all phases. This results the lower FET turns on all the time. The energy of output capacitors and inductors before the load change should be the same energy when output voltage reaches it maximum. By apply this energy law, the equation 2.7.1 can be found.

$$\frac{1}{2}LI_{pk}^{2}+\frac{1}{2}CV_{FL}^{2}=\frac{1}{2}LI^{2}+\frac{1}{2}CV_{OS-MAX}^{2} \qquad (2.7.1)$$

$$L\cdot\left(I_{pk}^{2}-I^{2}\right)=C\cdot\left(V_{OS-MAX}^{2}-V_{FL}^{2}\right) \qquad (2.7.2)$$

The minimum output capacitor can be calculated when the inductor current at peak time $t_{pk}$ is known. If this current is zero at peak time, the minimum output capacitor can be easy found in 2.7.3

$$C=\frac{L\cdot I_{pk}^{2}}{\left(V_{OS-MAX}^{2}-V_{FL}^{2}\right)} \qquad (2.7.3)$$

In the practical, the output voltage reaches to its maximum voltage earlier due to the time constant of ESR and output capacitor. Therefore, the inductor current is not equal to zero when the output voltage reaches its peak. This inductor current can be calculated in equation 2.7.4 at the time $t_{PK}$.

$$I=I_{pk}-\frac{V_{OS-MAX}}{L}\cdot t_{pk} \qquad (2.7.4)$$

Figure 2.25 shows a simplify circuit during the current transit from full load to light load.

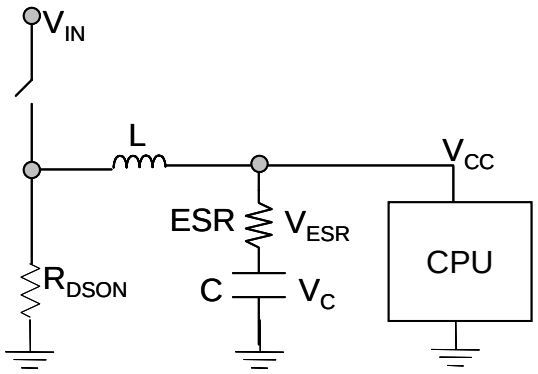



Figure 2.25 Simplify DC Converter During Load Transit From High to Low

Time $t_{PK}$ can be found by writing the voltage equation at $V_{CC}$.

$$V_{OS\_MAX} = V_{ESR} + V_C \qquad (2.7.5a)$$

$$V_{OS\_MAX} = \left( I_{pk} - \frac{V_{OS-MAX}}{L} \cdot t \right) \cdot ESR + \left( I_{pk} - \frac{V_{OS-MAX}}{L} \cdot t \right) \cdot \frac{t}{C} \qquad (2.7.5b)$$

The time $t_{PK}$ is the time when the slope of $V_{OS\text{-}MAX}$ is zero. In other words, to find $t_{PK}$, set $dV_{OS\text{-}MAX}$ /dt equals to zero.

$$t_{pk} = \frac{I_{pk} \cdot L}{V_{OS\_MAX}} - ESR \cdot C \qquad (2.7.6)$$

By substitute equation 2.7.6 into equation 2.7.4 and the result substitutes into equation 2.7.1b, the equation of minimum output capacitor can be found in 2.7.7.

$$C_{MIN} = \frac{-L \cdot \left( V_{OS-MAX}^2 - V_{FL}^2 \right) + \sqrt{\left[ L \cdot \left( V_{OS-MAX}^2 - V_{FL}^2 \right) \right]^2 + 4 \cdot \left( V_{OS-MAX} \cdot ESR \cdot L \cdot I_{pk} \right)^2}}{2 \cdot \left( V_{OS-MAX} \cdot ESR \right)^2} \qquad (2.7.7)$$

### 2.7.2 Bulk Output Capacitor Selection

In the transient analysis from light to full load, output capacitor can no longer be considered as an ideal capacitor. Capacitors are characterized according to their capacitance, equivalent series resistance (ESR) and equivalent series inductance (ESL). Figure 2.26 shows a practical capacitor model.

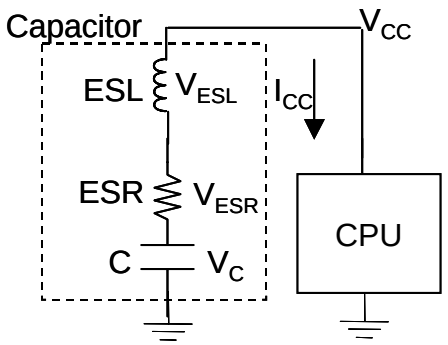



Figure 2.26 Practical Capacitor Model

When the processor demands the load, the output capacitors supply the current to processor first while the inductor current ramping up. Figure 2.27 shows the magnified of processor current and voltage reaction when the processor demands the load. The parasitic package capacitor of microprocessor has been neglected.

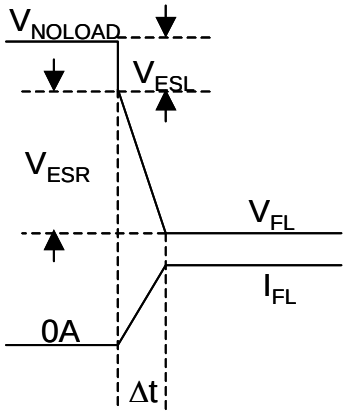



Figure 2.27 Zoom In of Rising Processor Load Current

When output capacitors supply the current, the processor voltage will drop. The total voltage drop is the sum of $V_C$, $V_{ESR}$ and $V_{ESL}$. $V_C$ is the integral of charge loss in the capacitor. $V_{ESR}$ is the proportional voltage due to the current flow through the ESR of capacitor. $V_{ESL}$ is the differential voltage that is caused by the slew rate di/dt of processor current through the ESL of capacitor.

$$V_C = \frac{1}{C}\int I_{FL} \cdot dt \qquad (2.7.8a)$$

$$V_{ESR} = ESR \cdot I_{FL} \qquad (2.7.8b)$$

$$V_{ESL} = ESL \cdot \frac{I_{FL}}{\Delta t} \qquad (2.7.8c)$$

The proportional and differential voltages are the most contributing factor of the voltage drop. To avoid violating the processor voltage specification during the transient, the designer should pay attention to the ESR and ESL when selecting the bulk output capacitors. The total voltage drop of capacitor cannot greater than the nominal voltage of the specification. Higher ESL results in lower slew rate of current; and higher ESR results in high voltage drop and limits the current provided by capacitor.

The designer can easily choose the ESR and ESL when comparing the load line slope to equations 2.7.8b and 2.7.8c.

$$V_{DROOP} = R_{DROOP} \cdot I_{FL} = \left( ESR + \frac{ESL}{\Delta t} \right) \cdot I_{FL} \qquad (2.7.9a)$$

$$R_{DROOP} = ESR + \frac{ESL}{\Delta t} \qquad (2.7.9b)$$

Typical output capacitor solutions are made up of a mixture of low capacitance ceramics along with high capacitance such as aluminum electrolytic or special polymer capacitors. Because ceramic capacitor has low ESR and ESL, it provides the initial high frequency current when the processor demands the current. Ceramic capacitors also help to reduce the ripple voltage during the static load.

### 2.7.3 Output Capacitor Versus Bandwidth

A capacitor has the typical characteristic of impedance versus the frequency as shown in Figure 2.28. Below the corner frequency, the impedance behaves capacitive. Above the corner frequency, the impedance behaves inductive. The impedance curve indicates the bandwidth of converter can be as high as the corner frequency before the impedance

capacitor increase. In reference [1-4], the crossover frequency $f_C$ of converter is equaled to the ESR zero frequency of the output capacitor. This conclusion is verified with three different output capacitor options in Chapter 4.

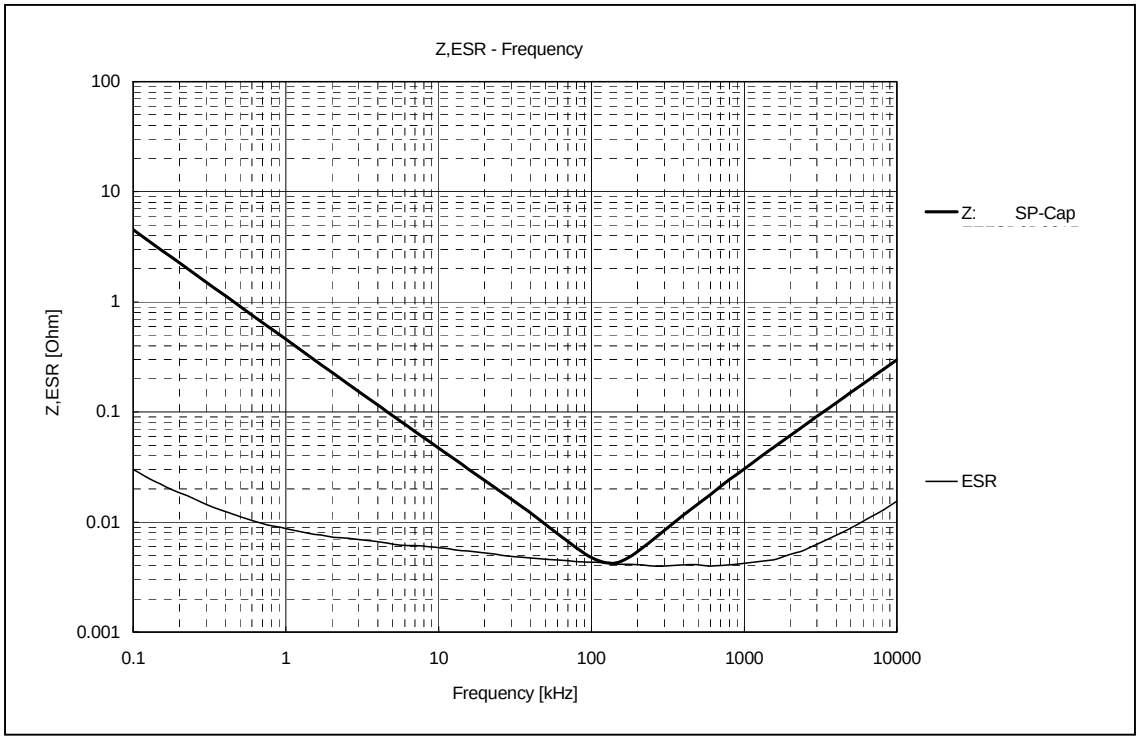



Figure 2.28 Typical Bulk Capacitor Impedance

## 2.8 Inductor Design

The output ripple voltage in VRC is equaled to the total equivalent ESR of output capacitors multiply by the total output inductor ripple current. As mentioned in Chapter 1, the total inductor ripple current is less than individual phase ripple current due to the affect of ripple cancellation in multiphase synchronous buck converter. The ripple current of each phase is shown in equation 1.1.1. A small inductance can be used to improve the transient response, and consequently a small output capacitance can be used to meet the transient response [14]. The inductance is reduced at a certain percentage as the current flow through it increases. Therefore, it is necessary to design the ripple current at heavy

load condition rather than light load. Besides this, the inductance of an inductor also has the tolerance as 10% to 20%. To guarantee meet the output ripple voltage specification, a practical method to design the inductance of each phase is that the ripple current can be calculated base on the output ripple voltage divided by the total equivalent ESR of output capacitors. Then, the inductance can be calculated by using equation 1.1.1.

## Chapter 3 Control Loop Design

### 3.1 DC Model

Figure 3.1 shows a synchronous buck converter along with parasitic components, which is repeat here again for convenient.

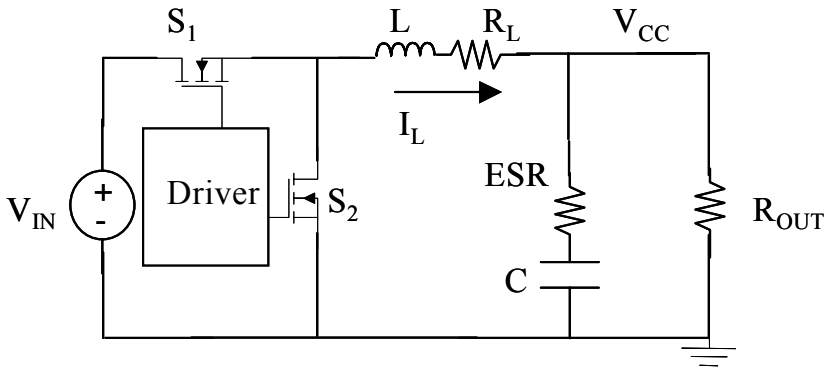



Figure 3.1 Synchronous Buck Converter with Parasitic Components

By using the small-ripple approximation, one can write the equations of inductor voltage and capacitor current during the on and off time.

$S_1$ On :

$$V_L = V_{IN} - R_L \cdot I_L - V_{CC} \qquad 3.1.1$$

$$I_C = I_L - \frac{V_{CC}}{R_{OUT}} \qquad 3.1.2$$

$S_2$ On :

$$V_L = -R_L \cdot I_L - V_{CC} \qquad 3.1.3$$

$$I_C = I_L - \frac{V_{CC}}{R_{OUT}} \qquad 3.1.4$$

By using the principle of inductor volt-second balance, the average inductor voltage is equal to zero over one switch cycle in the steady state.

$$< V_L > = 0 = D \cdot (V_{IN} - R_L \cdot I_L - V_{CC}) + (1 - D) \cdot (- R_L \cdot I_L - V_{CC}) \qquad 3.1.5a$$

$$< V_L > = 0 = D \cdot V_{IN} - R_L \cdot I_L - V_{CC} \qquad 3.1.5b$$

When the switch $S_1$ is on, the input current $I_{IN}(t)$ is equal to the inductor current. When the switch $S_1$ is off, the input current is zero. The average value of input current is

$$< I_{IN} > = D \cdot I_L \qquad 3.1.6$$

The dependent current in 3.1.6 and voltage in 3.1.5 sources can be combined into a DC transformer [15] in Figure 3.2; since $DV_{IN}$ dependent voltage source has value D time the input voltage $V_{IN}$ across the dependent current source, and the current source is the same constant D times the current $I_L$ through the dependent voltage source.

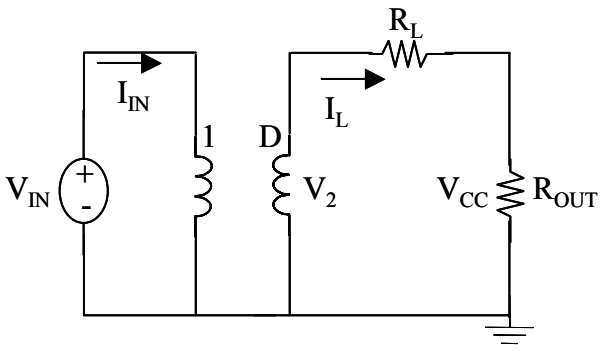



Figure 3.2 Average DC Transformer Model

One can write the steady state relationship of input and output voltage from Figure 3.2 by using transformer and voltage divider rules.

$$\frac{V_{CC}}{V_{IN}} = D\frac{R_{OUT}}{R_L + R_{OUT}} \qquad 3.1.6$$

### 3.2 Open Loop AC Model

To predict the low frequency characteristics in the converter that affects the output voltage, one needs to construct and model the small signal. One assumes that input voltage and duty cycle are equal to quiescent values and plus some small ac variation. This results can be extended such that the average inductor current, average input current and average output capacitor voltage are also equal to quiescent value and plus some superimposed small ac variations.

$$
\begin{aligned}
&< v_{IN}(t) >_{Ts} = V_{IN} + \hat{v}_{IN}(t) \\
&< i_{IN}(t) >_{Ts} = I_{IN} + \hat{i}_{IN}(t) \\
&< i_L(t) >_{Ts} = I_L + \hat{i}_L(t) \qquad (3.2.1) \\
&< d(t) >_{Ts} = D + \hat{d}(t) \\
&< V_{CC}(t) >_{Ts} = V_{CC} + \hat{v}_{CC}(t)
\end{aligned}
$$

By consider the transformer as two ports network and select input voltage and inductor current as independent terminal variables, one can express the average dependent terminal variables of input current and $V_2$ as functions of duty.

$$V_2 = (V_{IN} + \hat{v}_{IN})(D + \hat{d}) = V_{IN} \cdot D + V_{IN} \cdot \hat{d} + D \cdot \hat{v}_{IN} + \hat{d} \cdot \hat{v}_{IN} \qquad (3.2.2)$$

$$I_{IN} = (I_L + \hat{i}_L)(D + \hat{d}) = D \cdot I_L + \hat{d} \cdot I_L + D \cdot \hat{i}_L + \hat{d} \cdot \hat{i}_L \qquad (3.2.3)$$

Linearizing the above equations, we can get the small signal equation:

$$V_2 = V_{IN} \cdot \hat{d} + D \cdot \hat{v}_{IN} \qquad (3.2.4)$$

$$I_{IN} = \hat{d} \cdot I_L + D \cdot \hat{i}_L \qquad (3.2.5)$$

The open loop small signal model is then shown in Figure 3.3

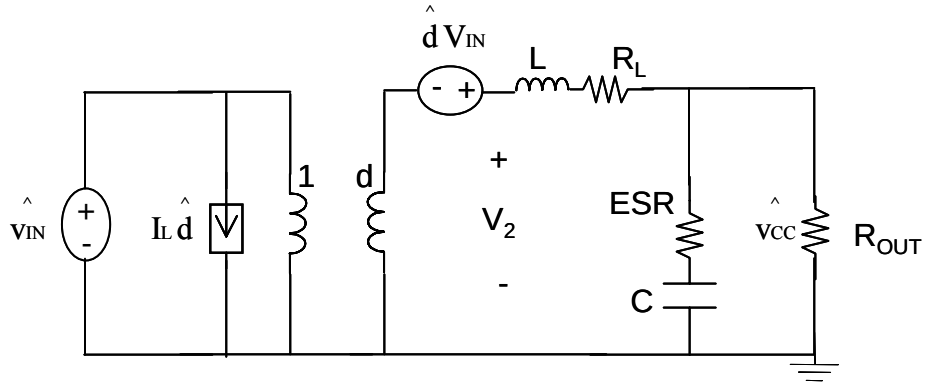



Figure 3.3 Small Signal Model

From Figure 3.3, one can obtain the open loop control to output transfer function by setting the small signal of input voltage equal to zero.

$$Gvd(s) = \frac{\hat{vcc}(s)}{\hat{d}(s)} = V_{IN} \frac{\left(1 + \frac{s}{S_{Z1}}\right)}{1 + \frac{s}{\omega o Q} + \frac{s^2}{\omega o^2}} \qquad (3.2.6)$$

$$\omega o = \frac{1}{\sqrt{LC}} \sqrt{\frac{1 + \frac{R_L}{R_{OUT}}}{\frac{ESR}{R_{OUT}} + 1}} \qquad (3.2.7a)$$

$$Q = \frac{1}{\omega o} \frac{1}{\frac{L}{R_L + R_{OUT}} + C \cdot \left(ESR + R_L // R_{OUT}\right)} \qquad (3.2.7b)$$

$$S_{Z1} = \frac{1}{ESR \cdot C} \qquad (3.2.7c)$$

Control to inductor current can also obtain by setting the small signal of input voltage to zero.

$$Gid(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = V_{IN} \frac{1}{s \cdot L + R_L + R_{OUT} // \left(ESR + \frac{1}{C \cdot s}\right)} \qquad (3.2.8)$$

### 3.3 Multiphase Close Loop Model

To model multiphase buck converter, first one can simplified the number of phase into 1-phase with equivalent component value [16]. To simplify the model, one assumes zero current balance in multiphase, which means all phases have to carry the same amount of current. Figure 3.4 shows the simplified circuit of multiphase synchronous buck converter with a droop current path.

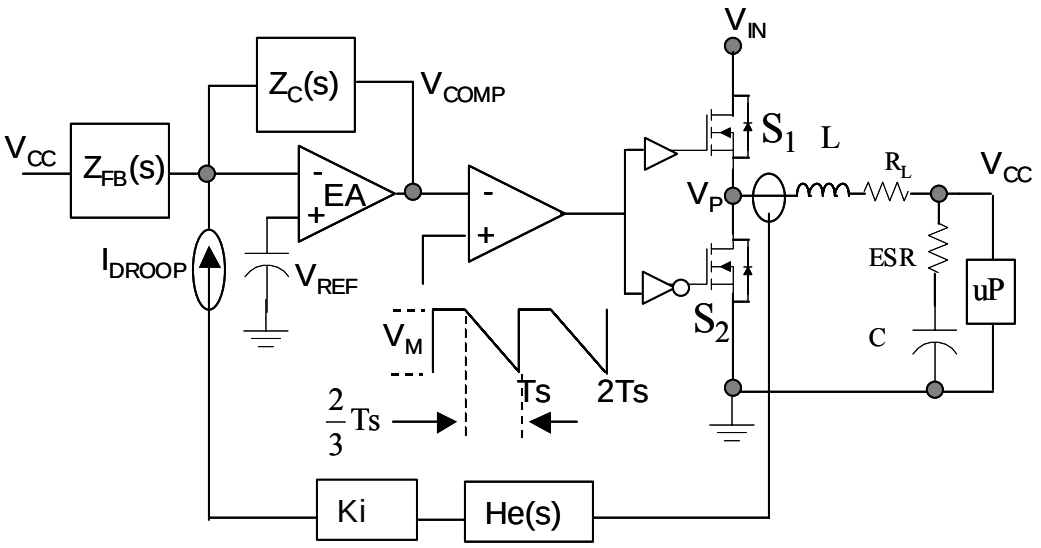



Figure 3.4 Simplified Multiphase Synchronous Buck with Droop Current

Pulse Width Modulator and Feed Forward:

Intersil ISL6247 controller, which uses in this thesis hardware, includes feed forward feature [6]. The peak-to-peak amplitude of the ramp oscillator is proportional to input voltage. The maximum duty of this controller is 2/3. The pulse width modulator gain can be computed as below. K is a constant.

$$\frac{D}{V_{COMP}} = \frac{2}{3 \cdot V_M} \qquad (3.3.1a)$$

$$V_M = K \cdot V_{IN} \qquad (3.3.1b)$$

$$\frac{D}{V_{COMP}} = \frac{2}{3 \cdot K \cdot V_{IN}} \qquad (3.3.1c)$$

The average voltage at the phase node VP is equal to the duty cycle times the input voltage.

$$D = \frac{V_P}{V_{IN}} \qquad (3.3.2)$$

By substitute equation 3.3.2 into equation 3.3.1c, the gain from the output of error amplifier to the phase node is:

$$\frac{V_P}{V_{COMP}} = \frac{2}{3 \cdot K} \qquad 3.3.3$$

This method is indicated that by feeding the input voltage into the saw-tooth oscillator, the pulse width modulation gain at the phase node is independent of the input voltage. Figure 3.4 can be represented as block diagram for close loop small signal analysis as shown in Figure 3.5.

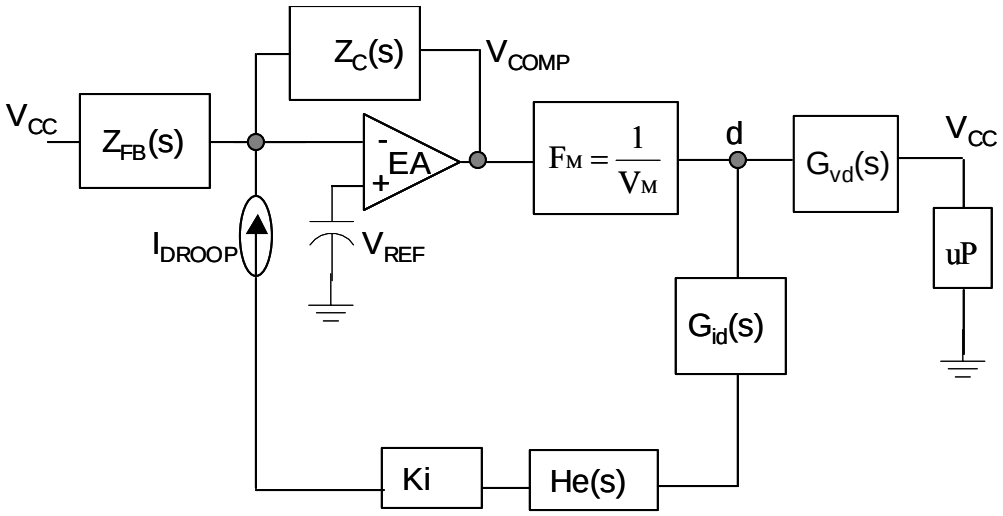



Figure 3.5 Block Diagram of Multiphase Buck Converter

The voltage $V_{COMP}$ at the output of error amplifier can be found by using the superposition method of $V_{CC}$, $I_{DROOP}$ and $V_{REF}$ sources.

Set $I_{DROOP}$ and $V_{REF}$ equal to zero, to find $V_{COMP}$:

$$V_{COMP} = -V_{CC} \cdot \frac{Z_C(s)}{Z_{FB}(s)} \qquad (3.3.4)$$

Set $V_{CC}$ and $V_{REF}$ equal to zero, to find $V_{COMP}$:

$$V_{COMP} = -I_{DROOP} \cdot Z_C(s) \qquad (3.3.5)$$

Set $I_{DROOP}$ and $V_{CC}$ equal to zero, to find $V_{COMP}$:

$$V_{COMP} = V_{REF} \cdot \left(1 + \frac{Z_{FB}(s)}{Z_C(s)}\right) \qquad (3.3.6)$$

Figure 3.5 can be redrawn with all block diagrams as shown in Figure 3.6.

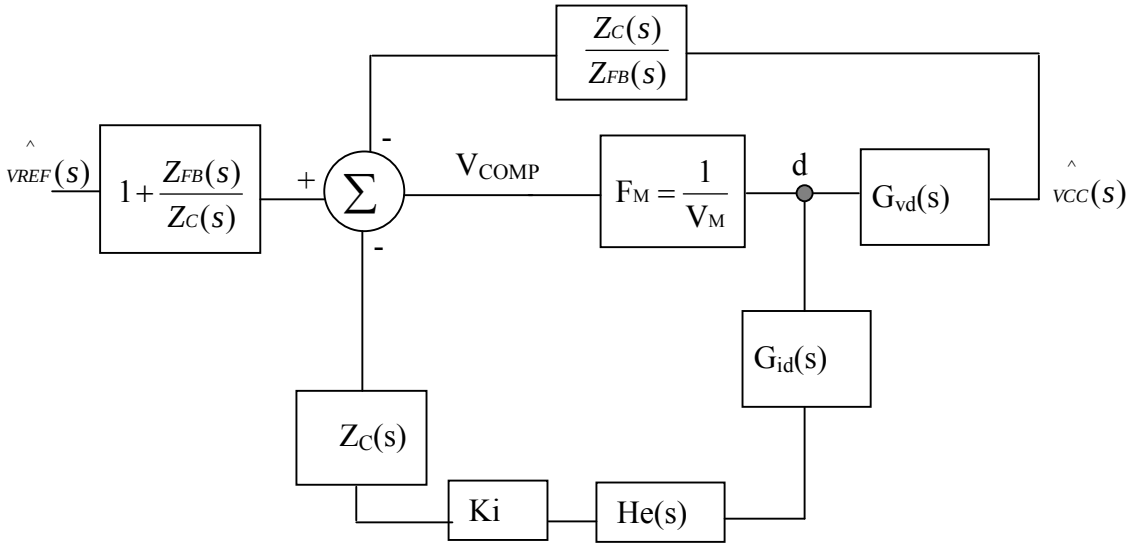



Figure 3.6 Close Loop Block Diagram of Multiphase Buck

For now we assume the small signal $V_{REF}$ equals zero. The following transfer functions can be obtained from Figure 3.6.

Voltage loop transfer function:

$$Gv(s) = Gvd(s) \cdot F_M \cdot \frac{Z_C(s)}{Z_{FB}(s)} \qquad (3.3.7)$$

Current loop transfer function:

$$Gi(s) = Gid(s) \cdot F_M \cdot Z_C(s) \cdot Ki \cdot He(s) \qquad (3.3.8)$$

Close current loop transfer function:

$$Gicl(s) = \frac{F_M}{1 + Gid(s) \cdot F_M \cdot Z_C(s) \cdot Ki \cdot He(s)} \qquad (3.3.9)$$

System loop transfer function:

$$Gloop(s) = \frac{Gvd(s) \cdot F_M \cdot \frac{Z_C(s)}{Z_{FB}(s)}}{1 + Gid(s) \cdot F_M \cdot Z_C(s) \cdot Ki \cdot He(s)} \qquad (3.3.10)$$

Ki is an inductor current gain. He(s) in the current loop is used to sample and hold the inductor current. In practice, this sampling restricts the useful frequency of the ac variation to values much less than the Nyquist rate fs/2. So a simple second order transfer function can be use:

$$He(s) = 1 + \frac{s}{\omega n \cdot Qz} + \frac{s^2}{\omega n^2} \qquad (3.3.11)$$

Where:

$$\omega n = fs \cdot \pi \cdot N\Phi \qquad (3.3.12a)$$

$$Qz = \frac{2}{\pi} \qquad (3.3.12b)$$

$N\Phi$ is total number of phase

The processor in laptop computer has different modes of operation to save power and extend battery life. When the processor recognizes to change the mode, the reference voltage of controller is also changed. This results the output voltage change along with reference voltage. The small signal transfer function from reference voltage to output voltage is:

$$\frac{\hat{V}_{CC}(s)}{\hat{V}_{REF}(s)} = \frac{\left(1 + \frac{Z_{FB}(s)}{Z_C(s)}\right) \cdot Gidcl(s) \cdot Gvd(s)}{1 + Gidcl(s) \cdot Gvd(s) \cdot \frac{Z_C(s)}{Z_{FB}(s)}} \qquad (3.3.13)$$

### 3.4 Compensator Design:

Figure 3.6 shows that this model is similar to the current mode control. In this model, the information of current and voltage loops are fed-back and then added together. The compensator $Z_C(s)$ appears in both voltage and current loops. Both voltage and current loops have resonant poles that caused by inductor and output capacitors. As a result, the poles and zeros can be designed by following the same guidelines for the current loop in the current mode control, such that:

$$\frac{Z_C(s)}{Z_{FB}(s)} = \frac{\omega i \cdot \left(1 + \frac{s}{\omega z}\right)}{s \cdot \left(1 + \frac{s}{\omega p}\right)} \qquad (3.4.1)$$

A zero ωz is placed to compensate for the power stage double pole so that the current loop will stable with a phase margin of about 90 degree. A pole ωp is placed in the high frequency range to filter the switching frequency and its harmonic noise.

Figure 3.7 and Figure 3.8 show the gain and phase plots of open loop of control to output and duty to inductor current transfer functions.

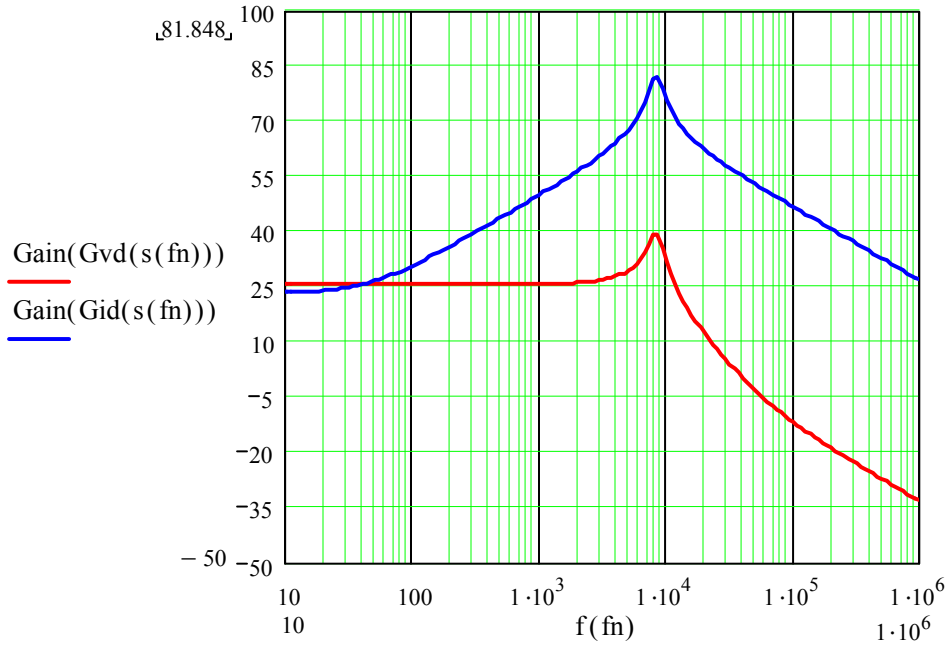



Figure 3.7 Gain Plot of Open Loop Duty to Output and Duty to Inductor Current

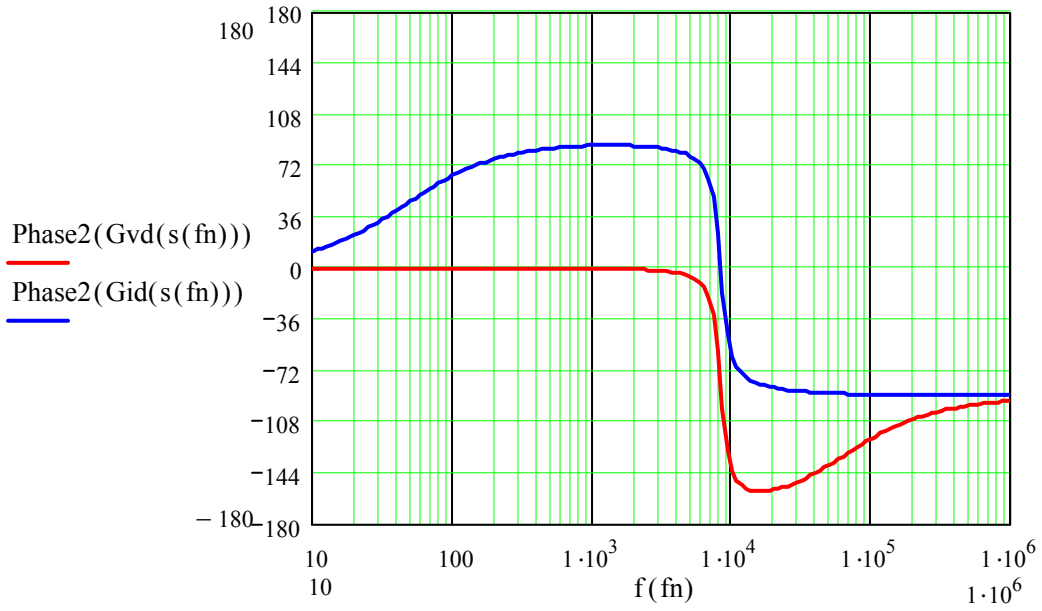



Figure 3.8 Phase Plot of Open Loop Duty to Output and Duty to Inductor Current

Figure 3.9 and Figure 3.10 show the gain and phase plots of voltage, current and close current loops transfer functions in close loop feedback.

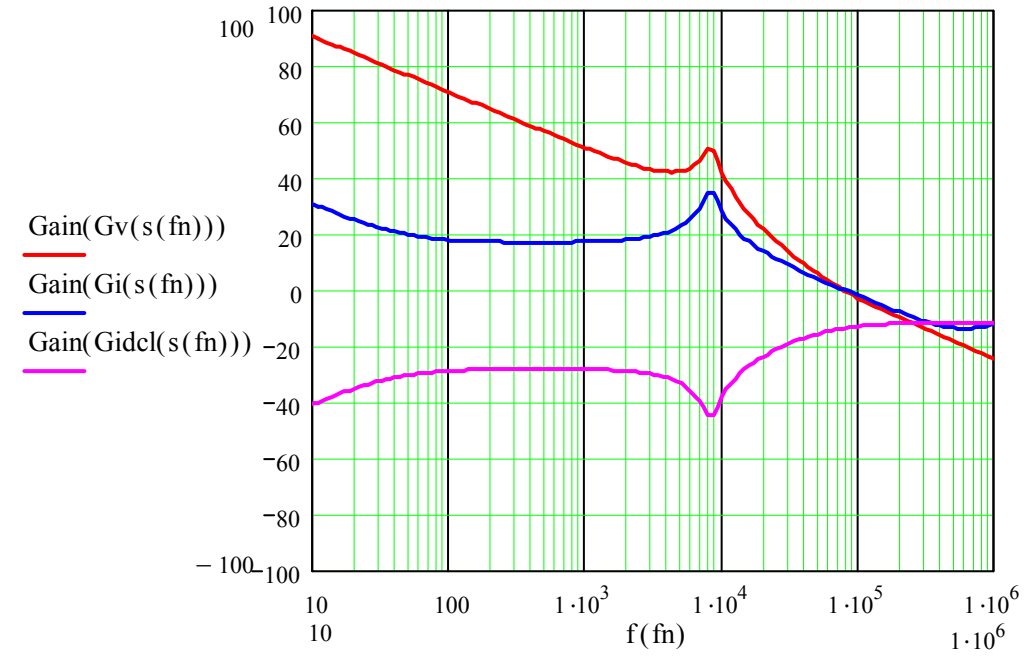



Figure 3.9 Gain Plot of Current and Voltage Loops

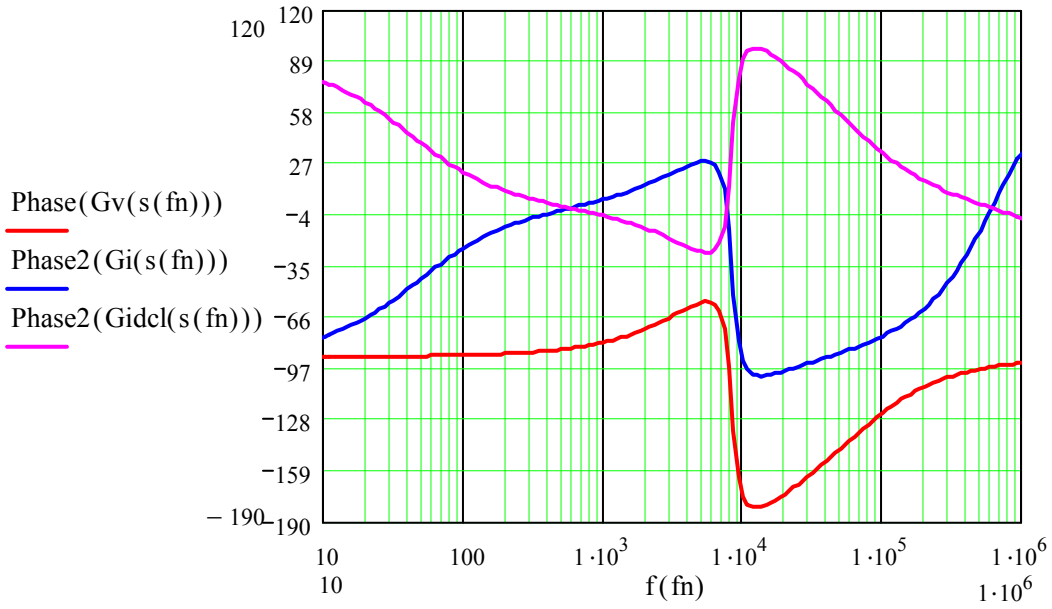



Figure 3.10 Phase Plot of Current and Voltage Loop

Figure 3.11 and Figure 3.12 show the gain and phase plots of converter close loop with load variation. As the load increases, the low-frequency gain decreases because the current loop gain increases. The crossover frequency is unchanged as load changes. The gain of close loop can be obtained by adding the voltage loop and inductor current close loop in decibels magnitude.

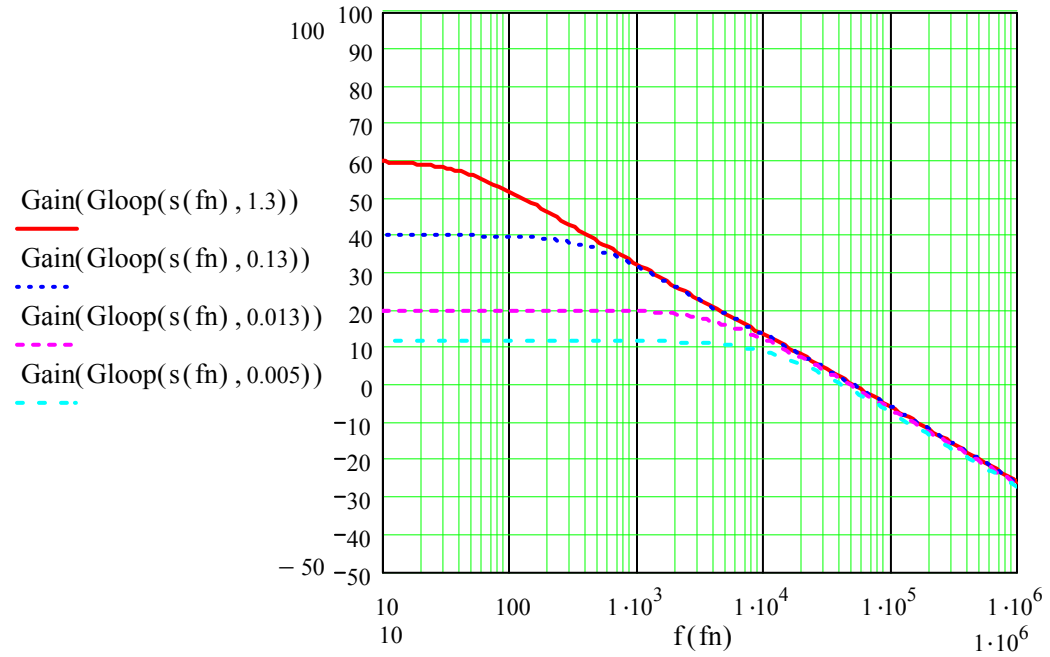



Figure 3.11 Gain of Converter Loop with Load Variation

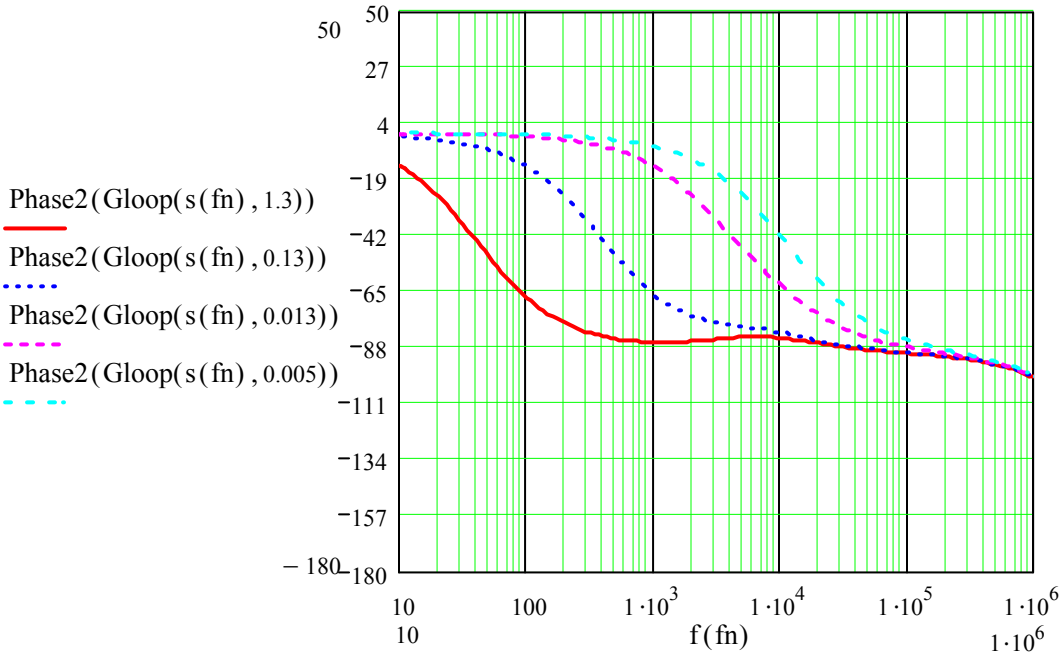



Figure 3.12 Phase of Converter Loop with Load Variation

### 3.5 Simulation Model

The simulation model can be draw as shown in Figure 3.13 to compare the result with the derived equation 3.3.10. Figure 3.14 shows the gain and phase plot.

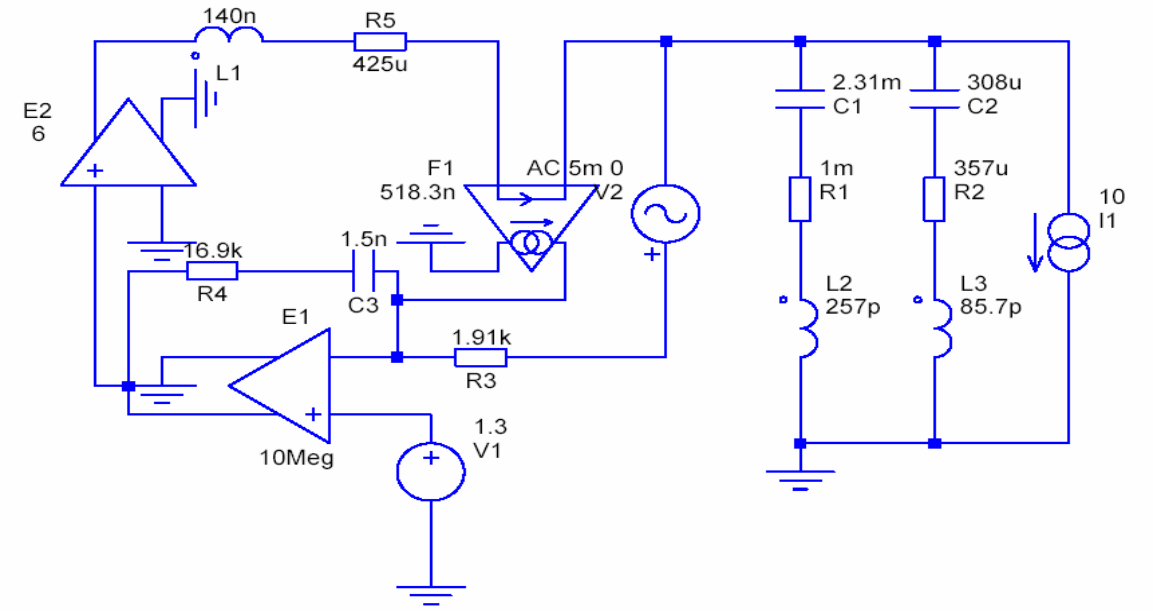



Figure 3.13 Simplis Simulation Model

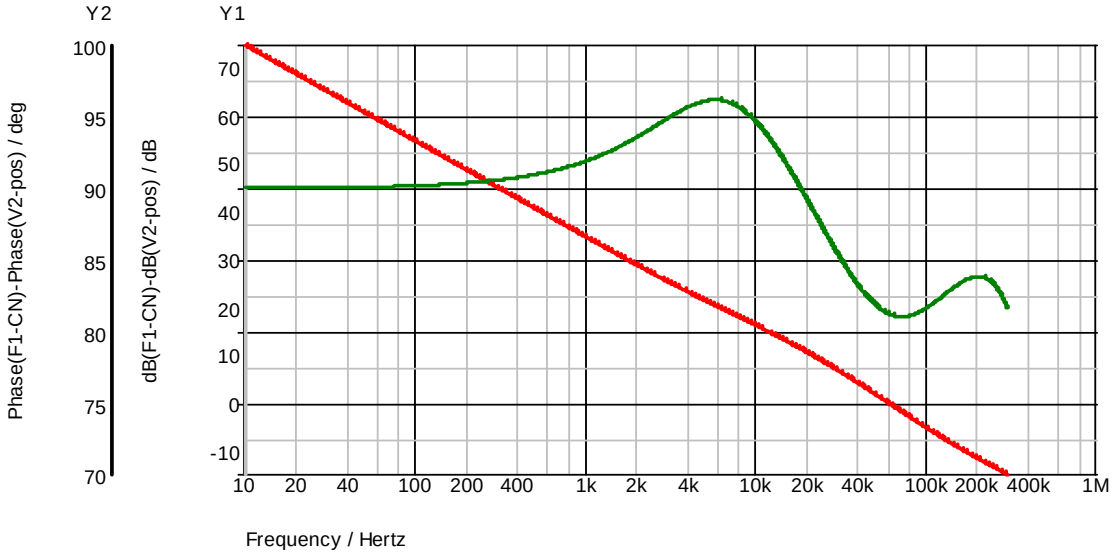



Figure 3.14 Gain and Phase Plot of Simulation Model

# Chapter 4 Experiment Results

## 4.1 Application Circuit Component Value

A 4-phase synchronous buck converter has been built to meet such an example of the Intel load line specifications in static and dynamic and output ripple voltage. The theoretical analysis and simulation of control loop are verified with the hardware results. The converter was also properly designed such that when the processor entered to or exited from a mode with minimum voltage undershoot or overshoot. The MOSFET had been selected to handle 20A per phase and provides high efficiency as well as the lower cost. Therefore, two of IRF7811W are paralleled for upper MOSFET; and two SI4362DY are paralleled for the lower MOSFET for each phase.

Converter Components Value:

$$\text{Number of Phase}: \ N\Phi = 4$$

$$\text{Input Voltage (V)}: \ V_{IN} = 19$$

$$\text{Output Inductor (H)}: \ L = \frac{0.56 \cdot 10^{-6}}{N\Phi}$$

$$\text{DCR of Inductor } (\Omega): \ R_L = \frac{1.7 \cdot 10^{-3}}{N\Phi}$$

$$\text{Output Capacitor (F)}: \ C = 7 \cdot 330 \cdot 10^{-6}$$

$$\text{Total ESR } (\Omega): \quad ESR = \frac{7 \cdot 10^{-3}}{7}$$

$$\text{Output Resistance } (\Omega): \ R_{OUT} = 1.3$$

$$\text{Switching Frequency (Hz)}: \ fs = 300 \cdot 10^{3}$$

$$\text{Sensing Resistor } (\Omega) \ \ Rsen = 820$$

$$\text{Current Gain}: \quad Ki = \frac{1.3 \cdot R_L}{Rsen}$$

$$\text{PWM Gain}: \quad F_M = \frac{2/3}{V_{IN}/9}$$

Compensation Network Circuit:

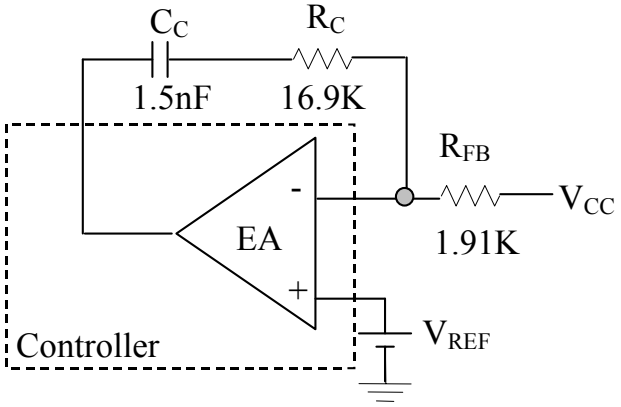



Figure 4.1 Compensation Network

### 4.2 Load Line and Efficiency

#### 4.2.1 Active Mode

Active mode is capable of delivering the maximum current. In Figure 4.2, the results of load line at different input voltage are matched very well. The processor voltage at no load condition is depended on the tolerance of DAC of controller and initial offset. The controller was randomly picked. The higher input voltage provided the lowest efficiency. The efficiency different between the highest and lowest voltage is 2.7% at full load condition. The input voltage was chosen to emulate 2, 3, 4 battery cells in series and a typical 19V for the adapter.

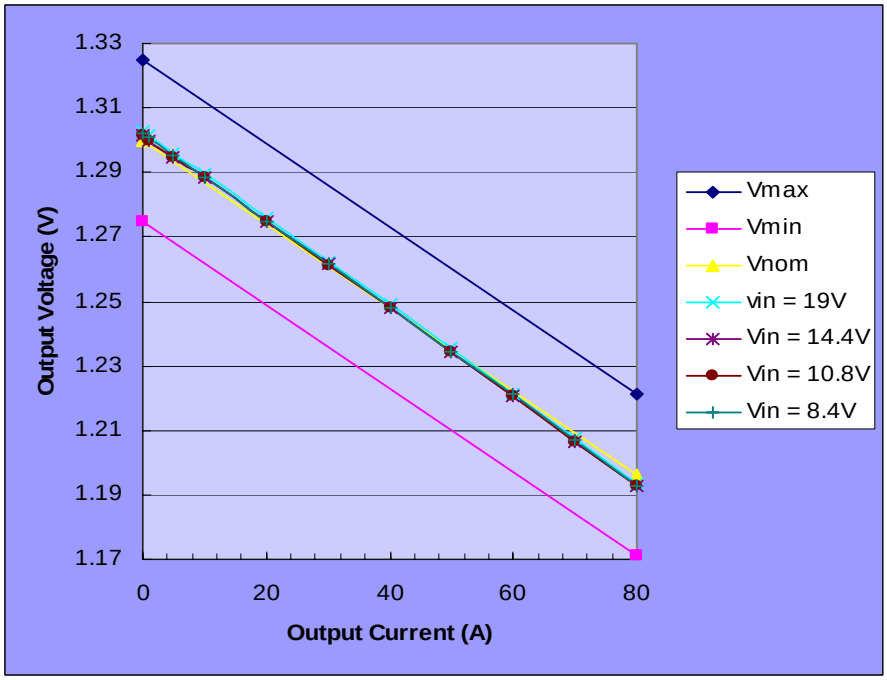



Figure 4.2 Load Line in Active Mode

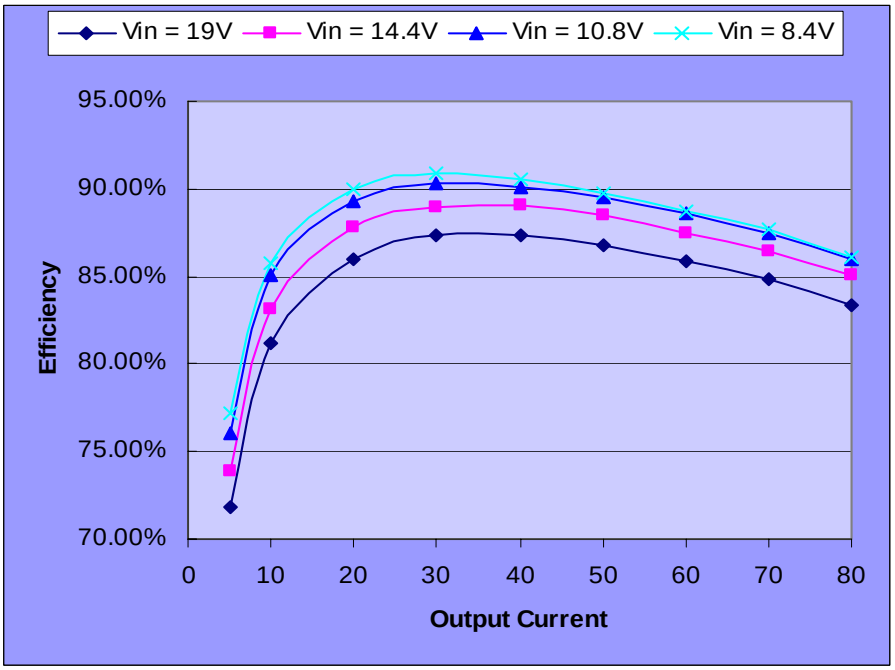



Figure 4.3 Efficiency in Active Mode

### 4.2.2 Deep Sleep Mode

Deep Sleep mode is usually run in very short time. Therefore, it is not necessary to reduce the number of phase. The maximum current to support during this mode is usually the leakage current of million transistors inside the processor. Each processor has different leakage current. The processor enters into Deep Sleep mode before enter into Deeper Sleep mode. The processor voltage in Deep Sleep mode is usually 1% to 2% lower than the voltage in Active mode. The tolerance of load line specification is same as in Active mode.

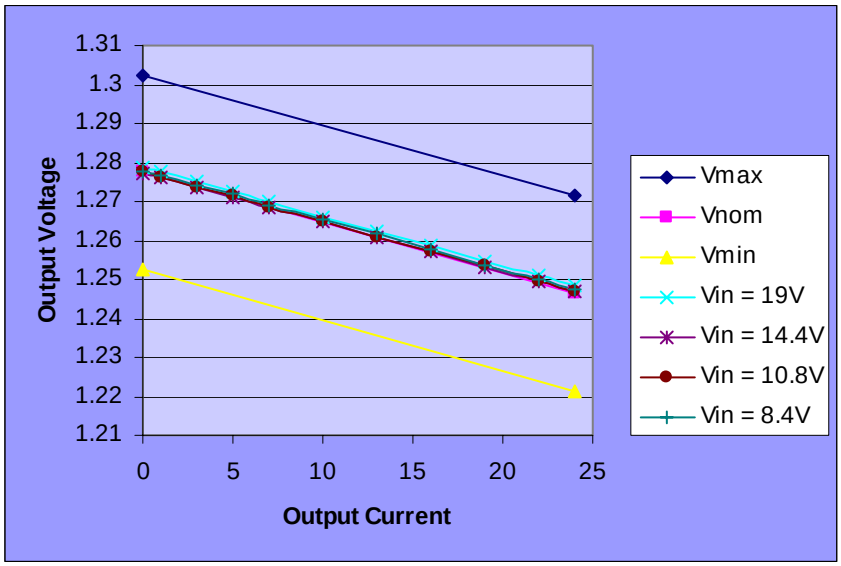



Figure 4.4 Load Line in Deep Sleep Mode

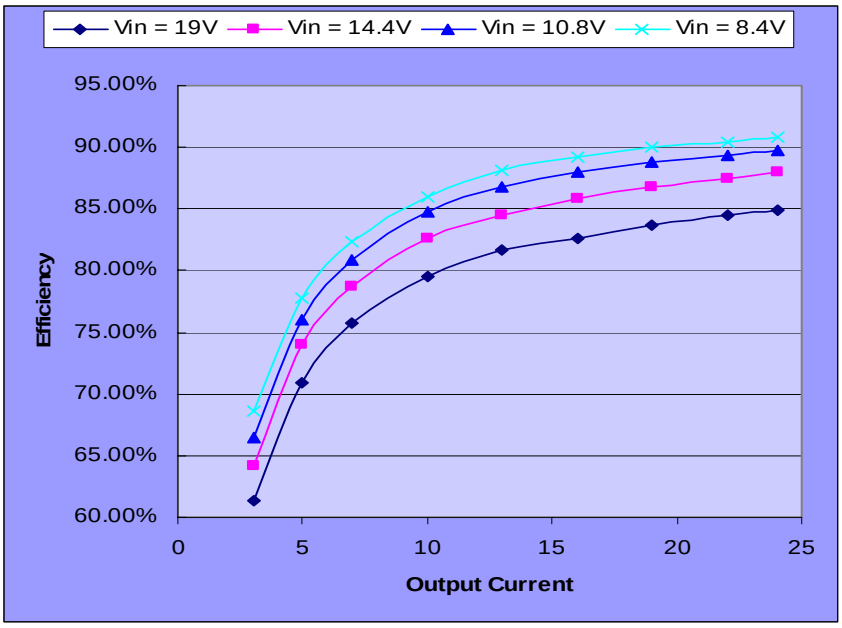



Figure 4.5 Efficiency in Deep Sleep Mode

### 4.2.3 Deeper Sleep Mode

Deeper Sleep mode is running under very low voltage and low current. Therefore, it does not require more than 1 phase to support the amount of current. The tolerance of load line specification is higher than in Active and Deep Sleep modes because the processor does not require tight tolerance specification this mode. Figure 4.7 shows significant efficiency improve by providing the VRC the battery voltage instead of adapter voltage.

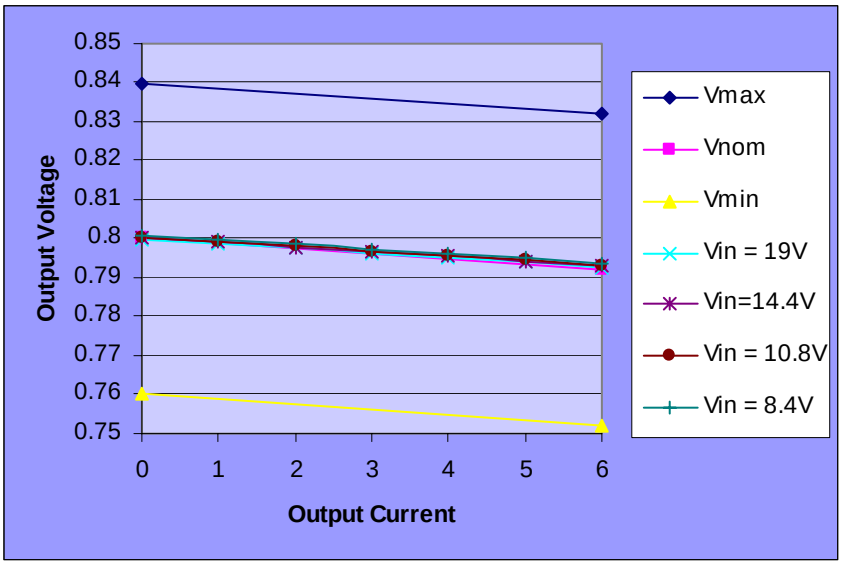



Figure 4.6 Load Line in Deeper Sleep Mode

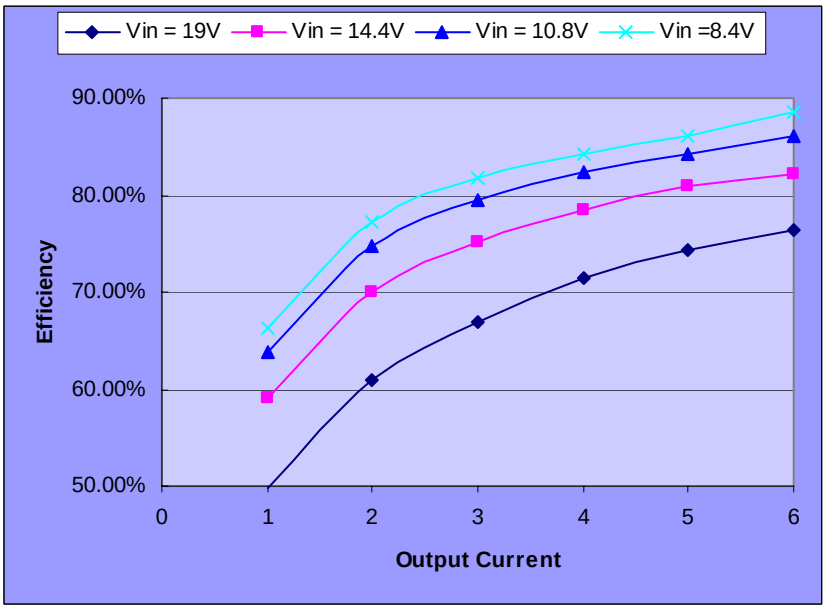



Figure 4.7 Efficiency in Deeper Sleep Mode

### 4.2.4 Efficiency versus Frequency in Active Mode

The efficiency results were obtained by changing the frequency while other parameters keep the same for comparison. The results showed that the efficiency was reduced by 4%

to 5% when the output current varied from 20 A to 80 A with twice the switching frequency. The efficiency of switching frequency at 930 khz was recorded with the maximum at 50A because the switching loss was significantly high. The extending efficiency curve will predict below 75% when the current reaches to 80 A.

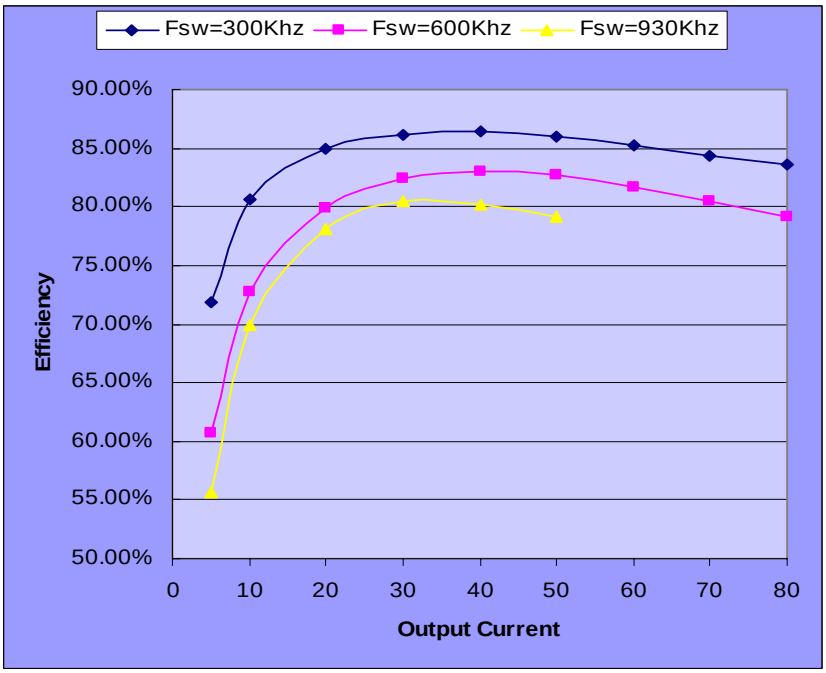



Figure 4.8 Efficiency vs. Frequency at 19V

### 4.2.5 Efficiency versus MOSFET

The efficiency could be improved by as much as 5% by selecting the better FOM of MOSFET. The results were compared to two paralleled of IRF7821 for upper and two paralleled of IRF7832 for lower for each phase.

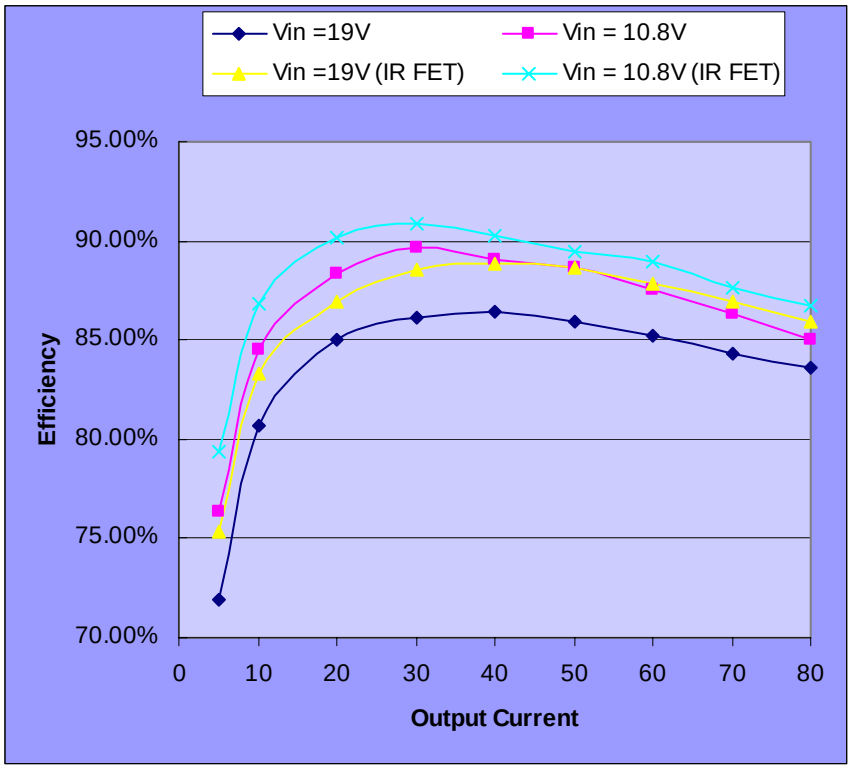



Figure 4.9 MOSFET Efficiency Comparison

### 4.2.6 Efficiency by Number of Phase

The efficiency could be improved significantly by reducing the number of phase when the converter can support the load with less number of phases. The results also showed that the efficiency could be improved by increasing the number of channels at certain load. For example, the efficiency of two channels is greater than one channel at 20 A load. In theory, the efficiency at full load of any number of phases can be predicted by the performance of one phase as shown in Figure 4.10.

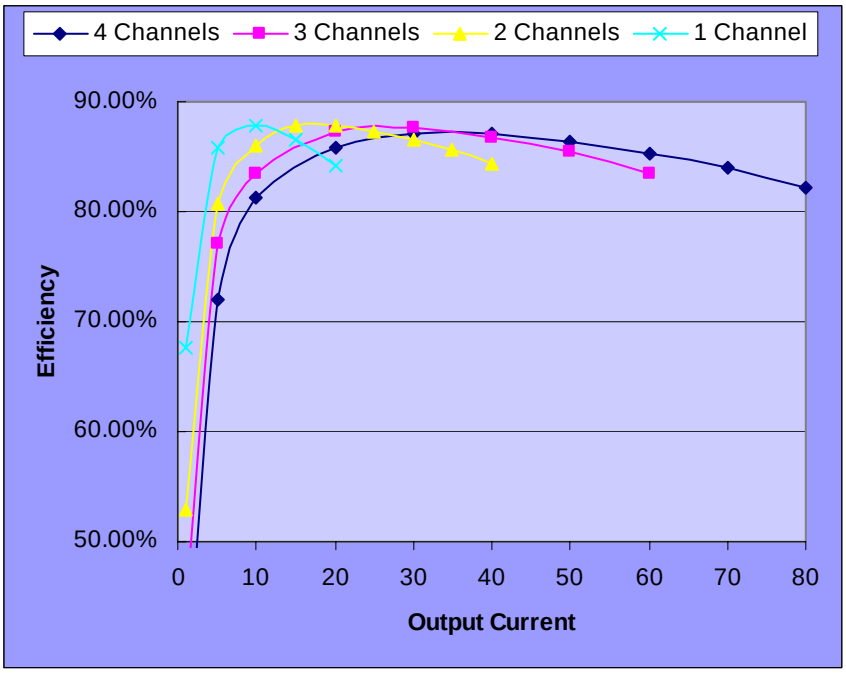



Figure 4.10 Efficiency vs. Number of Phase

### 4.3 Output Capacitor Options

Output capacitor takes very high portion in the total system cost in the VRC for laptop processor. Three cases of output capacitors have been examined and compared. All results meet the specifications. Option 1 provides the best solution for the load transient performance and lowest cost.

| Option | Low-Frequency Decoupling | Mid-Frequency Decoupling | Compensation Value |
|---|---|---|---|
| 1 | 7 x EEFSD0D331R (7mOhm) | 14 x 22uF (Ceramic) | $C_C$ = 1.5nF, $R_C$ = 16.9K |
| 2 | 8 x 2R5TPE330M9 (9m Ohm) | 14 x 22uF (Ceramic) | $C_C$ = 1.5nF $R_C$ = 13K |
| 3 | 6 x 2R5TPD680M5 (5mOhm) | 14 x 22uF (Ceramic) | $C_C$ = 1.5nF $R_C$ = 12.1K |

Table 4.3.1 Output Capacitor Options

### 4.3.1 Option 1

#### 4.3.1.1 Transient Response

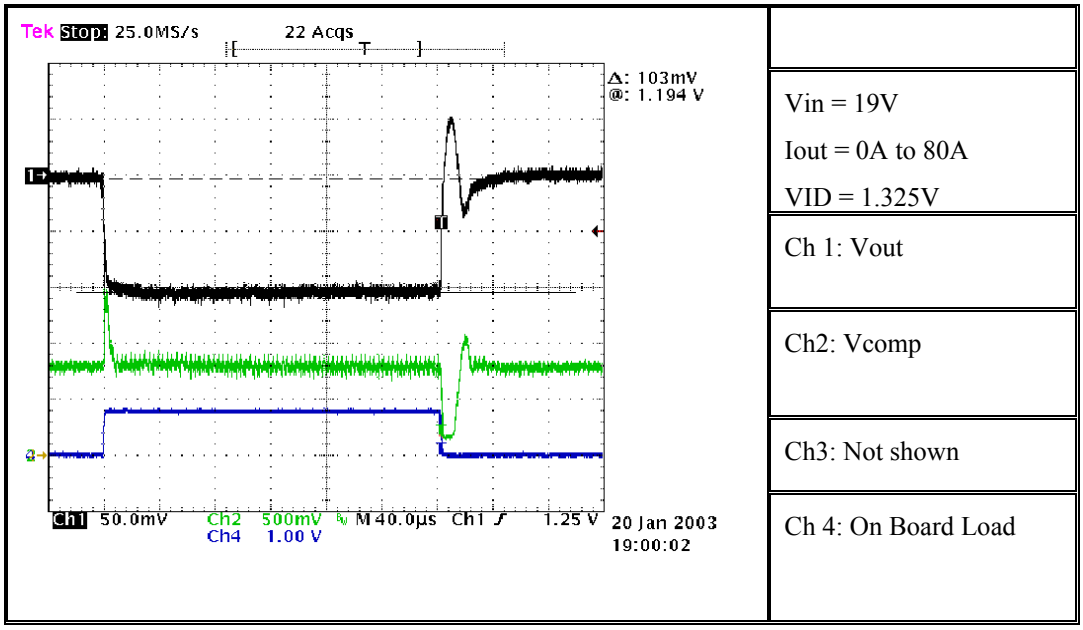



Figure 4.11 Transient Response of Option 1

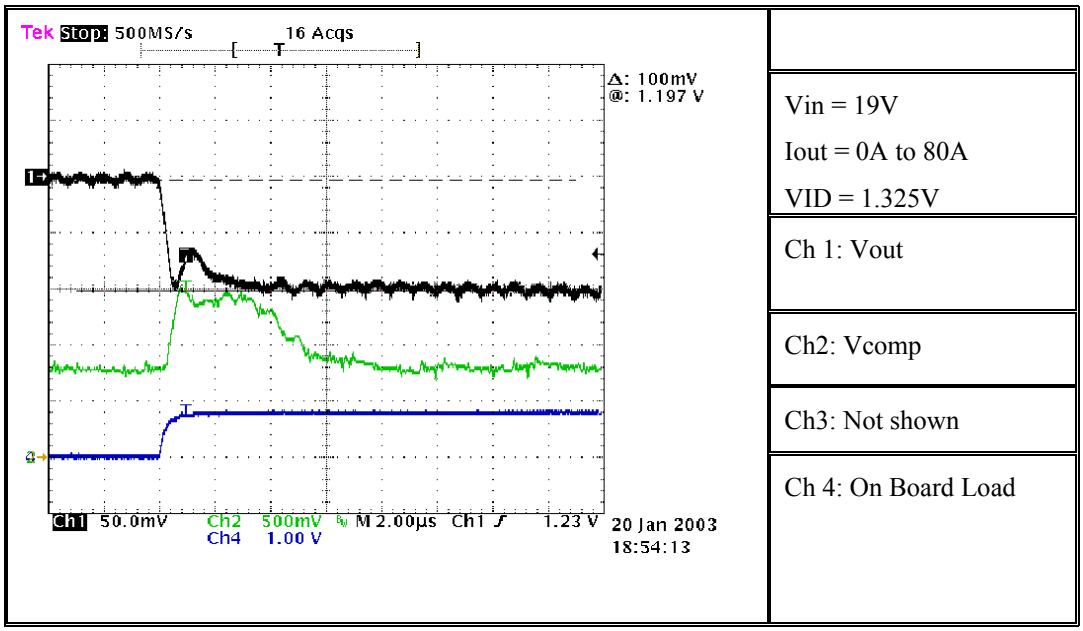



Figure 4.12 Zoom In of Load Current Rising Edge of Option 1

The slew rate of rising edge of the load is configured to 250A/uS and 150A/uS for the falling edge. In Figure 4.12, the initial processor voltage drop (100mV) of the VRC is met the load line specifications. This initial voltage drop should not lower than the nominal droop voltage, which is equaled to 104mV in this specification. The tolerance window, +/-20mV, should not utilize for the first initial voltage drop. After the load transient, the processor voltage is reached to the steady state in less than 4uS.

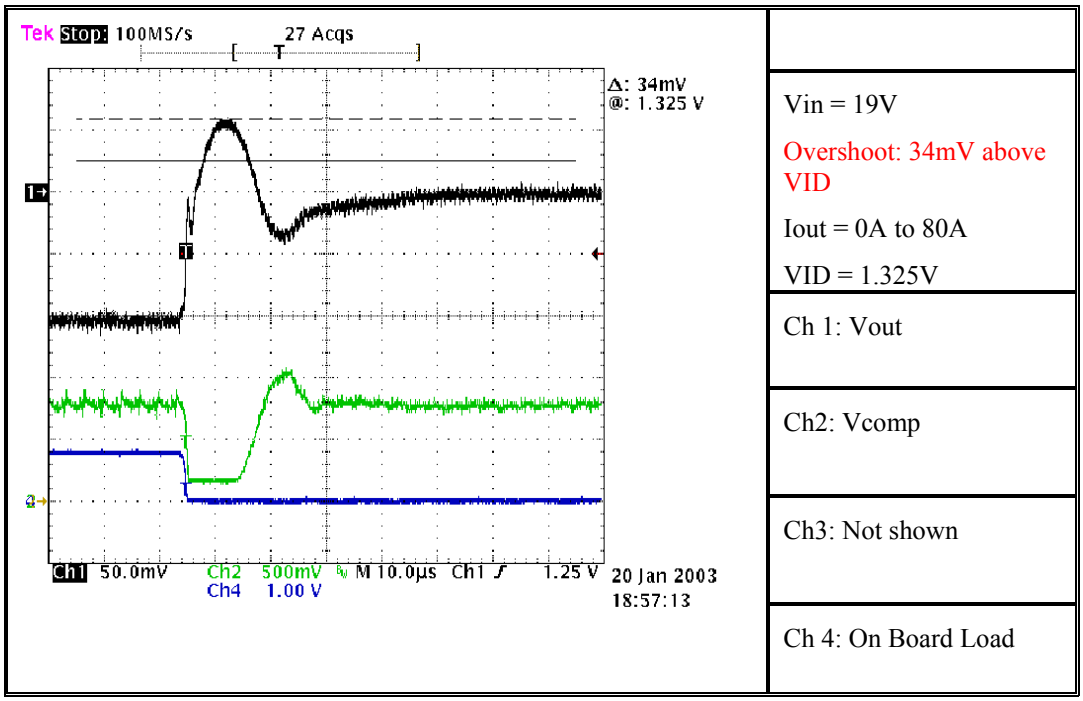


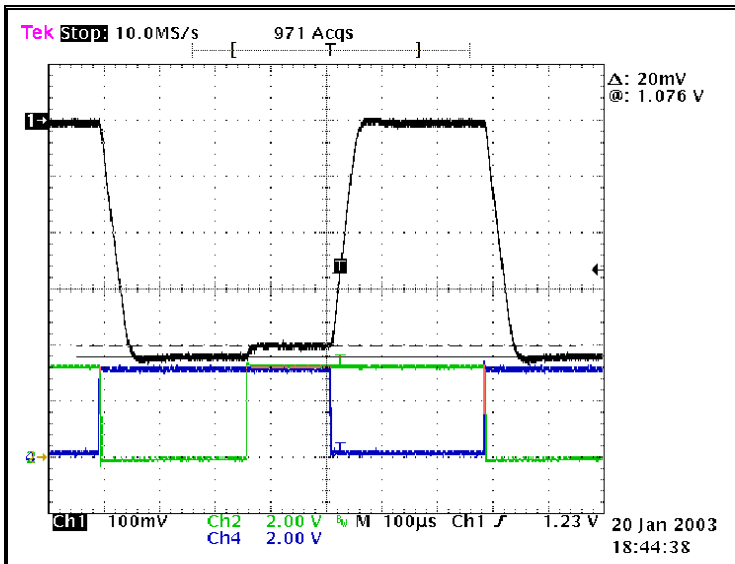

Figure 4.13 Zoom In of Load Current Falling Edge of Option 1

In Figure 4.13, the maximum output voltage of the VRC is met the load removable specifications as discussed in Chapter 2. The output voltage of the VRC has an overshoot of 34mV above the VID, which is 16mV less than the specifications. After the load removed, the processor voltage is reached to steady state in 40uS.

#### 4.3.1.2 Mode Transition

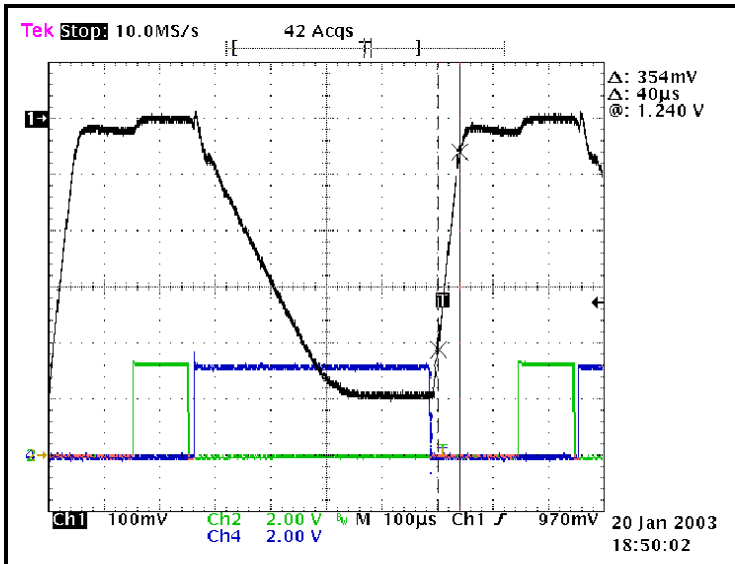
Geyserville transition mode offers mobile users two performance modes: Maximum Performance mode and Battery Optimized mode. Maximum Performance mode takes advantage of the additional power provided by an ac power source to provide a new level of mobile PC performance, while Battery Optimized mode provides optimal performance while running on battery. Intel's Geyserville technology enables this dual-mode capability by automatically changing the processor voltage and frequency when a user switches from AC or battery power. By reducing the voltage and frequency, power consumption will drop significantly with a relatively minor reduction in processor speed, allowing for robust performance without sacrificing battery life. The command for Geyserville mode is by change the VID and Deep Sleep reference at the same time.  The processor voltage should have minimized the undershoot and overshoot voltage when the processor enters or exits between modes. If the undershoot or overshoot is below or above the specification of load line, the processor will see the violation.

C4 transition mode is transiting from Active mode to Deep Sleep mode for very short time (around 10us) then finally enters into Deeper Sleep mode. During the entering into Deeper Sleep mode, the processor can exit any time. The converter should be able to respond and produce a stable output voltage. C4 mode can be achieved by changing the state of Deep Sleep and Deeper Sleep commands.




| |
|---|
| Vin = 19V<br>VID = 1.325V |
| Ch 1: Vout |
| Ch2: DSEN# |
| Ch3: Not shown |
| Ch 4: VID4 |

Figure 4.14 Geyserville Transition of Option 1




| |
|---|
| Vin = 19V<br>VID = 1.325V |
| Ch 1: Vout |
| Ch2: DSEN# |
| Ch3: Not shown |
| Ch 4: DRSEN |

Figure 4.15 C4 Transition of Option 1

#### 4.3.1.3 Loop Measurement Comparison

Figure 4.16 shows the gain and phase of the overall system loop. The crossover frequency of the VRC at zero decibel horizontal line is around 65kHz, which is same as the ESR zero frequency of output capacitors. The phase margin of the VRC is around 90 degree. These results agreed with the theoretical analysis and simulation results as shown in Figure 4.17 to Figure 4.19.

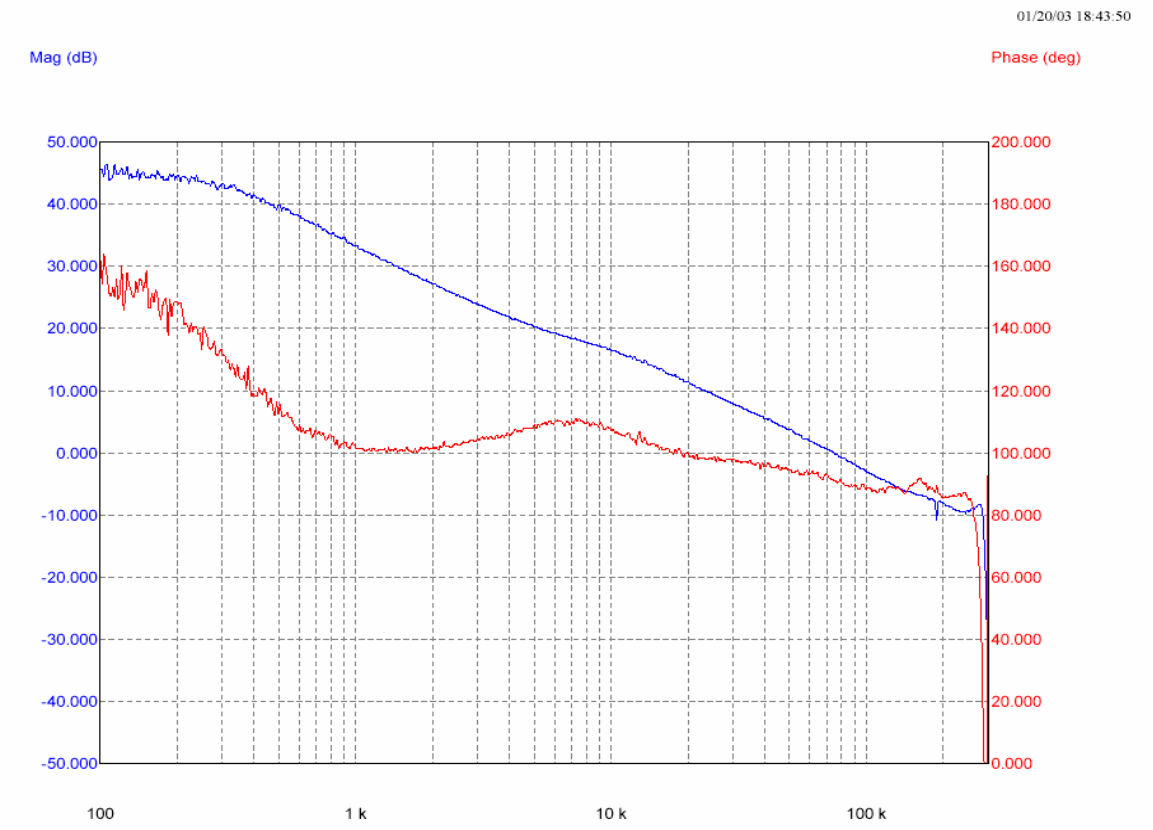



Figure 4.16 Gain and Phase of Overall System Loop Measurement of Option 1

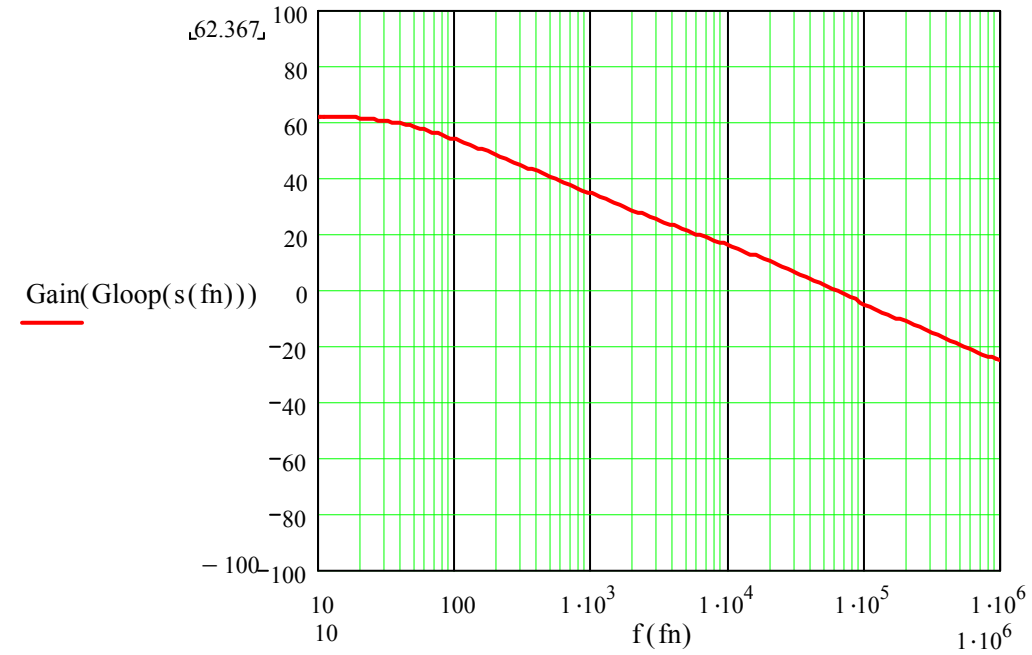



Figure 4.17 Gain Plot of Analysis Model of Option 1

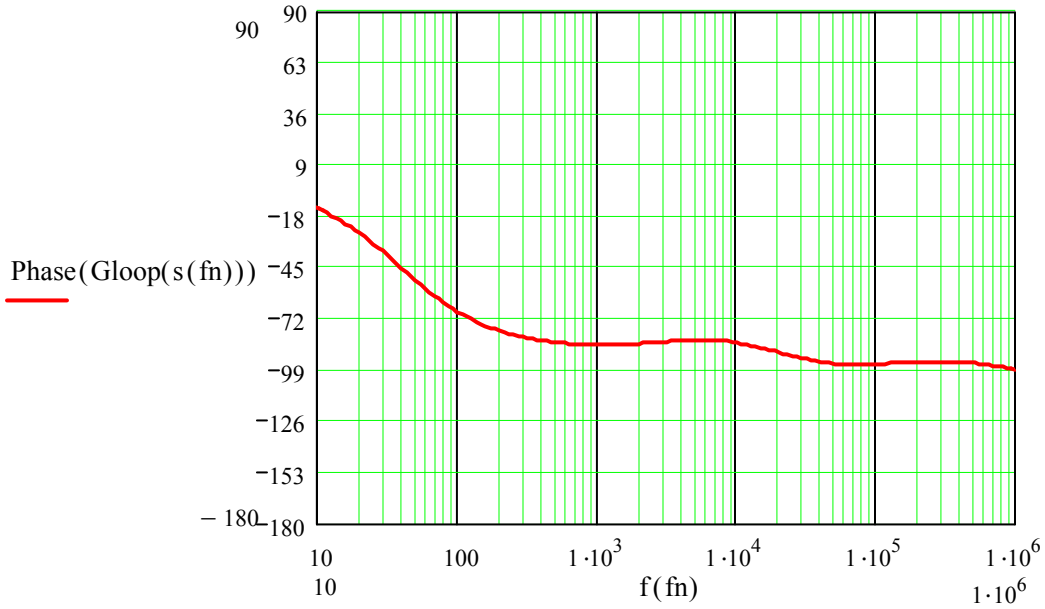



Figure 4.18 Phase Plot of Analysis Model of Option 1

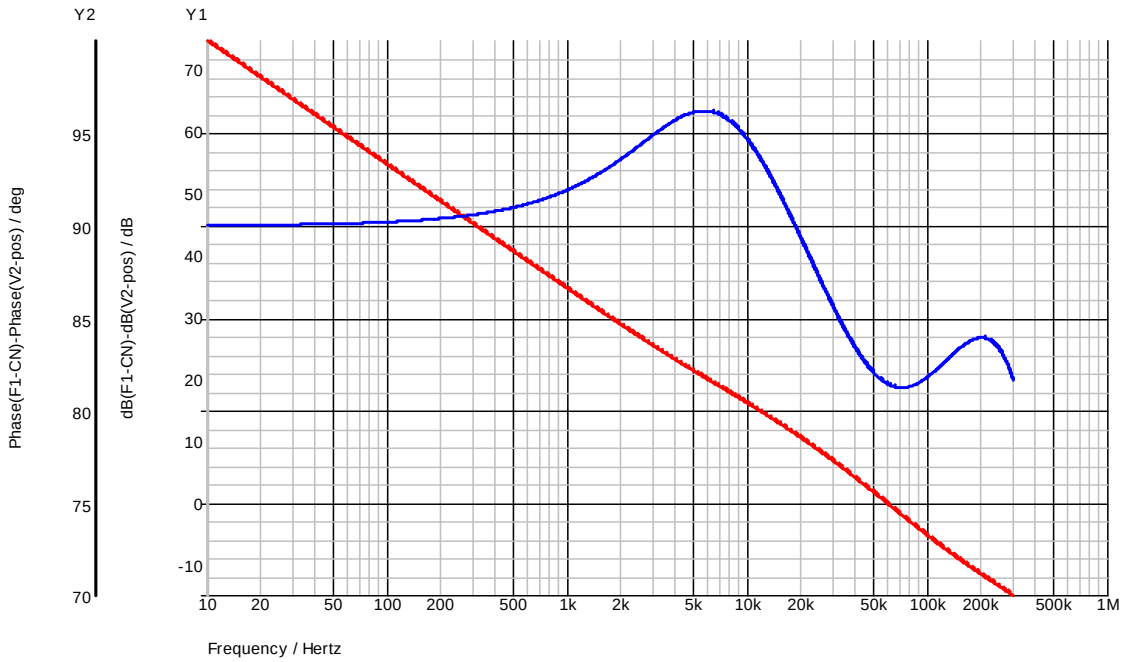



Figure 4.19 Gain and Phase Plot of Simulation of Option 1

### 4.3.2 Option 2

#### 4.3.2.1 Transient Response

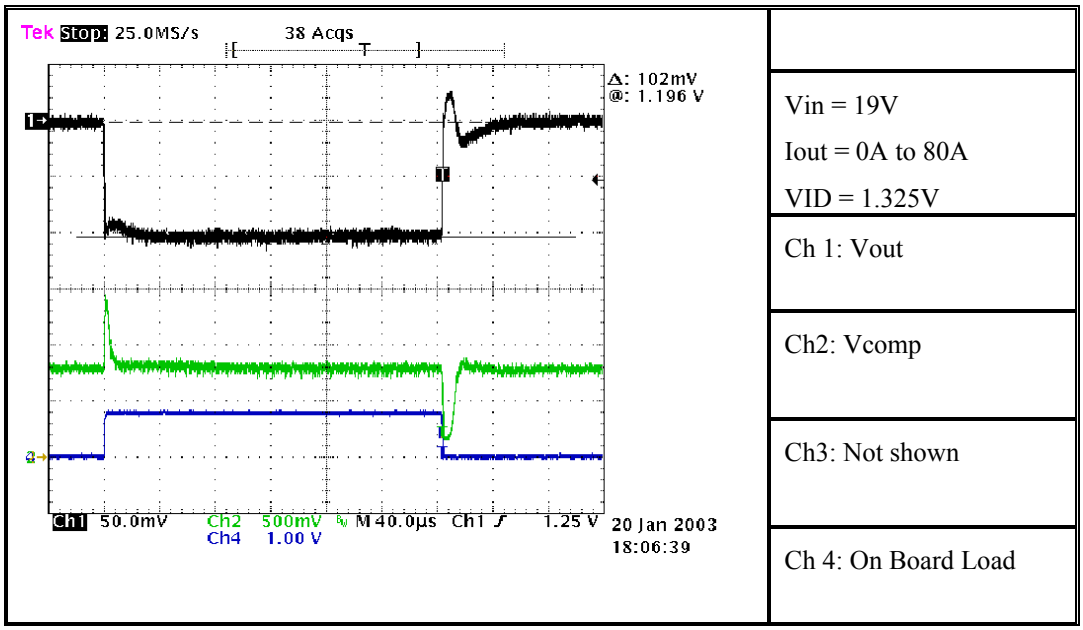



Figure 4.20 Transient Response of Option 2

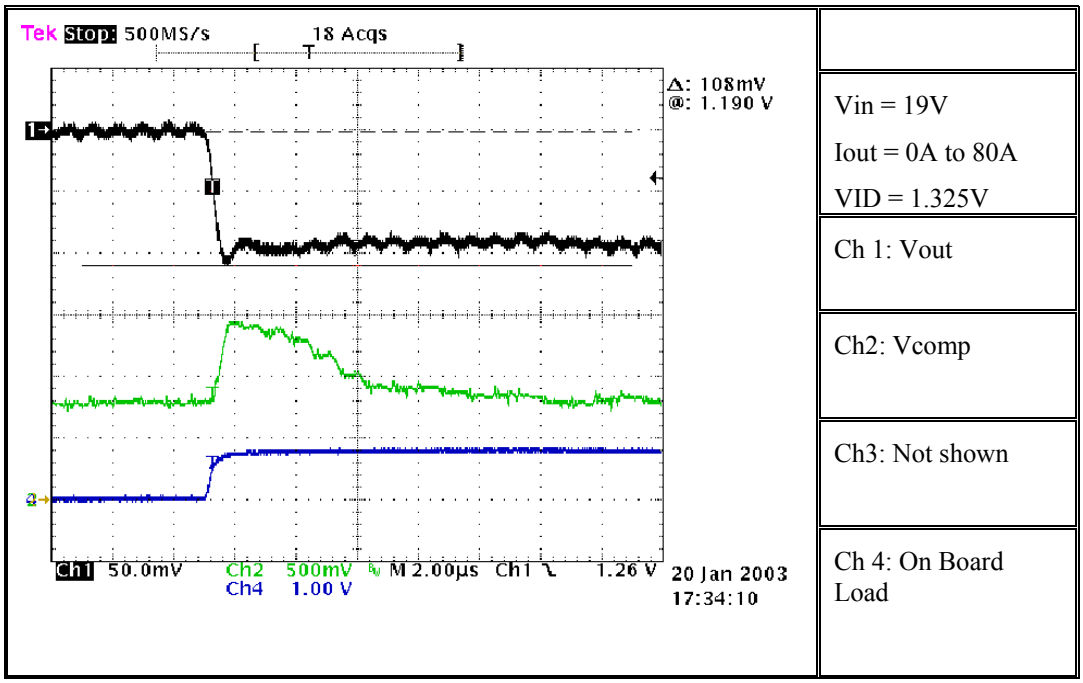



Figure 4.21 Zoom In of Load Current Rising Edge of Option 2

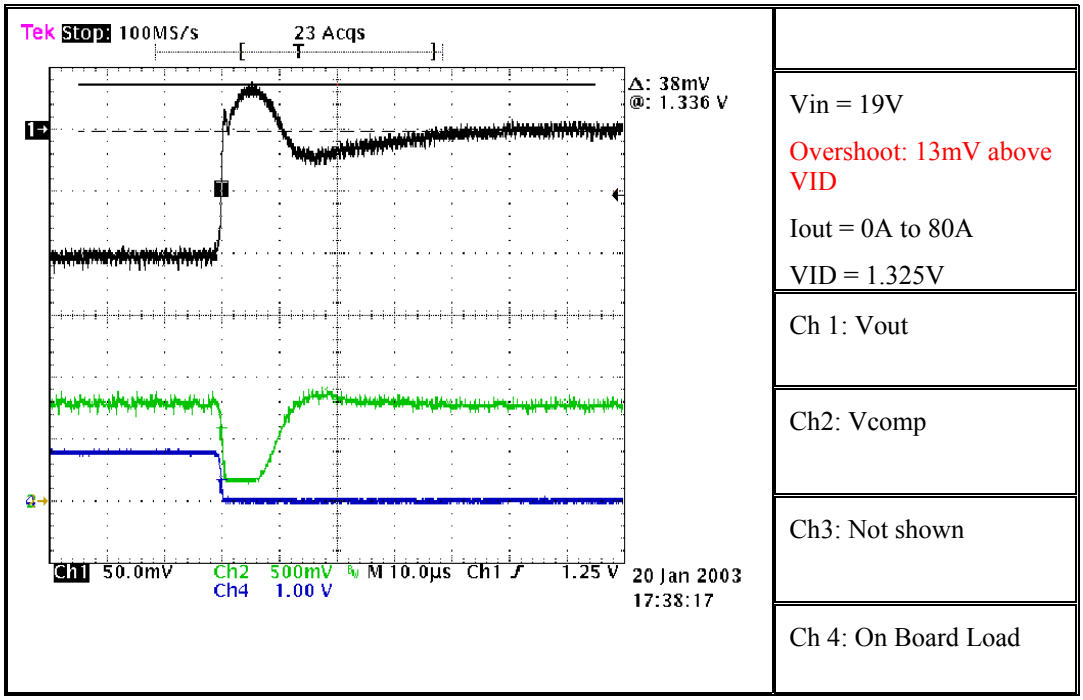



Figure 4.22 Zoom In of Load Current Rising Edge of Option 2

### 4.3.2.2 Mode Transition

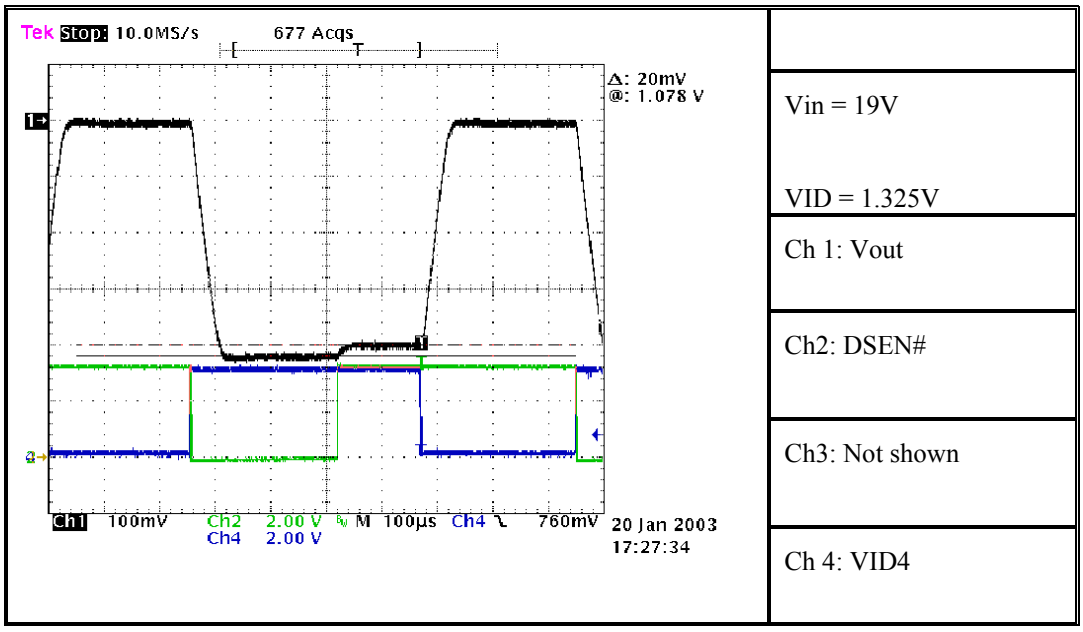



Figure 4.23 Geyserville Transition of Option 2

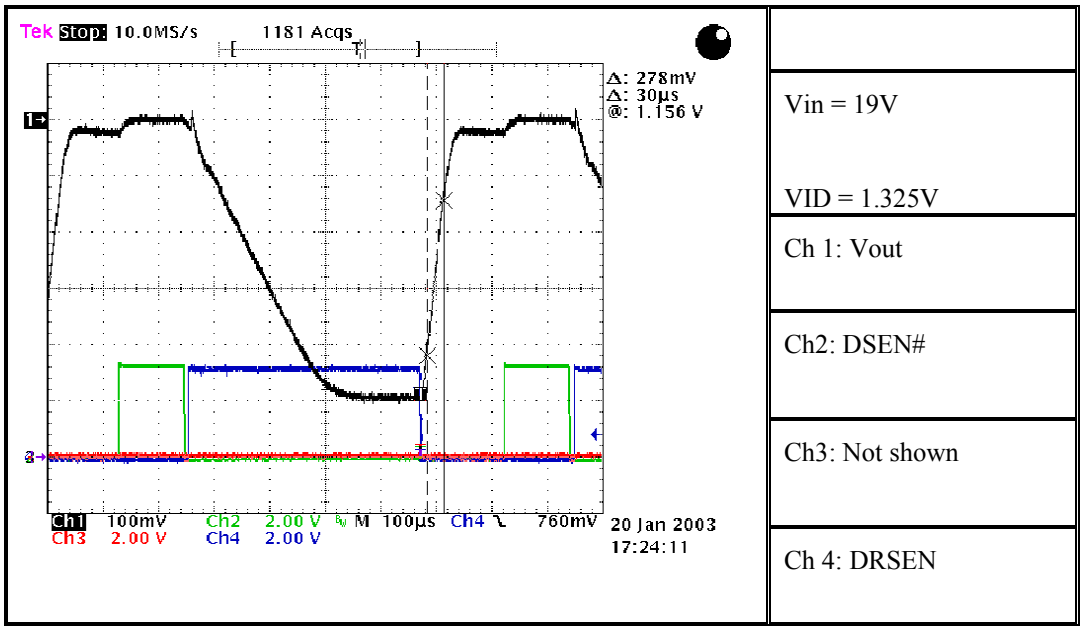



Figure 4.24 C4 Transition of Option 2

### 4.3.2.3 Loop Measurement Comparison

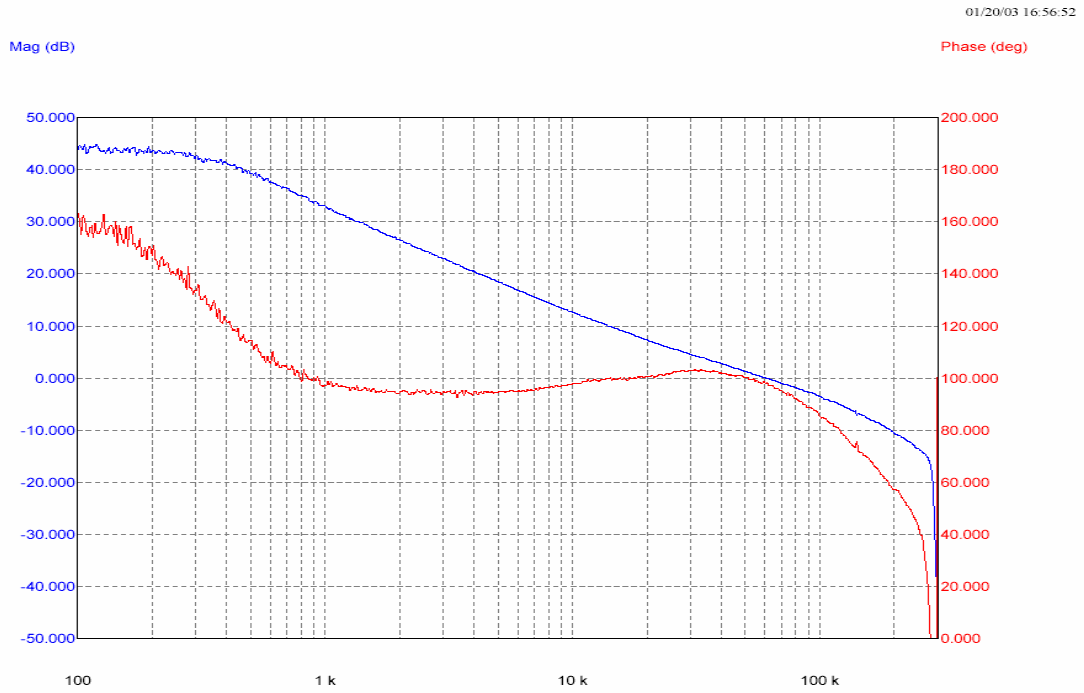



Figure 4.25 Gain and Phase of Overall System Loop Measurement of Option 2

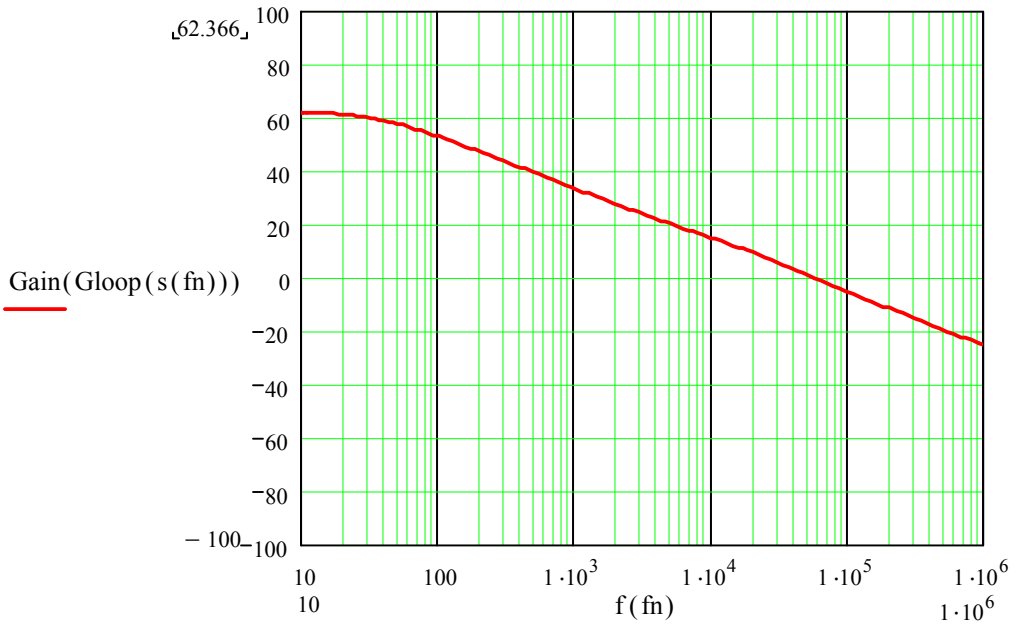



Figure 4.26 Gain Plot of Analysis Model of Option 2

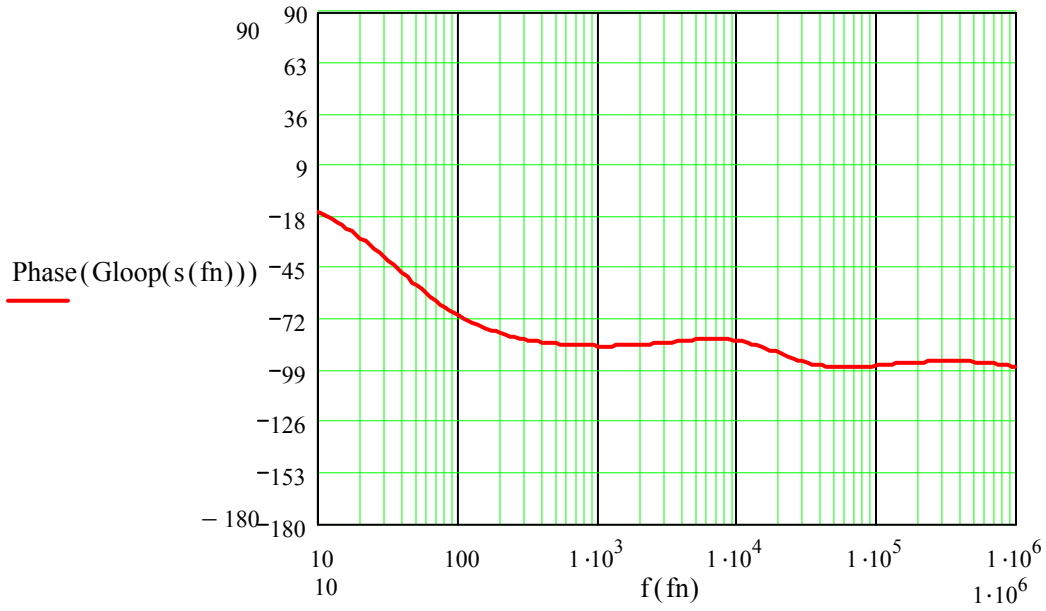



Figure 4.27 Phase Plot of Analysis of Option 2

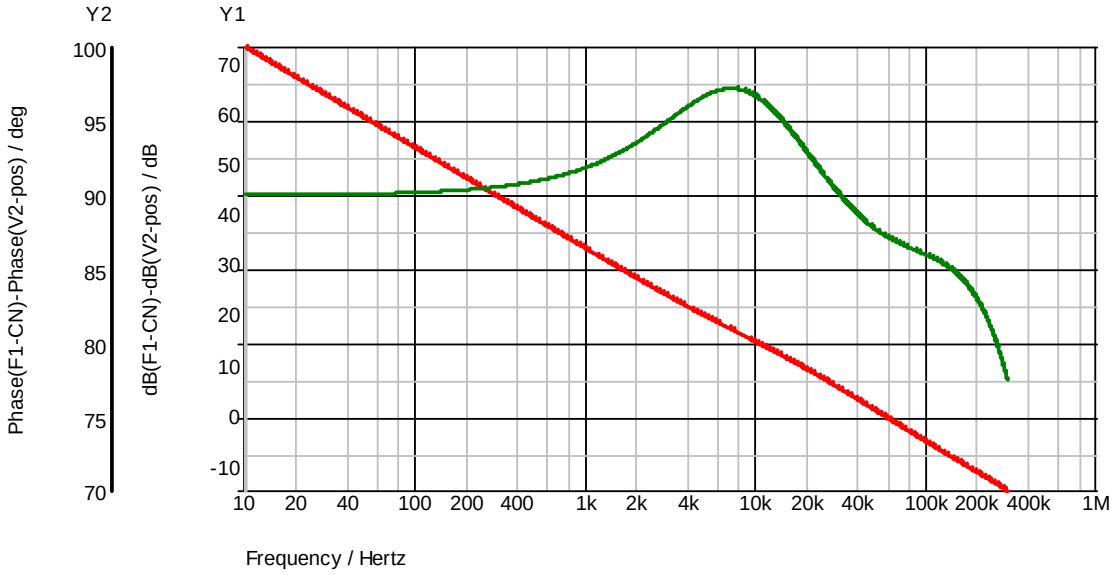
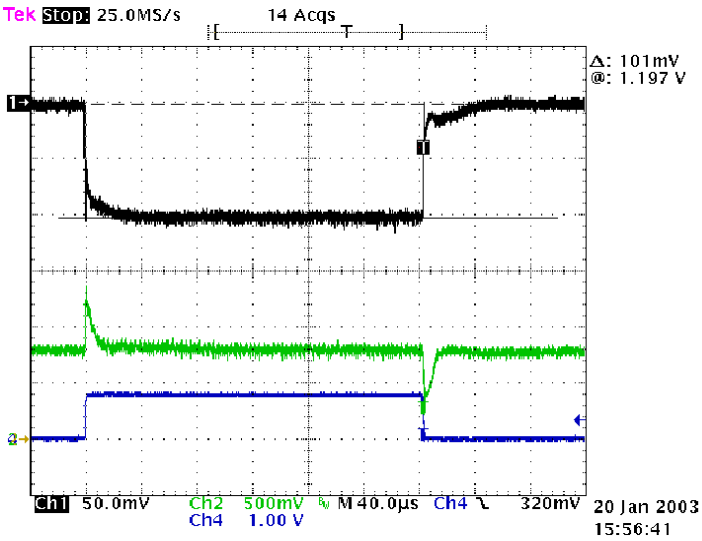



Figure 4.28 Gain and Phase Plot of Simulation of Option 2

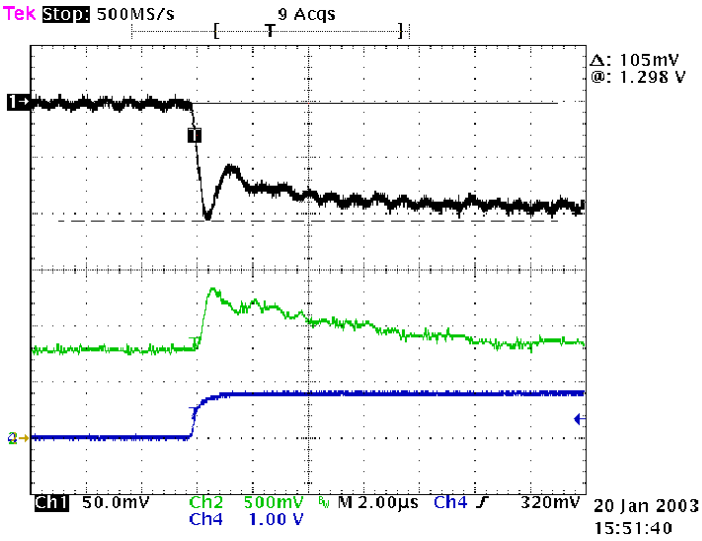
### 4.3.3 Option 3

#### 4.3.3.1 Transient Response




| |
|---|
| Vin = 19V<br>Iout = 0A to 80A<br>VID = 1.325V |
| Ch 1: Vout |
| Ch2: Vcomp |
| Ch3: Not shown |
| Ch 4: On Board Load |

Figure 4.29 Transient of Option 3




| |
|---|
| Vin = 19V<br>Iout = 0A to 80A<br>VID = 1.325V |
| Ch 1: Vout |
| Ch2: Vcomp |
| Ch3: Not shown |
| Ch 4: On Board Load |

Figure 4.30 Zoom In Rising Edge Transient of Option 3

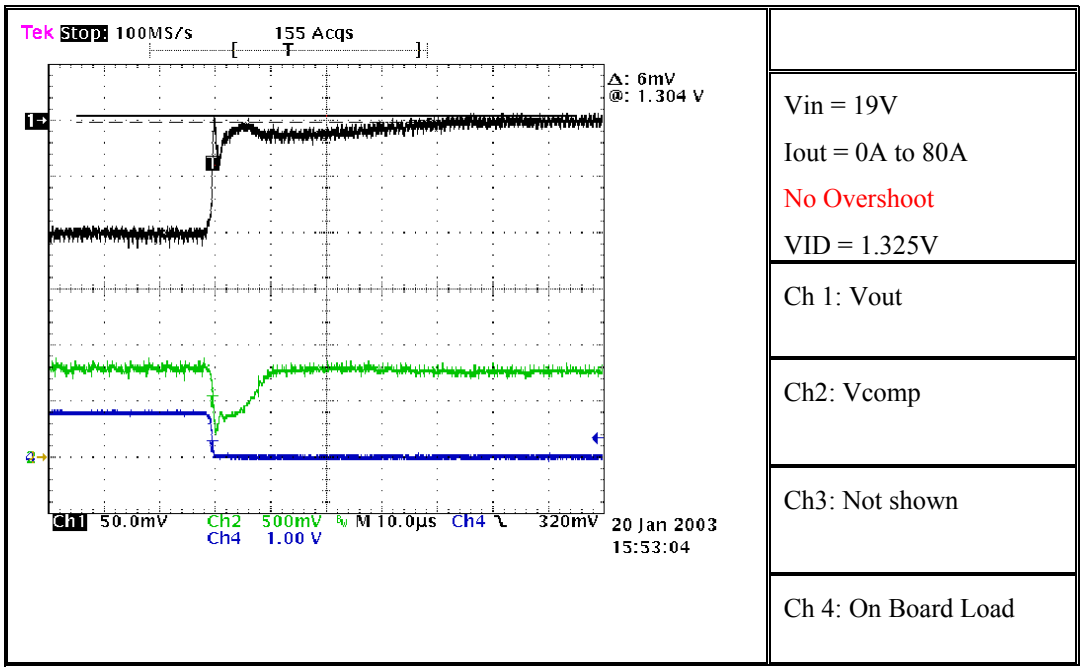



Figure 4.31 Zoom In Falling Edge Transient of Option 3

### 4.3.3.2 Mode Transition

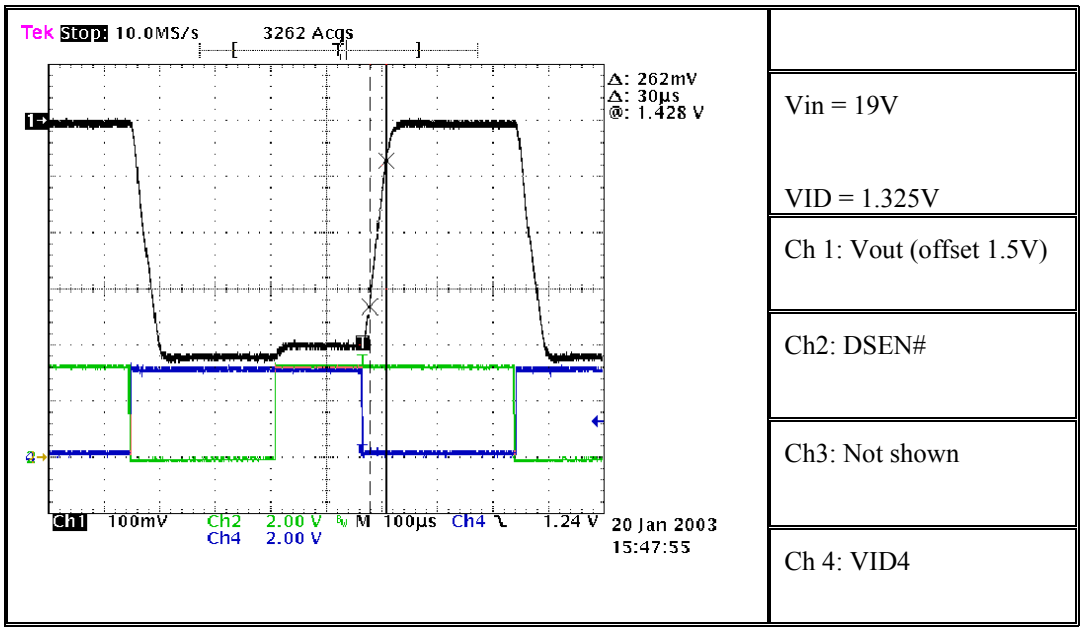



Figure 4.32 Gyserville Transition of Option 3

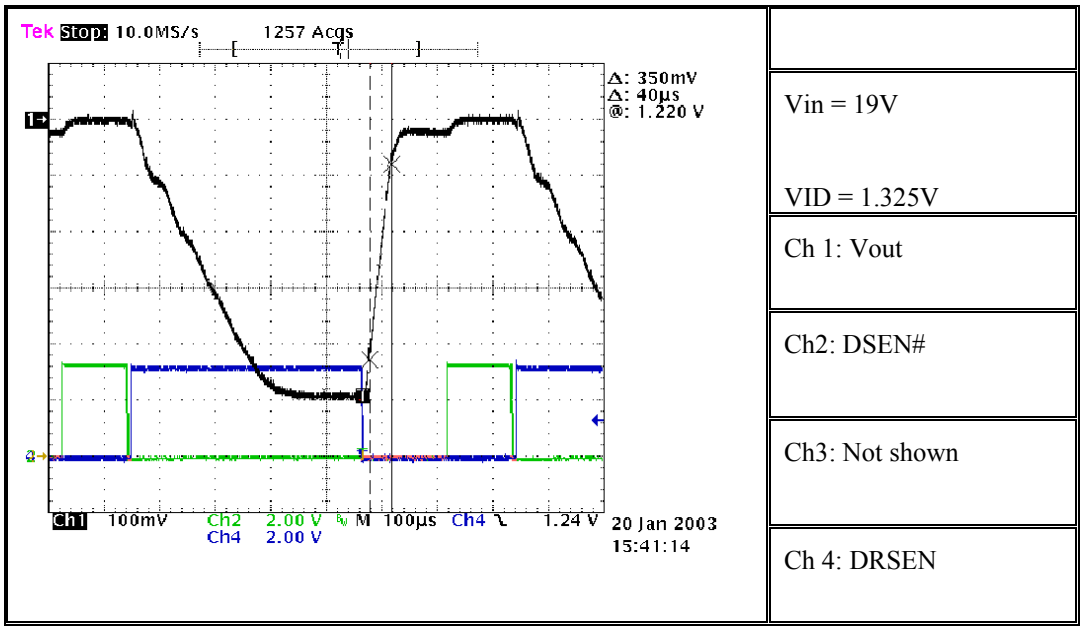



Figure 4.33 C4 Transition of Option 3

### 4.3.3.3 Control Loop Comparison

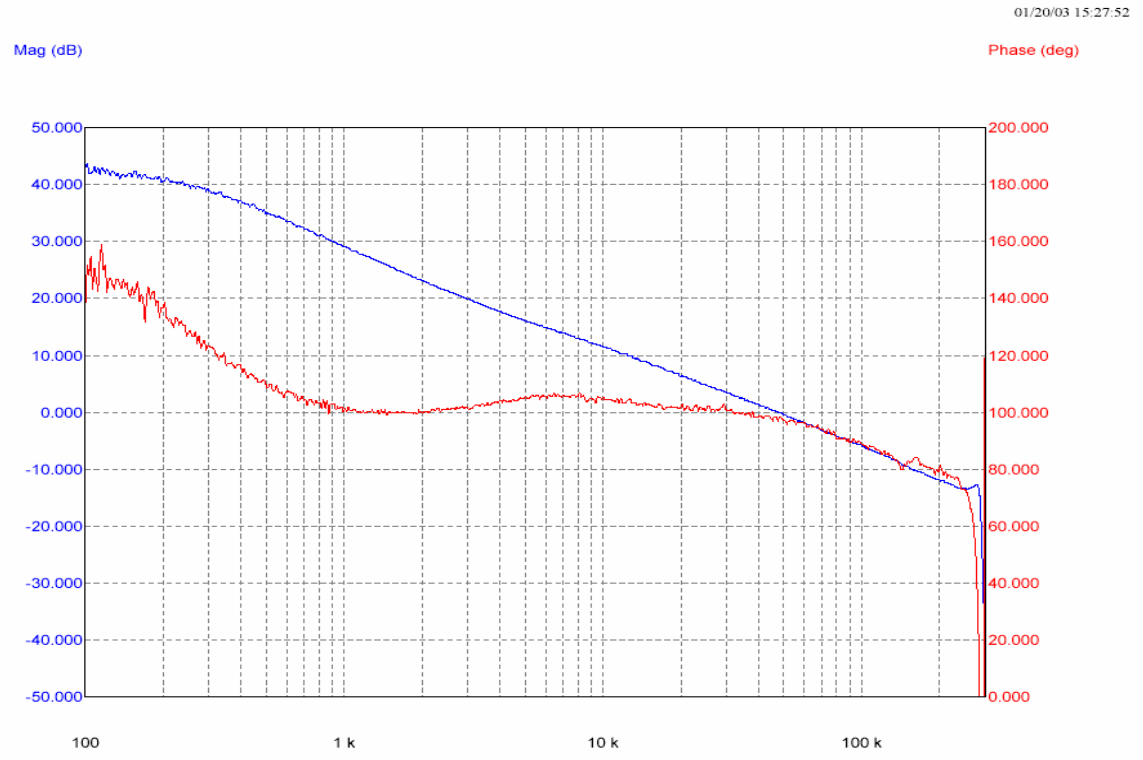



Figure 4.34 Gain and Phase of Overall System Loop Measurement of Option 3

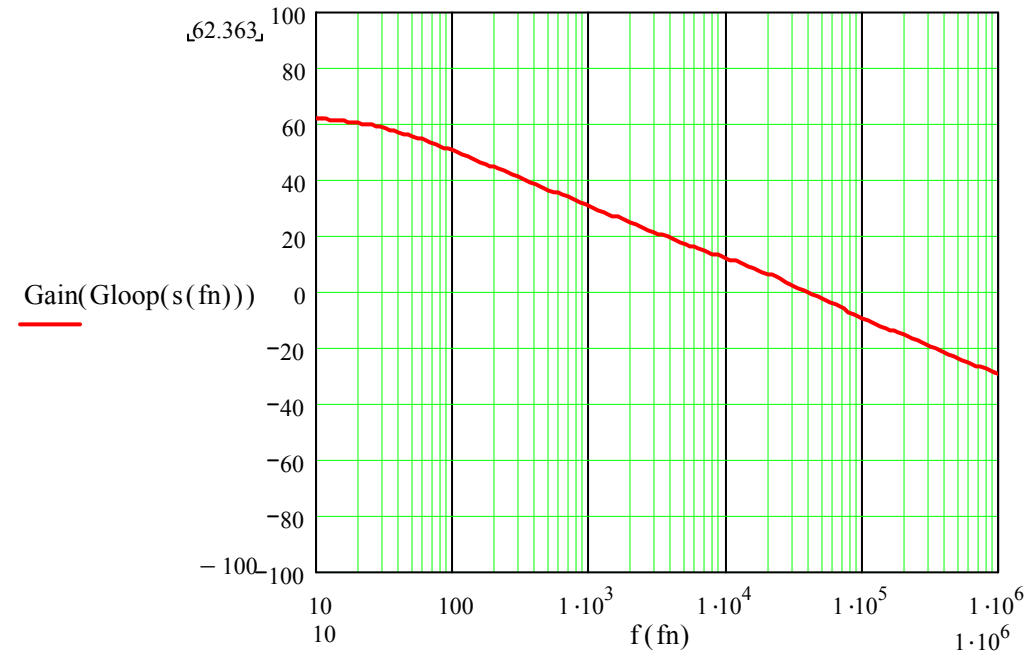



Figure 4.35 Gain Plot of Analysis Model of Option 3

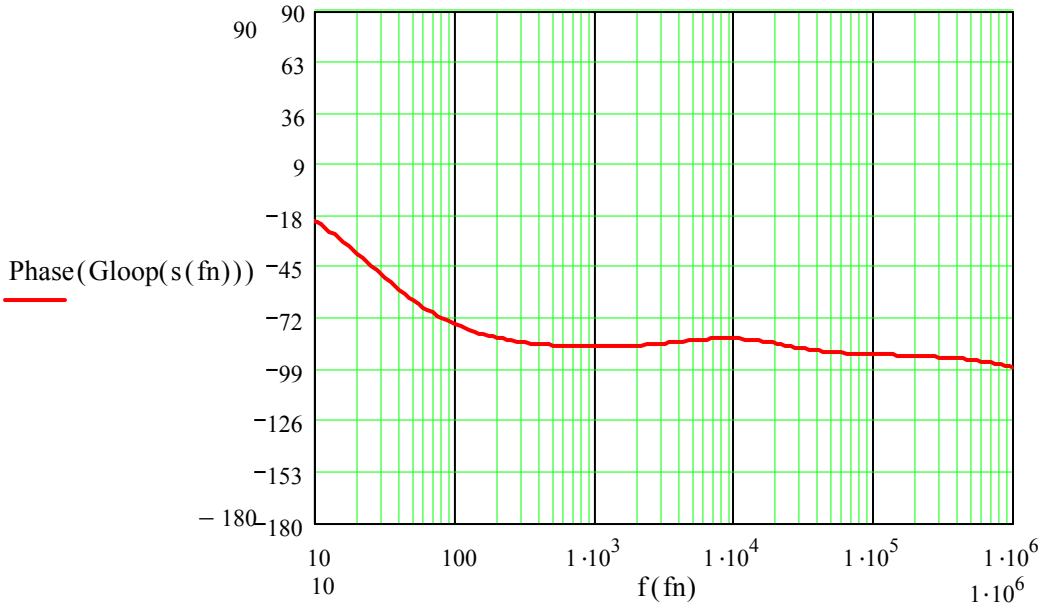



Figure 4.36 Phase Plot of Analysis Model of Option 3

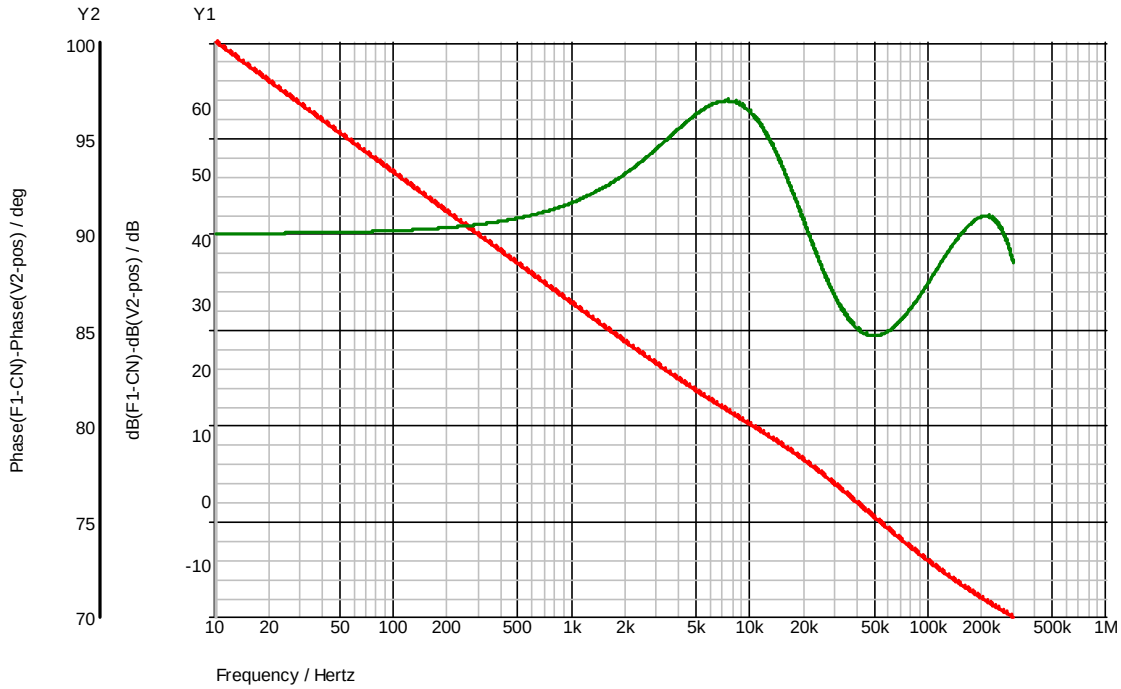
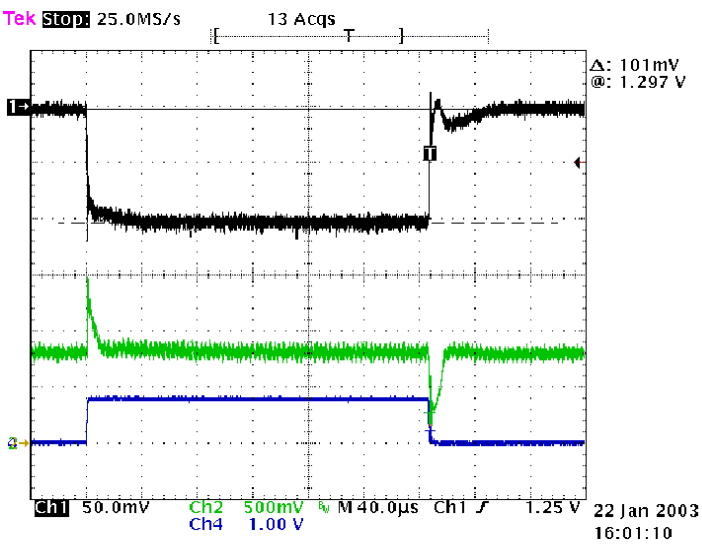



Figure 4.37 Gain and Phase Plot of Simulation of Option 3

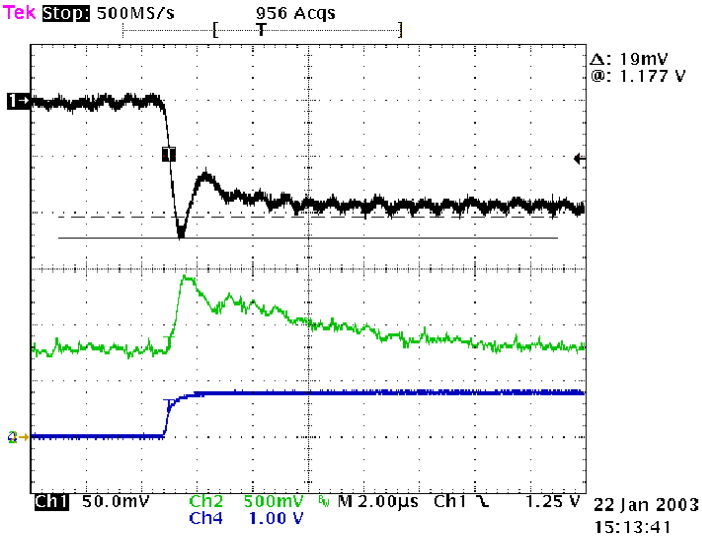
### 4.4 Ceramic Capacitor Trade Off

Ceramic capacitor has lower ESR and ESL than bulk capacitor. The results of a study showed that the initial voltage drop during the rising edge of load transient could reduce 10mV by adding six more ceramic capacitors. Figure 4.38 to Figure 4.41 show the results of this trade off. The bulk capacitance is still required enough to meet the load removable specifications.




| |
|---|
| Vin = 19V<br>Iout = 0A to 80A<br>VID = 1.325V |
| Ch 1: Vout |
| Ch2: Vcomp |
| Ch3: Not shown |
| Ch 4: On Board Load |

Figure 4.38 Transient Response of 5 x 2R5TPD680M5




| |
|---|
| 19mV Below Nominal Voltage |
| Vin = 19V<br>Iout = 0A to 80A<br>VID = 1.325V |
| Ch 1: Vout |
| Ch2: Vcomp |
| Ch3: Not shown |
| Ch 4: On Board Load |

Figure 4.39 Zoom in Rising Edge of Transient Response of 5 x 2R5TPD680M5

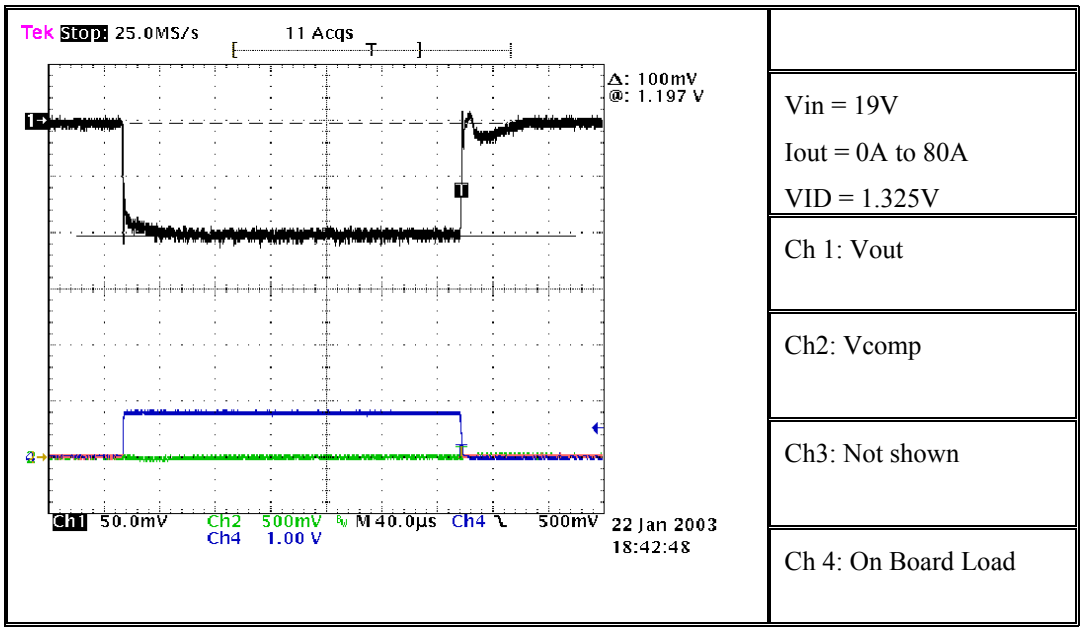



Figure 4.40 Transient Response of 5 x 2R5TPD680M5 and 20 x 22uF Ceramic

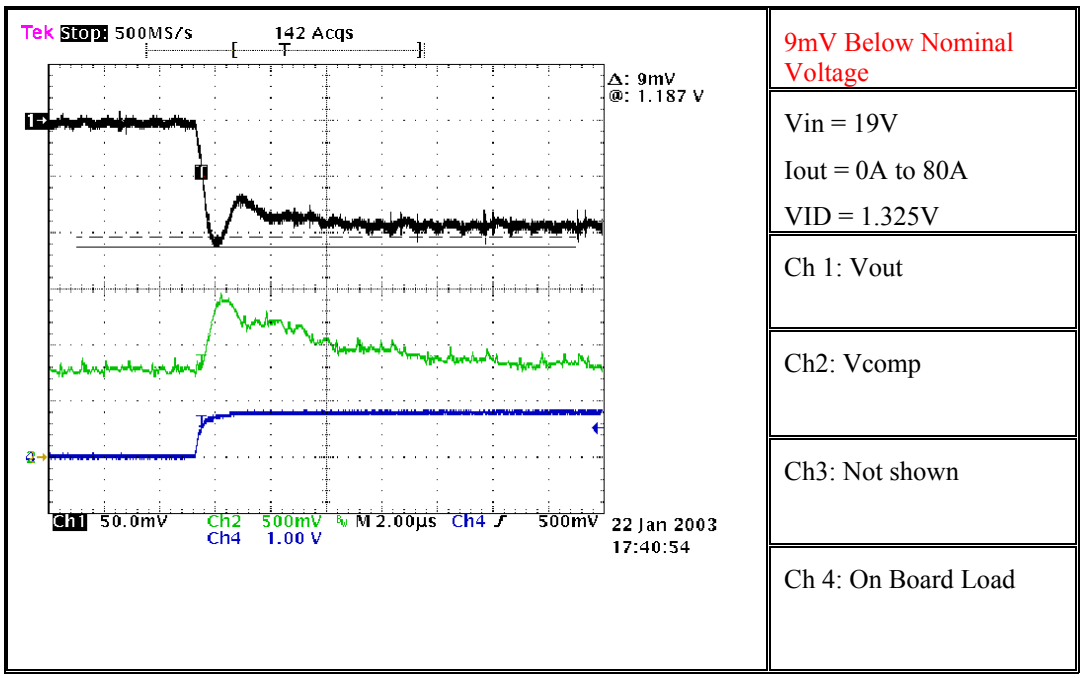



Figure 4.41 Transient Response of 5 x 2R5TPD680M5 and 20 x 22uF Ceramic

### 4.5 Time Constant Mismatch Effect Transient

The results of time constant mismatch effect the transient have examined with output capacitor of 9 x 680uF and 14 x 22uF ceramic capacitor. The waveform has been averaged for many cycles to eliminate the ripple voltage. Figure 4.42 shows the processor voltage with the same time constant. Figure 4.43 shows the processor voltage with RC time constant greater than 15% of L/R time constant. This results in a higher processor voltage because the current sense circuitry measures less current. When the load is removed, the processor voltage took a longer time to reach steady state. Figure 4.44 shows the opposite situation, which RC time constant is 15% less than L/R time constant.

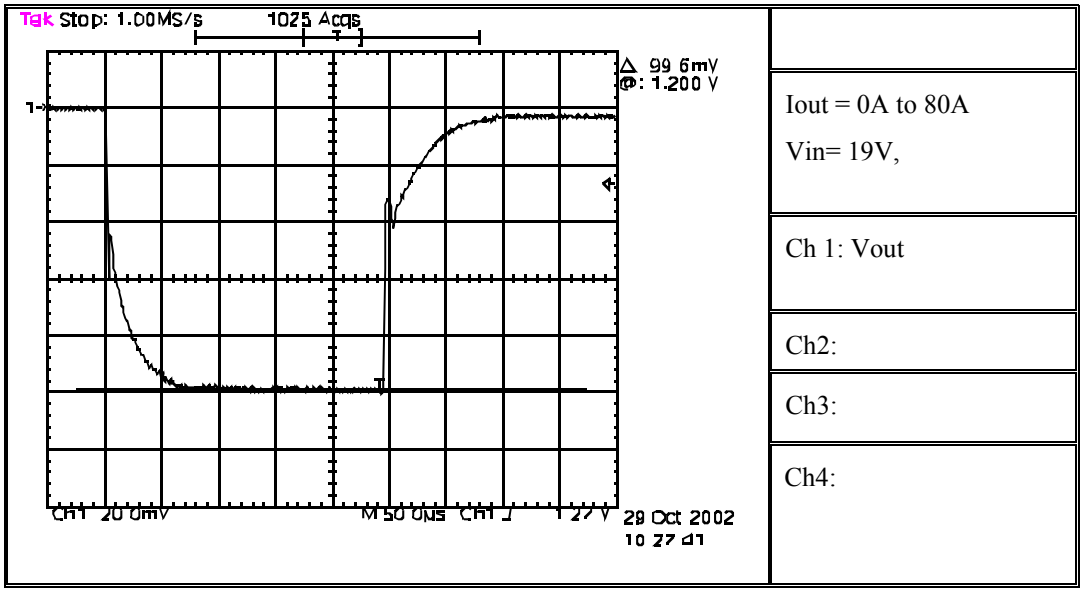



Figure 4.42 RC Time Constant Same as L/R

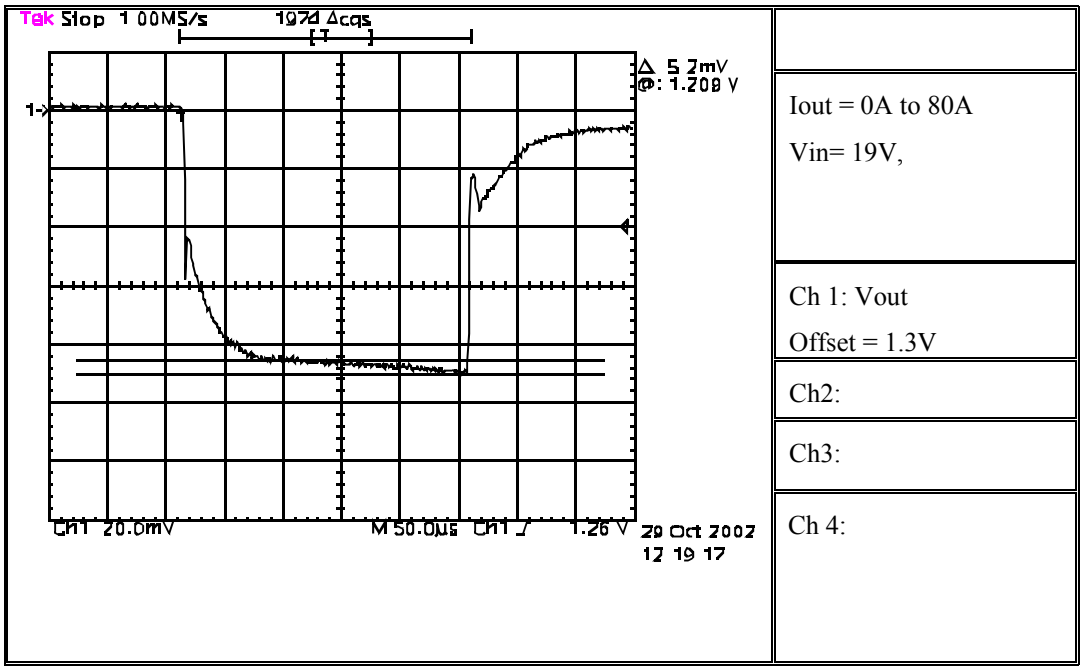



Figure 4.43 RC Time Constant Greater than 15% of L/R

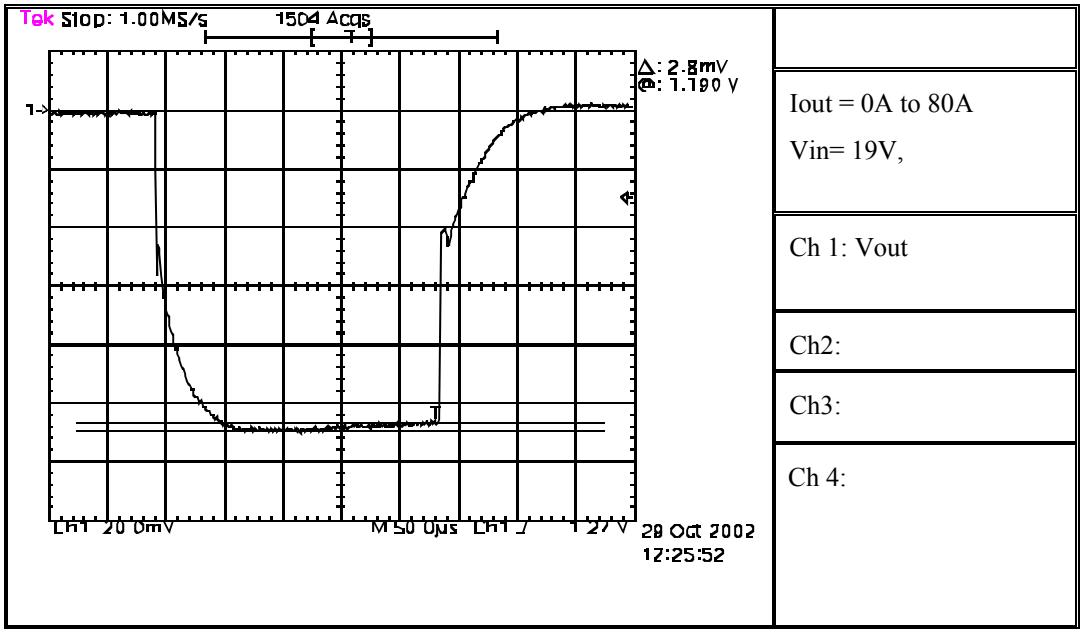



Figure 4.44 RC Time Constant Less than 15% of L/R

## Chapter 5 Conclusion and Future Work

In this thesis, a complete system analysis of the VRC for laptop processors has been designed to meet both static and dynamic performance requirements of the Intel specification in any mode of operation. The design of 4-phase synchronous buck converter provided higher efficiency and lower cost solution, which are the keys in the laptop system.

The power loss analysis, which introduced in Chapter 2, provided the designer the insight of power loss break-down for the VRC efficiency estimation. The efficiency of the system could be improved significantly by choosing better MOSFETs and reasonable switching frequency. Most of power loss in the VRC is direct proportional to the switching frequency. Therefore, the switching frequency of the VRC in the laptop computer higher than 500kHz is not a practical solution due to the concern of the battery life.

The VRC has to be designed in such a way that can guarantee to meet Intel specification in high volume production. Therefore, it is necessary to develop the tolerance analysis of VRC. In this thesis, the tolerance of load line had developed by using the RSS method. The results met the Intel specification in both low and high temperature of laptop environment.

The current loop is required in VRC in both desktop and laptop computers. It needs to balance the currents in multiphase synchronous buck converter and has channel-by-channel over current protection feature. The major advantage of the current control is easy to design to achieve the desired stability. In this thesis, the current loop is dynamically adjusting the output voltage level to save the power loss besides having

above features. As showed in Chapter 3, this current loop is still inside the voltage loop. An insight of overall system loop of multiphase synchronous buck converter along with the active droop current loop had been derived and used to predict the stability of converter. The results of this model have been compared to the simulation results and experiment results from three different output capacitors solutions. They are agreed with each other. The bandwidth of the VRC is dependent on the ESR frequency of output capacitors. This has been proven by experiment results of three output capacitor options. The overall system loop in Chapter 3 was derived base on the assumption of no small signal at reference voltage. In practice, the laptop computer has more than one mode operation. Therefore, the reference voltage of controller will change to respond to the processor's command to save the power loss of VRC. When the reference voltage of converter changes in such a way as Gyserville and C4 transition, the processor voltage could be largely undershooting or overshooting if the compensation network is not optimized. In this converter scheme, if the $C_C$ is greater than a certain value or 1.5nF in this study, the undershoot and overshoot could be clearly seen. In dc/dc converter for many other applications such as in desktop, the control loop analysis is neglecting the small variation of reference voltage. In VRC for laptop computer, the small signal transfer function from reference to output voltage has to be considered in the performance analysis to meet the Intel's specification. This issue will be a good topic for future work.

The output capacitor bank is the highest cost item in VRC for laptop computer. As derived in Chapter 2, the equation is used to predict the minimum output capacitance requirement to meeting the specification. The ESR and ESL of output capacitors have to

be less than the slope of load line to avoid the specification. The drop of processor voltage during increasing the load is clearly dependent on the ESR and ESL of output capacitors; and the peak of processor voltage during the load remove depended on the capacitance of output capacitors.

Base on the current sensor information, changing the number of phase on the fly can significantly improve the efficiency to further extend the battery life of the laptop computer, especially in light load as shown in Figure 4.10. The output voltage will be disturbed when the number of phase changes due to the energy of inductor. For example, during the number of phase is shutting down, the energy of inductor delivers to the output capacitor, which cause output voltage increases. To minimize the output voltage change and to meet the Intel specification, a controller needs to know when to turn-off and turn-on the phases. A preliminary study on this subject is started and will continue in near the future.

The efficiency of higher current rate such as 120A in desktop computer has been studied to predict the efficiency in the future laptop computer. Two solutions have been used to compare the efficiency. A 5-phase solution used to convert from 19V to 1.325V with the switching frequency at 300 kHz. The MOSFETs are two paralleled HAT2168H for upper and two paralleled HAT2165H for lower for each phase. A two-stage solution is used to convert 19V to 8V and 8V to 1.325V; both stages switched at 300 kHz. The output voltage of the first stage is chosen to be 8V because the output current would keep the same amount of MOSFET as 5-phase solution. For the first stage, the MOSFETs are two parallel of HAT2166H for upper and two parallel of SI7880DP for lower. For the second stage, the MOSFET are two parallel of HAT2168H for upper and two parallel of

HAT2160H for lower which is 20V device and lower on resistance than HAT2165H. Figure 5.1 shows the results of 2 solutions. The efficiency of the two stages solution is always lower than one stage solution under any load condition. The results of efficiency are opposed the results in [8-9]. A further analysis will study to determine the root cause.

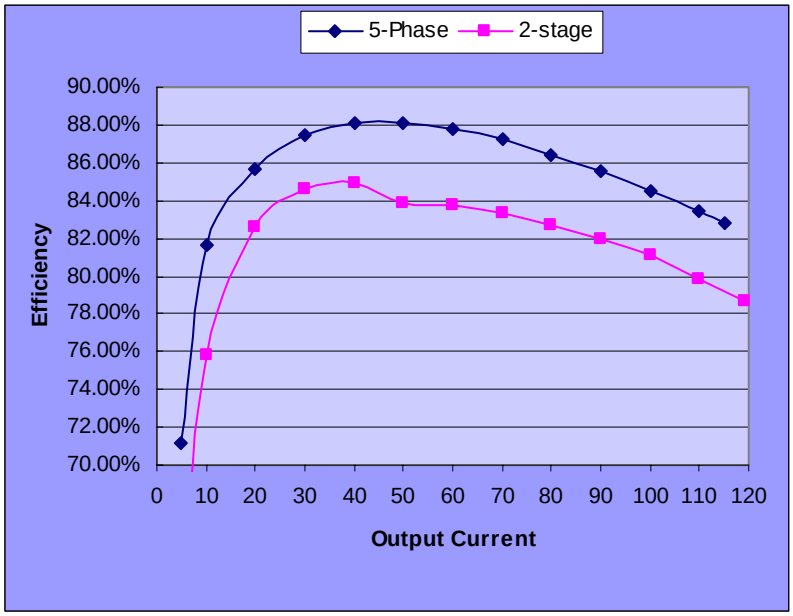



Figure 5.1 One and Two Stages Efficiency Solutions Comparison

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