Design and Analysis of Microwave Feedback Amplifiers

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***Abstract*--We have studied the basic theory of feedback amplifiers. A broadband single stage MESFET amplifier has been designed with 5 dB gain over the frequency range from 500 MHz to 12 GHz. A gain flatness of $\pm$0.18 dB was achieved. Meanwhile, the input VSWR and output VSWR were controlled to be less than 1.88:1. Both negative and positive feedback were used to extend the bandwidth. The amplifier is unconditionally stable within the whole interested frequency region, while we checked the stability up to 60 GHz.**

I. Introduction

Negative feedback can be used in the broadband amplifiers to control gain flatness and reduce the input and output VSWR at the same time. When the bandwidth requirement reaches a decade of frequency, the gain compensation based on the matching network becomes very difficult, while the feedback amplifier can be designed to have a very wide bandwidth (more than two decades) with small gain variations (tenths of a decibel). Also feedback can be designed to improve the circuit stability by reducing S_{12} over the frequency. Another advantage of the feedback technique is that the modified transistor S matrix after feedback is relatively insensitive to the device parameter variation, which makes the circuit more robust against process variations. The cost is degradation of noise figure due to the introduction of resistors, reduction of gain and reduced output power capability.

As shown in Figure 1, the two most common types of feedback are series feedback and parallel feedback. The series feedback is often used to improve S_{11} at the expense of reduced stability. The parallel feedback is used to flatten gain over frequency. A compound of both is often used. Reactive elements can also be used with the resistive feedback to peak the high-frequency gain. We will illustrate this through our design example.

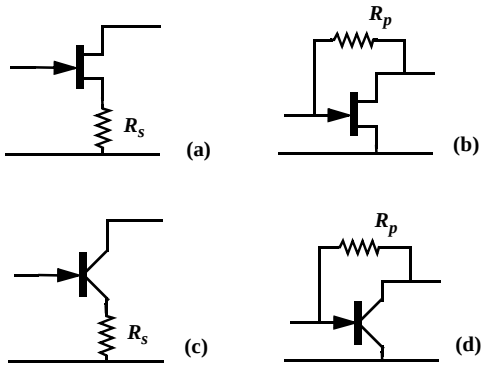

Figure 1. (a) MESFET with series feedback (b) MESFET with parallel feedback (c) Bipolar transistor with series feedback (d) Bipolar transistor with parallel feedback

Important efforts have been made in the past decades to extend these technique to higher frequency. Different design methods are developed during the years. Niclas *et al*. have reported design methods and experimental results for GaAs MESFET feedback amplifier up to 18 GHz, obtaining five or more octave bandwidth [1-2]. The design procedure relies on a known transistor model which works up to relative low frequency and then doing computer optimization at higher frequency. Later on Perez and Ortega reported two graphical methods [3] controlling the gain flatness, amplifier stability and matching, which rely on the knowledge of the measured S-parameters and need very little optimization to achieve the final design. And a method [4] based on rigorous calculation to achieve the optimum performance for stability and matching was reported by Sheau-Shong Bor *et al*., which provides more insight into the effects of the feedback and more control of the two-port amplifier for practical applications.

We will follow the Niclas' method in our design. The scaled EE217 MESFET model was used. The goal of our design is to achieve a wide bandwidth and excellent gain flatness and meanwhile to control the input and output reflection. The basic theory for the feedback circuit design at low frequency will be described in detail first. A few design issues and trade-offs will be discussed along with the analysis and the design procedure.

II. Basic Feedback Amplifier Circuit: Model, Theory and Analysis

A. Device Model

As shown in Figure 2, are the diagrams of the basic feedback circuit we were using for the amplifier including the parallel feedback resistor and two associated inductors L_{FB} and L_D.

Figure 2(a) is the high-frequency model. Inside the dashed-line box is the small signal model for the active device, the GaAs MESFET. A set of scaled standard EE217 MESFET parameter values were used in our project, which are listed in Table 1[5]. It is the parasitic reactive elements that restrict the

EE217 final project report, Spring, 1999.

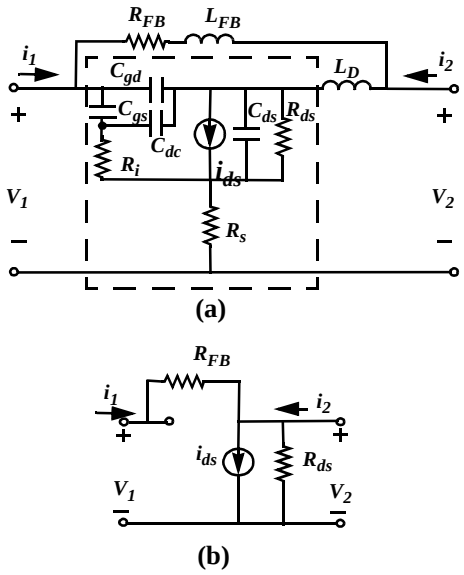

Figure 2. Circuit diagram of the basic feedback amplifier. (a) High-frequency model. (b) Low-frequency model.

TABLE 1. Parameter Values of the Transistor Model

g_m = 60 m mhos	C_{dg} = 0.05 pF
τ_0 = 3 psec	C_{dc} = 0.02 pF
$f_{roll\text{-}off}$ = 0 Hz	C_{ds} = 0.14 pF
C_{gs} = 0.47 pF	R_{ds} = 256.67 ohm
R_i = 4.83 ohm	R_s = 2.67 ohm

amplifier bandwidth ability. Two inductors, drain inductor L_D and feedback inductor L_{FB} are introduced to compensate the capacitive output and bring positive feedback.

Figure 2(b) is the low-frequency model when we ignore the reactive elements and R_i, R_s, which can be used to determine the amplifier's dc gain, input and output VSWR, and reverse isolation. Further simplification will cause error, so R_{ds} stays in our calculation below.

B. DC Gain and Input and Output VSWR Calculation

Based on the simplified dc model of the feedback amplifier, we can calculate its S-parameters.

Assuming R_i, R_s are small compared with the feedback resistor R_{FB}, which is true in our case, and load resistor $R_L = Z_0$, the relation between voltages and currents can be described by the admittance matrix,

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} 1/R_{FB} & -1/R_{FB} \\ (g_m - 1/R_{FB}) & (1/R_{FB} + G_{ds}) \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad (1)$$

Where,

$$G_{ds} = R_{ds}^{-1} \quad (2)$$

And

$$i_{ds} = g_m V_{gs} \quad (3)$$

$$V_{gs} = V_1 \quad (4)$$

Using elementary algebra, the admittance matrix converts to the S matrix,

$$S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \quad (5)$$

Its elements are,

$$S_{11} = \frac{1}{\Sigma}\left[\frac{R_{FB}}{Z_0}(1 + G_{ds}Z_0) - (g_m + G_{ds})Z_0\right] \quad (6a)$$

$$S_{12} = \frac{2}{\Sigma} \quad (6b)$$

$$S_{21} = -\frac{2}{\Sigma}[g_m R_{FB} - 1] \quad (6c)$$

$$S_{22} = \frac{1}{\Sigma}\left[\frac{R_{FB}}{Z_0}(1 - G_{ds}Z_0) - (g_m + G_{ds})Z_0\right] \quad (6d)$$

With

$$\Sigma = 2 + (g_m + G_{ds})Z_0 + \frac{R_{FB}}{Z_0}(1 + G_{ds}Z_0) \quad (6e)$$

The feedback resistor's influence on the gain and the input, output VSWR are implied in the S parameter expression.The choice of R_{FB} is clearly a compromise between gain and VSWR. We can consider three cases.

Case 1: Input and output VSWR are identical for the feedback resistor,

$$R_{FB} = (g_m + G_{ds})Z_0^2 \quad (7a)$$

and the S-parameters are:

$$S_{11} = -S_{22} = \frac{G_{ds}Z_0^2}{\Sigma}(g_m + G_{ds}) \quad (7b)$$

$$S_{12} = \frac{2}{\Sigma} \quad (7c)$$

$$S_{21} = -\frac{2}{\Sigma}[g_m(g_m + G_{ds})Z_0^2 - 1] \quad (7d)$$

$$\Sigma = 2 + (g_m + G_{ds})(2 + G_{ds}Z_0)Z_0 \quad (7e)$$

Case 2: Perfect matching at the output, $S_{22} = 0$, which requires the feedback resistor,

$$R_{FB} = \frac{g_m + G_{ds}}{1 - G_{ds}Z_0}Z_0^2 \quad (8a)$$

And the S-parameters are,

$$S_{11} = \frac{g_m + G_{ds}}{1 + g_m Z_0} G_{ds} Z_0^2 \quad (8b)$$

$$S_{12} = \frac{1 - G_{ds} Z_0}{1 + g_m Z_0} \quad (8c)$$

$$S_{21} = 1 - (g_m + G_{ds}) Z_0 \quad (8d)$$

$$S_{22} = 0 \quad (8e)$$

Case 3: Perfect matching at the input, S_{11} =0, which requires the feedback resistor,

$$R_{FB} = \frac{g_m + G_{ds}}{1 + G_{ds} Z_0} Z_0^2 \quad (9a)$$

and the S-parameters are,

$$S_{11} = 0 \quad (9b)$$

$$S_{12} = \frac{1}{1 + (g_m + G_{ds}) Z_0} \quad (9c)$$

$$S_{21} = -\frac{2}{\Sigma}\left[\frac{g_m (g_m + G_{ds}) Z_0^2}{1 + G_{ds} Z_0} - 1\right] \quad (9d)$$

$$S_{22} = -\frac{2}{\Sigma}\frac{G_{ds} (g_m + G_{ds}) Z_0^2}{1 + G_{ds} Z_0} \quad (9e)$$

By comparing these three cases, case 2 has highest gain but also highest input reflection coefficient, while case 3 yields lowest gain and best input match. Case 1 is a compromise with medium gain, and good control of both S_{11} and S_{22}. With a finite value of R_{ds}, S_{11} and S_{22} can't be zero at the same time.

Let's look at a special condition for case 1 with G_{ds} =0, or R_{ds} = ∞. Then perfect match can be achieved at both ends, S_{11} = S_{22} = 0. And the tranceconductance gain is,

$$S_{21} = 1 - g_m Z_0 = 1 - \frac{R_{FB}}{Z_0} \quad (10)$$

We can see the gain is determined by feedback resistance instead of the device parameters, which offers the immunity for the circuit performance from the process variation. Because of the gain reduction caused by the feedback, a high g_m transistor is favored in the microwave feedback design.

As we noticed, this analysis is only valid for the lower end of the bandwidth. The design extended to higher frequency can only be accomplished with the aid of the CAD tools, where all the device reactive parasitics, ignored parasitic resistances and matching network will come to the play. But there, the main effort will be made to maintain the flat gain to the maximum frequency and to improve the degraded matching. But the basic gain level and potential to a good matching are determined by the dc network. So the dc analysis is very useful and important.

C. Frequency Controlled Feedback

The conventional negative resistive feedback can only offer gain and VSWR to a relatively low frequency. "Frequency controlled feedback" is used to achieve wide bandwidth. In Figure 2(a), two inductors are used to accomplish this method. A feedback inductor L_{FB} is connected in series with the feedback resistor. And a drain inductor L_D is added before the output. These two inductors have different functions. L_D compensates the output capacitance at high frequency to recover the bandwidth. L_{FB} can reduce the feedback at high frequency to flatten the gain further. A good illustration will be given with the simulation of the design example in next section.

III. Sample Design

Based on the circuit theory and the chosen technology in section II, we designed a single-stage broadband microwave feedback amplifier. Figure 3 shows a completed design, including the basic feedback amplifier in the dashed-line box; a simple input matching network composed of L_1, C_1; and the biasing and decoupling circuits (L_{biasd}, L_{biasg}, C_{in}, C_{out}). Final circuit performance is evaluated with the transmission line implementation without the biasing chokes.

The design method and simulation results will be illustrated step-by-step to reveal how the design spec is achieved and to provide some insight to the feedback amplifier.

Finally, a simulation of the direct connection of two stages demonstrates the feedback amplifier can be easily cascaded to achieve higher gain while maintaining the bandwidth.

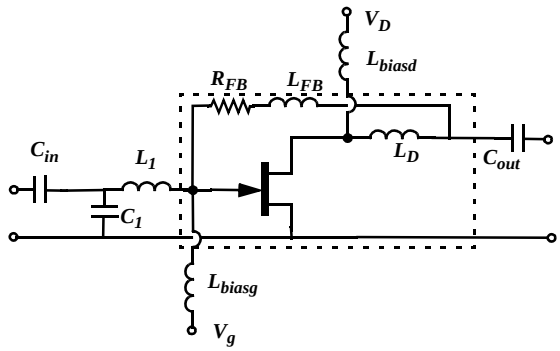

Figure 3. A single-stage feedback amplifier with input matching network and biasing RF chokes. R_{FB} = 170 Ω, L_D = 0.10 nH, L_{FB} = 0.73 nH, L_1 = 0.76 nH, C_1 = 0.25 pF.

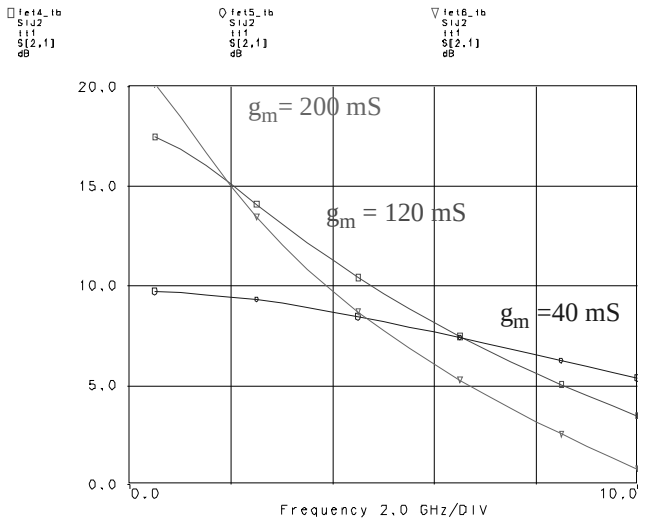

Figure 4. Gain magnitude vs. frequency of a bare MESFET of different g_m values

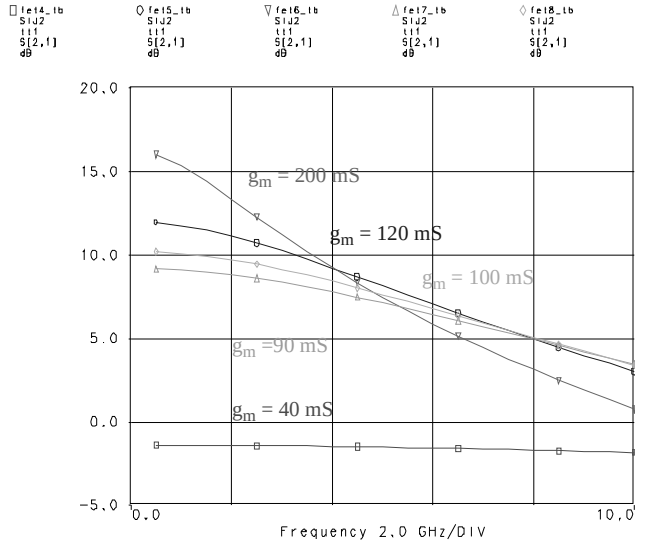

Figure 5. Gain magnitude vs. frequency for a MESFET with simple resistive feedback of different g_m values

A. Gain-Bandwidth Trade-off

First we studied the gain-bandwidth trade-off of the EE217 MESFET and the resistive feedback circuit to determine a reasonable spec for our design.,

As shown in Figure 4, the gain response vs. frequency for a bare EE217 MESFET of different g_m values are studied. By increasing g_m, the transistor dc gain is boosted. But very clearly, for a certain technology, the gain-bandwidth is pair of trade-off because by scaling g_m up, the parasitic output capacitance scales up too. For a single-stage amplifier, with a certain bandwidth requirement, the maximum gain will be limited by the technology. So devicewise, eliminating the reactive parasitics can extend the circuit bandwidth.

Circuits with simple resistive feedback also demonstrate this trade-off as shown in Figure 5. With a dc gain of 10 dB, 5 GHz bandwidth is achievable. With a higher bandwidth of 10 GHz, the maximum dc gain would be about 5 dB. Since a higher gain can be achieved by cascading two single-stage amplifier, we decide to design a single-stage with 5 dB dc gain. By further feedback technique and matching, we try to push the bandwidth as high as possible. Meanwhile, we want to control the input and output VSWR to less than 2:1, which implies S_{11} and S_{22} should be less than 0.333.

B. Amplifier Design and Simulation

(a) Gain Flatness and Bandwidth Enhancement

From the analysis of section IIB, we know when we choose $R_{FB,}$ there is a trade-off between gain and VSWR. In our design, we chose to get a relative good matching at both input and output. The main focus is to achieve a good gain flatness over a wide bandwidth. Simple matching network was adopted to compensate the degraded matching at high end of the bandwidth.

From equation (7a) and (7d), we can calculate the g_m to be used to get 5 dB dc gain and the feedback resistance. And we did simulation similar as the one shown in Figure 5 with g_m values near the calculated value and with corresponding R_{FB} values. We found g_m of 60 mS provides dc gain of 5 dB, the corresponding R_{FB} is 170 W. The gain response with only resistive feedback is shown in Figure 6, curve (a). 5 dB gain is achieved at dc, but it rolls down very quickly at the frequency region we are interested. And its phase frequency response is shown in Figure 8(b). The 3 dB point is around 11 GHz, the gain phase is 90 degree.

Positive feedback is used to compensate the gain

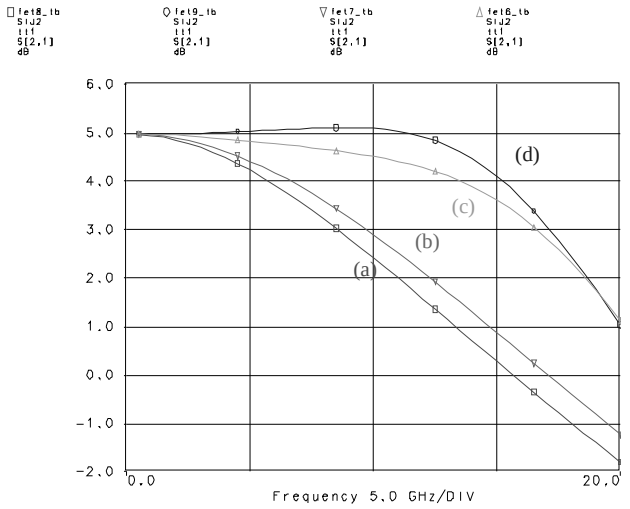

Figure 6. Gain magnitude frequency response of the basic feedback amplifier shown in Figure 2(a). Curve (a) R_{FB} = 170 Ω, L_D = 0, L_{FB} = 0, (b) R_{FB} = 170 Ω, L_D = 0, L_{FB} = 0.5 nH, (c) R_{FB} = 170 Ω, L_D = 0.35 nH, L_{FB} = 0, (d) R_{FB} = 170 Ω, L_D = 0.35 nH, L_{FB} = 0.5 nH.

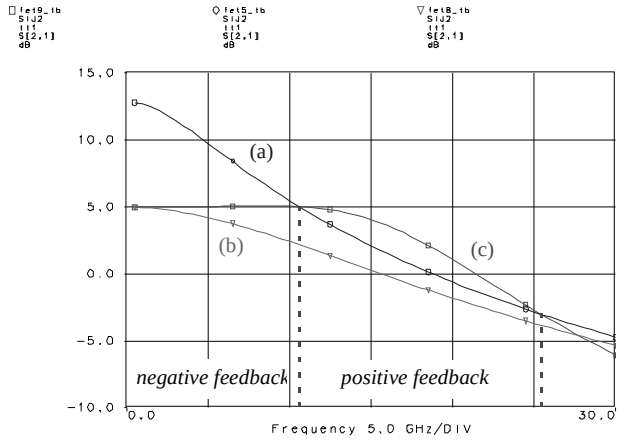

Figure 7. Comparison of gain magnitude frequency response among (a) bare transistor without feedback, (b) with only resistive feedback, (c) with both resistive feedback and the inductors, L_D = 0.35 nH, L_{FB} = 0.5 nH.

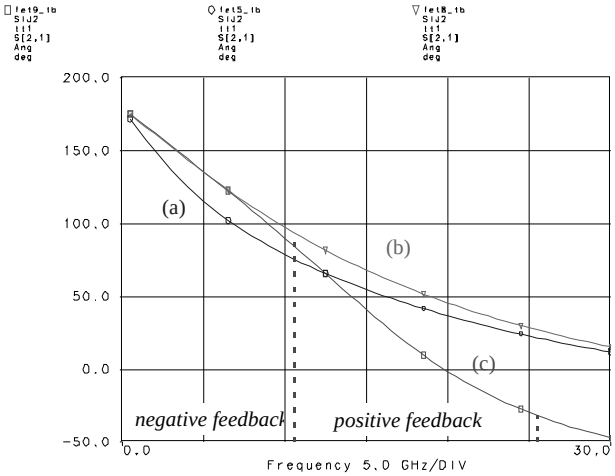

Figure 8. Comparison of gain phase frequency response among (a) bare transistor without feedback, (b) with only resistive feedback, (c) with both resistive feedback and the inductors, L_D = 0.35 nH, L_{FB} = 0.5 nH.

degradation at the high end of the bandwidth. Two inductors were added to achieve this. The connection is shown in Figure 2(a). A comparison of the gain magnitude frequency response in Figure 6 well demonstrates the function of the two inductors. As stated above, curve (a) shows gain in dB rolls down linearly without any inductor. Curve (b) shows L_{FB} can reduce the negative feedback at high frequency. At low frequency it doesn't affect the gain. Curve (c) shows the main contribution of the bandwidth recovery is from L_D. Curve (d) is the gain response with both L_{FB} and L_D. Bandwidth is recovered to 12 GHz, with gain 5 ± 0.1 dB. The use of the two inductors in the feedback is so called "frequency controlled feedback".

In Figure 7 and Figure 8, we compared both gain magnitude and phase frequency response among three cases, (a) bare transistor, (b) resistive feedback, and (c) frequency controlled feedback. Comparing (a) and (b), we can see the resistive feedback basically works at very low frequency, by eliminating the dc gain. And it has very little effect on the phase frequency response. However, by using the frequency controlled feedback. The gain flatness is maintained until 12 GHz. A positive feedback frequency region appears as marked in the figures. If we look at the phase curve (c), we know a zero is introduced to compensate the pole which is at 11 GHz. That's how we get the positive feedback.

L_D was chosen to compensate the capacitive component of the output impedance so that the resonance occurs at the upper band edge. L_{FB} was chosen to get the optimum positive feedback. The final values of L_D and L_{FB} were obtained from the CAD tools optimization. We found in a large range, various combinations of L_{FB} and L_D produce good gain flatness and bandwidth. And the program doesn't necessarily give the optimal values which are practical for implementation. We kept in our mind a larger L_{FB} value than that of the L_D makes more sense in the layout since L_{FB} connects from the output of the transistor to the input of the transistor. So optimization was terminated when the performance was achieved with a pair of practical parameters.

(b) Input VSWR and Output VSWR

Now the broadband potential of the basic feedback amplifier as shown in Figure 2(a) or in the dashed-line box of Figure 3 is almost exhausted. We want to come back to check the input and output VSWR. And a simple LC input matching network was designed to improve the input matching, which is shown in Figure 3. Figure 9 and Figure 10 shows simulation results before and after the addition of the input matching network.

Input and output reflection coefficients can be calculated from equation 7(b). Comparing curve (a) and (b) in Figure 9 and Figure 10, the feedback does provide good matching at both

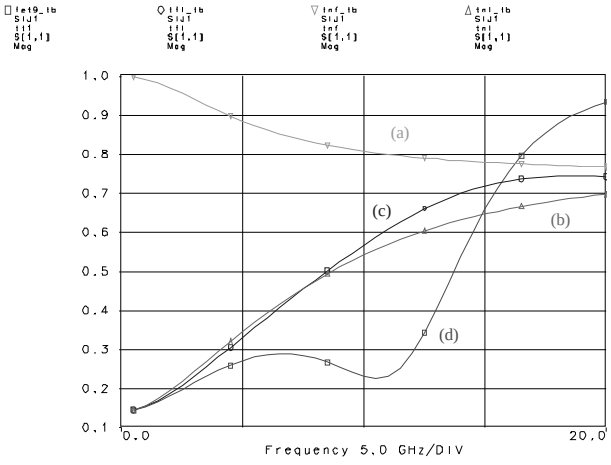

Figure 9. Comparison of the input reflection coefficient S_{11}. (a) Bare transistor, (b) Resistive feedback, (c) Frequency controlled feedback, R_{FB} = 170 Ω, L_D = 0.35 nH, L_{FB} = 0.5 nH, (d) Frequency controlled feedback with additional input matching network.

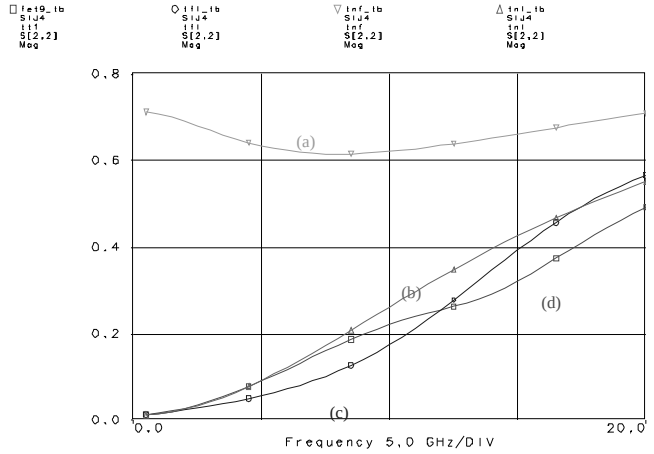

Figure 10. Comparison of the input reflection coefficient S_{22}. (a) Bare transistor, (b) Resistive feedback, (c) Frequency controlled feedback, R_{FB} = 170 Ω, L_D = 0.35 nH, L_{FB} = 0.5 nH, (d) Frequency controlled feedback with additional input matching network.

input and output. S_{11} = 0.1463, S_{22} = 0.0130. But the matching turn worse when the frequency increases. At 12 GHz, S_{11} = 0.5937, S_{22} = 0.3318. S_{11} is more problematic, At the frequency band edge it is already out of the spec.

Comparing curve (c) and (b) in Figure 9 and Figure 10, we can see S_{11} is degraded a little near the frequency band edge, but S_{22} is improved above 1 GHz. At 12 GHz, S_{11} = 0.6438, S_{22} = 0.2548.

So a simple LC matching network is added to the input to improve S_{11}. Since the concern here is reflection instead of power gain, we will pursue impedance match instead of conjugate match. We chose the *L* section matching network described in Pozar's book [6]. As shown in Figure 11, different configuration should be used for different normalized load impedance we are trying to match. Given z_L, the type of configuration can be determined, and the required values of *B* and *X* can be calculated from the formula given in [6].In our case, Z_L here is the input impedance Z_{in} of the basic amplifier before matching. From the measurement by the software, at 12 GHz, z_{in} = 0.28 - 0.52*j*, so type (b) should be used. As shown in Figure 3.

Comparing curve (d) and (c), we can see, the LC network

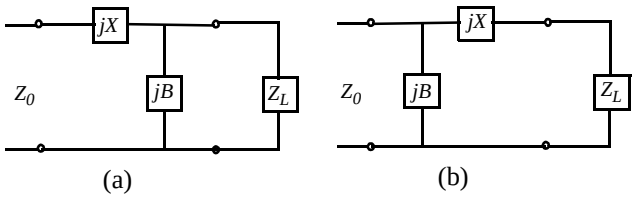

Figure 11. *L* section matching networks. (a) Network for z_L inside the 1+*jx* circle. (b) Network for z_L outside the 1+*jx* circle.

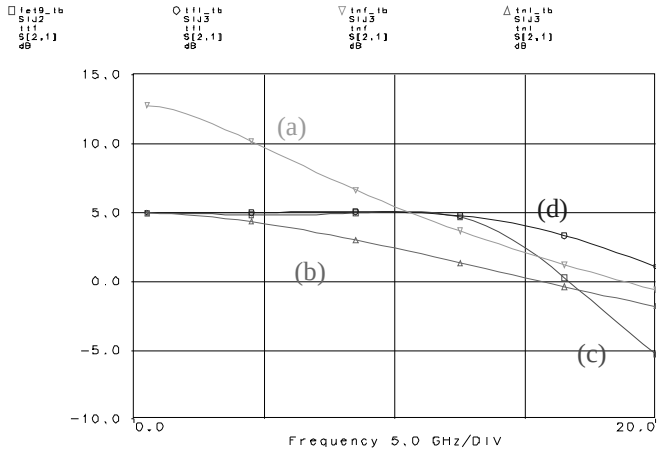

Figure 12. Comparison of gain magnitude frequency response among (a) bare transistor without feedback, (b) with only resistive feedback, (c) with both resistive feedback and the inductors, L_D = 0.35 nH, L_{FB} = 0.5 nH, (d) frequency controlled feedback with additional input matching network.

brings down S_{11} dramatically near its resonance frequency 11.5 GHz. A local minimum S_{11} occurs at 10.5 GHz. At 12 GHz, S_{11} = 0.2922. And as we can see, the matching at input actually degrade the output match a little. At 12 GHz, S_{22} = 0.2555. So it is still within the spec. In this case, an output matching network is not necessary.

And overall, after some optimization, a design of 5 dB gain, 12 GHz bandwidth, ±0.15 dB gain flatness is achieved. Input VSWR is less than 1.8. Output VSWR is less than 1.7. Circuit parameters are listed in Figure3. Large value should be chosen for the biasing and decoupling circuit elements.

Curve (d) in Figure 12 shows with the input matching network, the amplifier remains a good gain flatness.

(c) Transmission Line Implementation

Since the wide bandwidth and small inductance and capacitance value we used in our design, it is possible to. implement the Ls and Cs by transmission line. The overall

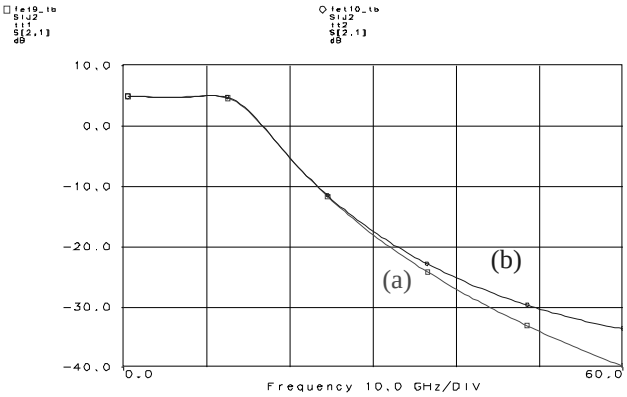

Figure 13. Gain magnitude frequency response of the complete design. (a) with ideal Ls and Cs, (b) with transmission line implementation.

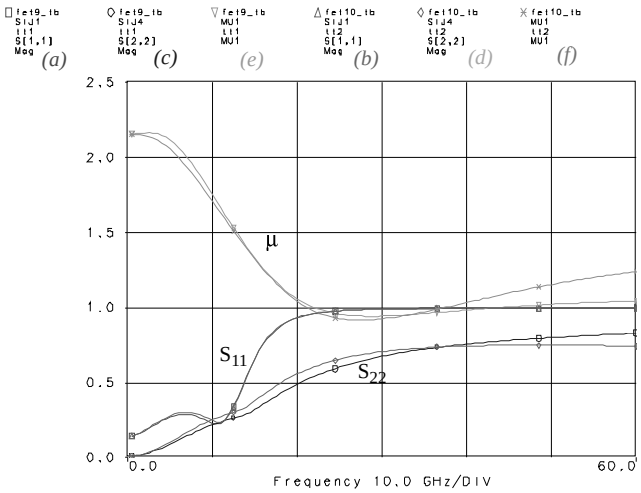

Figure 14. Comparison of S_{11}, S_{22} and stability parameter μ between the completed design with ideal Ls and Cs and the transmission line implementation. Curve (a), (c), (e) belong to the ideal case. Curve (b), (d), (f) are results of the transmission line implementation.

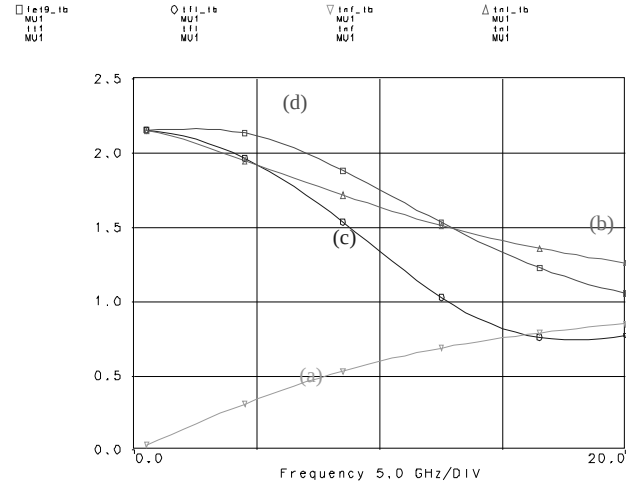

Figure 15. Comparison of stability parameter μ among (a) bare transistor, (b) resistive feedback, (c) frequency controlled feedback, (d) complete design with input matching network and ideal Ls, Cs.

performances are shown in Figure 13 and Figure 14. In Figure 13, we can see the gain deviation starts around 25 GHz, which is much higher than the frequency band edge. Some differences can be seen in S_{11} and S_{22} within the bandwidth in Figure 14, but which are small. So in the transmission line implementation, the gain flatness is ±0.18 dB, input VSWR is less than 1.88:1, output VSWR is less than 1.83:1 with 5 dB gain, 12 GHz bandwidth.

The parameters of the transmission lines used are listed in Table 2.

TABLE 2. Transmission line parameters

Element	Impedance (Ω)	Length at 12 GHz (degree)
L_1	150	21.9
L_{FB}	150	21.0
L_D	150	2.88
C_1	10	10.8

(d) Circuit Stability

Circuit stability was checked step-by-step. A criteria for unconditional stability:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^* \Delta| + |S_{21} S_{12}|} > 1$$

is used to test circuit stability. If μ > 1, the device under test is unconditional stable. For the frequency region which is conditional stable, stability circles were drawn to check the stable margin.The larger the μ is, the more stable the circuit is.

Figure 15. shows a comparison of μ among the different design stages. The bare transistor is always conditional stable. With resistive feedback, the μ is larger than 1 up to more than 20 GHz. But the inductors L_{FB} and L_D made circuit more unstable, μ is less than one when frequency is above 13 GHz. By adding input matching network, the unconditional stability is recovered up to 21 GHz. Actually, when frequency is above 40 GHz, the circuit is unconditional stable again. So we need to check stability circle between 21 GHz and 40 GHz.

The stability circles were drawn for up to 60 GHz to see if there is enough stable margin provided by the design. Figure 16 shows the stability circle of transmission line implementation. Since S_{11} and S_{22} are less than 1 in the frequency region as shown in Figure 15. So on the smith chart, the region outside stability circle and inside unity circle is stable region. We can see from Figure 16, for both input and output, there is plenty of stability margin since the stability circles just cut the very edge of the unit circle.

(e) Cascaded Two-stage Feedback Amplifier

We tried to cascade two stage feedback amplifier together to see the gain performance. Figure 17 shows the simulation result. 10 dB gain can be achieved at 12 GHz. The gain flatness degraded because nothing was done for the impedance matching between the two stages. It shows the feedback amplifier has potential to achieve higher gain by cascading with a wide bandwidth.

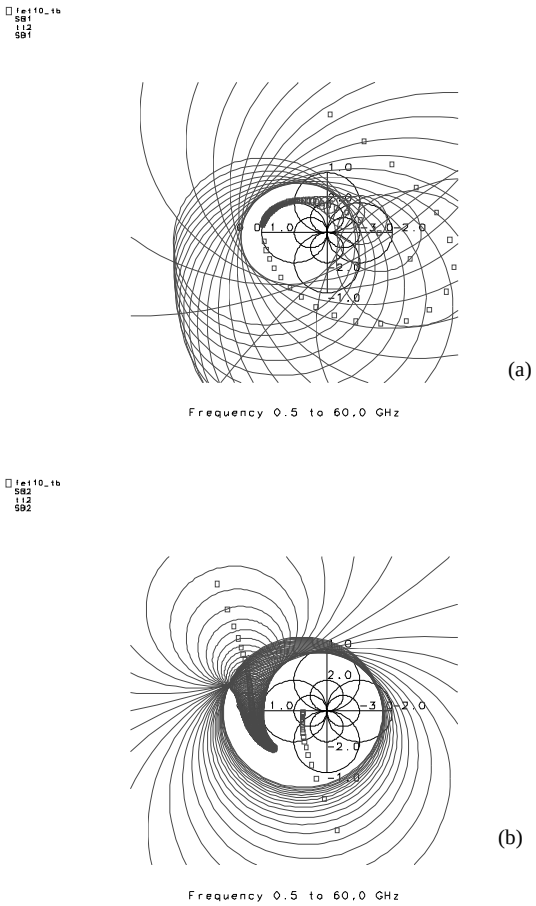

Figure 16. (a) input stability circle (b) output stability circle for frequency from 0.5 GHz to 60 GHz. The converging end is the 60 GHz end.

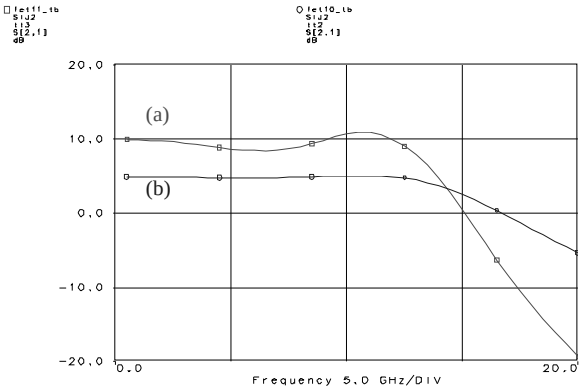

Figure 17. Gain frequency response for a two-stage cascaded amplifier (a) compared with that of a single stage (b).

IV. Conclusion

A broadband single-stage microwave feedback amplifier was designed, simulated and optimized. Frequency controlled feedback is used to achieve wide bandwidth. A simple input matching network is added to reduce input impedance matching. Circuit can be implemented using transmission line. The final performances after the transmission line implementation are concluded here: 5 dB gain, 12 GHz bandwidth, ± 0.18 dB gain flatness. Input VSWR is less than 1.88:1. Output VSWR is less than 1.83:1.

The main advantage of this circuit is flat gain over a wide bandwidth. The circuit structure and the requested matching network are simple. And it is relatively easy to cascade.

A design method is also illustrated though the design procedure.

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