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Design and Implementation of a Real-time Traffic Light Control System Based on FPGA

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***Abstract*— In this paper, the design and implementation of a real-time traffic light control system based on Field-programmable Gate Array (FPGA) technology is reported. The traffic light control system is designed with VHDL language. Its function was verified with simulation. After that, the VHDL design was downloaded to FPGA board hardware to verify its function in experiment. The designed traffic light control system was shown to work properly as expected.**

Keywords—Traffic Light Control System, Field-programmable Gate Array (FPGA).

I. INTRODUCTION

Through using VHDL language to the traffic light controller design, the traffic light control circuit uses digital signal automatic control to realize two groups of lights which are red, yellow and green.[9]-[12] Those lights command vehicles and pedestrians passing safely at the crossroad, which bases on the data of traffic state transition.[1]

Most of control systems are made by advanced PLC (Programmable Logic Controller) technology, which even can effectively imitating the experienced traffic policeman‘s thought. In addition, FPGA cannot compare the Anti-dry round benefit and fast speed benefit. However, PLC has a disadvantage for traffic light design. Most PLC costs more than $400(could be 10 times of FPGA cost), which has not considered the expansion module. The PLC technology is mostly used in heavy industry and Precision Instruments production [8].

There are two kinds of the VHDL design, which are modeling and synthesis. The modeling VHDL design has significant advantage in complicated system design. In addition, the VHDL should not be thought as a programming language. This language is designed to describe the logic circuit. A classic model is a very helpful point to start programming the project. [3]

The FPGA traffic light control system needs to consider the current traffic situation, which is base on the data from sensors. The FPGA gets current signals of vehicles passing crossroad and base on those signals send next step order. Also, in the specific road the traffic light should be set specifically [2]. In addition, the FPGA need to consider the time, which means separating the traffic situation by the time [4].

In the FPGA programming the codes should be packaged base on different models, which could increase he programs' flexibly [2]. The states machine is good way to separate the system to different function model. Also, the states machine is easy to realize in VHDL language. [4]

An advanced system should include traffic lights controller, countdown controller and LED display controller. Led display showing the countdown time which give the driver a directly time conception to reduce the probability of traffic accident. According to the simulation phase, the time split module is necessary based on the real-life requirement. [6]

II. TRAFFIC LIGHT CONTROL SYSTEM DESIGN

In the traffic lights design, the external hardware includes two sets of traffic lights and two LED displays (Figure 1 draws the east - west and north-south traffic light and LED display). The software system bases on:

(a) Circuit synthesis module concept: the traffic signal system is divided into several small circuits. Each module is written in VHDL codes. Those small circuits also connect together. This subdivided working design increases the speed of debugging and programming (see Figure 1).

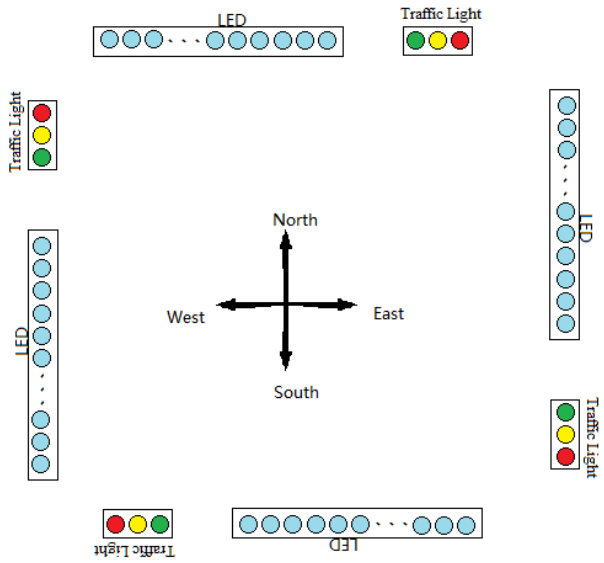

Fig. 1. Schematic diagram of crossroads

(b) Parameterization concept: the traffic light circuit can be adjusted by the time (increase or decrease the count time in circuit) to increase the flexibility of process

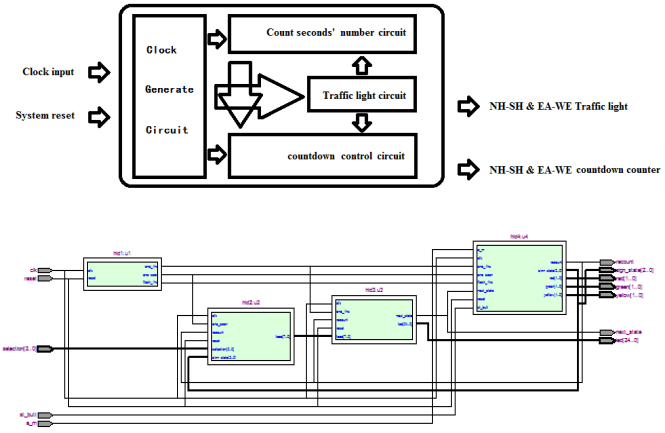

Fig. 2. Traffic signal light system structure

At the traffic lights signal system, it is most likely to use the automatic control mode. In order to avoid the occurrence of accidents the circuit must be given a stable clock to make system working normally. Therefore, the hld1 clock circuit (see Figure 2) main function is to produce a stable output signal which is used as several circuits' enabling control and synchronization signal

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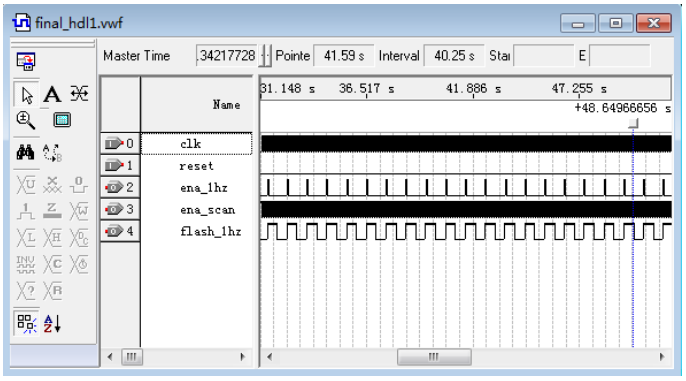

Fig. 3. Clock generation circuit diagran

In Figure 3, the external signal generator provides 1kHZ clock signal then the output signal scan system splits this clock signal's frequency. "ena_1hz" produces a cycle of pulse signal each second. "flash_1hz" produces a 1Hz pulse clock signal

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The special point during the design process is using constant parameter. The intention of using constant parameter is in order to make the program easier to read and modify. Changing the values of the constants updates constant's value for whole program, which enhance the flexibility of this project. In addition, at the programming process all of the constant parameters inputs and outputs are given some evident names. It increases efficiency of debugging and makes the project easy to be fixed by another programmer, because the function of every part is obvious.

On the crossroads, a countdown display for vehicles and pedestrians in one direction may raise passing efficiency. Therefore, main function of "hld2", which is the number of seconds count selection circuit (see Figure 1), is producing the required digital display (i.e. the numerical seconds countdown). This number is used on the countdown display circuit's output.

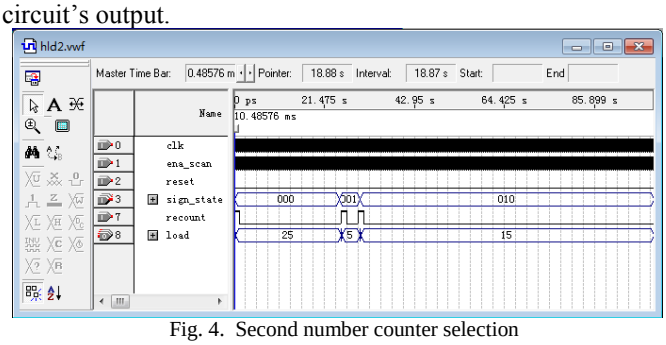

Fig. 4. Second number counter selection

Description of choice by counting the timing diagram circuit (see Figure 3): this program defines in normal traffic. Under this condition, the maintain time of red light vector, yellow light vector and the green light vector are 15s, 5s and 25s on both meridional and transmeridional direction.

Base on the real life experience, some traffic light already use the countdown display. Their role is telling the vehicles and pedestrians how much time they have by the traffic signal changing. So, the vehicles and pedestrians know whether there

is enough time to pass the intersection, which can avoid some accidents. For example, when north-south direction is green, vehicles run normally in this direction. And, the vehicle is waiting for red light vectors in east-west direction. If the vehicles in north-south direction realize no passing by the countdown display, they could slow down and wait for the next pass. The vehicle in the east-west direction can run normally without wait for the north-south direction vehicle. The crossroads will run smoothly. Considering the traffic jam makes vehicles waiting in a long line and some drivers are difficult to see the countdown display clearly, which may affect vehicles running. Therefore, the light vector-emitting diode countdown is realizable for the drivers and pedestrians even a mile away. The main function of Signal_Light_vector3 countdown control circuit (see Figure 3) is receiving Signal_Light_vector2 circuit output value, and converting it to be BCD code which is used in light vector-emitting diode display. The vehicles and pedestrians can clearly know how long time left before the lights changing

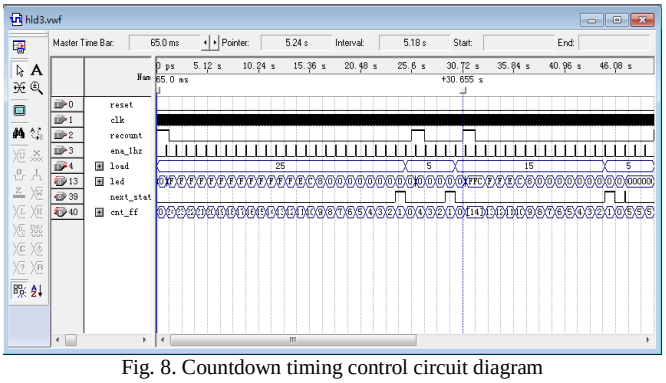

Fig. 8. Countdown timing control circuit diagram

This program is the using of look-up table method and light vector-emitting diodes (LED) to realize the countdown displaying. In Figure 9: when the internal counter start counting, the green lamp light, load minus 1 and put it into COUNT_ff. And then, COUNT_ff pointed the corresponding value in the case statement transmit which drives the LED displaying the remaining time. The conv_integer() also be used in the programming. It can convert COUNT_ff's value (assigned) to integer. From the figure 8, LED is a 25 bit signal output, which controls the output light vector emitting diode. This 25 bit output signal can be displayed by seven groups control LED which use "1" to "0" to extinguish the light vector. The program code in Appendix 3 is countdown control circuit.

Most traffic light systems use the automatic control mode to direct the traffic. But, in order to prevent traffic congestion during the rush hour sometimes the manual control is required, which give policemen ability to direct the traffic. Therefore, "hld4" traffic signal control circuit (see Figure 7) main function is to switch manual and automatic mode. Police officers could control the traffic light signal system operation by the external input.

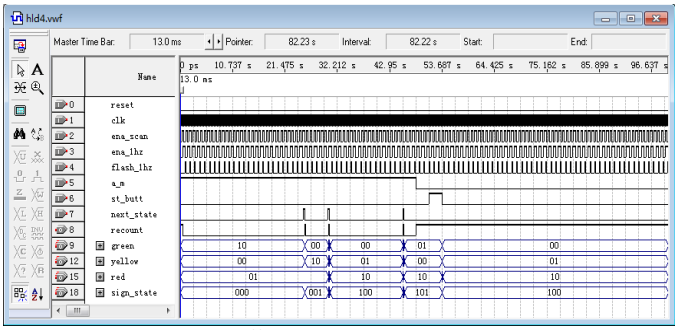

Fig. 10. Traffic Light Signal control diagram

According to the chart: when a_m=1 (the automatic mode) the next_state can be triggered.

Red, Green, Yellow was 01, 10, 00, when rewgsn=1. At this state, working light vectors are red ones for east-west direction (red = 01) and the green ones for north-south direction (green = 10).

Red, Green, Yellow was 01, 00, 10, when rewysn=1. At this state, working light vectors are red ones for east-west direction (red = 01) and the yellow ones for north-south direction (yellow = 10).

Red, Green, Yellow was 10, 01, 00, when gewrsn=1. At this state, working light vectors are green ones for east-west direction (Green = 01) and the red ones for north-south direction (red = 10).

When next_state_butt = 1, the state automatic switches to manual (auto_manual=0). Since reset = 1, Red, Green, Yellow is changed from 10, 01, 00 to 01, 10, 00 (i.e. red light vector for east-west direction, green light vector north-south direction, the initial state)

The hld5 circuit's job is to connect all of the sub circuits and process the timing analysis. When the process is completed, downloaded it to the FPGA and finished the hardware circuit verification.

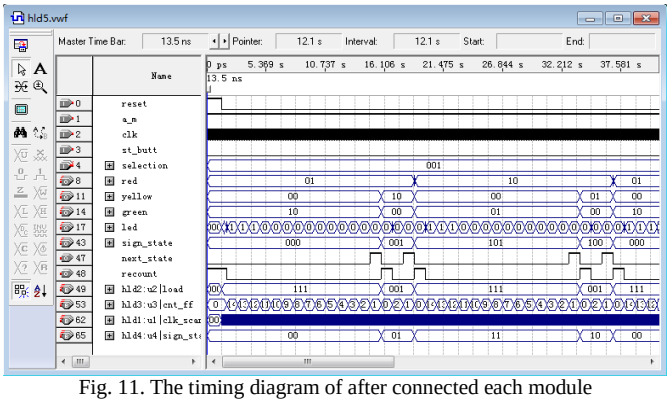

Fig. 11. The timing diagram of after connected each module

In most programming languages, at the beginning the program always calls the library to provide the basic procedure command. However, if it is a complex program,

library commands might not support completely. Therefore, a subroutine is required for programming.

This problem also exists in hardware description language (VHDL). In VHDL program's the first row (Library IEEE;) is to use IEEE 's library files in purpose. But, if the device is not in the library, that device have to be definite by user.

A package should contain at least one of the following structures:

(1)Constant Description: the channel to define the width of system data bus.

(2)The VHDL data type specification: mainly used to organize the general data type in the whole design.

(3)The element definition: Provision the VHDL elements involved in design file at the port define interface.

(4)The subroutine: subprograms are incorporated into the package, which makes them easy to be called in different parts of the design

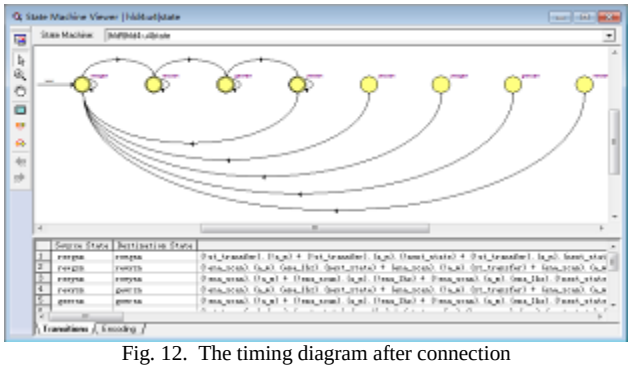

Fig. 12. The timing diagram after connection

III. RESULTS AND DISCUSSION

According to the graphics above, there are some insurmountable advantages for using state machine:

(1) State machine do not have the pure hardware digital control system's disadvantage which is no flexibility.

(2) Due to the structure of the state machine design is fixed relatively, especially in defining symbol Enumeration type state, it increase VHDL synthesizer's speed as much as possible. In addition, this device has many functions such as the controlled or automatic optimization state machine.

(3) State machines are easy to product a high quality synchronous sequential logic module. State machines is an undoubtedly good choice, because large-scale logic circuit design has too much competition and risk phenomenon

(4) Compared to other structure description in VHDL language, state machine has program level bright, structure clear, easy to read and understand benefits. In addition, it has unique advantage in debug, modifying and module transplantation.

(5) For the high-speed operation and control, the state machine has much more advantage. In the VHDL, a state machine can be composed of multiple processes and a structure can contain multiple state machines. In addition, a separate state machine's ability, which is in order to complete the calculation and control working, can rival a simply CPU function.

(6) High reliability.

The graphics below show the board demo successful follow the logic function:

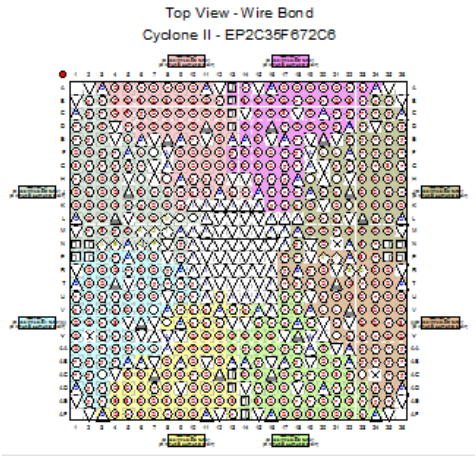

Fig. 13. Pin plan after all in/out put connect

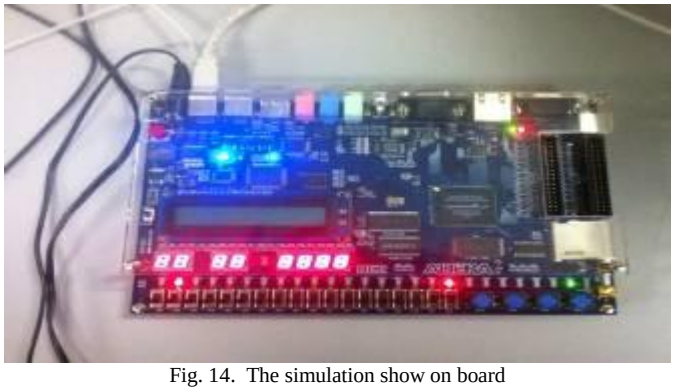

Fig. 14. The simulation show on board

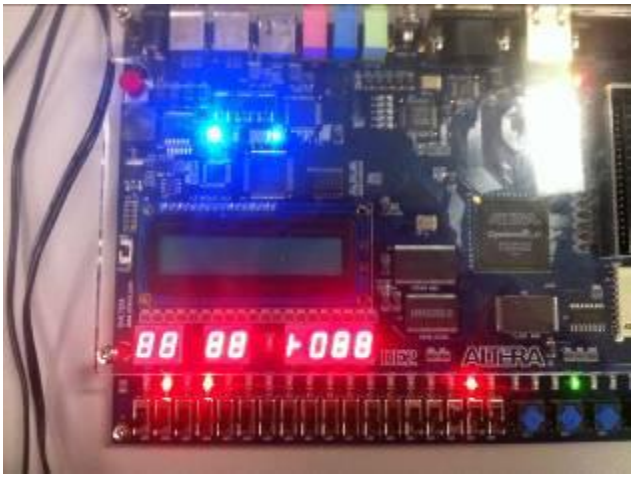

Fig. 15. The simulation show on board

IV. CONCLUSION AND FUTURE WORK

This design uses the VHDL hardware language description by text. In the establishment of the general

expectation function, it uses the hierarchical design to realize alternating lit the traffic lights, the countdown time display and vehicles' and pedestrians' safe passing command. The program's data can be set base on actual conditions (flexible modification). In the future, we will further improve the function of some modules, such as FPGA/CPLD kit validation.

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