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Design and Implementation of a Low Power Ternary Full Adder

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In this work, the design and implementation of a low power ternary full adder are presented in CMOS technology. In a ternary full adder design, the basic building blocks, the positive ternary inverter (PTI) and negative ternary inverter (NTI) are developed using a CMOS inverter and pass transistors. In designs of PTI and NTI, W/L ratios of transistors have been varied for their optimum performance. The ternary full adder and its building blocks have been simulated with SPICE 2G.6 using the MOSIS model parameters. The rise and fall times of PTI show an improvement by a factor of 14 and 4, respectively, and that of the NTI by a factor of nearly 4 and 17, respectively over that of earlier designs implemented in depletion-enhancement CMOS (DECMOS) technology. The noise margins improve by a factor of nearly 2 in PTI and NTI, respectively.

The ternary full adder has been fabricated in MOSIS two micron n-well CMOS technology. The full adder and its building blocks, NTI and PTI have been tested experimentally for static and dynamic performance, compared with the SPICE simulated behavior, and close agreement is observed.

The ternary-valued logic circuits designed in the present work which do not use depletion mode MOSFETS perform better than that implemented earlier in DECMOS technology. The present design is fully compatible with the current CMOS technology, uses fewer components and dissipates power in the microwatt range.

Key Words: *CMOS Ternary Full Adder, Ternary Logic, 3-Valued Logic, Low Power CMOS Full Adder*

1 INTRODUCTION

The performance of two levels (binary logic) is limited due to interconnect which occupies large area on a VLSI chip. In a VLSI circuit, approximately 70 percent of the area is devoted to interconnection, 20 percent to insulation, and 10 percent to devices [1]. One can achieve a more cost effective way of utilizing interconnections by using a larger set of signals over the same area in multiple-valued logic (MVL) circuits. This also solves the problem of pinout (the limit to the amount of data that can enter and exit a chip). Commercially multiple-valued logic circuits have made an appearance with the four-valued read-only memory (ROM) which Intel used in the control store of its 8087 numeric coprocessor [1]. Hitachi has introduced into the market a 16-valued mass memory with a high storage capacity. Kameyama et al. [2] reported a 32 × 32 bit signed digit (SD) multiplier implementation using MVL circuits realized in current-mode CMOS technology. The chip area and power dissipation of MVL multiplier implementation reduced to half that of the fastest conventional binary realization of the same multiplier.

The main draw back in multiple valued logic circuits is that their design techniques are more complex than the binary logic circuits [3]. The implementation of MVL circuits have ranged through integrated injection logic, emitter coupled logic, CMOS and n-MOS technologies and charge-coupled devices. In this work, the design of ternary-valued logic circuits have been explored over other ternary-valued logic due to the following reasoning. In a numerical system, the number N is given by $N = R^d$ where R is the radix and d is the necessary number of digits up to the next highest integer value where necessary. If the cost or complexity C in any system is assumed to be proportional to R × D [4], then $C = k(R \times d) = k[R(\ln N/\ln R)]$ where k is some constant. Differentiating with respect to R will show that for a minimum cost C, R should be equal to $e(2.718)$. Since in practice R must be an integer, this suggests that $R = 3$(ternary) would be more economical than $R = 2$(binary) [4].

Several authors [5–9] have used CMOS integrated circuits for the realization of three-valued logic circuits. These designs have used power supply voltages higher than the MOSFETs threshold voltage which resulted in high power consumption in the circuits. Mouftah and Smith [10] have reported a family of low-power three-valued CMOS circuits. In order to further reduce the power dissipation, increase the speed and eliminate the use of linear resistors in these circuits, Heung and Mouftah [11] proposed a design of ternary logic circuits based on the use of depletion enhancement complementary metal-oxide-semiconductor (DECMOS) technology. However, their implementation is not compatible with the current CMOS technology. The present CMOS technology does not use depletion mode transistors. The prime objective in our work is to minimize the number of transistors used, eliminate the use of resistors to lower the power consumption, reduce the propagation delay time and eliminate depletion mode transistors. The reduction in the number of transistors is our main focus as that enabled a more compact design which utilized the less chip area. The designs of positive ternary inverter (PTI), negative ternary inverter (NTI) and simple ternary inverter (STI) are based on use of a CMOS inverter and pass transistors/CMOS transmission gate at its output. The pass transistors at the output of inverter have been used to pull the output node to the required voltage levels and also provide sufficient equivalent resistance for the ternary logic implementation. The two unary operators PTI and NTI have been used to design a J_k arithmetic circuit, and ternary gate (T-gate) which is essentially a multiplexer. Fourteen such T-gates have been finally used in design of a ternary full adder. The design has been fabricated in MOSIS two micron CMOS n-well process, tested and performance verified.

2 DESIGN OF CMOS 3-VALUED LOGIC CIRCUITS

Three types of basic ternary operations are defined by [11]

$$\overline{X}_C = \begin{cases} C & \text{if } X = 1 \\ 2 - X & \text{if } X \neq 1 \end{cases} \quad (1)$$

C in Eq. (1) takes the values of logic 2 for a PTI, logic 1 for a STI and logic 0 for a NTI which correspond to higher level (1), middle level (0) and lower level (−1), respectively.

Fig. 1 shows the schematic of a positive ternary inverter (PTI). A p-MOSFET (Q_3) is connected to the output of a standard CMOS inverter. Mouftah and Garba [12] have pointed out that by altering the length-to-width ratio of the PMOS and NMOS channels can significantly

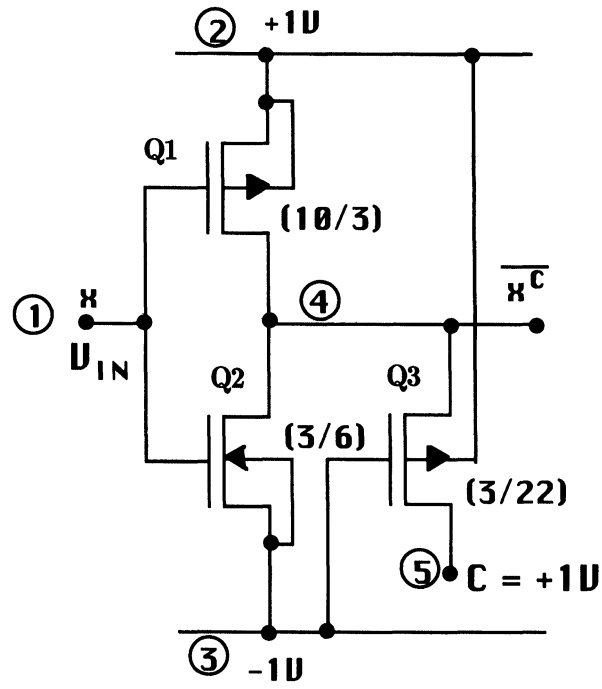

FIGURE 1 Positive ternary inverter.

change the resistance of channels. Thus, the resistance of the circuit is directly proportional to its L/W ratio which can be effectively used to change the resistance of transistors to suit design needs. However, there is a lower limit to the value of L and W due to the limitations imposed by the design rules of the foundry which in the present case is W/L of 3/2. In Fig. 1 the gate of p-MOSFET (Q_3) has been tied to the negative power supply to keep it constantly turned on. A control signal, C of +1V is applied to the source of p-MOSFET (Q_3). The W/L ratio of p- and n-MOSFETs (Q_1 and Q_2) in CMOS inverter are 10/3 and 3/6, respectively, and that of p-MOSFET (Q_3) connected to the output is 3/22. The p-MOSFET (Q_3) pulls the output of the CMOS inverter to +1V during the cycle where both transistors of the inverter are nearly in cut-off.

Fig. 2 shows the schematic of a negative ternary inverter (NTI). An n-MOSFET (Q_3) is connected to the output of a CMOS inverter with its gate tied to the positive power supply to keep it constantly turned on. A control signal, C of −1V is applied to the source of n-MOSFET(Q_3) and that pulls the output of CMOS inverter to that value. The CMOS inverter is forced to a value of −1V in phase where both transistors of the CMOS inverter are in the cut-off region. The W/L ratio of p- and n-MOSFET (Q_1 and Q_2) comprising the CMOS inverter are 19/3 and 12/3, respectively and that of n-MOSFET(Q_3) connected to the output is 6/23. The

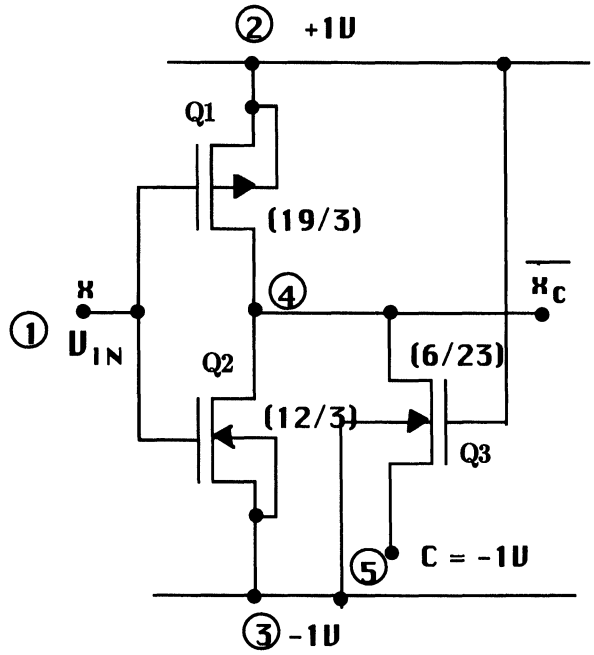

FIGURE 2 Negative ternary inverter.

value of 6/23 was chosen for W/L ratio so as to make it more resistive and avoid the pass transistor to latch the output of the whole circuit to -1V.

Fig. 3 shows the schematic of a simple ternary inverter (STI) designed by connecting a CMOS transmission gate to the common drain output of a CMOS inverter. The gates of p- and n- MOSFETs (Q_3 and Q_4) in the transmission gate are tied to negative and positive power supplies, respectively. The W/L ratio of p- and n-MOSFETs (Q_1 and Q_2) are 77/3 and 75/3, respectively and the corresponding values of transistors (Q_3 and Q_4) in transmission gate are 3/3 for both. The transmission gate aids in pulling up a control signal, C of 0V to the output when the inverter is in cut-off.

Figures 4 and 5 show the circuits for ternary NAND and ternary NOR, respectively. They are designed by connecting a CMOS transmission gate to the common drain output of a binary CMOS NAND and NOR. The gates of p- and n-MOSFETs (Q_5 and Q_6) in the transmission gate are tied to negative and positive power supplies, respectively. It can be seen from the Fig. 4 for ternary NAND that the transmission gate at the output helps pull the output to 0V when transistors (Q_1, Q_2, Q_3 and Q_4) are in cut-off. This happens in cases when inputs X = 0, Y = 0; X = 0, Y = 1; and X = 1, Y = 0, respectively. Similary operation of ternary NOR for the Fig. 5 can be explained. The output pulls to 0V when X = -1, Y = 0; X = 0, Y = -1; and X = 0, Y = 0, respectively.

3 TERNARY FULL ADDER DESIGN

A ternary full adder is a circuit that will add two trits and a previous carry trit, and generate a sum trit and a carry trit (a trit is equivalent of a bit in a binary system). It can be implemented by using two ternary half adders and a binary OR gate by analogy with the typical binary full adder. The advantage of multiple-valued carry ripple adders is in fact that the carry is always binary. Since the carry propagation makes up most of the delay in a carry ripple adder, this suggests that a multiple-valued adder could have a speed advantage over its binary counterpart because each digit carries more information than the binary case [13]. In the present design, the full adder is composed of fourteen T-gates which are essentially multiplexers. Each T-gate is further composed of a J_k

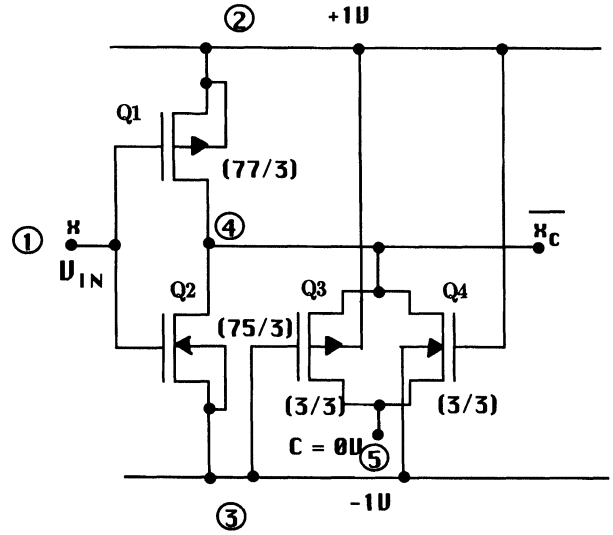

FIGURE 3 Simple ternary inverter.

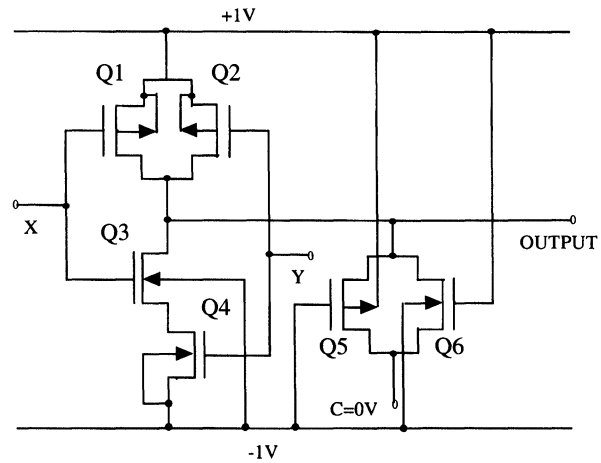

FIGURE 4 Ternary NAND circuit.

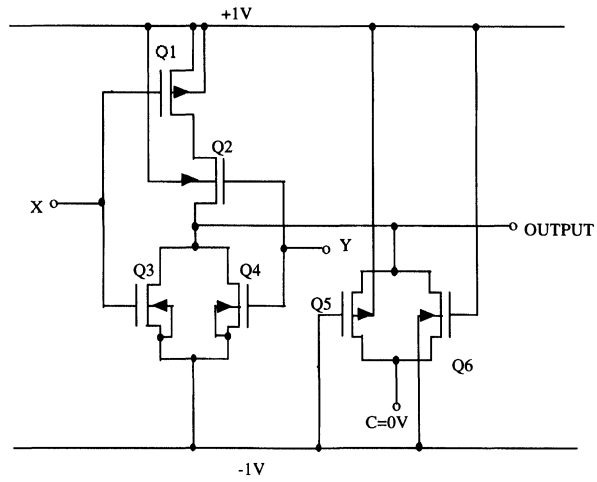

FIGURE 5 Ternary NOR circuit.

arithmetic circuit. The J_k arithmetic function is defined by

$$J_k(X) = \begin{cases} 1 & if X = 1 \\ -1 & if X \neq k \end{cases} \quad (2)$$

where k can take values of logic 0, logic 1 and logic 2 which corresponds to higher level (1), middle level (0) and lower level (-1), respectively. The block diagram of a J_k arithmetic circuit is shown in Fig. 6 which uses the logic design described in Ref. 13. The design of the T-gate circuit is based on the J_k arithmetic circuit. The function of the T-gate is described as follows [11]

$$T(y_1, y_2, y_3; X) = y_i \quad (3)$$

where i will take a value of 1 if X takes the value of -1, 2 if X is 0, and 3 if X is 1. The block diagram of a T-gate is shown in Fig. 7. Each ternary switch consists of a p-channel and n-channel enhancement transistor. The source of p-channel MOSFET is connected to the drain of n-channel MOSFET and vice versa. A control signal, C controls the n-channel MOSFET directly, and the p-channel MOSFET is controlled by $\overline{C}$. When C is equal to $+1$V the switch will be on, for C equal to -1V the switch will be off. The J_{-1}, J_0, J_1 signals of the J_k arithmetic circuits are connected to C of the ternary switch that has inputs y_1, y_2, y_3, respectively. The value of input to the J_k arithmetic circuit determines which one of the signals (y_1, y_2, y_3) will be steered to the output thus functioning as a multiplexer. The full adder comprises of fourteen T-gates as shown in Fig. 8. Since the J_k arithmetic circuit part of the T-gate is common, we can effectively reduce the component count by making it common for three stages. The area occupied by the ternary adder as a whole can be conserved in this way. The complete ternary full adder has been simulated using SPICE 2G.6 and the corresponding truth table is summarized in Table 1.

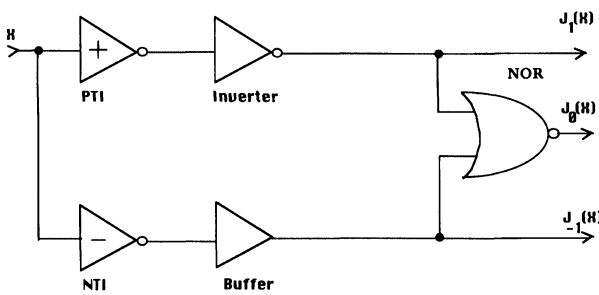

FIGURE 6 Block diagram of a J_k arithmetic circuit.

4 DESIGN VERIFICATION AND DISCUSSION

The design was fabricated in MOSIS two micron CMOS n-well process. The static and dynamic performance of the device were studied experimentally and compared with the corresponding SPICE 2G.6 simulation. Averaged Level 2 MOSFET model parameters from MOSIS were used and are summarized in Tables 2 and 3, respectively.

Figures 9(a) and (b) show the voltage transfer characteristics of PTI and NTI obtained from SPICE 2G.6 simulation, measurements, and Ref. 11, respectively. It can be seen from Figs. 9(a) and (b) that measured PTI and NTI characteristics have close agreements with the corresponding SPICE 2G.6 simulation. The present design of PTI and NTI also exhibit sharper voltage transfer characteristics compared to designs in Ref. 11.

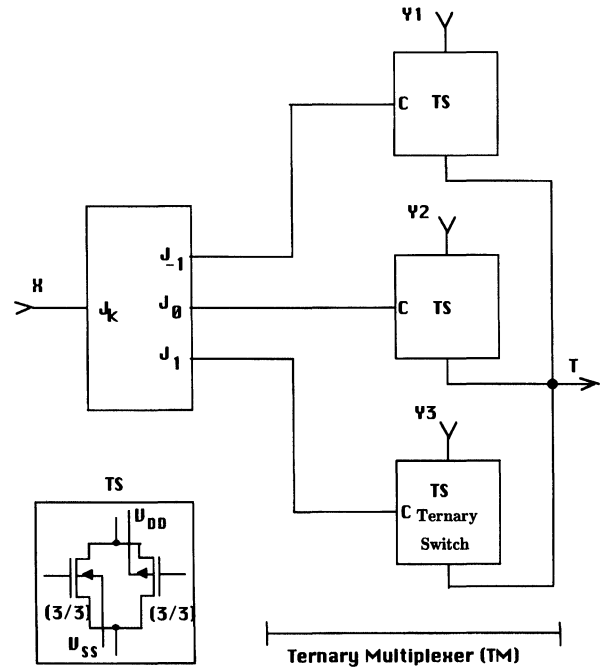

FIGURE 7 A ternary T-gate.

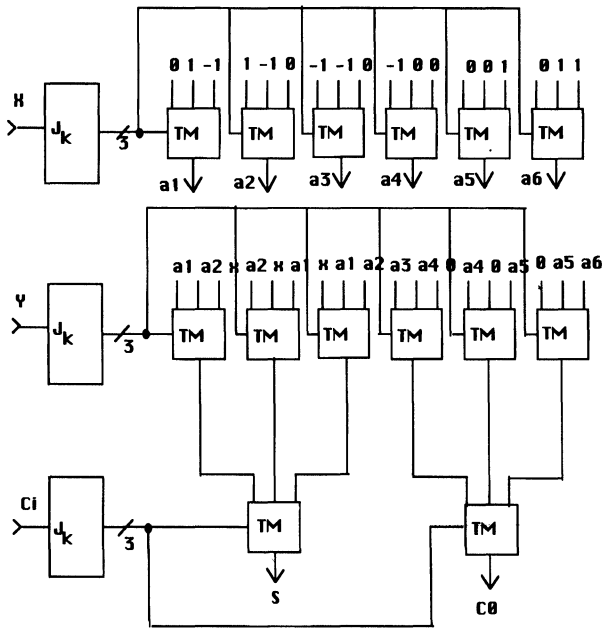

FIGURE 8 A ternary full adder.

TABLE 1
Truth table of a ternary full adder derived from SPICE simulation

x	y	c_i	s	c_o
−1	−1	−1	0	−1
−1	−1	0	1	−1
−1	−1	1	−1	0
−1	0	−1	1	−1
−1	0	0	−1	0
−1	0	1	0	0
−1	1	−1	−1	0
−1	1	0	0	0
−1	1	1	1	0
0	−1	−1	1	−1
0	−1	0	−1	0
0	−1	1	0	0
0	0	−1	−1	0
0	0	0	0	0
0	0	1	1	0
0	1	−1	0	−0
0	1	0	1	0
0	1	1	−1	1
1	−1	−1	−1	0
1	−1	0	0	0
1	−1	1	1	0
1	0	−1	0	0
1	0	0	1	0
1	0	1	−1	1
1	1	−1	1	0
1	1	0	−1	1
1	1	1	0	1

Table 4 summarizes noise margins corresponding to PTI and NTI, respectively. It can be seen from the Table 4 that significant improvement in noise margins in PTI and NTI is observed over the corresponding designs in Ref. 11.

Table 5 summarizes simulated rise time (t_r), fall time (t_f) of PTI and NTI, respectively, and propagation delay times (t_{pLH}, t_{pHL}) of ternary full adder circuit. The simulated transient behavior of these circuits are compared with corresponding circuits implemented in DECMOS technology [11] for 0 pF and 15 pF equivalent load capacitance, C_L and unbuffered circuit conditions. It can be seen from Table 5 that the rise and fall times of PTI shows an improvement by a factor of 14 and 4 and that of NTI by a factor of nearly 4 and 17, respectively over that of earlier designs implemented in DECMOS technology. It is also seen in Table 5 that the present full adder design performs better than the counterpart DECMOS design.

The fabricated device was tested for its performance evaluation and meets the required logic levels of ternary full adder summarized in Table 1. The PTI and NTI circuits were tested under pulse transient conditions with an equivalent 15pF load capacitance, C_L and compared with the corresponding simulations. The results are summarized in Table 5 for C_L = 15pF. The 15pF load capacitance corresponds to a 15pF input capacitance to the TEK 2467B oscilloscope used in the measurement which acts as a load to the device under test. It is seen from Table 5 that the measured values are in good agreement with the corresponding values obtained from simulations.

The power dissipation calculated from SPICE is summarized in Table 6 for PTI, NTI and ternary full adder, respectively. It is noticed that both designs in the present work and Ref. 11 exhibit power consumption in the microwatt power range. It is worth mentioning that the present design uses nearly one half of the silicon area of Ref. 11 for the design of a ternary full adder circuit.

5 CONCLUSIONS

A ternary full adder has been designed using fourteen T-gates and implemented in MOSIS two micron CMOS n-well process. The T-gate uses a J_k arithmetic circuit and three ternary switches. The J_k arithmetic circuit mainly consists of PTI and NTI apart from NOR, inverter and buffer circuits.

The PTI and NTI have been designed using an inverter and pass-transistors at its output. The design of PTI and NTI is fully compatible with the MOSIS two micron CMOS n-well process. It is shown that the performance

TABLE 2
Averaged SPICE NMOS model parameters

NMOS Parameters		
LD = 0.24974U	TOX = 421.00001E-10	NSUB = 2.296064E16
VTO = 0.94	KP = 5.504E-5	GAMMA = 0.9961
PHI = 0.6	UO = 628.787	UEXP = 0.22018
UCRIT = 115298	DELTA = 1.041739E-5	VMAX = 83151.5
XJ = 0.25U	LAMBDA = 1.67204E-2	NFS = 2.509221E12
NEFF = 1	NSS = 1E10	TPG = 1
RSH = 27.36	CGDO = 3.283127E-10	CGSO = 3.28322E-10
CGBO = 4.96808E-10	CJ = 4.1066E-4	MJ = 0.467277
CJSW = 3.9772E-10	MJSW = 0.334688	PB = 0.8

TABLE 3
Averaged SPICE PMOS model parameters

PMOS Parameters		
LD = 0.25000U	TOX = 421.00001E-10	NSUB = 5.917000E15
VTO = 0.96	KP = 2.296E-5	GAMMA = 0.5057
PHI = 0.6	UO = 262.000	UEXP = 0.22505
UCRIT = 21136.5	DELTA = .721685	VMAX = 41563.6
XJ = 0.25U	LAMBDA = 5.597E-2	NFS = 8.0389E11
NEFF = 1.001	NSS = 1E10	TPG = 1
RSH = 70.00	CGDO = 3.286622E-10	CGSO = 3.28322E-10
CGBO = 4.75120E-10	CJ = 12.0692E-4	MJ = 0.431872
CJSW = 1.9981E-10	MJSW = 0.177313	PB = 0.7

of PTI, NTI and ternary full adder implemented in CMOS technology closely matches with designs implemented in corresponding DECMOS technology. There is very good agreement between simulated and measured voltage transfer characteristics, noise margins and transient times for PTI, NTI and ternary full adder, respectively. A description of the design of ternary NOR, ternary NAND and simple ternary inverter without using depletion mode transistors and resistors are also included for completeness.

In the low power design range, the present design of ternary circuits uses lesser number of components and thereby reducing the chip area to nearly one half compared to designs of DECMOS technology. Furthermore, the use of depletion mode devices in the present work has been eliminated.

In the present work, the design of ternary full adder and its building blocks are designed within the limitation of the MOSIS foundry for the fabrication such as the non-availability of process modification to vary threshold voltages of MOSFETS. However, the present design could be further improved with the flexibility in process modification.

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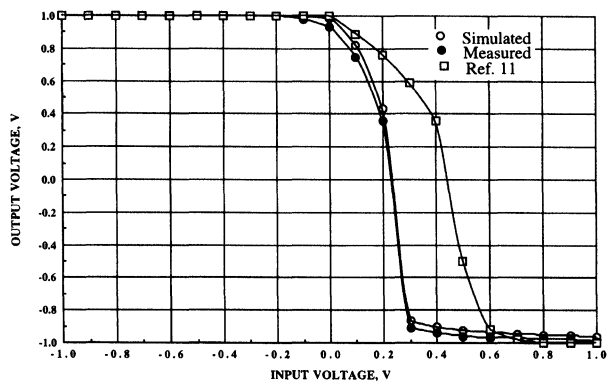

FIGURE 9 (a). Voltage transfer characteristics of a PTI.

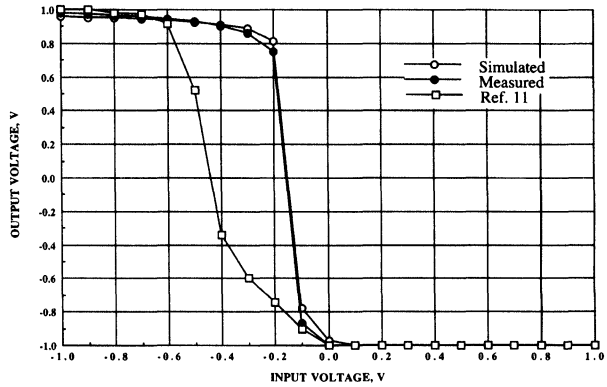

FIGURE 9 (b). Voltage transfer characteristics of a NTI.

TABLE 4
Noise margins characteristics

Gate		Noise Margin, Volts	
		1– –1	–1 –1
PTI	Present Work	0.10	0.70
	Measured	0.10	0.70
	Ref. 11	0.10	0.45
NTI	Present Work	0.80	0.10
	Measured	0.80	0.10
	Ref. 11	0.45	0.10

TABLE 5
Transient times

Gate	Load (C_L, pF)	t_r, ns(10–90%) –1 –1	t_f, ns(90–10%) 1 – –1
PTI	0 (Sim)	5	3
	0 (Ref. 11)	70	13
	15 (Sim)	405	415
	15 (Meas)	400	417
NTI	0 (Sim)	4	4
	0 (Ref. 11)	15	70
	15 (Sim)	416	210
	15 (Meas)	426	223
Ternary	0 (Sim)	15*	22**
Full	0 (Ref. 11)	50*	83**
Adder	15 (Sim)	474	739
	15 (Meas)	458	714

*t_{pLH}
**t_{pLH}

TABLE 6
Power dissipation

Gate	Power dissipation	
	Present work	Ref. 11
PTI	0.8 nW	1.97 μmW
NTI	12 μW	29 nW
Ternary Full Adder	15 μW	0.14 μW

*Power dissipation obtained using SPICE model parameters of Tables 2 and 3.

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Biographies

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