Design and Implementation of Real Time Data Acquisition System using Reconfigurable SoC

(DAS using RSoC)

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***Abstract*—System on chip (SoC) technology is widely used for high speed and efficient embedded systems in various computing applications. To perform this task, Application Specific IC (ASIC) based system on chips are generally used till now by spending maximum amount of research, development time and money. However, this is not a comfortable choice for low and medium-level capacity industries. The reason is, with ASIC or standard IC design implementation, it is very difficult task where quick time to market, upgradability and flexibility are required. Therefore, better solution to this problem is design with reconfigurable SoCs. Therefore, FPGAs can be replaced in the place of ASICs where we can have more flexible and re-configurable platform than ASIC. In the embedded world, in many applications, accessing and controlling are the two important tasks. There are several ways of accessing the data and the corresponding data acquisition systems are available in the market. For defence, avionics, aerospace and automobile applications, high performance and accurate data acquisition systems are desirable. Therefore, an attempt is made in the proposed work, and it has been discussed that how a reconfigurable SoC based data acquisition system with high performance is designed and implemented. It is a semicustom design implemented with Zynq processing system IP, reconfigurable 7-series FPGA used as programmable logic, hygro, ambient light sensor and OLEDrgb peripheral module IPs. All these sensor and display peripheral modules are interfaced with processing unit via AXI-interconnect. The proposed system is a reconfigurable SoC meant for high-speed data acquisition system with an operating frequency of 100MHz. Such system is perfectly suitable for high speed and economic real time embedded systems.**

Keywords*—Application Specific Integrated Circuit (ASIC); Advanced eXtensible Interface (AXI); data acquisition system; Field Programmable Gate Array (FPGA); Peripheral Module (PMOD); System on Chip (SoC)

I. INTRODUCTION

Many cases, the term ‘SoC’ was referred as an Application Specific Integrated Circuit (ASIC). The best example of an ASIC based application is mobile phone. Complex circuitry with multiple functions with high speed logic, interfacing of many peripherals including memory is implemented on single chip meant for specific application is known as application specific integrated circuit. The solution with SoC gives low cost with bulk volume production and enables high speed data transfers between the various system blocks [1].

The data acquisition is an integral part of any measurement and control systems used in various applications. The principle of data acquisition is to acquire real world physical parameters such as temperature, light intensity, pressure, sound etc. through appropriate sensors that are connected through multiple channel data selectors using time division multiplexing with serial peripheral interface technique or parallel processing technique [2]. The real and physical data which is in analog nature has to be converted in to digital representation using digitization. The process of conversion of analog signal into digital signal is known as digitization. After digitization, the digital data is read by the processor and process the data in readable format and then it will be sent to the display devices if standalone measurement is required. Otherwise, the data can be accessed remotely by using web-based data acquisition techniques using WiFi network.

Development time, cost and lack of flexibility are the major drawbacks of ASIC based SoCs [1]. These are appropriate choice for bulk volume production and where there are no requirements for upcoming enhancements. Because of this reason, low or medium volume market industries depends on a convenient solution, system on a programmable IC, an exact essence of system on reconfigurable device [1], [2]. This can be done with FPGAs which are reconfigurable and flexible than ASIC based SoCs. It is a better solution that using an FPGA for applications where system enhancements are desired [3]. The technical details of peripheral modules, Hygro, ALS and OLEDrgb are referred from [4], [5] and [6], respectively.

The earlier researchers were implemented FPGA based data acquisition designs using ISE software and Spartan 3, Spartan 6 FPGAs respectively. Daniel Roggow et al explained a laboratory workstation configuration with ZedBoard. They have demonstrated workstation setups for MP-1: Quadcopter Interface, MP-2: Digital Camera, MP-3: Target Acquisition and MP-4: UAV Control and they have received a good feedback from the students [7].

It is to be noted in [8], described about the system with three modules named as signal processing, data acquisition

with FPGA and data storage. It was designed by VHDL and simulated with ISE.

FPGA based high speed ADC with a sampling rate of 80 Mega samples and used DMA without loss of data and DDR3 memory was used for manipulations of data was discussed in [9]. The design was implemented with VHDL.

DAQ with Network Control Module using FPGA was discussed in [11]. LabView software tool was used to design and development of their design and tested with National Instruments data acquision and FPGA devices.

In [12], a 32 channel DAQ system for medical imaging and clinical application was presented. It was developed with FPGA, NI's PXI, ADC, signal generator, timing and synchronization modules. FFT-hardware was implemented in FPGA for the purpose of high frame rates, demodulation of the signal and higher order harmonics spectral characteristics.

In [13], Satillite tracking data with respect to the humidity, temperature and light data measurements with Zynq processor based reconfigurable SoC discussed efficiently.

Smart monitoring of automobile data logger design and prototype implementation with Zed Board and Xilinx platform was explained in [14].

The FPGA based processor designs, verifications of various applications are referred from [15], [16], [17], [18], [19] and [20].

As per the present survey of history in related work, the majority of the research work methodology is conventional FPGA front end flow designs using CAD tools. Therefore, the corresponding technology and performance of the designs are restricted within the technology scope of hardware and software tools used. Definitely, there is a requirement in the performance-based enhancements in the SoC based designs. Therefore, by adding today's technology towards SoC designs, especially in the design of high-speed real time embedded system-based applications, an attempt is made to design and develop the high-performance based data acquisition system in Zynq-7000 architecture platform.

II. Design of SoC based Data Acquisition System

A. Methodology

The proposed system methodology is a semicustom SoC block design using multiple IP integration using front end CAD tool, Xilinx Vivado System Design Suite and SDK software. The proposed system architecture consists of Zynq processing system interfaced with hygro, ALS and OLEDrgb via AXI interconnect. The hardware part of the design is loaded in to the Artix7 FPGA, which acts as a programmable logic device. The data processing and controlling part is implemented with application software with SDK and ARM9 processor, acts as processing system. The hardware used for verification are Artix 7 FPGA and the multiple sensors interfaced with FPGA. The results can be monitored by either standalone system or remote system through WiFi network. In the proposed system, peripheral modules, Hygro and ALS are used to access temperature, humidity and ambient light intensity. These parameters are displayed on OLEDrgb display and hyper terminal. The complete procedural flow with respect to CAD tool is illustrated in Fig. 1.

B. Design Procedure

The proposed research work is based on FPGA based SoC using Zynq processor. It provides a perfect stage for the implementation of flexible system on chips. Because, Zynq is a sandwich of a processing-system (PS) and programmable-logic (PL) [1], [3]. The PS is prepared with a dual-core ARM processor (ARM Cortex-A9). And the Artix 7 FPGA is used as programmable logic.

In the proposed work, Zed board is used that consists of Zynq architecture, integrated memory, a various number of peripherals, general purpose ports and high-speed interfacing ports for communication. The Programmable Logic is used for design and implementation of logic with high speed. And the processing system cares about software routines, operating systems, and provides the communication between software and hardware [2]. To meet this need, Xilinx high level synthesis tool, Artix 7 FPGA and ARM processor are used.

In the proposed architectural design of data acquisition system, AXI peripheral interconnect block is used to interface Zynq processing system with all peripheral interfaces as shown in Fig. 2.

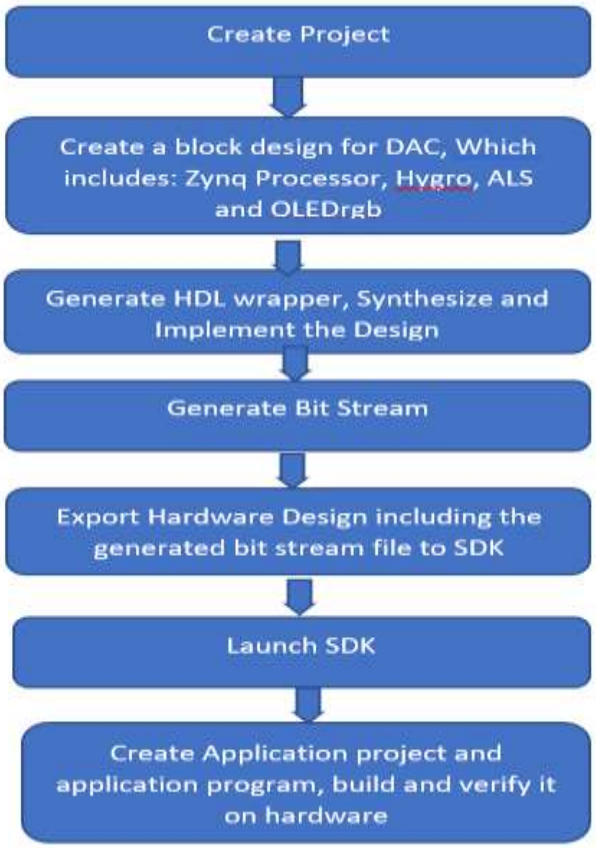

Fig. 1. Design and Implementation flow of SoC based DAS.

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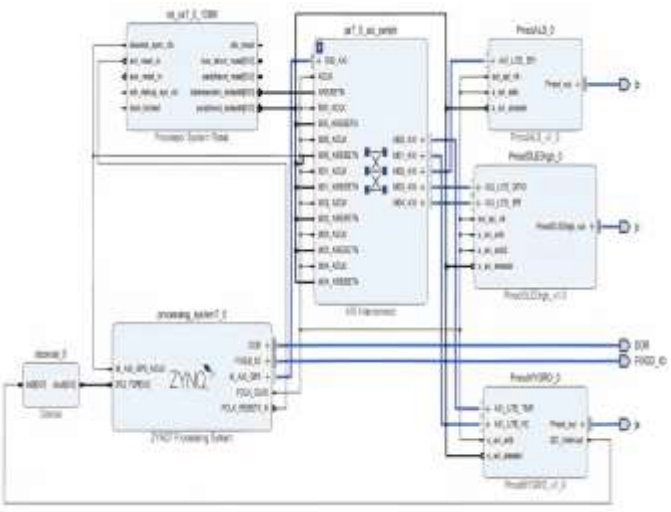

Fig. 2. Block Diagram of Data Acquisition System.

In this design, three peripheral modules are used, that are Hygro, ALS and OLEDrgb. The Hygro PMOD consists of temperature and humidity sensors. Hence, in order to select these parameters, one interrupt signal is used. And this interrupt is connected through Concat block. We can observe from Fig. 2, an interrupt-IRQ (Interrupt Request) is connected to output of Concat block and the input of Concat is connected to I2C Interrupt from PMOD Hygro. This Hygro PMOD is connected to port Ja of the Zed board. The other PMOD, ALS is connected to port Jb. To display the acquired and processed data, OLEDrgb is used which is connected to port Jc. In order to reset the system, one reset block, 'Processor System Reset' is used.

In the proposed system, we can view these parameters, in the hyper terminal. Hence, in its Peripheral I/O pins, one UART peripheral is enabled.

After completion of the block level design, validate it and make sure there will be no errors in the design. Then, generate HDL wrapper for the design, after that synthesize and implementation processes has to be done. Once if implementation is to be done successfully, then bit stream can be generated.

Next process is exporting the hardware including bitstream and launch software design kit (SDK) software to create and build the application project. Application project in the proposed system is developed using C. Here, the zed board consists of programmable logic (PL) and processing system (PS) are sandwiched in single IC. The created design will be loaded in PL, which is an ARTIX 7 FPGA. The control process, that is accepting the input data, processes it and displays the appropriate results at the display devices will be done by software logic instructed to processing system.

III. HARDWARE INTERFACE

Once, application project is ready, then make sure we have to interface PMOD Hygro to output connector A, ALS to connector B and OLEDrgb is connected to the output connector C as we have created our design in Fig. 2. The peripheral modules, hardware connectivity with zed board are shown in Fig. 3.

As there are three PMODs used in the proposed system,as illustrated in Fig. 4, their specifications and interface configuration details are explained as follows.

A. HYGRO Interface

The HYGRO PMOD consists of T1 HDC1080, which is an integrated digital temperature and humidity sensors. It provides accurate measurement with low power. It operates in a range of 2.7 V to 5.5 V supply. It is more economical and suitable for wide range of low power applications. The temperature and humidity sensors are calibrated with ±0.2°C (typical) and ±2% accuracy.

Fig. 5 illustrates the interfacing of HYGRO PMOD with Zynq Processor. It has dual modes of operations known as measurement mode and sleep mode. After power up, it will be in sleep mode and waits for I2C input and commands. The commands are used to trigger and read measurements, check the status condition of the battery and configure the timing conversions. Whenever it obtains a command to trigger a measurement, it switches to measurement mode from sleep mode. If it completes the measurement, it will return to sleep mode. The default mode of this device is, first it will measure temperature and then humidity. The bit pattern of the 16-bit temperature register is, first it will hold14-bit acquisition value and the two least significant bits are always zero.

The result accuracy depends on the time conversion. The temperature and relative humidity can be calculated using equations 1 and 2, respectively [3].

$$\text{Temperature } (^0\text{C}) = \frac{\text{Temperature}[15:00]}{2^{16}} * 165^0\text{C} - 40^0\text{C} \quad (1)$$

$$\text{Relative Humidity } (\%\text{RH}) = \frac{\text{Humidity}[15:00]}{2^{16}} * 100\%\text{RH} \quad (2)$$

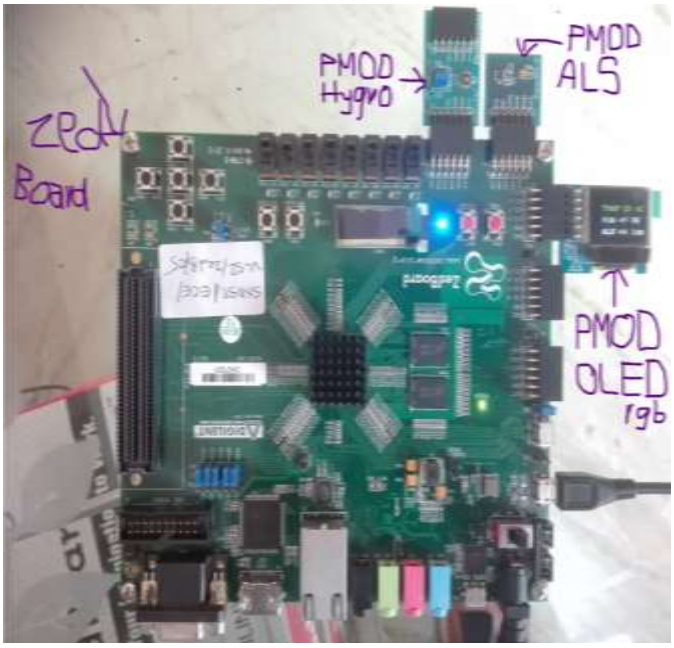

Fig. 3. Interfacing of HYGRO, ALS, OLEDrgb PMODs with PL via PS.

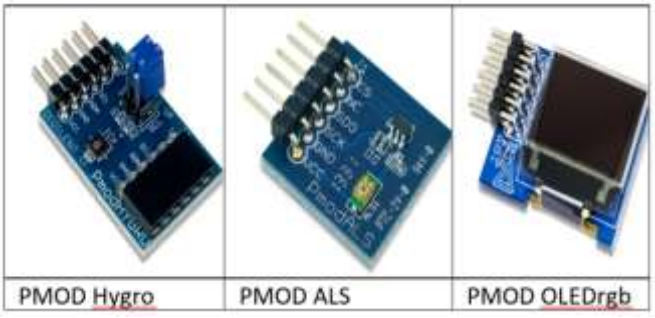

Fig. 4. PMODs used in Data Acquisition System.

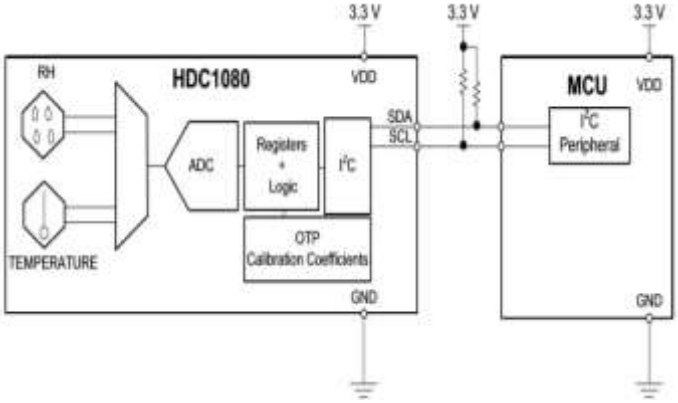

Fig. 5. Interfacing of HYGRO with Zynq Processor.

To complete the measurement of humidity and temperature, it is required to organize the register address to 0x02. We have to configure logic HIGH to Bit-12 to measure both humidity and temperature parameters. In order to set the resolution of a temperature, configure logic LOW to Bit-10 for 14-bit resolution or set it to logic HIGH for resolution of 11-bit.

In order to set the desired humidity measurement resolution, set the bits 9 and 8 of configuration register to 00 to achieve 14-bit resolution, or set to 01 to achieve 11-bit resolution or set to 10 to achieve 8-bit resolution. The measurements are triggered by setting an address pointer to 0x00 then, measurements waiting period will be completed, depending on the time conversion and read the output data [3]. Fig. 6 shows the timing signals under read operation when data is ready.

B. ALS Interface

The peripheral module ALS is a single ambient light sensor. When the ALS is exposed with light, it will convert the light into voltage signal. This analog voltage signal is converted into 8-bits of digital data by the analog to digital converter. The range of values from 0 to 255 indicates low light level to a high light level [4].

The pin configuration of ALS [4], Pin.1 is Chip Select (CS), Pin.2 is no connection (NC), Pin.3 is Serial Data Out (SDO), Pin.4 is Serial Clock (SCK), Pin.5 is ground pin, and Pin.6 is Power Supply, VCC (3.3V/5V). The operating voltage range of this ALS is 2.7V to 5.25V. However, the proposed work requires 3.3V.

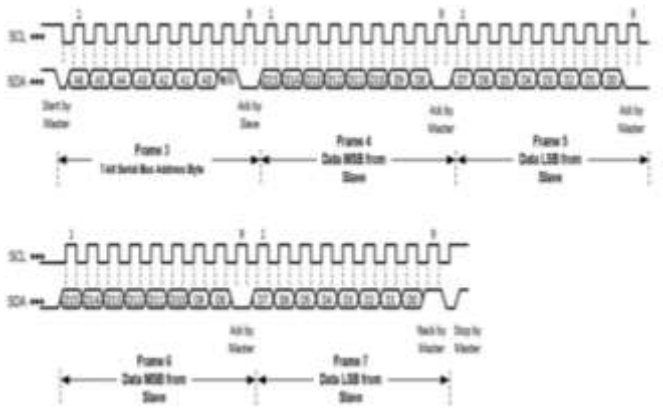

Fig. 6. Humidity and Temperature Measurement.

It communicates with the Zed board, via serial peripheral interface and requires a serial clock frequency (SCK) of 1 MHz and 4 MHz. When CS pin is made low, it operates in a regular mode of operation and brings a single reading in sixteen serial clock (SCLK) cycles [4]. The information bits are kept on the dropping edge of the serial clock. It is valid on the succeeding growing edge of SCLK. It consists of 3 zeroes at starting, the 8-bits of data with the most significant bit at first, and 4 zeroes at the end.

C. OLEDrgb Interface

There are six ports are used between the peripheral module, OLEDrgb to Zynq processing system via AXI interconnect. AXI_LITE_GPIO is connected to M03_AXI, AXI_LITE_SPI is connected to M04_AXI. Because, it is connected through SPI protocol. The input clock to this module is, ext_spi_clk, driven by the processing system through FCLK_clk0. s_axi_aclk of Hygro and s_axi_aclk of ALS are connected to s_axi_aclk and s_axi_aclk2 of OLEDrgb to have the communication appropriately.

The reset signal is generated from the processor reset block to all the peripheral modules including AXI interconnect as shown in the Fig. 2. The output port is connected to jC in order to interface the OLEDrgb to Zed Board as illustrated in Fig. 8.

IV. Development of Application Software

The process, export the created project into the software development kit using the Vivado software, will create “Hardware Base system” or “Hardware Platform”. Once, the hardware platform is created, software system is used or developed to complete the real time application. This software system is in the form of three layers over the hardware system base [10] as illustrated in Fig. 7. The second layer is board support package layer, which will set functions and drivers of low level that are needed by following layer over the board support package layer to communicate with hardware used. Application software is created with C or C++ and it will run over the operating system and it is the highest level of abstraction from the bottom hardware [1], [10].

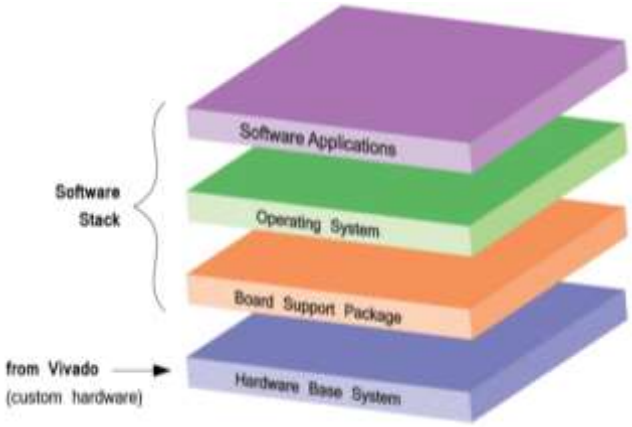

Fig. 7. Software Layers Over the Custom Hardware [10].

V. Results and Discussion

The Xilinx software development kit is used to create our data acquisition application. Compilation and debugging processes are also done within this tool. In the proposed application, we have connected three peripheral modules: Hygro, ALS and OLEDrgb as illustrated in Fig. 3. The application software is developed to read the temperature and humidity from Hygro Pmod and ambient light intensity from ALS Pmods respectively. These three data values are processed and displayed on OLEDrgb display Pmod as shown in Fig. 8.

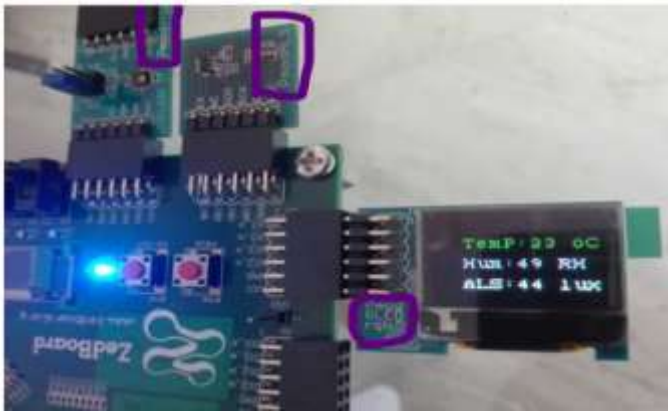

Fig. 8. Display of Temperature, Humidity and Ambient Light Intensity on OLEDrgb.

TABLE I. Utilization Report

Table I(A). LUT, Slice Registers, Muxes and Slices					
Name	***Slice LUTs (53200)***	***Slice Registers (106400)***	***F7 Muxes (26600)***	***F8 Muxes (13300)***	***Slice (13300)***
DAC_i	2007	2530	8	4	473
PmodALS_0	387	590	0	0	166
PmodHYGRO_0	580	541	8	4	211
PmodOLEDrgb_0	431	666	0	0	174
PS7_Axi_peripheral	593	696	0	0	242
Rst_ps7_0_100M	18	37	0	0	13

TABLE I. (B). LUT as Logic, Memory and FlipFlop Pairs

Name	***LUT as Logic (53200)***	***LUT as Memory (17400)***	***LUT Flip Flop Pairs (53200)***
DAC_i	1901	106	1130
PmodALS_0	370	17	265
PmodHYGRO_0	570	10	273
PmodOLEDrgb_0	414	17	300
PS7_Axi_peripheral	532	61	272
Rst_ps7_0_100M	17	1	15

TABLE I. (C). IOBs and LOGIC utilization

Name	***Bonded IOB (200)***	***Bonded IOPADS (130)***	***ILOGIC (200)***	***OLOGIC (200)***
DAC_i	1901	106	1130	2
PmodALS_0	370	17	265	1
PmodHYGRO_0	570	10	273	0
PmodOLEDrgb_0	414	17	300	1
PS7_Axi_peripheral	532	61	272	0
Rst_ps7_0_100M	17	1	15	0

The area of the proposed design occupied in the Artix 7 FPGA is represented in Table I. The LUT area for total DAC is 3.77%. Slice registers occupy 2.38%, total Slices occupy 5.59%.The detailed utilization report for LUT, Slice Registers, Muxes and Slices are illustrated in Table I(A). LUT as Logic, Memory and FlipFlop Pairs reports are specified in Table I(B). The number of input and output blocks and input logic and output logics are illustrated in Table I(C).

The proposed design, timing constraints are met satisfactorily as specified in the Table II. All the worst negative slacks for setup, hold and pulse widths are positive. There are zero negative slacks for setup, hold and pulse widths. Numbers of Failing end points are also zero. There were total 5636 end points for each setup and hold. And for pulse width, total end points are 2687.

The comparison of proposed system that is Reconfigurable data acquisition with respect to ASIC based data acquisition systems are illustrated in Table III and Fig. 9. Therefore, the summarized advantages of Reconfigurable data acquisition systems are listed as follows.

1) The existed data acquisition systems are implemented with ASIC (Application Specific Integrated Circuit) based, which does not include the enhancement facility in increasing the number of channels and the corresponding data acquisition and signal conditioning circuitry enhancement. The non-recurring engineering cost and time to market is very high. Whereas the proposed system is implemented with Reconfigurable device, and the corresponding cost and development time is very less. Hence, it is best suitable for low and medium industrial applications and even academic institutions can develop such systems.

2) The software and hardware used in the proposed system is suitable for low powered and high-speed applications which can meet with ASIC based designs.

3) Many embedded systems used LCD, LED or monitors for data acquisition purpose. Whereas in the proposed system, OLEDrgb is used for display of results which is a tiny, clarity colour display of 94 X 64 pixels [5].

TABLE II. DESIGN TIMING SUMMARY REPORT

Table II. Timing Report		
Setup	***Hold***	***Pulse Width***
Worst Negative Slack (WNS): 2.417ns	Worst Hold Slack (WHS): 0.026ns	Worst Pulse Width Slack (WPWS): 3.750ns
Total Negative Slack(TNS); 0.00ns	Total Slack(TNS); 0.00ns	Worst Pulse Width Negative Slack (WPWS):0.00ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 5636	Total Number of Endpoints: 5636	Total Number of Endpoints: 2687

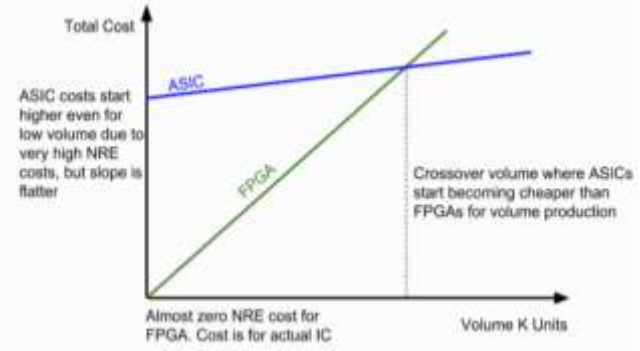

Fig. 9. ASIC Versus FPGA based Data Acquisition Systems.

TABLE III. COMPARISON ANALYSIS OF RECONFIGURABLE DATA ACQUISITION SYSTEM VS ASIC BASED DATA ACQUISITION SYSTEM

S.No.	**ASIC based Data Acquisition SoC**	**Reconfigurable Data Acquisition SoC**
1	Once the circuit design is taped out, alteration is not possible. Hence, it is less flexible for enhancement of the designs	In Reconfigurable data acquisition, FPGAs are used. With these, either partial or full reconfiguration is possible.
2	Not suitable for applications where design up gradation is very much required such as Radars, mobile applications etc.	These are extremely suitable for Radars, mobile base stations, high computing data applications etc.
3	These are not suitable for prototype of a design. ASICs are also prototype by FPGAs.	Best suitable for prototype and validation of a design.
4	Difficult for low and medium level industries because of unbearable NRE cost. Hence, it is a hard barrier to design entry and lot of time is required to market the end product.	Many advantages such as less NRE cost, easy barrier to design entry, less time required to market.
5	No doubt these are energy efficient, high performance and cost per unit will be less with bulk volume production.	With latest 7-series FPGAs, these are also more or less equivalent to ASIC based designs in terms of performance and power consumption

VI. CONCLUSION

The Reconfigurable SoC based data acquisition system is designed, implemented and made successfully functional using Xilinx Vivado System Design Suite 2018.1, Xilinx Software Development Kit (SDK), Zed development board, and three peripheral modules. Advantages of this proposed system has been clearly discussed with the comparison analysis of Reconfigurable data acquisition with respect to ASIC based data acquisition system. It is a cost effective, low powered and high accurate Reconfigurable embedded application.

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