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DESIGN OF 1µBAR RESOLUTION PRESSURE MEASUREMENT AND DISPLAY ASIC FOR MEMS CAPACITIVE PRESSURE SENSOR AND IMPLEMENTATION USING FPAA AND FPGA

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ABSTRACT

This paper proposed the design and implementation of 1µbar resolution pressure measurement ASIC (Application Specific Integrated Circuit) processing circuit for MEMS capacitive pressure sensor using FPAA (Field Programmable Analog Array) and FPGA (Field Programmable Gate Array). ASIC for altimeter application was designed to measure a pressure for the range from -100 mbar to 900 mbar. It has analog signal processing circuit and digital processing circuit, and its prototype is implemented using FPAA and FPGA respectively. Capacitance to Voltage (C-V) and Capacitance to Frequency (C-F) conversion techniques are used to measure the change in capacitance from MEMS pressure sensor. Simulation of the circuit is carried out in Anadigm tool and Xilinx v6.1. Prototype ASIC model is implementation is carried our using AN231E04 (FPAA) and Xilinx Spartan 3AN (FPGA). The implementation result shows 409 mV/pF and 21.9 kHz/pF sensitivity for C-V and C-F technique respectively. The frequency from C-F is computed in FPGA, and measured pressure is displayed in mbar with 1µbar resolution.

Keywords: ASIC, FPAA, FPGA, altimeter, pressure measurement, ASIC prototype, capacitive pressure sensor, MEMS pressure sensor.

1. INTRODUCTION

The emergence of ASIC processors for the specific applications has paved the way to achieve the efficient use of hardware resources than the general purpose processor. The FPGA and FPAA are the programmable ASIC processor, and they are popular for their flexibility in the field of prototyping. The objective of this work is to design and prototype ASIC to process the measured pressure from MEMS capacitive pressure sensor, and to display the measured pressure at 1µbar resolution using FPAA and FPGA. FPAA and FPGA reduce the time-to-market particularly in the design phase providing reconfigurability in analog and digital domain respectively. This work was proposed to design of ASIC signal conditioning and the processing circuit for MEMS capacitive differential pressure sensor (CDPS) proposed in the work [1-6] and to develop a smart pressure sensor using C-V and C-F conversion techniques and custom designed digital processing circuit.

Xiao-Dong Huang *et al.* developed a fully integrated absolute capacitive pressure sensor in which, the pressure-sensing part of the sensor is a solid state capacitor, which is based on the sandwich structure consisting of poly-Si/gate oxide/n- well Si [7].The flexible structure, the composite membranes are deformed, causing a load deflection bending in response to applied pressure. As a result of the experiment, pressure applies from 800 hPa to 1100 hPa at room temperature, the capacitance varies from 1207 pF to 1220 pF, which causes the variation of the capacitance about 13 pF, showing the sensitivity is about 43.6 fF/hPa.

Tomio Nagata *et al.* proposed a system design for low-pressure measurement with compensated circuitry on single silicon chip [8]. The compensated circuitry is designed with reference converter along with sensor converter. The system consists of capacitance to frequency (C-F) converter circuit as the capacitance change is realized with the change in frequency of applied signal. Schmitt trigger is implemented to convert it into the square pulse, which is digitized using 12 bit up/down counter. High sensitive CDPS structure with square and circular diaphragm polyimide membrane with and without bossed diaphragm is proposed in [1-6]. Deflection and capacitive characteristics for the differential pressure range are analyzed. Simulation result for circular bossed diaphragm shows 467 nm/mbar and 0.25 fF/mbar deflection and capacitive sensitivity. Similarly square bossed diaphragm shows 469 nm/mbar and 0.49 fF/mbar deflection and capacitive sensitivity. Simulation result shows 109 nm/mbar and 146 nm/mbar deflection sensitivity and 0.36505 fF/mbar and 0.5764 fF/mbar capacitive sensitivity for without center bossed circular and square polyimide diaphragm membrane [1-6].

Several work reports on signal conditioning circuits for piezoresistive pressure sensor [9]. D. P. Morales et al. describes the application of FPGA and FPAA [10] as a unique system for interfacing sensors and depicts the use of both analog and digital field programmable technologies which implies some advantages over traditional microcontroller based interfaces.

The functional blocks in the analog module are designed using Anadigm Designer2 software and implemented in FPAA (AN231E04) [11]. Giuseppe et al. proposed the signal conditioning system for capacitive sensors using FPAA [12] and the resolution of the measured pressure depend on the ADC resolution of

FPAA [13]. The gain of each channel is adjusted automatically, and it is independent according to the amplifier input signal such that a good conversation resolution, irrespective of the wide dynamic range of the signal [14-15].

This paper is organized as follows: Section II discusses the design of proposed ASIC for pressure measurement system. Implementation of ASIC using FPAA and FPGA was discussed in Section III. The simulation and implementation results are discussed in section IV followed by the conclusion.

2. ASIC DESIGN

MEMS capacitive pressure sensors working principle, design and characterization were discussed in [1-4] consist of fixed plate and flexible diaphragm membrane, both are placed parallel to each other separated by a small distance with the air dielectric. This sensor is designed to measure differential pressure in the range of -100 mbar to 900 mbar which is equivalent to the atmospheric altitude of -1500 ft to 50000 ft. To display the altitude in feet, the µbar pressure measurement system is required. This design aims to give 1 µbar resolution which is equivalent to 0.05 ft altitude.

The capacitance of the sensor changes on the change in atmospheric pressure, and the capacitance, is inversely proportional to the distance between the plate and the diaphragm. The ASIC processor is developed to realize the changes in capacitance, due to variation in atmospheric pressure, in terms of frequency variation. The basic block diagram of the custom designed ASIC processor is shown in Figure-1.

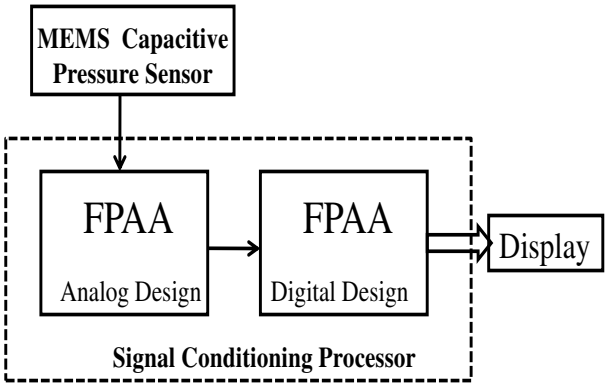

Figure-1. Basic block diagram of ASIC processor for 1µbar resolution pressure measurement.

2.1 Analog module

The MEMS capacitive pressure sensor is connected to FPAA through a resistor feedback network. The analog signal conditioning is processed in FPAA and digital processing in FPGA. Both the reconfigurable devices are used for a prototype implementation of the proposed design, and its circuit parameters are modified by n number of times based on the real-time sensor parameters.

Two analog signal conditioning methods are used for FPAA implementation namely, Capacitance to Voltage (C-V) conversion and Capacitance to Frequency (C-F) conversion. The designed circuit is first implemented using Anadigm Designer2 software to study the circuit characteristics for the given input parameters.

In C-V conversion method, the design is to achieve the variation of output voltage range of more than 3V for the sensor capacitance range from 1 pF to 2 pF. Therefore, the resolution of display depends on the resolution of ADC in FPAA. In C-F conversion method, to achive 1 µbar resolution the variation in output frequency required is 1 MHz, for the capacitance changes from 1 pF to 2 pF. The output of the analog module is an analog square wave. A comparator is designed in FPAA module to convert it into a digital pulse, which acts as input for digital circuit block in FPGA.

The digital block consists of a counter, encoder, comparator, and memory elements. The custom designed digital module counter is implemented to count the digital pulse for a specific period at regular intervals. The digital output of the counter is manipulated to display the value of pressure. The functional block diagram of ASIC is shown in Figure-2.

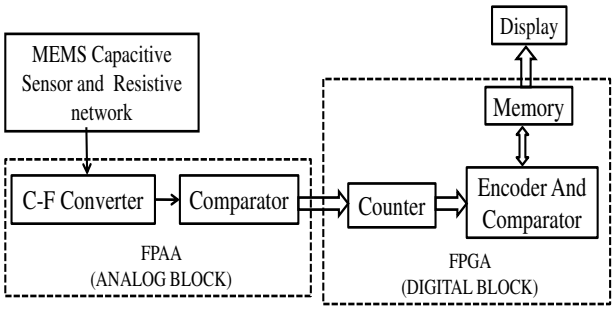

Figure-2. Functional block diagram of ASIC Processor.

2.1.1 C-V Conversion method

In this method, the capacitance variation is converted into the digital data using ADC. The functional block diagram of C-V conversion method is shown in Figure-3.

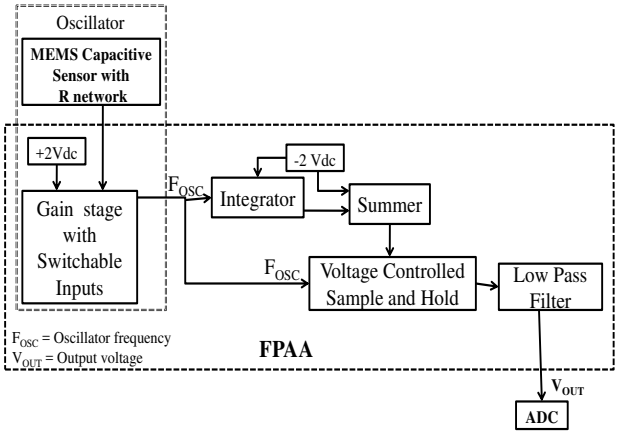

Figure-3. C-V conversion block in FPAA.

The basic principle behind the C-V conversion method is the frequency variation of the oscillator is converted into a variation in time with the help of an integrator. The integrator output is ramp signal, which is fed to a summer. The summer extends the ramp in order to increase the range of the output voltage and is given to a sample and hold block. The voltage at the sample and hold section is determined by the oscillation frequency.

2.1.2 C-F Conversion method

The MEMS capacitive sensors capacitance with external resistors network is used construct an oscillator circuit, whose output frequency is proportional to the measured pressure and its implementation block diagram in FPAA is shown in Figure-4. C-F converter is constructed using gain switch configurable analog module (CAM) in FPAA. The frequency of an oscillator varies according to the variation of the capacitance of the sensor. The oscillator output is given to the comparator to produce the square wave.

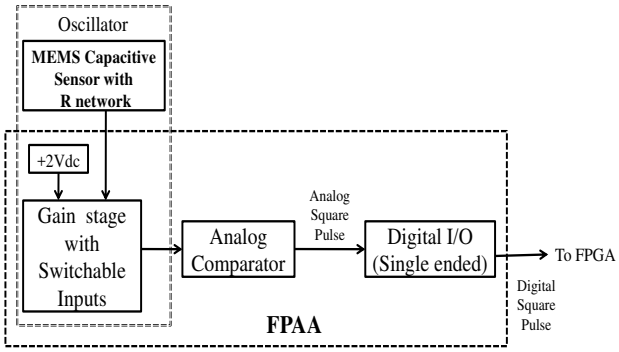

Figure-4. C-F conversion block in FPAA.

2.2 Digital processing circuit

The custom designed digital processing circuit built with 24-bit BCD counter; registers, encoder and LCD interface circuit, implemented using FPGA shown in Figure-5. The square output pulse from FPAA is given as input to the custom designed digital circuit. The timer module is designed to give trigger pulse for every 1s using on-board clock frequency. The counter counts the pulse for the specific time provided by the timer module, and the count is transferred to the 24-bit register. The data of 24-bit from the register which is manipulated into six 8-bit the ASCII (American standard code for information Interchange) codes, whose values represent the measured pressure. This ASCII code is transferred to external LCD module along with three 8-bit command codes to display the measured pressure.

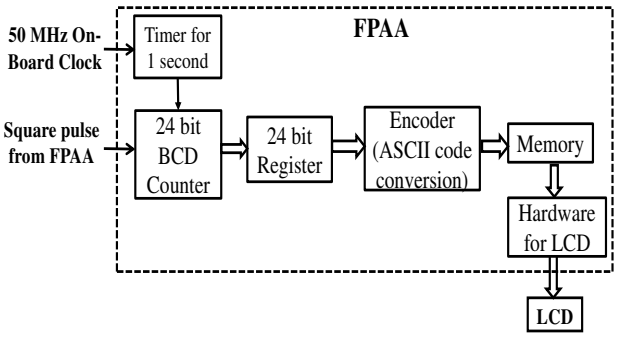

Figure-5. Digital processing circuit in FPGA.

2.3 Software execution

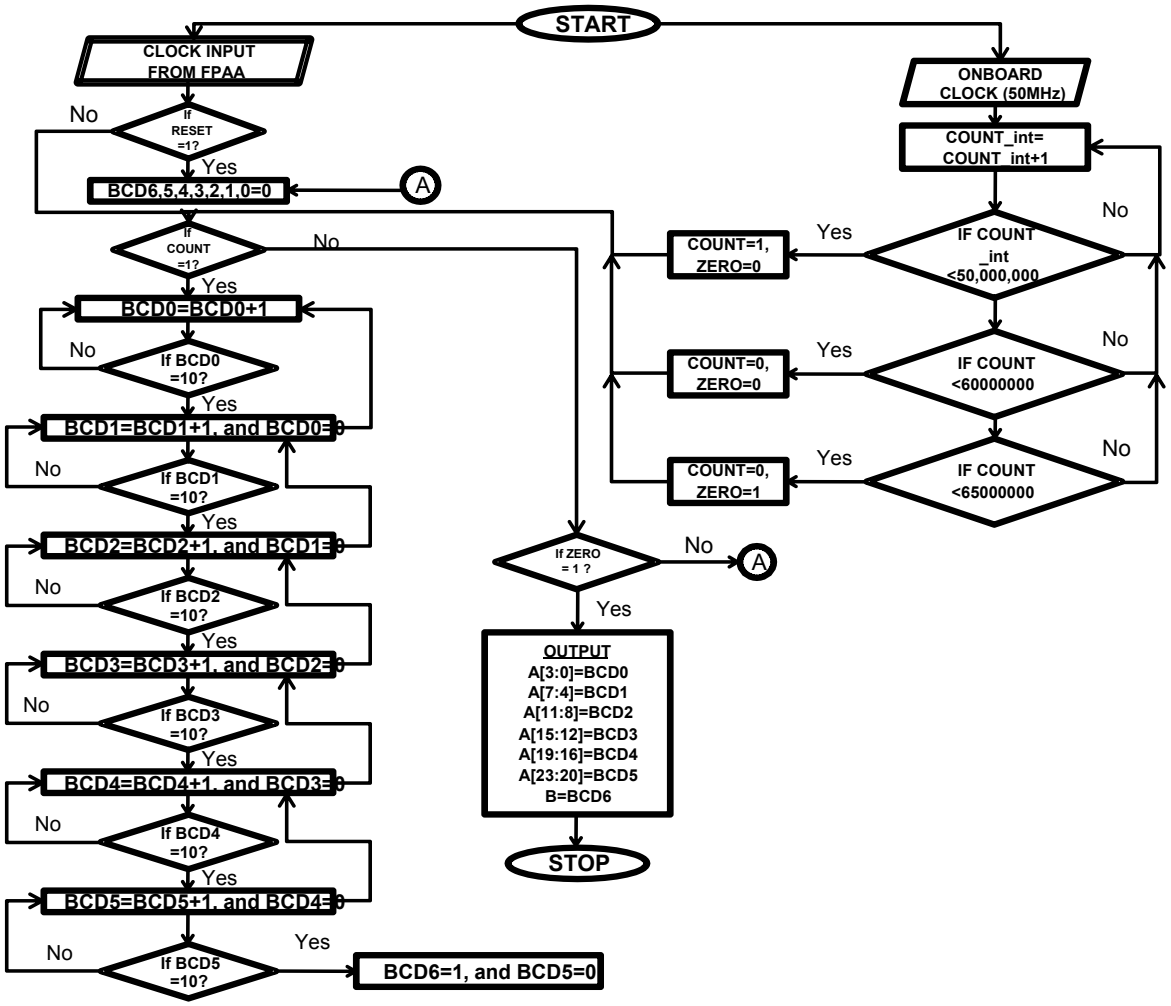

Figure-6. Execution flow for 1 µbar resolution display in FPGA.

A 1 µbar resolution display execution flow chart is shown in Figure 6, it uses custom designed 24-bit BCD counter. The data from the 24-bit register is taken for manipulation of the measured pressure with 1 µbar resolution pressure change.

The algorithm for the BCD counter module is as follows

Step 1: Start the program by counting the internal clock (50 MHz) output by 26-bit ripple up counter, which is acted as timer module.

Step 2: If the counter output (count int) < 50,000,000 i.e., the time period of 1s for 50MHz clock value of count =1 (high) and zero =0 (low); If 50,000,000 count int<60,000,000, then count =0 and zero =0; if count int 60,000,000 then count =0; and zero =1; when all the bits of the output become 1s the next count will reset the counter. The value of count and zero, control the counting operation of BCD counter in main module.

Step 3: If the reset =1 (high), then reset the 24-bit BCD counter and all its outputs become 0s counting action will be stopped.

Step 4: If the reset =0 (low) and count =1, then 24-bit BCD counter counts the clock pulse from the FPAA. Counting initiated and it is as follows. (24-bit BCD counter has six 4-bit counters as sub-module which has the outputs BCD0, BCD1, BCD2, BCD3, BCD4, and BCD5 respectively).

- The clock from the FPAA is given to counter0, if its output (BCD0) exceeds 1001 (9) the next counter (counter1) output is incremented by 1 and BCD 0 is reset to 0000 (0) and continue the count.
- If the counter1 output (BCD1) exceeds 1001 (9), then the output of next counter is incremented by 1 and BCD1 is reset to 0000 for next count.
- Similarly, the successive counters are incremented by 1. When the previous counter outputs exceed 9 or 1001 and then previous counters are reset to zero, for further counting operation.

Step 5: If count =0 and zero =0, then the BCD counter stops the counting operation and the output of each 4-bit counter (sub-module) is stored in the 24-bit register from (BCD0- BCD5) to (LSB-MSB) of the register.

Step 6: If count = 0 and zero =1, then the 4-bit counters are reset to 0s and ready for next counting operation.

Step 7: Step 4, 5, 6 are repeated and counting operation is continued, after 1sec counting period the output of 24-bit counter updates the 24-bit register.

3. IMPLEMENTATION OF ASIC USING FPAA AND FPGA

The implementation of the proposed custom designed ASIC processor using FPAA (AN231E04) for the analog module and Xilinx Spartan 3AN (FPGA) for the digital module is shown in Figure-7. Anadigm designer2 software is used for simulating the designed analog circuits and also used to generate synthesized codes to dump into the AN231E04 module for implementation. Digital module circuit is implemented using Verilog HDL, behavioral simulation is done in the ISim simulator, synthesis and implementation of the design is done using Xilinx 6.1 and FPGA.

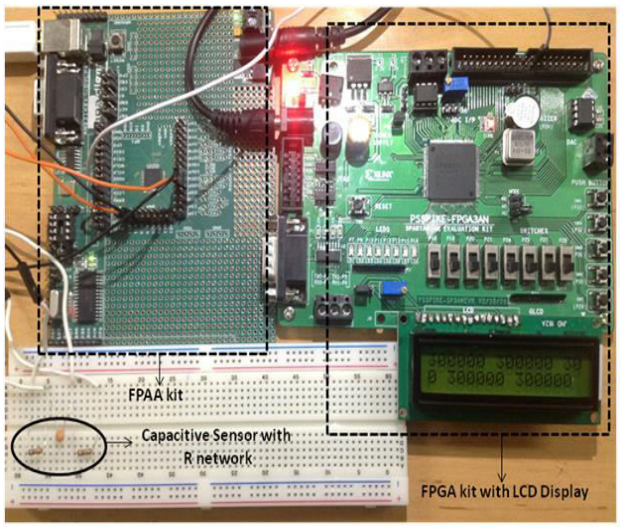

Figure-7. Experimental setup to implementation ASIC using FPAA and FPGA.

3.1 C-V Conversion method

The C-V conversion method has functional blocks such as oscillator; integrator, summer, sample and hold, and low pass filter are implemented in (AN231E04) FPAA. They are implemented by using various reconfigurable CAMs in FPAA. The design is done in Anadigm designer2 software. The in-built -2V DC supply is connected to integrator as input and one its output act as one of the inputs for summer. The oscillator section along with MEMS capacitive sensor has the same function as mentioned in C-F conversion. The gain switch CAM with RC feedback network generates oscillation. The generated oscillation acts as input to comparator section of the integrator CAM. The repeating ramp signal is available at the output of the integrator CAM, as DC voltage is given as input to it. Output of the integrator ramps for 0V, it is reset to 0V by the comparator output as control signal. The reset action is controlled by the comparator to which the oscillation is given as input. Then, the ramp signal is given to the Sum InvCAM; by the increasing the gain of the Sum Inv CAM the full voltage range of the FPAA from -3V to 3V is covered. The design and implementation of analog module (C-V conversion method) in FPAA is shown in Figure-8.

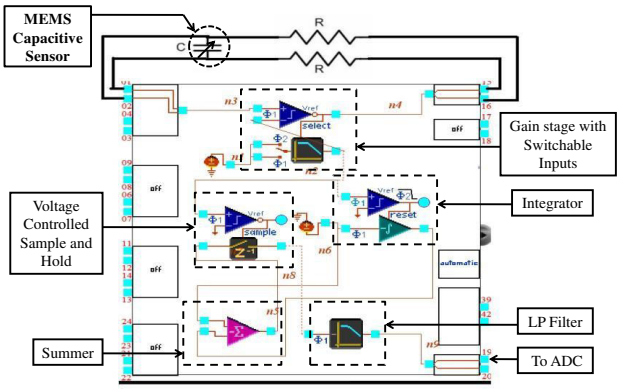

Figure-8. Implementation of analog module (C-V conversion method) in FPAA.

3.2 C-F Conversion method

The oscillator is built using gain switch CAM available within FPAA and the MEMS capacitive sensor and resistors network is connected externally to FPAA is shown in the experimental setup. The hysteresis is necessary to produce sustained oscillations that can be achieved by using the comparator of the switch gain CAM is as shown in Figure-9.

Conditions for sustained oscillation in FPAA are:

a) The polarity of the two gains should be opposite.
b) One gain should be less than +1 and another gain should be greater than -1.

Feedback network is formed by connecting external resistors between positive terminal (P) of I/O cells 1 and 3 and another resistor between negative terminals (N) of the I/O cell 1 and 3. Then, the MEMS capacitive sensor is connected between positive and negative terminals of the I/O cell 1. When the supply is given to the FPAA, the differential voltage of +1.5V and -1.5 V will be available at I/O cell3 of P and N terminals respectively which charges and discharges the capacitor through resistors.

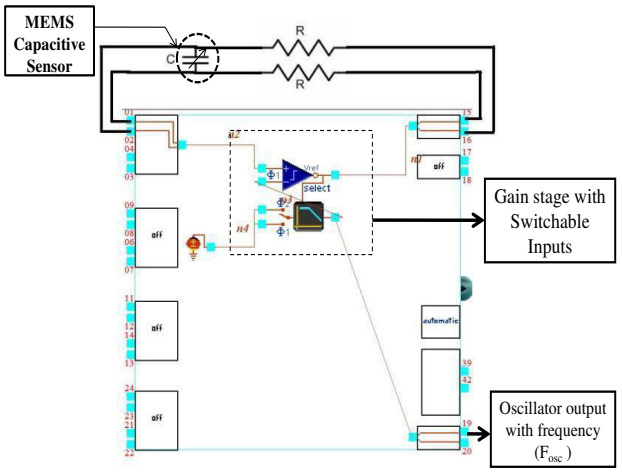

Figure-9. Oscillator circuit design in FPAA using gain switch CAM.

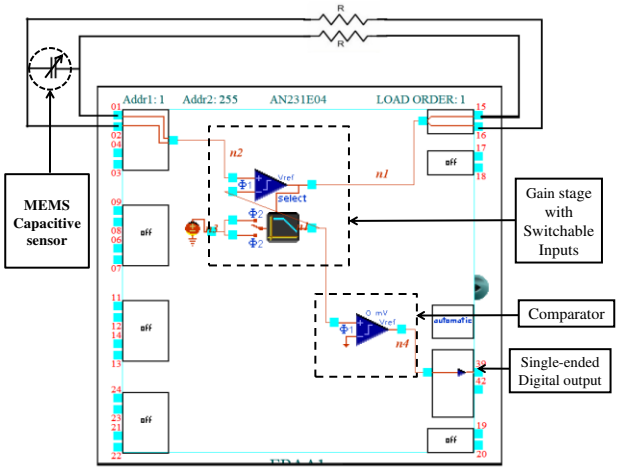

Figure-10. Implementation circuit of C-F conversion analog module in FPAA.

The voltage across the capacitor is given as input to the comparator in the FPAA through I/O cell 1. The rising and falling of voltage due to charging and discharging of the capacitor is compared with output of the gain stage. The comparator output switches from high to low and vice versa, which switches the output of the gain stage. This process continues, and the oscillation is sustained at the output of the gain stage. The frequency of the oscillation F_{osc} is inversely proportional to time constant (RC) and the gain of the gain switch CAM. The implementation of analog module (C-F conversion method) in AN231E04 is shown in Figure-10. The oscillator output is given to a comparator which is configured to signal ground mode. The comparator produces the square pulse, and the oscillations are compared with ground potential. This analog square pulse has both positive and negative voltages available at its rails. Single ended comparator in the digital I/O cell is used to convert it into digital output, which acts as input to FPGA.

4. RESULTS AND DISCUSSIONS

Analog signal conditioning for the MEMS capacitive pressure sensors are implemented using AN231E04 (FPAA) and their capacitance to frequency characteristics are obtained. The digital module synthesized in Xilinx tool and simulated using ISim simulator and implemented in Xilinx Spartan 3AN (FPGA).

4.1 C-V Conversion

C-V Conversion method using FPAA is shown in Figure-11. It is tested using different values of fixed capacitors, instead of MEMS capacitive sensors for prototyping. The ceramic capacitors of capacitance range from 1pF to 10pF with feedback resistor R = 20 kΩ are connected and the output voltage is noted for each capacitance value.

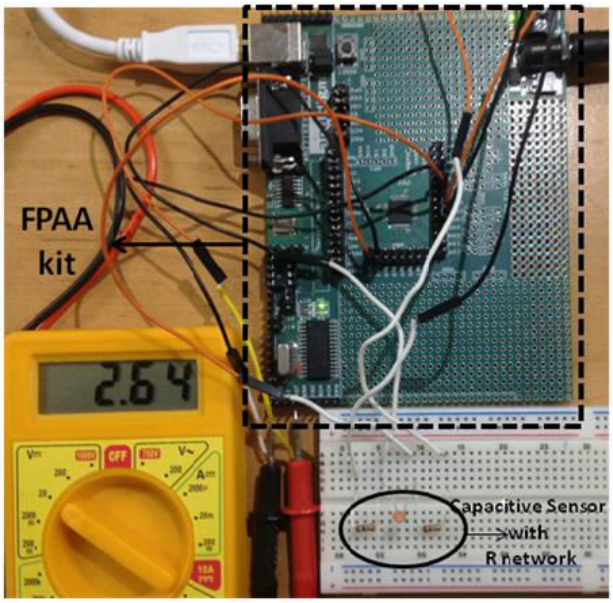

Figure-11. Experimental setup of C-V Conversion Method using FPAA.

Figure-12 shows the C-V characteristic input capacitance to output voltage using C-V conversion method. When the capacitance varied from 1 pF to 2 pF, the output voltage varies from -1.2V to 2.89V. From this relationship between output voltage and the input capacitance, it is observed it has linear characteristics. The sensitivity is 0.409 V/pF.

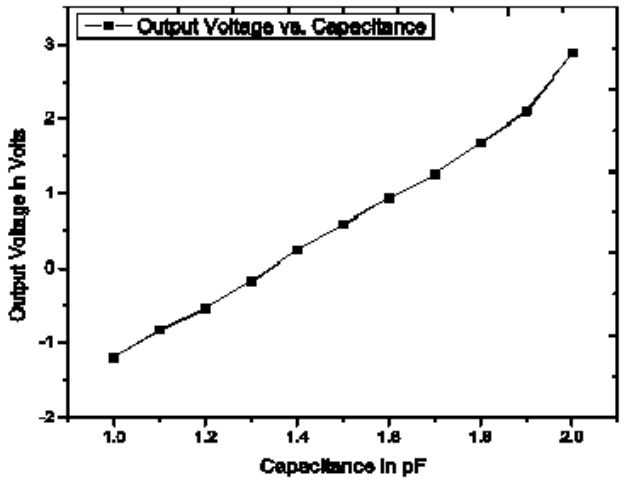

Figure-12. Output Voltage of Oscillator Vs Sensor Capacitance using C-V conversion method.

4.2 C-F Conversion

The implemented C-F conversion design is tested using various values of standard fixed capacitor instead of MEMS capacitive sensor value. The fixed capacitors of capacitance range from 1 pF to 2 pF is used with a feedback resistorR = 15 kΩ. The frequency of the output signal measured.

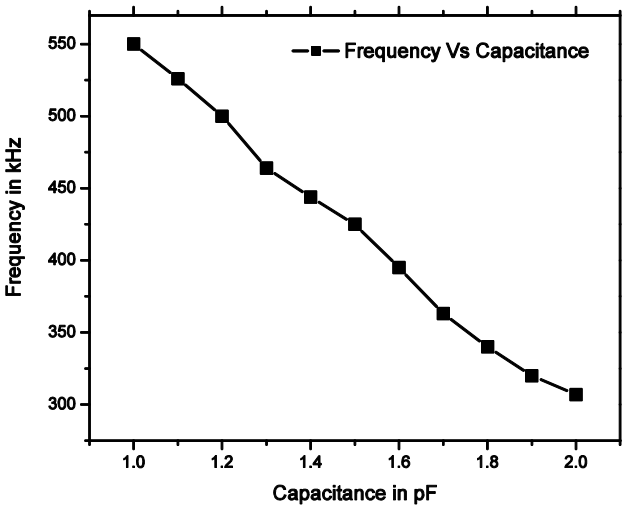

Figure-13. Relationship between the capacitance and output frequency of C-F conversion circuit.

It is observed the output frequency varies from 526 kHz to 307 kHz for 1 pF to 2 pF input capacitance. The relationship between capacitance and output frequency is almost linear, and it shows the frequency sensitivity of 35 kHz/pF. The relationship between the capacitance and output frequency of C-F conversion circuit in FPAA is depicted in Figure-13.

4.3 Simulation results of digital processing circuit

The simulation results for 2 pF capacitance shows the output frequency of 307 kHz in FPAA. The LCD is configured for six decimal digits, seven segment display to have 1 µbar resolution. The digital pulse from FPAA acts as ripple input for digital counter module. The 24 bit counter data is divided into 6 nibble data, and each nibble data is connected to corresponding BCD decoder. Figure-14 shows the simulation data of the counter and the BCD counter values of the 6-digit pressure value BCD5 = 0010, BCD4 = 0111, BCD3 = 0101, BCD2 = 0000, BCD1 = 0000, BCD0 = 0000 and its equivalent decimal display is 374.000 mbar is as depicted in Figure-14.

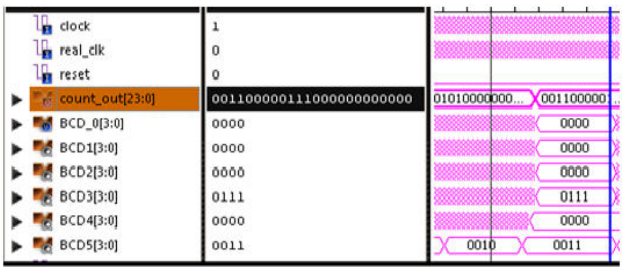

Figure-14. Simulation output of 24 bit counter and BCD decoder for 2 pF sensor capacitance.

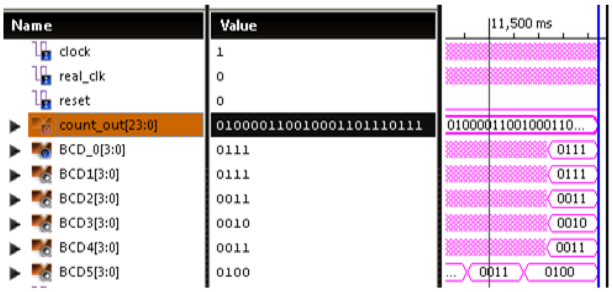

Figure-15. Simulation output of 24 bit counter and BCD decoder for 3 pF sensor capacitance.

Similarly, for 3 pF capacitance the output pulse from the FPAA is 432.369 kHz. The digital pulse from FPAA act as ripple input for digital module 24 bit counter. Figure 15 shows the simulation data of the counter and the BCD counter values of the 6-digit pressure value BCD5 = 0100, BCD4 = 0011, BCD3 = 0010, BCD2 = 0011, BCD1 = 0111, BCD0 = 0111 is as depicted in Figure-15 and its equivalent decimal display is 432.377 mbar.

The higher three decimal digit is used to show the mbar variation of the pressure, and the lower three decimal number is used to display the µbar variation as it is recognized by 1 MHz range change of frequency.

4.4ASCII Encoder and hardware for LCD module

Figure-16 depicts the RTL schematic of digital processing circuit using C-F method. BCD counter is responsible for the single decimal digit of the value of

pressure, the output of counter BCD0, BCD1, BCD2, BCD3, BCD4, BCD5 represents the (Least Significant Decimal Digit) LSD 0, LSD 1, LSD 2, LSD 3, LSD 4, LSD 5, respectively. Single bit register BCD6 is used to represent the LSD 6 of the pressure value.

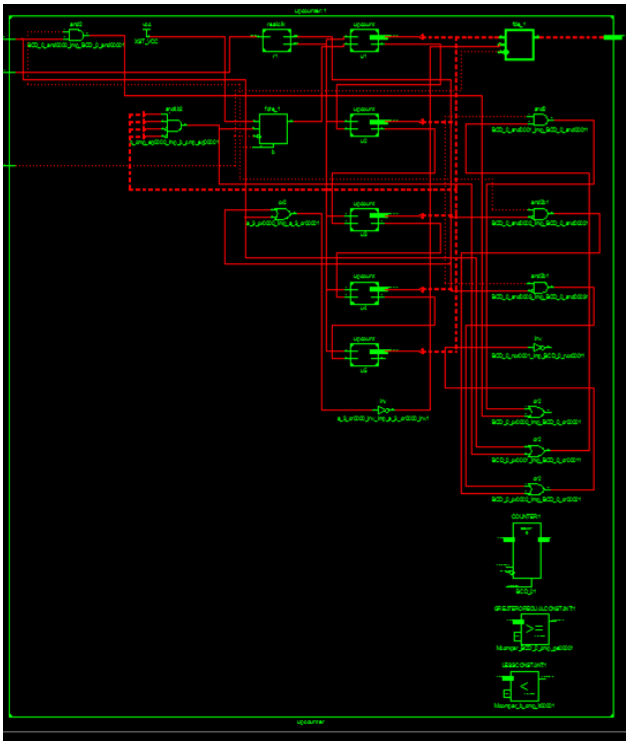

Figure-16. RTL Schematic of digital processing circuit.

LCD module is chosen to display the measured pressure. So, a separate hardware module for LCD with state machine is designed and implemented. Each 4-bit output of the BCD counters and value of register BCD 6 were converted into 8-bit ASCII code by a custom designed encoder which is sent to LCD state machine as data, after the command codes for initialization. A decimal point is placed before LSD2, which separates the µbar and millibar variation of the pressure. RTL Schematic of LCD interface circuit is shown in Figure-17.

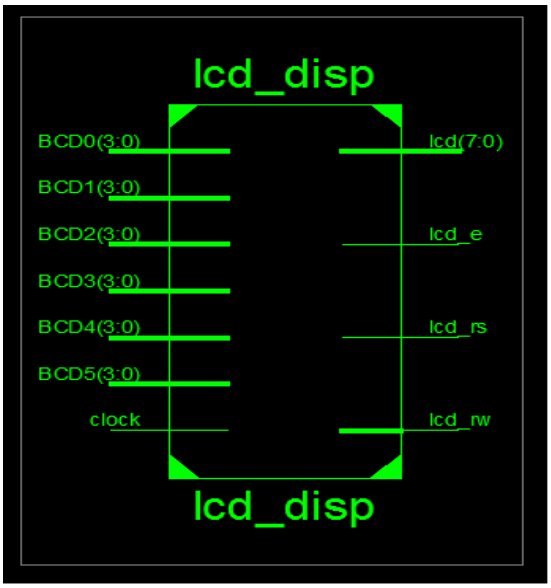

Figure-17. RTL Schematic of LCD interface circuit.

5. CONCLUSIONS

ASIC processor for the 1 µbar resolution pressure measurement and display processing circuit was designed using C-V and C-F conversion methods and implemented using FPAA and FPGA modules. Fixed value capacitor is used instead of MEMS capacitive pressure sensor in implementation. The capacitance value is varied from 1 pF to 2 pF. The dynamic variation achieved in C-V and C-F methods are 4.09 V and 219 kHz respectively. Analog and digital processing circuits are designed and implemented using FPAA and FPGA respectively. The C-F conversion technique is used for converting sensor capacitance to frequency and RTL schematic is extracted from digital processing circuit and LCD interface module. The sensitivity in C-V and C-F are 0.409 mV/pF and 21.9 kHz/pF respectively. The C-F conversion method is to be considered for designing digital module in this work over C-V conversion process, due to the resolution limitation of ADC in FPAA.

ACKNOWLEDGEMENTS

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REFERENCES

[1] Eswaran.P and Malarvizhi.S. 2012. Modeling and Analysis of High Sensitive MEMS Capacitive Differential Pressure Sensor with Polyimide Diaphragm, Advanced science Letter. 19(12): 3449 3453.

[2] Eswaran.P and Malarvizhi.S. 2012. Simulation Analysis of MEMS Based Capacitive Differential Pressure Sensor for Aircraft Application, Advanced Materials Research. 403-408: 4152-4156.

[3] Eswaran.P and Malarvizhi.S. 2012. Design Analysis of MEMS Capacitive Differential Pressure Sensor for Aircraft Altimeter. International Journal of Applied Physics and Mathematics. 2(1): 14-20.

[4] Eswaran.P and Malarvizhi.S. 2012. Sensitivity Analysis on MEMS Capacitive Differential Pressure Sensor with Bossed Diaphragm Membrane. Proceedings of International Conference on Devices, Circuits and Systems (ICDCS), Karunya University, Coimbatore, India. pp. 705-709.

[5] Eswaran.P and Malarvizhi.S. 2013. MEMS Capacitive Pressure Sensors: A Review on Recent Development and Prospective. International Journal of Engineering and Technology. 5(3): 2734-2746.

[6] Eswaran.P and Malarvizhi.S. 2015. Modeling and analysis of MEMS capacitive differential pressure sensor structure for altimeter application. International Journal of Microsystem Technologies Micro- and Nanosystems Information Storage and Processing Systems, DOI 10.1007/s00542-015-2756-4.

[7] Xiao-Dong Huang, Jian-Qiu Huang and Ming Qin. 2007. A Fully Integrated Capacitive Pressure Sensor with High Sensitivity. IEEE sensor conference. pp. 1052-1054.

[8] Tomio Nagata, Hiroaki Terabe, SirouKuwahara and Sizuki Sakurai. 1991. Digital compensated capacitive pressure sensor using CMOS technology for low pressure measurement. IEEE International conference on Solid-State Sensors and Actuators, 1991. Digest of Technical Papers, TRANSDUCERS '91, pp. 308-311.

[9] S.Vlassis and S. Siskos. 2000. A Signal Conditioning Circuit for Piezoresistive Pressure Sensors with variable Pulse-Rate Output, Analog Integrated Circuits and Signal Processing, Kluwer Academic publisher. 23, pp. 153-162.

[10] D. P. Morales, A. Garcla, A. J. Palma and A. Martinez-Olmos. 2010. Merging FPGA and FPAA reconfiguration capabilities for IEEE 1451.4 compliant smart sensor applications, IEEE Trans. Electron Device. 57: 217-220.

[11] Anadigm Designer2, Tutorial. Available online: http://www.anadigm.com/_doc/UM020800-U001.pdf.

[12] Giuseppe Merendino, Sergio Callegari, Alessandro Golfaelli, Michele Zagnoni and Marco Tartagni. 2005. Signal Conditioning for Capacitive Sensors with Field Programmable Analog Arrays. IEEE International Symposium on Signals, Circuits and Systems, 2005. ISSCS 2005, 1: 138-140.

[13] Morales. D. P., Garcia. A., Palma. A. J. 2008. Enhancing ADC resolution through Field Programmable Analog Array dynamic reconfiguration. International Conference on Field programmable Logic and Application. pp. 635-638.

[14] LdoBaccigalupi and Annalisa Liccardo. 2007. Field Programmable Analog Arrays for Conditioning Ultrasonic Sensors, IEEE Sensors Journal. 7(8): 1176-1178.

[15] Xuhai Chen and Min Du. 2012. Automatic Gain Control for Multi-channel Electrochemical Detection System Combining FPGA and FPAA. International Conference on Biomedical Engineering and Informatics (BMEI 2012). pp. 456-458.