

DESIGN OF 8-BIT COMPARATOR BASED GDI LOGIC USING FINFET TECHNOLOGY

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Abstract

This paper presents the implementation of 8-bit comparator circuit using GDI (Gate Diffusion Input) logic. And GDI Logic reduces the number of transistor count. A GDI is faster than other techniques like Domino logic and uses less area. The Low power 8-bit comparator is proposed in this paper which has an advantage of minimum power dissipation, reduced propagation delay and increase number of bits required as compared to 4-bit HSD comparator. Simulation of designs has been done using 20 nm FinFET Technology and the results show that proposed 8-bit comparator. So we have made a comparative analysis between GDI logic and Domino logic. The GDI dissipates 31.37% power which is almost 55% less than HSD comparator.

Keywords: 8-bit comparator, GDI logic, power consumption

1 INTRODUCTION

Comparator plays an important role in the performance of many circuits such as analog to digital converters, data transmission, switching power regulator, memories, dynamic logic, sensing amplifiers etc. Domino logic circuits have been the excellent choice in the design of high-performance modules in modern microprocessors. The only limitation of domino logic circuits is their relatively low noise margin compared to that of the standard static CMOS circuits. Comparators are widely used in central processing units (CPUs) and microcontrollers (MCUs). XNOR gate can be used as a basic comparator because it produces an output high only if the two inputs are equal. A digital comparator is an electronic circuit which compares two numbers in binary form and generates a one (HIGH) or zero (LOW) at its output depending on whether the bits are same or not. The digital circuits designed using domino logic styles can be considerably faster and more compact than circuits designed using conventional static CMOS technology.

GDI technique is superior to other design techniques in terms of low power and high-speed VLSI design as this technique uses a simple GDI cell consisting of only two transistors, to implement various complex logic functions. This technique improves the logic level swing. It allows propagation delay, and area of digital circuits while maintaining the low complexity of the logic design. Characteristics performances and also allows a simple design of any logic circuit using a small GDI cell. GDI technique enables simpler gates, lower transistor count, and lower power dissipation in many implementations, as compared with conventional CMOS, n-MOS Pass transistor logic, and transmission gates.

In a digital system, the magnitude comparator is a very useful and basic arithmetic component. A compact, good cost benefit, high-performance magnitude comparator plays an important role in almost all hardware sorters. One of the most important problems in computer science is sorting. Many fundamental processes in communication and computing systems require data sorting. Sorting network using comparator play a key role in the areas of parallel computing, multiprocessing, and multi-access memories. A magnitude comparator is also used in a

microprocessor for decoding instructions and data processing in Digital Signal Processors (DSP). Advancement in the next generation communication systems also requires efficient digital comparators.

Fin-type Field Effect Transistors (FinFETs) are promising substitutes for bulk CMOS circuits. The Double-Gate (DG) FinFET is of most interest because of its excellent suppression of Short-Channel Effects (SCEs) and its relatively easy fabrication and integration. Due to novel device structure, FinFET technology provides less static power consumption. The main characteristic of the FinFET is that it has a conducting channel wrapped by a thin silicon "fin" from which it gains its name. The thickness of the fin determines the effective channel length of the device. The FinFET technology provides less static power consumption and this will less subthreshold leakage and results in better performance.

2 COMPARATOR DESIGN

The comparator is a hardware electronic device that takes two numbers as input in the binary form and determines whether one number is greater than, less than or equal to the other number. XNOR Gate is a basic comparator because its output is "1" only if its two input bits are equal. We have designed the 8-bit comparator using GDI Logic.

A. GDI Logic

The GDI Logic is a new technique of low power digital combinational circuit design is described. This technique allows reducing power consumption. It allows propagation delay, and area of digital circuits while maintaining the low complexity of the logic design.

GDI Logic consisting of two transistor network N, G, and P being the three inputs. The source terminal of NMOS is acting as one input terminal and source terminal of PMOS is acting as another input terminal. The output is taken from the drain terminal of both the transistors. The supply and ground are

connected to the bulk of PMOS and NMOS respectively. Fig.1. shows the GDI Logic circuit is given below.

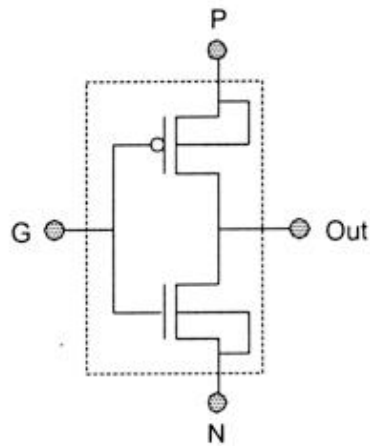


Figure 1: GDI Logic Circuit

The GDI Logic consists of four terminals. They are

- G (Common gate input of NMOS and PMOS transistor),
- P (Outer diffusion node of PMOS transistor),
- N (Outer diffusion node of NMOS transistor),
- Out (Common diffusion node of both transistors).

The PMOS will produce its output as strong logic 1 and weak logic 0. Similarly, NMOS produces its output as strong logic 0 and weak logic 1. When G is 1 then the nmos is turned ON and the N input passes to the output. Similarly when G is set as 0 then the pmos is turned ON and the P input passes as output through pmos. If NMOS is switched, the N input passes through the nmos transistor and if the input N is at logic 1 then the output is weak logic 1. Similarly, if the PMOS is turned ON then if the P input terminal is at logic 0 then the output is weak logic 0.

The GDI Logic allows implementation of a wide range of complex logic functions using only two transistors. This method is suitable for the design of fast, low power circuits, using a reduced

number transistors as compared to existing techniques that is high-speed domino.

B. Proposed 8-bit comparator

The proposed 8-bit comparator is designed in this paper and to increase the number of bits. Here power consumption is low because 4-bit comparator requires less number of bits. For 8-bit we use two 4-bit numbers, 4 EX-NOR and 4 input AND gate, OR gate.

An 8-bit comparator compares the two 8-bit numbers by cascading of two 4-bit comparators. For the lower order comparator, the A=B cascade input must be connected high, while the other two cascading inputs A, B must be connected to low. The outputs of the higher order comparator become the outputs of this 8-bit comparator.

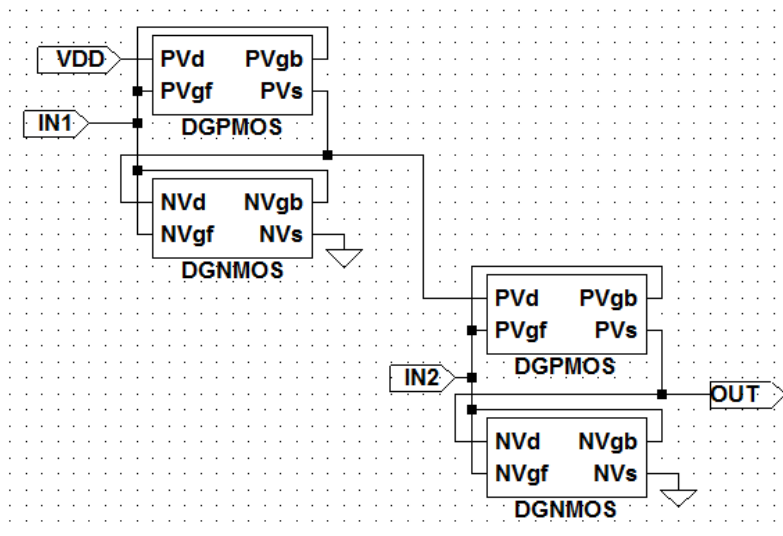


Figure 2: Circuit diagram for 8-bit comparator using FinFET Technology

The above diagram shows the 8-bit comparator circuit. Here, The Proposed 8-bit comparator is designed as per the basic gates such as AND, OR, and NOR are designed using GDI technique.

The output logic statements of this comparator are,

- If $A_3=1$ and $B_3=0$, then A is greater than B ($A>B$).
- If A_3 and B_3 are equal, and if $A_2=1$ and $B_2=0$, then $A>B$.
- If A_3 and B_3 are equal & A_2 and B_2 are equal, and if $A_1=1$ and $B_1=1$, then $A>B$.

Table 1: Truth Table for 8-bit comparator.

Inputs		Outputs		
A	B	A<B	A=B	A>B
00001100	00001100	0	1	0
00001010	00010001	1	0	0
00001111	00000101	0	0	1
00011000	00011000	0	1	0

The truth table followed by the 8-bit comparator is shown in Table I. A and B are the two 8-bit input signals to the comparator which compares the two binary inputs. The output signals are $A<B$, $A=B$, $A>B$.

3 SIMULATION AND WAVEFORM

The 8-bit comparator is designed with the new structure of GDI (Gate Diffusion Input) logic. The Proposed comparator shows reduced power consumption, delay, and area when compared to existing designs. Schematic design of 8-bit comparator is done using HSPICE tool using 20nm FinFET technology.

Consider the 8-bit comparator with eight inputs A_0, A_1, A_2, A_3 and B_0, B_1, B_2, B_3 and the output is obtained in $A<B$, $A=B$, $A>B$. Different binary inputs combinations are applied at the input of the comparator and analyzed for greater than, less than and equal to values. The average delay is generated by this 8-bit comparator is shown in Fig.4.

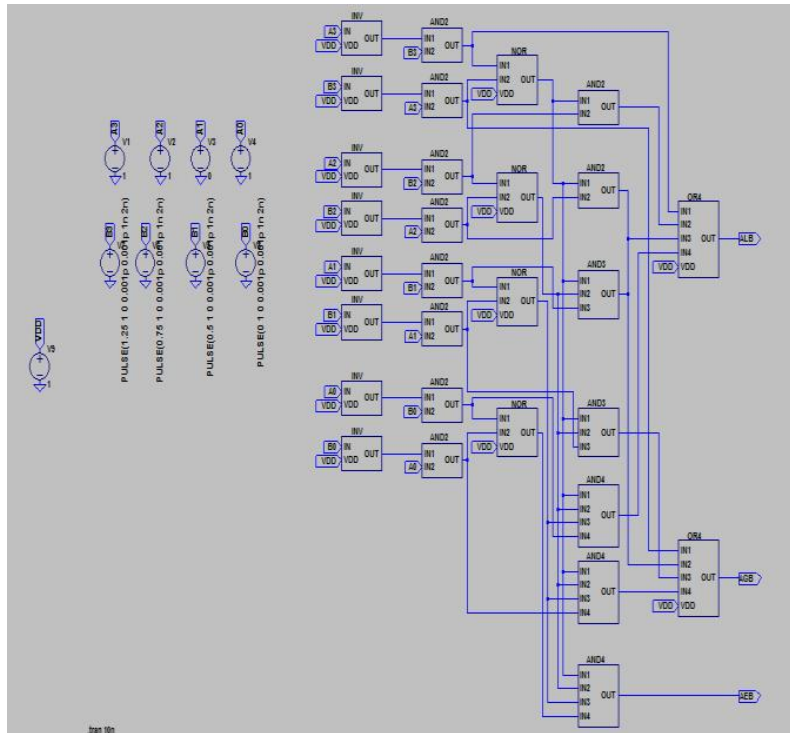


Figure 3: Schematic view of FinFET based 8-bit comparator

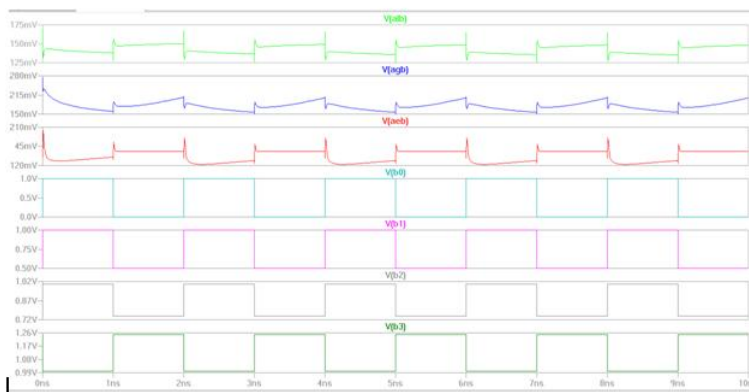


Figure 4: Proposed waveform of FinFET based 8-bit comparator

4 RESULT ANALYSIS

In this paper, we have considered several parameters which will have a use for comparative analysis between the 4-bit comparator and 8-bit comparator and those parameters are power, delay, area [6]. and here use the technology was a 20 nm FinFET Technology. The GDI based 8-bit comparator dissipates 31.37 W power which is almost 55% less than 4-bit High-Speed comparator. Also, GDI based comparator is faster than other techniques and it uses less area.

Table 2: Comparative analysis of 4-bit comparator and 8-bit comparator

Logic style	4-bit comparator			8-bit comparator		
	Power (μ W)	Delay (μ sec)	Area (μ m ²)	Power (μ W)	Delay (μ sec)	Area (μ m ²)
GDI	31.3	23.0	25.85	9.86	20.47	10.10
HSD	53.2	25.46	27.21	114.3	29.75	75.42

5 CONCLUSION

In this paper, the 8-bit comparator circuit designs that use as the higher number of bits are proposed. The comparative design and analysis of 4-bit comparator and 8-bit comparator using GDI logic. For comparison, we took power, delay, area. we conclude that 8-bit comparator based on GDI logic technique dissipates 31.37% power which is almost 55% less than 4-bit HSD (High-Speed Domino) comparator. The proposed designs are simulated using the HSPICE simulation tool at 20 nm FinFET technology. Among the presented design techniques, GDI proves to have the best analysis values and lowest transistor count. Hence, these proposed designs may be suitable for low power and delay in VLSI circuit applications. These are used in the address

decoding circuitry in computers and microprocessor based devices to select a specific input/output device for the storage of data.

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