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Design of Carry Look Ahead Adder using Ternary Logic

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ABSTRACT:*Now a days power consumption, area, cost and speed are the major parameters to design the circuit. The binary logic contains Logic level '0' (Low) and Logic level '1' (High) and the ternary logic contains Logic level '0' (Low) and Logic level '1' (High) and logic Z (High Impedance). While designing the digital circuits, Binary logic takes a 4 number of memory cells to represent a single digit of information, whereas a ternary logic takes 3 number of memory cells to represent the same single digit of information. So, by using ternary logic, we can reduce chip area and interconnects, power consumption, delay.*

In this paper, we have designed ternary logic gates like TNOT, TAND, TNAND, TOR, TNOR, TXOR and ternary adder circuits like Half Adder (THA), Full adder (TFA), Ripple Carry Adder (TRCA) and Carry Look Ahead Adder (TCLAA). In this paper, we aim to enhance the performance of ternary logic gates and ternary adders in terms of delay (Logic+Route), number of slices LUTs, number of bonded IOBs. The results are simulated by using Xilinx ISE Design Suite 14.5 software.

KEYWORDS:*Binary Logic, Ternary Carry Look Ahead Adder (TCLA), Ternary Logic***.**

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I. INTRODUCTION

Over the decades we have been using binary logic. The binary logic technology has come across many changes and advances. In this binary logic we are having two levels i.e., logic low and logic high that can be represented as logic level '0' and logic level '1'. Unlike binary logic, ternary logic requires 3 number of bits to represent a digit due to which the number of memory cell requirement is less compared to binary logic. Ternary logic also known as Multi-Valued Logic (MVL) or Non-binary logic.

The ternary logic consists of switch with more than 2 states. Such as 3-value switch with logic states '0','1' and 'Z'. Multi-level electronic systems were used in digital application to build multi-number base systems, which offer a prominent reduction in implementation, power consumption, complexity and area. The largest commercial use of Multiple-Valued logic is in the area of MVL memories. The MVL can be used to overcome the existing difficulties in binary digital systems, such as the design of fault simulators. The various application of ternary logic is used in memories, serial to parallel operations, communications and digital signal processing etc.

II. TERNARY LOGIC GATES

Ternary Inverters: Ternary inverter is a circuit that gives the output in inverted form of input. The Fig. 1 shows the symbolic representation of three states of inverters i.e., Standard Ternary Inverter (STI), Positive Ternary Inverter (PTI) and Negative Ternary Inverter (NTI).

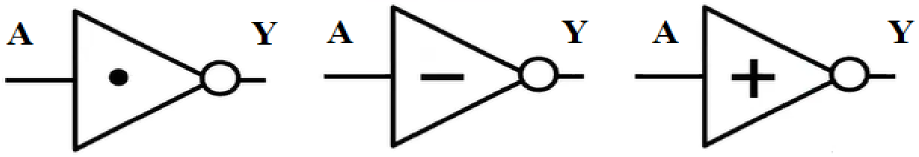


Fig. 1: Symbols of Ternary Inverters (a) STI (b) NTI (c) PTI

Table 1: Truth Table of Inverters

Input	Output		
	STI	NTI	PTI
0	Z	Z	Z
1	1	0	Z
2	0	0	0

The symbols ‘·’, ‘+’, and ‘-’ are used to represent Standard, Positive and Negative ternary inverters. The input and output of STI inverter takes three possible voltage levels which are ‘0’, ‘1’ & ‘Z’. In STI, the outputs are ‘Z’, ‘1’ & ‘0’ for the inputs ‘0’, ‘1’ & ‘Z’. The PTI and NTI outputs take only two voltage levels, which are ‘0’ & ‘Z’. In case of NTI, the outputs are ‘Z’, ‘0’ & ‘0’ for the inputs ‘0’, ‘1’ & ‘Z’. However, in PTI, the outputs are ‘Z’, ‘Z’ & ‘0’ for the inputs ‘0’, ‘1’ & ‘Z’.

Ternary AND & NAND Gates

Generally, AND gate operation is defined as Y = Min (A, B) i.e., where Y is an output and A, B are the inputs. The output expression Y of T-AND gate for the inputs A and B is given by

T-AND= Y = Min (A, B) (1)

The following Fig. 2 shows the symbol of Ternary AND gate.

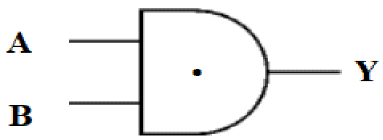


Fig.2: Symbol of STI Ternary AND Gate

Similarly, the output expression Y of T-NAND can be written as shown below i.e.,

T-NAND = T-AND = Y = $\overline{\text{Min (A, B)}}$ (2)

The following Fig. 3 shows the symbol of Ternary NAND gate.

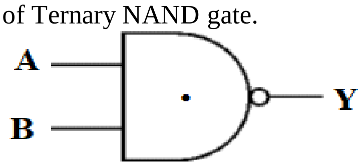


Fig. 3: Symbol of STI Ternary NAND Gate

Ternary OR & NOR Gates

Generally, OR gate operation is defined as Y = Max (A, B) i.e., where Y is an output and A, B are the inputs. The output expression Y of T-OR gate for the inputs A and B is given by

T-OR= Y = Max (A, B) (3)

The following Fig. 4 shows the symbol of Ternary OR gate.

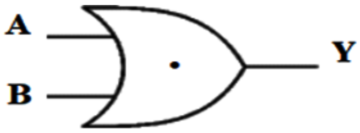


Fig. 4: Symbol of STI Ternary OR Gate

Similarly, the output expression Y of T-NOR can be written as shown below i.e.,

T-NOR = T-OR = Y = $\overline{\text{Max}}$ (A, B) (4)

The following Fig. 5 shows the symbol of Ternary NOR gate

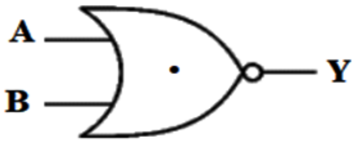


Fig. 5: Symbol of STI Ternary NOR Gate

Ternary EX-OR&EX-NOR Gates

Ternary Ex-OR is the ternary addition by neglecting carry. The expression can be written as shown below i.e.,

$$\text{T-EX-OR} = A \oplus B \qquad (5)$$

$$\text{T-EX-NOR} = \overline{\text{T-EX-OR}} = \overline{A \oplus B} \qquad (6)$$

The following Fig. 6 & Fig. 7 shows the symbols of Ternary EX-OR & EX-NOR gates.

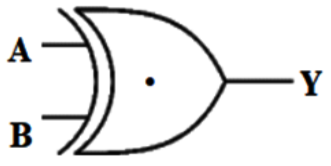


Fig. 6: Symbol of STI Ternary EX-OR Gate

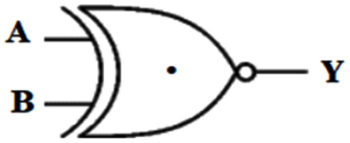


Fig. 7: Symbol of STI Ternary EX-NOR Gate

The Table 2 shows the truth table for Ternary AND, NAND, OR, NOR, EX-OR and EX-NOR Gates

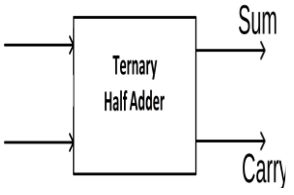
Table 2: Truth Table of Ternary AND, NAND, OR, NOR, EX-OR and EX-NOR Gates

A	B	STI-AND	STI-NAND	STI-OR	STI-NOR	STI-EX-OR	STI-EX-NOR
0	0	0	Z	0	Z	0	Z
0	1	0	Z	1	1	1	1
0	Z	0	Z	Z	0	Z	0
1	0	0	Z	1	1	1	1
1	1	1	1	1	1	Z	0
1	Z	1	1	Z	0	0	Z
Z	0	0	Z	Z	0	Z	0
Z	1	1	1	Z	0	0	1
Z	Z	Z	0	Z	0	1	Z

III. ADDERS USING TERNARY LOGIC

TERNARY HALF ADDER (THA)

Ternary half adder is a circuit for the addition of two ternary inputs. The circuit does not consider a carry generated in the previous addition. It consists of two inputs A & B and two outputs Sum & carry. The representation of THA is shown in below Fig. 8 and its truth table is shown in Table 3. The implementation of Ternary Half Adder is shown in below Fig. 9.



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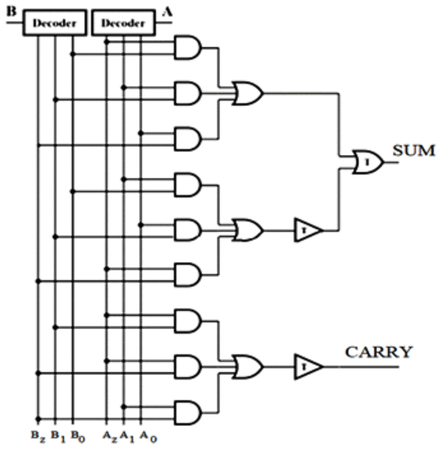

Fig. 9: The Implementation of THA

Truth Table for THA

Inputs		Outputs	
A	**B**	**Sum**	**Carry**
0	0	0	0
0	1	1	0
0	Z	Z	0
1	0	1	0
1	1	Z	0
1	Z	0	1
Z	0	Z	0
Z	1	0	1
Z	Z	1	1

From the above Truth Table, we can write the equations for Sum and Carry are

$$\text{Sum} = A_Z B_0 + A_1 B_1 A_0 B_Z + 1.(A_1 B_0 + A_0 B_1 + A_Z B_Z) \qquad (7)$$

$$\text{Carry} = 0+1.\ (A_Z B_1 + A_1 B_Z + A_Z B_Z) \qquad (8)$$

TERNARY FULLADDER (TFA)

The ternary full adder is a circuit that adds two inputs along with the previous carry generated. The ternary full adder can be generated by two ternary half adders. The ternary full adder consists of three inputs i.e., A, B and Cin, whereas coming to output it has two outputs i.e., Sum and Carry. The representation of TFA is shown in below Fig. 10 and its truth table is shown in Table 4. The implementation of Ternary Full Adder is shown in below Fig. 11.

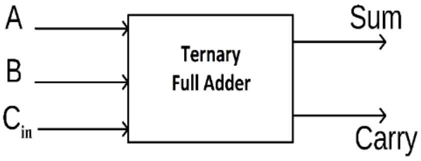

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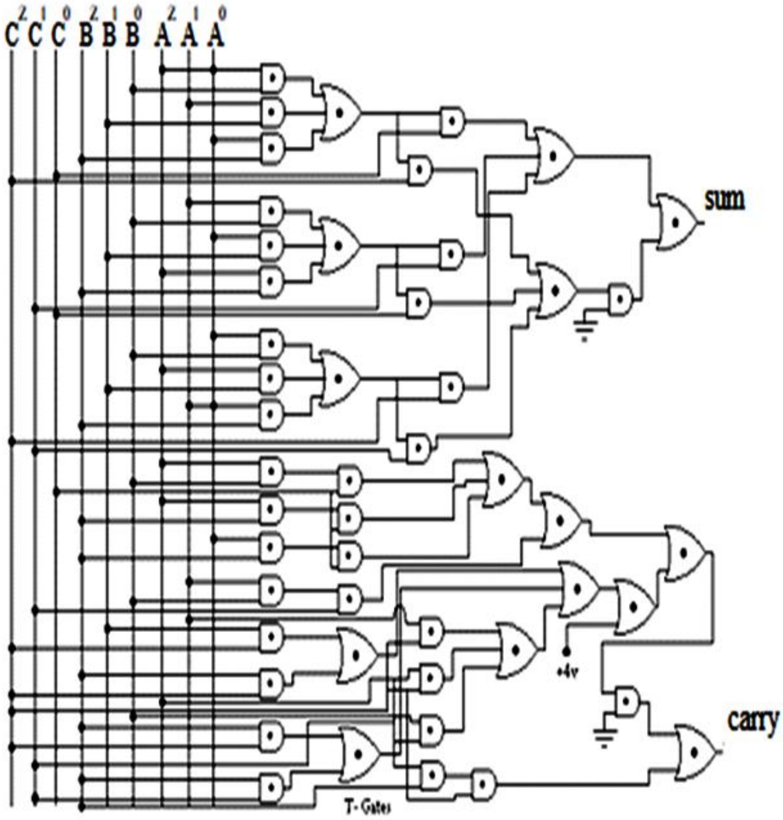
Table 4: Truth Table for TFA

Inputs			**Outputs**	
A	**B**	**C$_{in}$**	**Sum**	**Carry**
0	0	0	0	0
0	0	1	1	0
0	0	Z	Z	0
0	1	0	1	0
0	1	1	Z	0
0	1	Z	0	1
0	Z	0	Z	0
0	Z	1	0	1
0	Z	Z	1	1
1	0	0	1	0
1	0	1	Z	0
1	0	Z	0	1
1	1	0	Z	0
1	1	1	0	1
1	1	Z	1	1
1	Z	0	0	1
1	Z	1	1	1
1	Z	Z	Z	1
Z	0	0	Z	0
Z	0	1	0	1
Z	0	Z	1	1
Z	1	0	0	1
Z	1	1	1	1
Z	1	Z	Z	1
Z	Z	0	1	1
Z	Z	1	Z	1
Z	Z	Z	Z	Z



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From the above Truth Table, we can write the equations for Sum and Carry are

$$\text{Sum}=A_Z B_0 C_0 + A_1 B_0 C_1 + A_0 B_0 C_Z + A_1 B_1 C_0 + A_0 B_1 C_1 + A_Z B_1 C_Z + A_0 B_Z C_0 + A_Z B_Z C_1 + A_1 B_Z C_Z + 1.(A_1 B_0 C_0 + A_0 B_0 C_1 + A_Z B_0 C_Z + A_0 B_1 C_0 + A_Z B_1 C_1 + A_1 B_1 C_Z + A_Z B_Z C_0 + A_1 B_Z C_1 + A_0 B_Z C_Z) \quad (9)$$

$$\text{Carry}=A_Z B_Z C_Z + 1.(A_Z C_Z + A_0 B_Z + A_Z B_Z + A_1 C_Z + A_Z C_1 + B_Z C_1 + B_1 C_Z + B_Z C_Z + A_1 B_1 C_1) \quad (10)$$

TERNARY RIPPLE CARRY ADDER (TRCA)

The structure of binary and ternary ripple carry adder are same but the difference present in the applying of logic levels at the input side. In binary, Logic level ‘0’ (Low) and Logic level ‘1’ (High) are the inputs and in ternary the Logic level ‘0’ (Low), Logic level ‘1’ (High) and Logic ‘Z’ (High-Impedance) are the inputs.

The ternary ripple carry adder is shown in Fig. 12 is a combinational logic circuit in which the carry output of first stage full adder is given as the carry input of the second stage full adder. Similarly, the second stage full adder carry output is given as the carry input of the succeeding full adder stage and so on. In this ripple carry adder, the sum and carry outputs of particular stage is generated only when the carry output of previous stage is given as the carry input to that stage, which means one stage has to wait for the previous stage carry to compute its outputs. So, in this adder, a carry is propagated from one stage to another stage due to which the delay has been increased from stage to stage. To add two n- bit ternary numbers, it needs n full adder stages. So as thenumber of bits increases, the number of full adder stages also increases and the propagation delay increases depends on the number of stages.

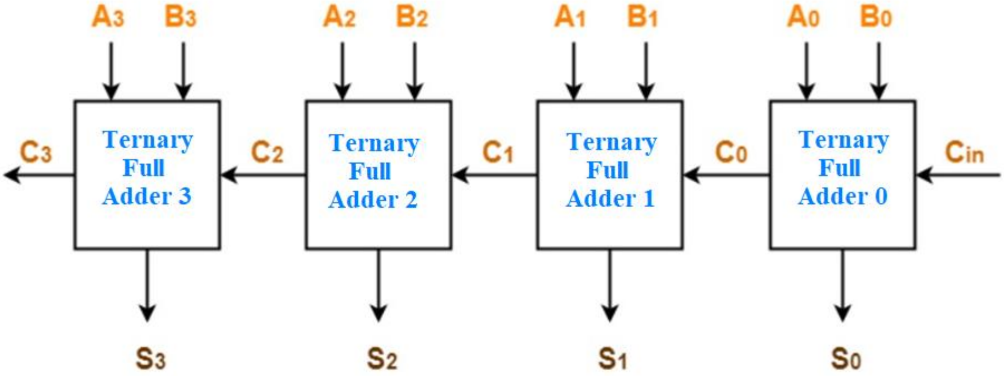

Fig. 12: Ternary Ripple Carry Adder (TRCA)

TERNARY CARRY LOOK AHEAD ADDER (TCLAA)

The ternary carry look ahead adder is an improvised version of ternary ripple carry adder. A ternary carry look ahead adder is an electronic adder that is used for ternary addition. It generates the carry output of each stage simultaneously without waiting for the carry output of previous stage due to which none of the stages has to wait for the previous stage carry to compute its outputs. So, there is a less propagation delay in TCLAA compared to TRCA. The quick additions have been performed so that it is also known as ternary fast adder.

Ternary Carry look Ahead Adder consists of Partial Full Adder, Propagation and generation Carry block. It avoids Carry propagation through each adder. It uses the concepts of generating and propagating carries.

The 4-bit ternary carry look ahead adder is shown in Fig. 13. It consists of 4-bit inputs that are A0-A3, B0-B3 & C0-C3 with S0-S3 and C4 are the outputs. In this adder, when A = B = '1', it generates the carry output of that stage is equal to '1' irrespective of the carry coming from the previous stage may be either '0' or '1' and when A = 0/1, B = 1/0, it generates the carry output of that stage is equal to '1' when a carry '1' is propagated from the previous stage.

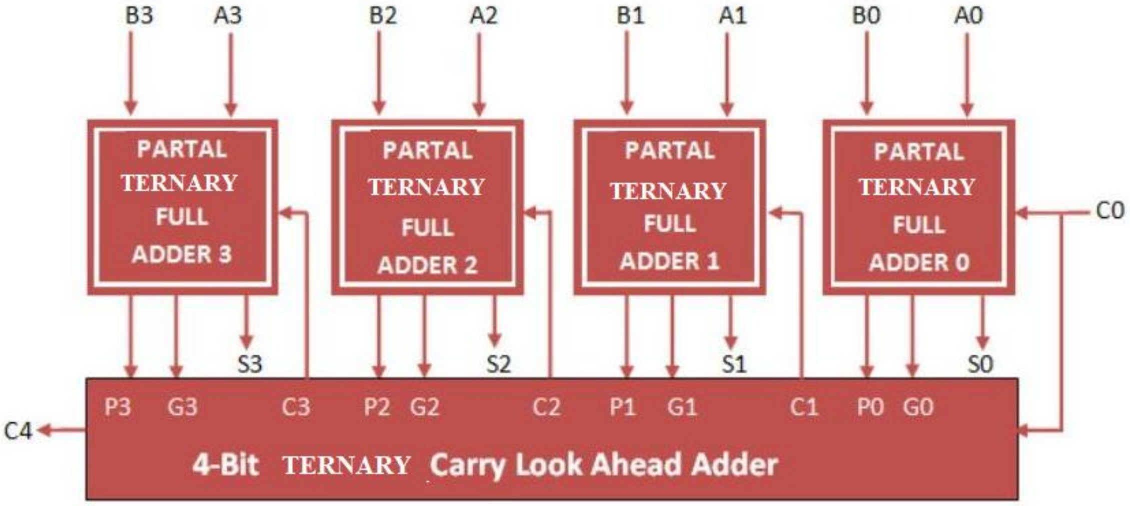
B3
A3
B2
A2
B1
A1
B0
A0
PARTAL TERNARY FULL ADDER 3
PARTAL TERNARY FULL ADDER 2
PARTAL TERNARY FULL ADDER 1
PARTAL TERNARY FULL ADDER 0
C0
S3
S2
S1
S0
P3
G3
C3
P2
G2
C2
P1
G1
C1
P0
G0
C4
4-Bit TERNARY Carry Look Ahead Adder

Fig. 13: Ternary Carry Look Ahead Adder (TCLAA)

IV. SIMULATION RESULTS

TERNARY LOGIC GATES:

TNOT Gate

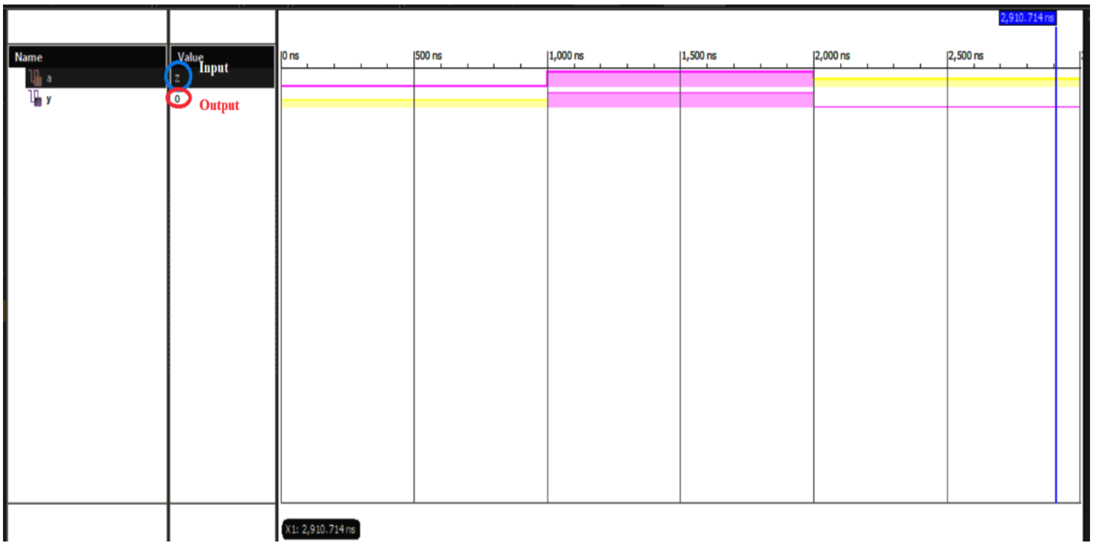

Fig. 14: Simulation Result of TNOT Gate

TAND Gate

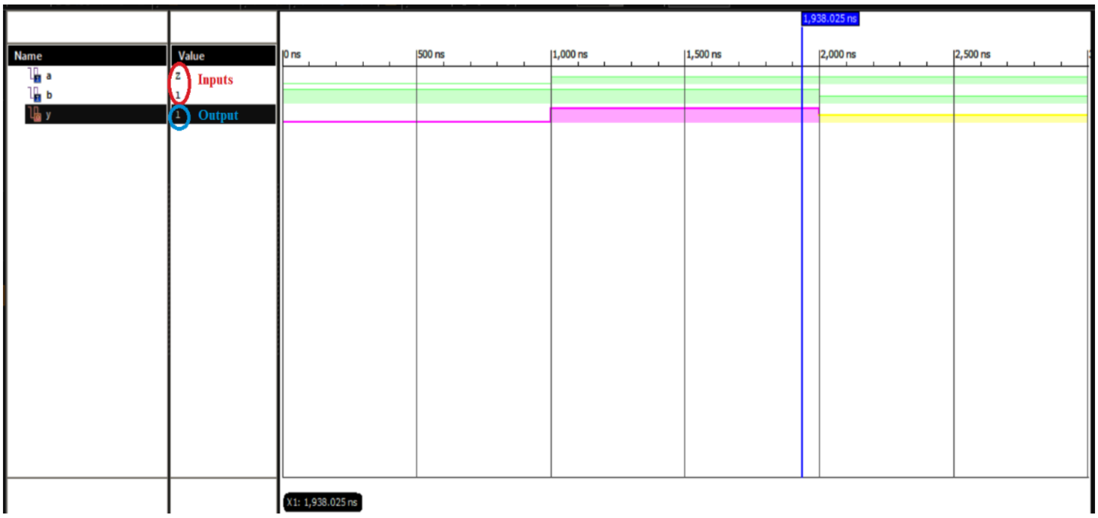

Fig. 15: Simulation Result of TAND Gate

TOR Gate

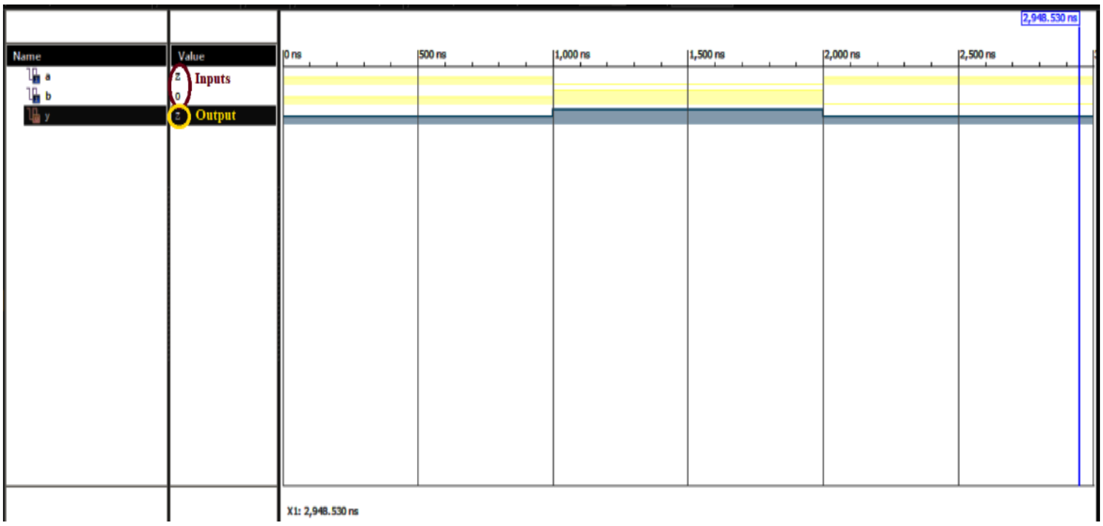

Fig. 16: Simulation Result of TOR Gate

TNAND Gate

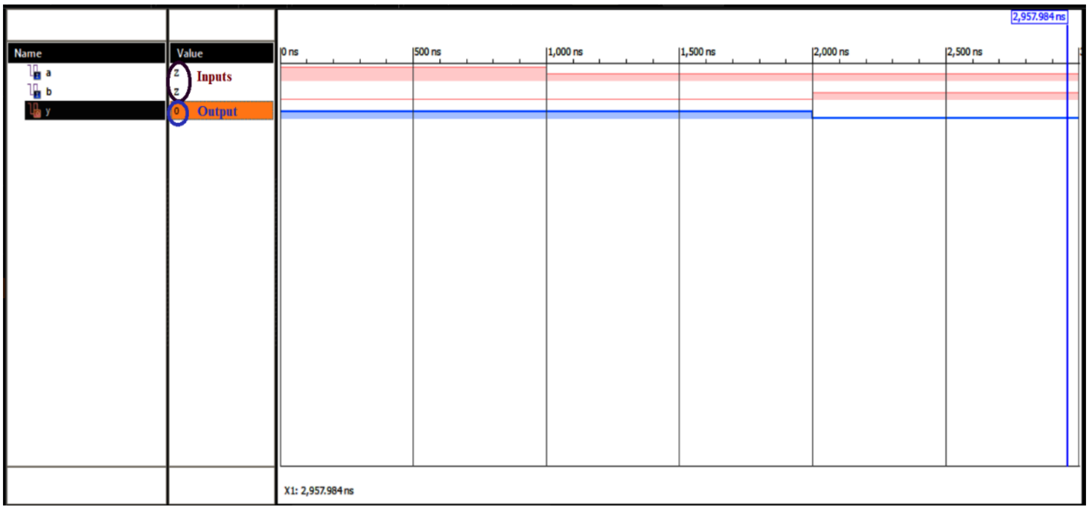

Fig. 17: Simulation Result of TNAND Gate

TNOR Gate

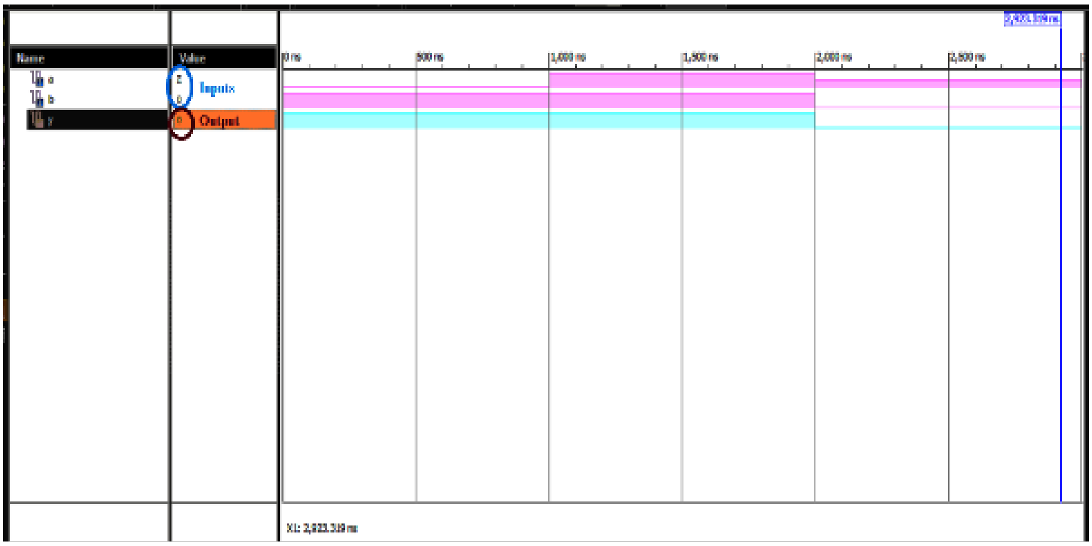

Fig. 18: Simulation Result of TNOR gate

TXOR Gate

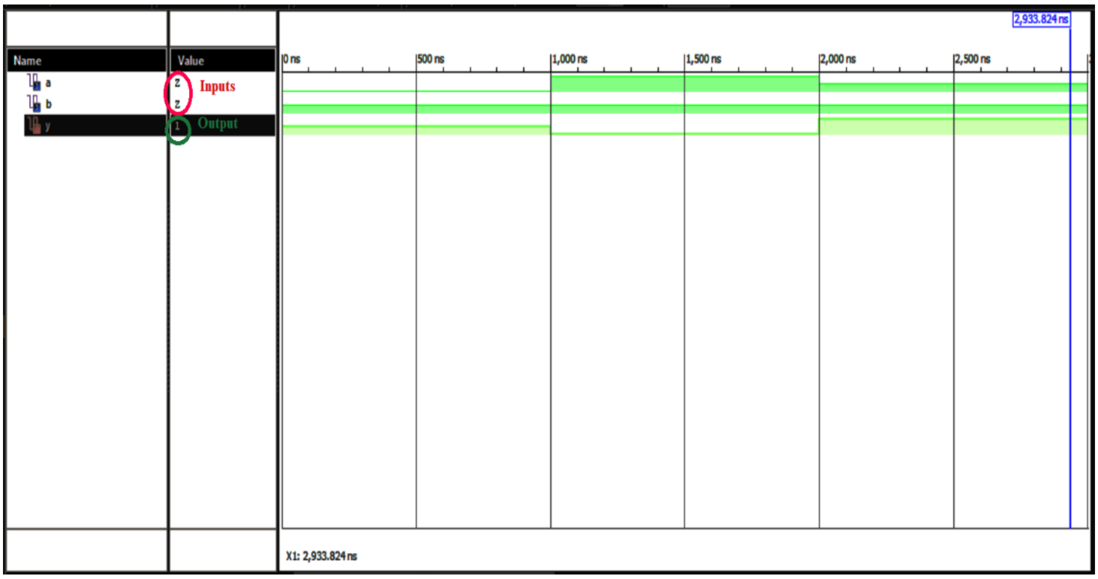

Fig. 19: Simulation Result of TXOR gate

TERNARY ADDERS:

TERNARY HALF ADDER

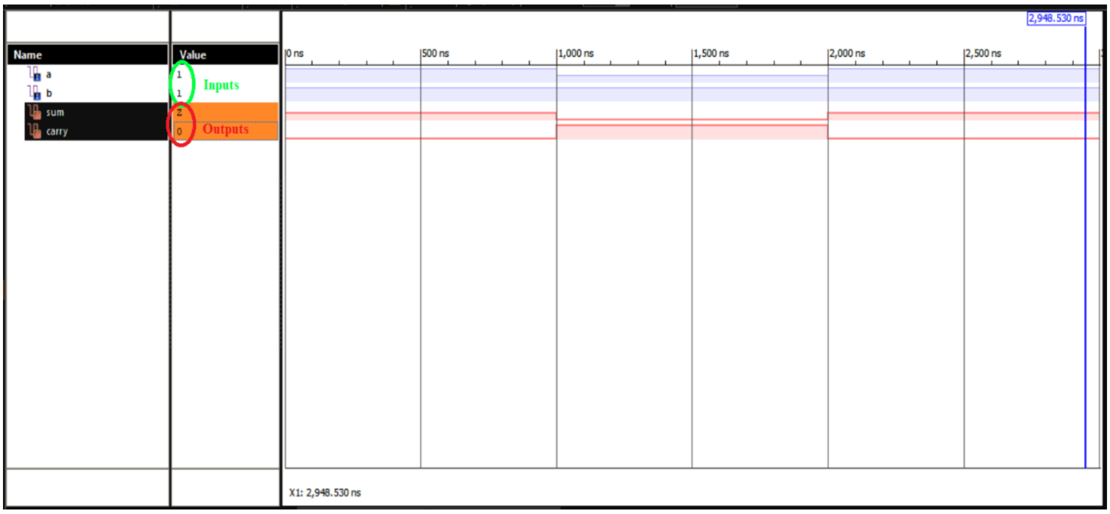

Fig. 20: Simulation Result of Ternary Half Adder

TERNARY FULL ADDER

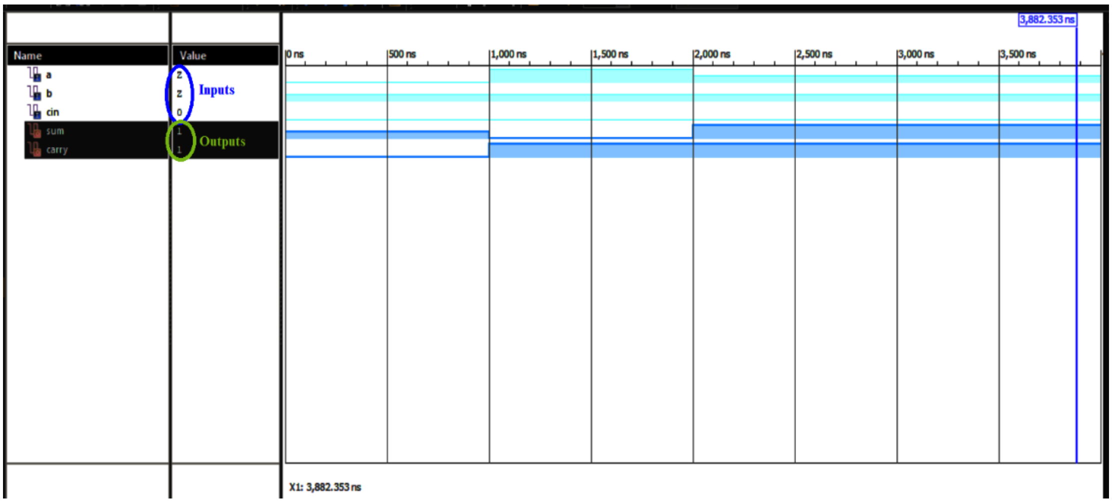

Fig. 21: Simulation Result of Ternary Full Adder

TERNARY RIPPLE CARRY ADDER

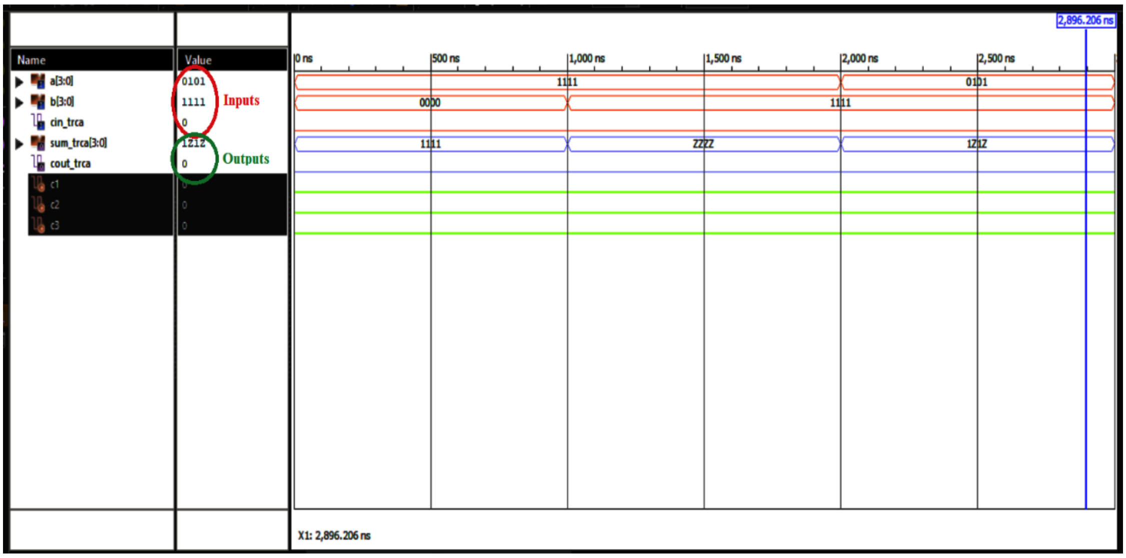

Fig. 22: Simulation Result of Ternary Ripple Carry Adder

TERNARY PARTIAL FULL ADDER

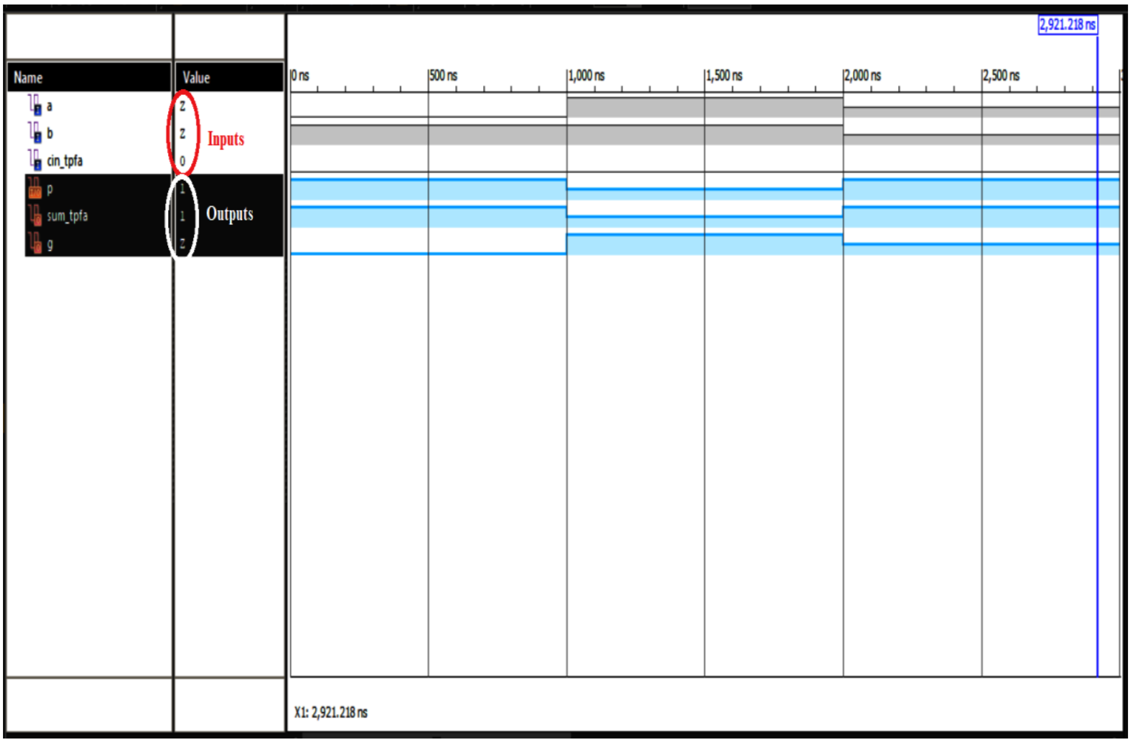

Fig. 23: Simulation Result of Ternary Partial Full Adder

TERNARY CARRY LOOK AHEAD ADDER

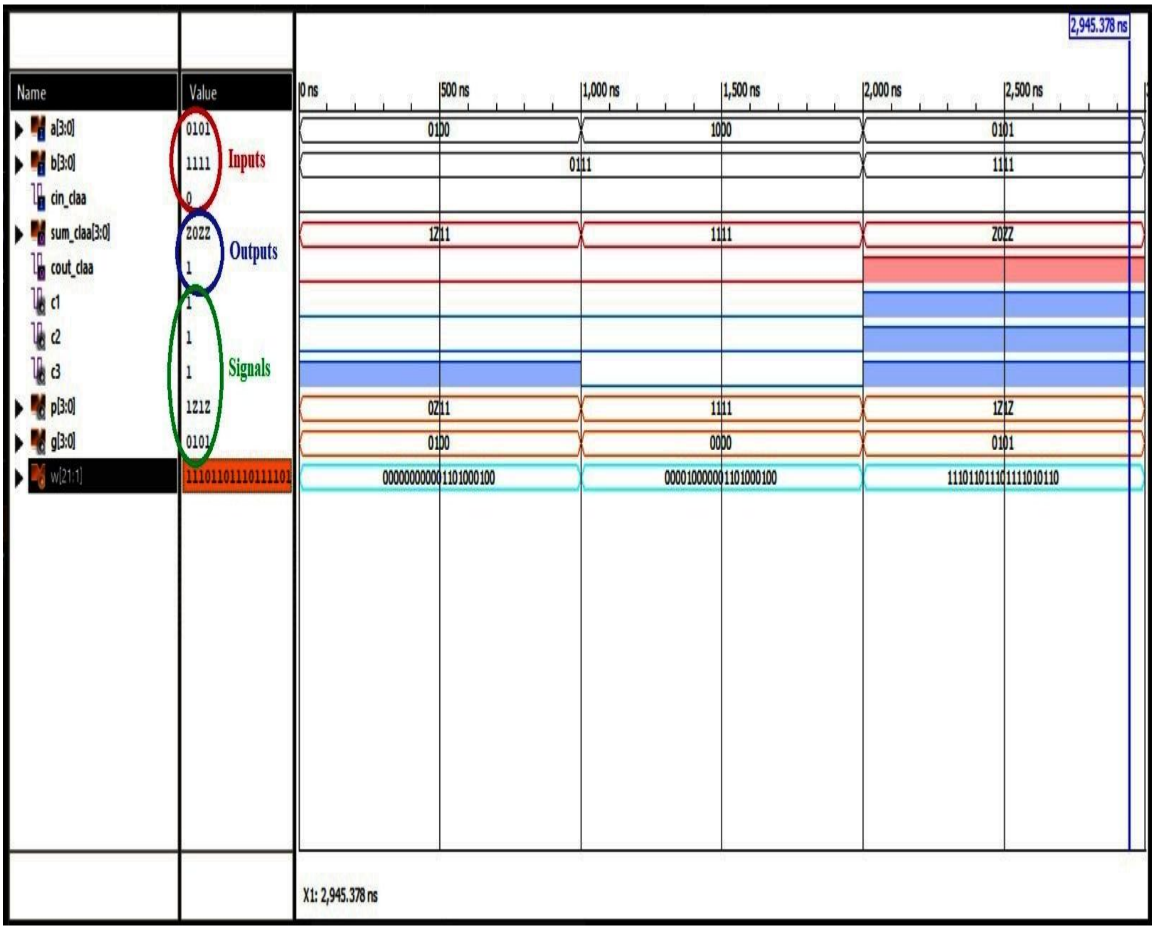

Fig. 24: Simulation Result of Ternary Carry Look Ahead Adder

Table 5: Parameters Comparison of Different Adders using Ternary Logic

Ternary Adder Design	Delay (Logic + Route)	No. of Slices	No. of Slice LUTs	No. of bonded IOBs
Half Adder (THA)	6.320 ns	2	3	4
Full Adder (TFA)	6.422ns	3	5	5
Ripple Carry Adder (TRCA)	10.538 ns	12	20	14
Carry Look Ahead Adder (TCLAA)	6.610 ns	62	58	14

CONCLUSION& FUTURE SCOPE

Finally, the functionality of ternary logic gates like TNOT, TAND, TNAND, TOR, TNOR, TXOR and ternary adder circuits like Ternary Hall Adder (THA), Ternary Full Adder (TFA), Ternary Ripple Carry Adder (TRCA) and Ternary Carry Look Ahead Adder (TCLAA) are verified & simulated by using Xilinx ISE Design Suit 14.5 software.Adders have been designed and obtained the parameters of No. of Slices, No. of Slice LUTs, No. of bonded IOBs and the Delay (Logic + Route) to ensure the Speed of the adders. So, by using ternary logic, we can reduce chip area, interconnectsand delay compared to binary logic.

In future, if we can make use of ternary logic for implementing all combinational circuits instead of binary logic then we can achieve better performance with increase in speed.

REFERENCES

[1]. Nancy S. Soliman, Mohammed E. Fouda, Lobna A. Said, Ahmed H. Madian and Ahmed G. Radwan, "N-digits Ternary Carry Lookahead Adder Design" 2019 IEEE International Conference on Microelectronics (ICM).

[2]. Chetan Vudadha and M.B.Srinivas, "Design Methodologies for Ternary Logic Circuits", 2018 IEEE International Symposium on Multiple-Valued Logic.

[3]. Sunmean Kim, Sung-Yun Lee, Sunghye Park, Kyung Rok Kim and Seokhyeong Kang, “A Logic Synthesis Methodology for Low-Power Ternary Logic Circuits”, 2020 IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS.

[4]. An eBook on “Ternary Digital System: Concepts and Applications”-http://www.esciencemedicine.com/ebooks by A P DHANDE, V T INGOLE, V R GHIYE

[5]. A.P.Dhande , R.C.Jaiswal and S.S.Dudam, “Ternary Logic Simulator Using VHDL”, SETIT 2007 4th International Conference: Sciences of Electronic, Technologies of Information and Telecommunications March 25-29, 2007 – TUNISIA.