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Design of High Speed 32 Bit Multiplier Architecture Using Vedic Mathematics and Compressors

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Abstract: ***Multiplier unit is the key block of digital signal processors as well as general purpose processors that substantially decide the speed of processor. Design of high speed multiplier is need of the day. This paper introduces a high speed multiplier architecture using Vedic mathematics Urdhwa-Tiryakbhyam sutra, however speed of multiplier greatly depends upon the addition of partial products. To further increase the speed of multiplier a novel approach of 4:2 and 7:2 compressors has been used, these compressors are very efficient in terms of speed of addition and require lower gate count. Vedic mathematics, compressors and reconfigurable multiplication architecture has been used to implement high speed 32 bit multiplier. The delay of 32 bit proposed multiplier is 44.249 ns. Upon comparison, the proposed multiplier is 1.5 times faster than existing Vedic multiplier and almost 2 times faster than conventional and booth multiplier. The architecture has been implemented using Verilog language and the tool used for simulation is Xilinx ISE 14.5.***

Keywords: VLSI, FPGA, Compressors, Vedic Mathematics.

1. Introduction

Enhancing the speed of multiplication is indispensable for current high performance digital signal processors and general purpose processors. High speed multiplication is becoming one of the key operations in signal processing and RISCs. Several multiplier architectures have been introduced over the past few decades such as booth's multiplier [7] and conventional multiplier and these multiplier are very popular in modern VLSI design. These algorithm have very time consuming processes such as addition, shifting and subtraction which requires a large number of steps before arriving the final answer also these steps reduce the speed exponentially with growing number of bits in multiplicand and multiplier. This demands a very efficient architecture of multiplier.

A novel multiplier architecture based on Vedic mathematics has been explored to address the disadvantages associated with existing multiplier architecture. Vedic mathematics is ancient system of mathematics that was reintroduced by Bharati Krishna Tirthaji Maharaj [3]. He was the scholar of Sanskrit, mathematics and philosophy. Bharati Krishna Tirthji Maharaj simplified various complex mathematical problems in 16 Sutras and 13 sub sutras which deals with trigonometry, algebra, Geometry and has various applications in signal processing, control engineering and VLSI. One of the primacy of Urdhwa Tiryakbhyam sutra is that all the partial products are obtained simultaneously which efficiently increase the speed of multiplication. As addition of Partial products consumes most of the time in multiplication, 4:2 and 7:2 compressors [1] have been introduced in this paper. Compressors are nothing but a coherent architecture for addition of more than 3 bits simultaneously. The novel compressor architecture introduced in this paper requires a few gates as compared to full adder based compressor. First 8 bit and 16 bit multiplier have been implemented using Urdhwa Triyakbhyam sutra [7] and compressors. To further design high speed multiplier architecture reconfigurable multiplier technique has been used.

2. Vedic Mathematics

Vedic mathematics is the part of Sthapatya Veda which is an up Veda of Atharwa Veda [14]. Bharati Krishna Tirthji maharaj (1884-1960) thoroughly studied Vedas and introduced Vedic mathematics in 16 sutras and 13 up sutras which covers every area of mathematics. To be precise Vedic mathematics is the composition of very simplified methods to solve various complex mathematical problems. Vedic mathematics is not magic but a logical way to look into mathematics and all sutras in Vedic mathematics are purely logical. All sixteen sutras are given below-

1. Ekadhikena Purvena
2. Nikhilam navatascaramam Dasatah
3. Urdhva - tiryagbhyam
4. Paravartya Yojayet
5. Sunyam Samya Samuccaye
6. Anurupye - Sunyamanyat
7. Sankalana - Vyavakalanabhyam
8. Puranapuranabhyam
9. Calana - Kalanabhyam
10. Ekanyunena Purvena
11. Anurupyena
12. Adyamadyenantya - mantyena
13. Yavadunam Tavadunikrtya Varganca Yojayet
14. Antyayor Dasakepi
15. Antyayoreva
16. Gunita Samuccayah.

2.1 Urdhwa Tiryakbhyam Sutra

Urdhwa Triyakbhyam Sutra is one of the sutras of Vedic mathematics and provides a very simple way to multiply two decimal numbers. Same technique has been used to multiply two binary numbers so that algorithm can be implemented in a digital systems [14]. The algorithm works very efficiently in multiplying two binary numbers as well. Urdhwa Tiryakbhyam is the Sanskrit word which means vertical and crosswise respectively. As all the partial products calculated in parallel and require only AND GATE so the multiplier based on this method is independent of processor frequency. Figure 1 explains the multiplication of two 8 bit binary numbers using Urdhwa Tiryakbhyam Sutra.

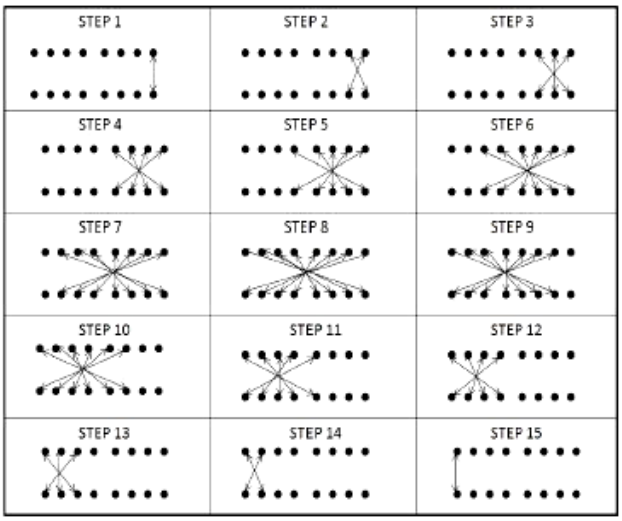

Figure 1: Pictorial representation of Urdhwa Tiryakbhyam sutra for 2 8-bit binary multiplication [1]

Figure 1 shows the algorithm to multiply two 8 bit binary numbers using Urdhwa Tiryakbhyam Sutra. Each arrow in fig 1 represents one partial product thus 64 partial products will be required for two 8 bit binary multiplication. In fig 1 left most point is LSB and right most point is MSB.

3. Compressor Architecture

Compressor is the digital architecture for addition of more than 3 bits simultaneously. Various Compressor architecture 3:2, 4:2, 5:2 and 7:2 are available, due to its property to reduce larger number of bits into smaller one this architecture is called compressor. In this paper a novel approach to make 4:2 and 7:2 compressor has been used and compared with full adder based compressor.

3.1 4:2 Compressor

4:2 compressor consist of 5 inputs one is carry and 4 input bits and gives three output bits [2]. A general block diagram of 4:2 compressor has been shown in fig 2.Various approaches have been proposed to improve the speed of compressor.

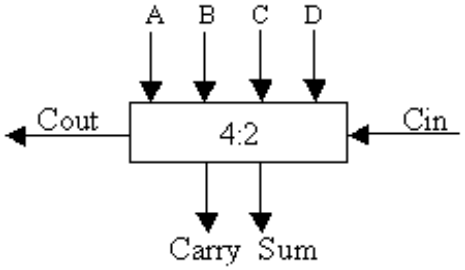

Figure 2: Block representation of 4:2 compressor

An optimized 4:2 compressor architecture has been proposed in this paper to reduce the critical path of compressor. The optimized logic diagram of 4:2 compressor has been shown in fig 3, upon comparison of proposed compressor architecture with full adder based 4:2 compressor that has been shown in fig 4 it can be seen that the propagation delay of proposed multiplier is low.

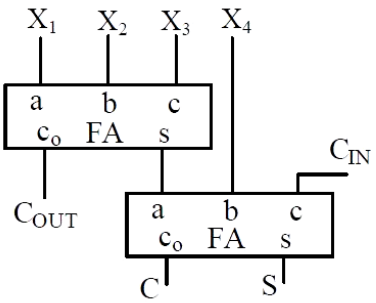

Figure 3: Full adder based 4:2 compressor

Full adder based compressor has large number of XOR GATE and each XOR gate needs 7 transistor to implement it furthermore this increases power consumption of design comparing this to proposed compressor where full adder has been implemented using MUX and XOR and complementary pass transistor logic (CPL) further reduce the delay and power consumption.

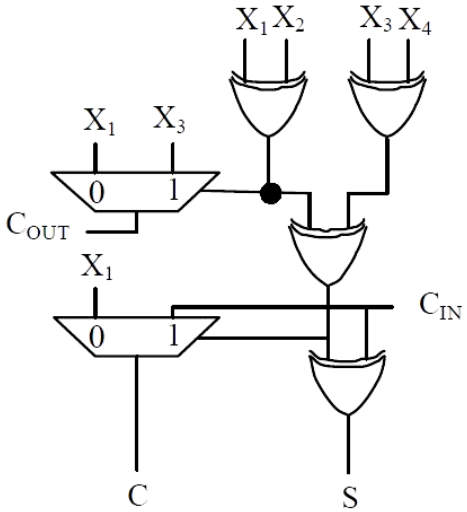

Figure 4: Optimized 4:2 compressor architecture [2]

3.2 7:2 Compressor

Similar to 4:2 compressor 7:2 compressor is able to add 9 bits (2 carry bits from previous stage and 7 input bits) simultaneously. 7:2 compressor has been implemented using

two 4:2 compressor, two full adder and one half adder and the architecture of same has been shown in fig 5 [1].

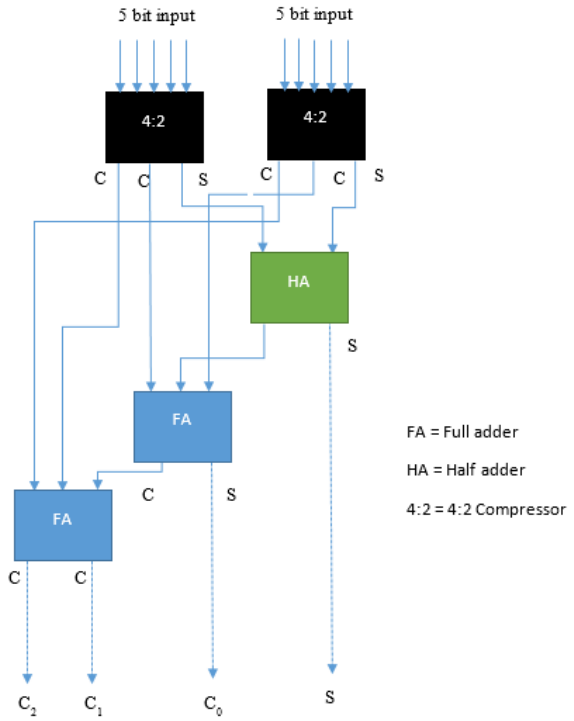

Figure 5: 7:2 compressor using 4:2 compressor, half adder and full adder [1]

7:2 compressor has also been coded in Verilog and tested in Xilinx ISE design suit 14.5. It has been seen that the proposed 7:2 compressor is 1.05 times faster than the conventional 7:2 compressor.

4. Proposed Methodology

In this paper 8 bit high speed multiplier architecture has been implemented using Vedic mathematics (Urdhwa Tiryakbhyam Sutra), proposed 4:2 and 7:2 compressors have been introduced for the addition of partial products, this approach significantly increase the speed of Vedic multiplier. Significance of 4:2 and 7:2 compressors has already been shown in previous section.

Further high speed 32 bit multiplier is designed using Urdhwa Tiryakbhyam, compressors and reconfigurable multiplication method.

4.1 8 Bit and 16 Bit Multiplier Architecture

8 bit multiplier architecture is implemented by Urdhwa Tiryakbhyam sutra. Now Let us consider two 8 bit multiplier and multiplicand X_7-X_0 and Y_7-Y_0 has to be multiplied this can be achieved by Urdhwa Tiryakbhyam method discussed in section 3. The following equation shows the procedure to generate all partial products. After that all partial product has been added using proposed compressors, full adder and half adder.

$$P_0 = X_0Y_0 \quad (1)$$
$$P_1 = X_0Y_1+X_1Y_0+C_1 \quad (2)$$
$$P_2 = X_2Y_0+X_0Y_2+ X_1Y_1+C_2 \quad (3)$$
$$P_3 = X_3Y_0+ X_0Y_3+ X_2Y_1+ X_1Y_2+C_3+ C_4 \quad (4)$$
$$P_4 = X_4Y_0+ X_0Y_4+ X_3Y_1+ X_1Y_3+ X_2Y_2+C_5+C_6 \quad (5)$$
$$P_5 = X_5Y_0+ X_0Y_5+ X_4Y_1+ X_1Y_4+X_3Y_2+ X_2Y_3 +C_7+ C_8+ C_9 \quad (6)$$
$$P_6 = X_6Y_0+ X_0Y_6+ X_5Y_1+ X_1Y_5+ X_4Y_2+ X_2Y_4+ X_3Y_3+C_{10}+C_{11}+ C_{12} \quad (7)$$
$$P_7 = X_7Y_0+ X_0Y_7+ X_6Y_1+ X_1Y_6+ X_5Y_2+ X_2Y_5+ X_3Y_4+X_4Y_3+C_{13}+C_{14}+C_{15}+C_{16} \quad (8)$$
$$P_8 = X_7Y_1+ X_1Y_7+ X_6Y_2+ X_2Y_6+ X_5Y_3+ X_3Y_5+ X_4Y_4+C_{17}+C_{18}+C_{19}+C_{20} \quad (9)$$
$$P_9 = X_7Y_2+ X_2Y_7+ X_6Y_3+ X_3Y_6+ X_4Y_5+ X_5Y_4+C_{21}+C_{22}+C_{23}+C_{24} \quad (10)$$
$$P_{10} = X_7Y_3+ X_3Y_7+ X_6Y_4+ X_4Y_6+ X_5Y_5+ C_{25} + C_{26}+ C_{27}+ C_{28} \quad (11)$$
$$P_{11} = X_7Y_4+ X_4Y_7+ X_6Y_5+ X_5Y_6+ C_{29}+ C_{30}+ C_{31} \quad (12)$$
$$P_{12} = X_7Y_5+ X_5Y_7+ X_6Y_6+ C_{32}+ C_{33}+ C_{34} \quad (13)$$
$$P_{13} = X_7Y_6+ X_6Y_7+ C_{35}+ C_{36} \quad (14)$$
$$P_{14} = X_7Y_7+ C_{37}+ C_{38} \quad (15)$$
$$P_{15} = X_7Y_7 \quad (16)$$

Equations (1) to (16) denote all the vertical and crosswise partial products and their addition according to Urdhwa Tiryakbhyam C_1 to C_{38} are carries. P_{15}-P_0 denote 16 bit output where P_0 is LSB and P_{15} is MSB.

16 bit high speed multiplier has also been implemented using Urdhwa Tiryakbhyam Sutra and using above mentioned equations. Compressors and look ahead carry adder has been used to add all partial products. A significant improvement has been observed in 16 bit multiplier as compared to conventional multiplier. Both 8 bit and 16 bit multiplier has been coded in Verilog language and synthesized in Xilinx ISE 14.5.

4.2 32-Bit High Speed Multiplier Architecture

However a different approach of multiplication with use of reconfigurable multiplier [13] in combination with Urdhwa Tiryakbhyam and compressors has been used to design a very efficient architecture for 32 bit multiplication.

To implement 32 bit multiplier A and B defined as the 2n-bits wide multiplicand and multiplier, respectively. A_H, B_H are their respective n most significant bits whereas A_L, B_L are their respective n least significant bits. A_L*B_L, A_H*B_L, A_L*B_H, A_H*B_H is the crosswise products. The product of A and B can be expressed as follows:

$$\text{PRODUCT (32 BIT)} = (A_H*B_H)\,2^{2n} + (A_H*B_L + A_L*B_H)\,2^n + A_L*B_L \text{ [13]}$$

Fig 6 describes the methodology used to implement 32 bit multiplier that is very efficient in terms of its speed. All the 16 bit and 8 bit multiplication have been implemented using Vedic Mathematics Urdhwa Tiryakbhyam Sutra. Final product of 32 bit multiplier has been calculated using above mentioned reconfigurable multiplier formulae.

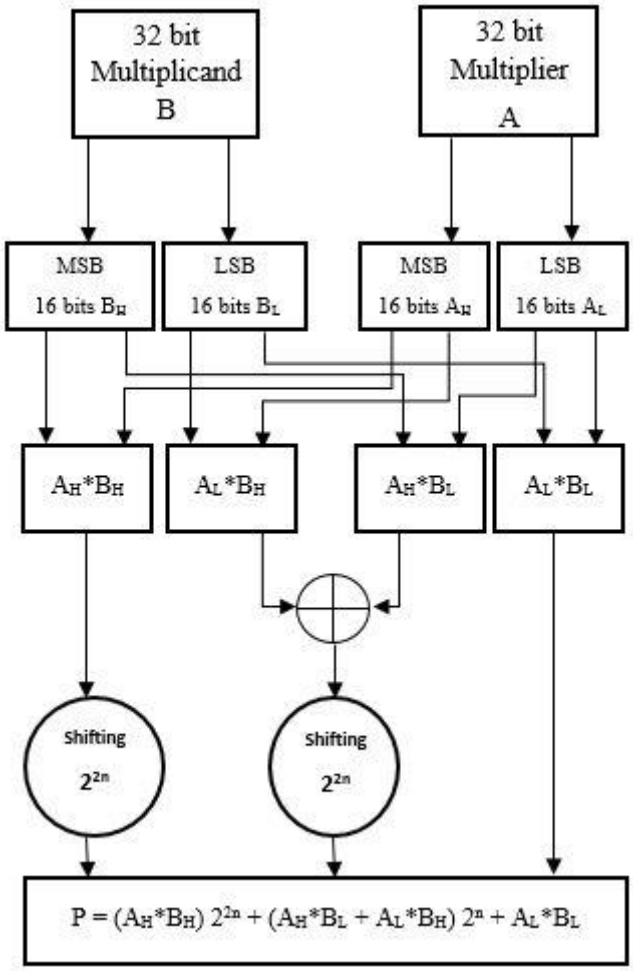

Figure 6: 32 bit proposed multiplier architecture

32 bit multiplier is coded in Verilog HDL (Hardware Description Language). Logic synthesis and simulation was done using EDA (Electronic Design Automation) tool in XilinxISE14.5 - Project Navigator and ISim simulator integrated in the Xilinx package. Spartan6 device XC6SLX16 has been used for synthesis in Xilinx.

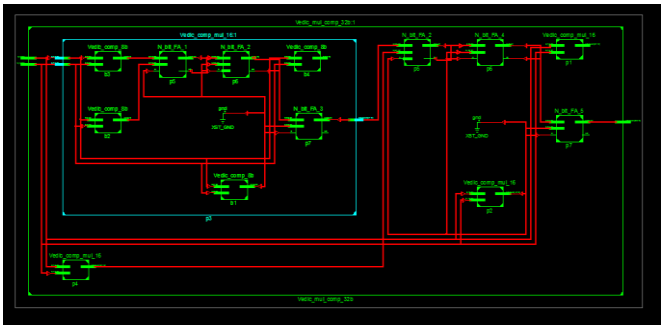

Figure 7: RTL of proposed 32 bit multiplier

upon comparison with various available multiplier proposed multiplier is best in speed. RTL and Simulation results have been shown in fig 7 and fig 8. Below simulation results have been shown.

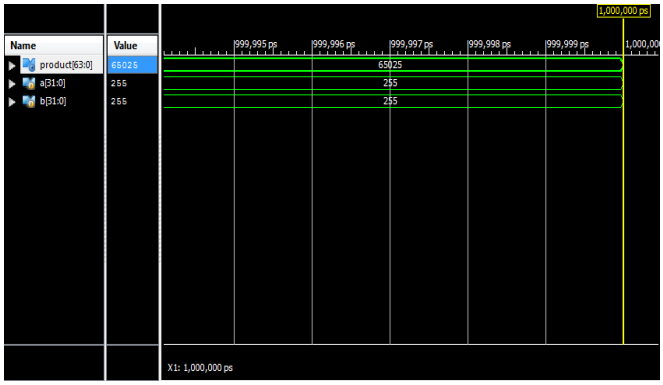

Figure 8: Simulation Result of proposed 32 bit multiplier

5. Results

The proposed 32 bit multiplier is coded in Verilog language, Simulated and synthesized using Xilinx XST for Spartan 6 xc6slx16-3csg324. Outputs are generated and verified for various possible inputs using Xilinx test bench.

Various popular multiplier such Vedic Multiplier, booth Multiplier and Conventional multiplier has also been implemented in Verilog HDL and compared with proposed 32 bit multiplier in terms of logic delay and route delay. A significant performance has been seen in proposed multiplier. All the results are tabulated in Table 1

Table 1: Comparison of Various Multiplier Architecture

Architecture	*Proposed 32 multiplier*	*Vedic Multiplier*	*Booth's multiplier*
Total Delay(ns)	44.249	63.120	128.068
Logic Delay(ns)	11.121	14.998	42.342
Route Delay(ns)	33.128	48.122	85.726
Logic level(ns)	38	57	75

From Table 1 it is evident that the proposed multiplier has reduction in total delay and logic level upon comparison with various multiplier it has been seen proposed multiplier is almost 2 times faster than Booth's multiplier and 1.5 times faster than conventional Vedic multiplier.

6. Conclusion

This paper presents a novel way of realizing 32 bit high speed multiplier using various research methods such as Urdhwa Tiryakbhyam sutra, compressors and reconfigurable multiplication method, methodology to implement same has also been discussed. As speed is major concern proposed multiplier is best in speed. As future work multiplier performance can be tested in ALU and can be compared with other existing multiplier.

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