Design of Low Power 6-bit Digitally-Controlled Oscillator (DCO)

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Abstract: A low power 6-bit CMOS ring based digitally controlled oscillator (DCO) design is presented. The design is proposed based on binary-to-thermometer (BT) decoder current mirror digital-to-analog converter (DAC) and ring-based voltage controlled oscillator (VCO). The DCO is implemented using 0.18 μm CEDEC Mentor Graphic CMOS process at 2.0 V supply voltage. The simulation results show that the proposed DCO consumed only 9.5764 mW of power besides the output voltage is 1.8121 V and local oscillator clock frequency is 33 MHz. The phase noise parameter is -132 dBc/Hz with an offset frequency of 100 kHz has also been reported for the proposed circuits.

Keyword: Ring Oscillator, Digitally-Controlled Oscillator, Digital-to-Analog Converter, Phase Noise.

1. Introduction

Radios, mobile phones, televisions, computers, are just a few models that depend on PLLs for right process that has been used widely in the communications world. A PLL is a control system that produces an output signal [1] ─ [3]. The phase is linked to the phase of an input reference signal. There are comprised of a phase detector and a variable frequency oscillator. From the oscillator's output, the PLLs measure the input signal's phase with the phase of the signal derived and regulate the oscillator's frequency to hold the phases coordinated. To control the oscillator in a feedback mesh circuit, the phase detector's signal has been used. The other essential purpose of a PLL is to synchronize communications between chips [1]. A reference clock is directed along with the parallel data is interconnected. Since chip-to-chip communication most frequently happens at a lower rate than the on-chip clock rate, the reference clock is separated, but still synchronize with the system clock. However other chip the reference clock is used to synchronize all the input flip-flop, which can present a significant clock load in the case of wide data buses [4]. Applying clock buffers to deal with this problem introduces skew between the data and the sample clock. A PLL aligns, that is de-skews, the output of the clock buffer with the respect to the data. In addition, the PLL can multiply the frequency of the incoming reference clock, allowing the core of the second chip to operate at higher frequency than the input reference clock [5].

There are some types of PLLs that are, analog phase-locked loop (APLL), also known as a linear phase-locked loop (LPLL), software phase-locked loop (SPLL), all digital phase-locked loop (ADPLL), and digital phase-locked loop (DPLL) [6] ─ [8]. The upsurge of the operating range by adding more capacitance loading will effect in a lower maximum frequency and higher power consumption. The reduction of the power consumption has developed a key alarm in modern electronic systems since power consumption is of great fear for portable battery-charger in the computing system.

This paper proposed ring-based DCO, which is the combination of a (DAC) [9] and differential ring-based VCO [10, 11]. The current-steering converter is the leading formation for extremely high speed DAC. The current-steering DAC has the benefits of being quite cost efficient. Generally, a self-calibrated circuit can be designed to solve these problems [12] ─

Received: November 3rd, 2013. Accepted: April 18th, 2014

[14] but the circuit will utilize more power and need a large chip area. The segmented current steering is the current method for designing digital-to-analog converters. It merges the benefits of binary weighted and thermometer-coded designs. Successively, the circuit area is reduced with the segmented DAC, as shown in Figure 1.

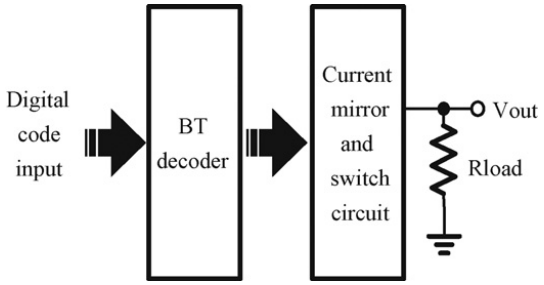


Figure 1. Single ended DAC construction [9]

Ring oscillators can be developed in any standard CMOS process and might need fewer chip area. The design is forthright and ring architectures can be used to offer multiple output phases and wide tuning ranges. With the purpose of reducing the chip area, design of a CMOS differential ring oscillator has been performed notwithstanding its characteristic decreased the phase noise. Therefore, Ring-based VCO (RVCO) is normally familiar because of a moderately small area and toughness over process and temperature changes. The RVCO must be implemented by using differential as a substitute of single ended circuits as delay circuits.

2. Construction of DCO

Normally oscillators are found in wireless communication devices and used in synthesizers, mixers and phase lock loops. Apart from a controllable frequency, the specifications for DCO are frequency range, tuning sensitivity, power consumption, output power, phase noise etc. In this paper, we present a DCO for fully digital PLL application capable of supplying local oscillator clocks at 33 MHz to 3 GHz with low phase noise as well as low power consumption. As mentioned earlier, the proposed DCO is consists of single ended current steering DAC and ring-based VCO, as shown in figure 2. The DAC circuit contained BT decoders and current mirror circuits. There are three current mirrors of different weighting in the current mirrors circuit. Each current mirror regulated a 2-bit BT code decoder.

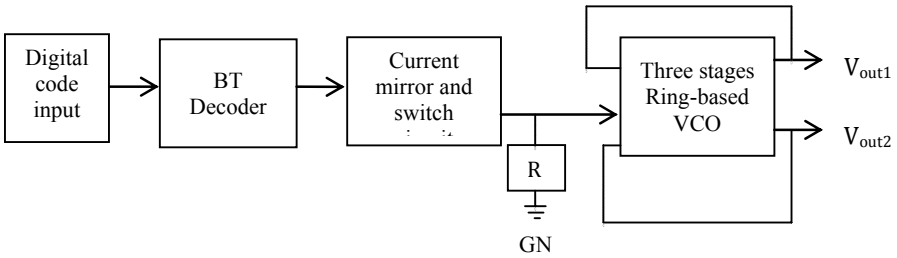
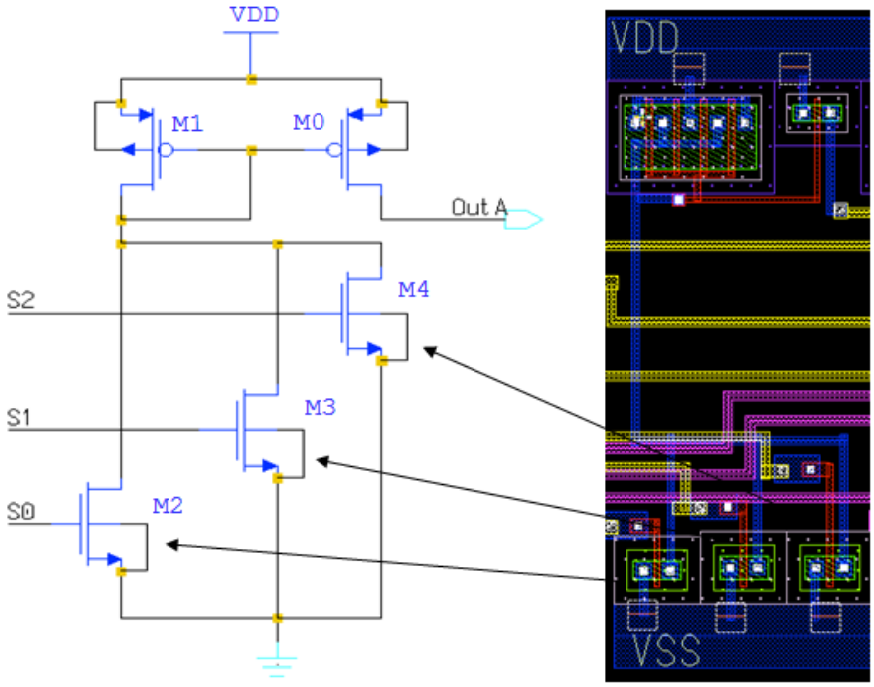


Figure 2. The proposed ring-based DCO

The DAC has gained the advantage of low chip area. It is been obliged low transistor count of this formation. Hence, this DAC has more probability to use low power. The construction circuit of one 2-bit BT decoder comprises of one AND gate and one OR gate in the transistors level. Figure 3 represents the circuit of one 2-bit current mirror circuit of DAC. The transistors M_2, M_3 and M_4, act as switches. These switches turned on the current route. The BT decoder stage generated the signals, S_0, S_1 and S_2. When the switches were turned on, operative resistance looks as if in the middle of the drain of M_1 and GND.



(a) (b)

Figure 3. The Current mirror DAC circuits (a) Schematic, (b) layout

The I_{unit} was the current of the unit output of the 2-bit DAC when the inputs of the switches is 100_2. The I_1 was verified by the parallel resistance of the switches (M_2, M_3 and M_4). The current switch of the 6-bit single-ended DAC needs 9 NMOS transistors acted as switches. The switches set the current will be on or off. I_{out} accumulated the currents from the current mirrors. PMOS transistors M_0 and M_1 were acted as a basic current mirror. The widths of the switches (M2, M3, M4) transistors were amended to achieve an appropriate current on M_1. Figure 4 describes a 2-bit BT decoder current mirror DAC.

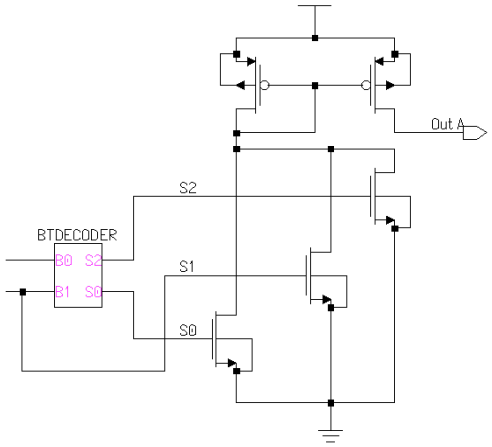


Figure 4. A 2-bit BT decoder current mirror DAC

Different current were acquired by altering the width of the PMOS M_0. The DAC needed three different current sources that are I_{unit}, $4I_{unit}$ and $16I_{unit}$. It is the purpose of smaller area of

the DAC. The aspect ratio of M_0/M_1 were attuned to get the unit current I_{unit}, The aspect ratio of M_2/M_4 and M_{10}/M_{11} also attuned to obtain the current unit for each current mirror circuit, which is $4I_{unit}$ and $16I_{unit}$ respectively. As for VCO, there are massive study has been performed to evaluate and amend the phase noise of ring oscillator [15] ─ [18]. From these studies, it has been testified that the phase noise is reduced by the improved channel thermal noise and the decreased output voltage swing. The Ring-based VCO circuit consists of three-stage ring oscillator.

The circuit is designed for every CMOS, either PMOS or NMOS, is W/L=0.9/0.18. The method, which is using multiple-pass loop, adds supplementary feed forward loops that work in conjunction with the main loop. It is to decrease the delay of the stages. Other configurations are possible to obtain a different frequency increase or decrease even though the illustration of an oscillator with an odd number of stages, with the feed forward loops passing over a single stage. Adjusting the strength of the latch using the $V_{control}$, from V_{dac} that is connected to the switches N11 and N13 regulates the interval of the stage, and the VCO frequency. Higher control voltages effect in a stronger connection between N5 and N7. It creates more complicated to switch the output voltage, and therefore reducing the frequency.

3. Results and Discussion

As mentioned above, the proposed ring-based DCO is a combination of DAC and ring-based VCO. The proposed ring-based DCO circuit is designed for low phase noise and wide frequency tuning range. These circuits are implemented using EDA CEDEC Mentor Graphic 0.18 μm CMOS process. It is 6-bit ring-based Digitally Controlled Oscillator with the value of supply voltage is 2.0 V. The value of the load resistor, R_L, is 50 Ω, meanwhile the transistor count is 75 MOS. For DAC, the V_{dac} is 69.810 mV, meanwhile the output voltages for VCO are, V_{out1} is 1.8121 V. The power dissipation is 9.5764 mW. The core size is estimated around 6000 μm^2 (130.02 μm X 46.21 μm).

From the wave output, Figure 5 shows the digital input by using function 'Pattern'. The input voltage for high input, V_{IH}, is 2 V meanwhile the input voltage for low input, $V_{IL,}$ is -2 V. This DCO has 6 inputs since it is 6-bit DCO.

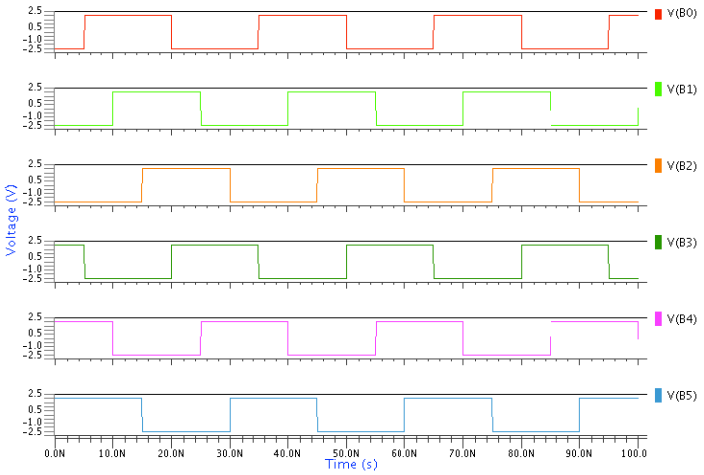


Figure 5. The inputs for 6-bit DCO

Figure 6 depicts that the output voltage for 6-bit BT decoder current mirror DAC. The output voltage, V_{dac}, is 69.810 mV. This output voltage will be the input voltage or $V_{control}$ for three-stage ring oscillator.

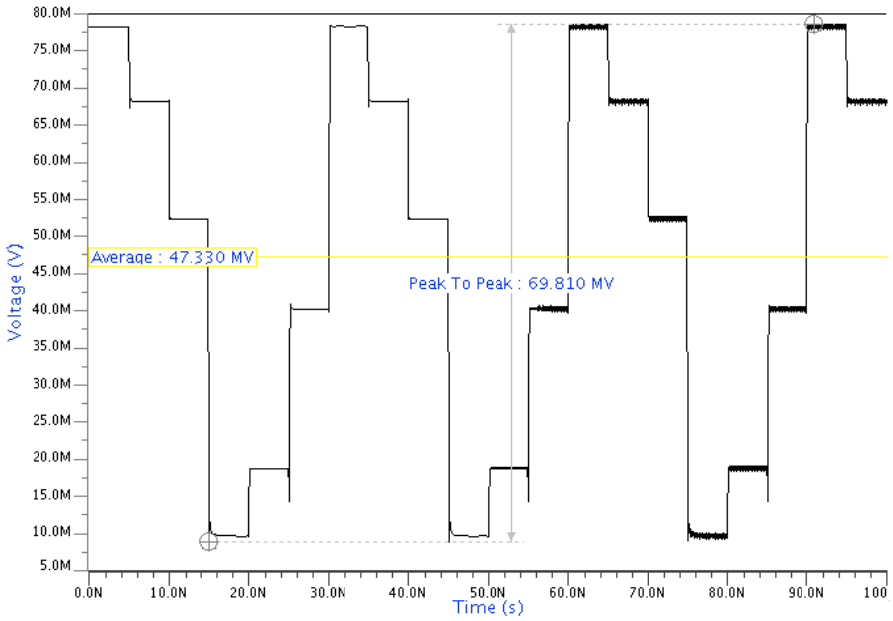


Figure 6. The output voltage for DAC

V_{dac} will be the $V_{control}$ to the three-stage ring oscillator for VCO. The voltage output for DCO is 1.8121 V, slightly lower than the supply voltage (2 V), might be there are current dissipated through the circuits. It dissipated 9. 395%. In figure 7, the phase noise point out at offset frequency 100KHz is -132 dBc/Hz.

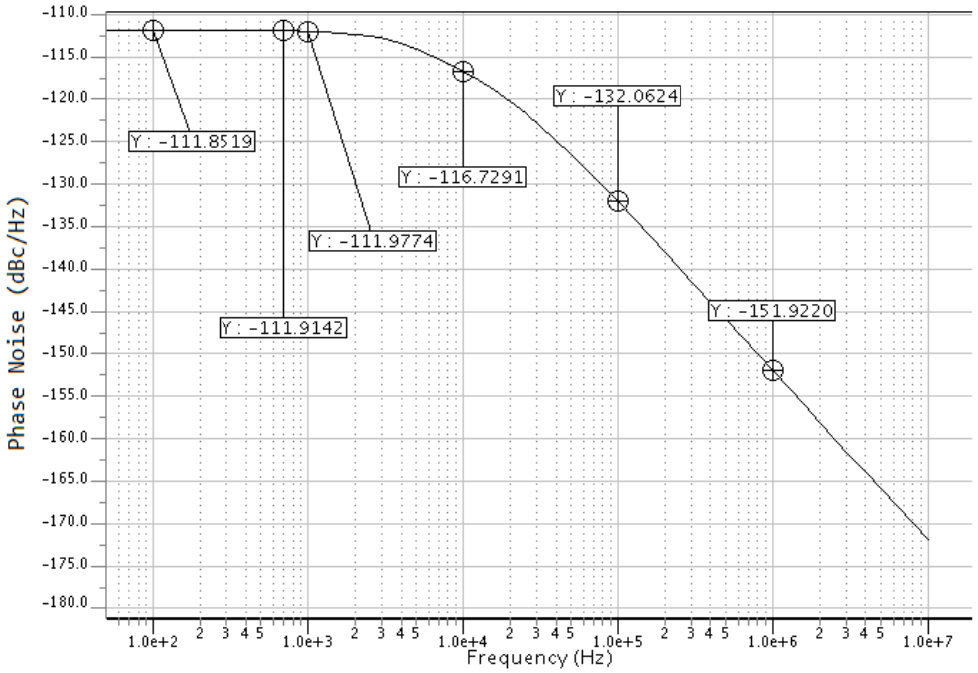
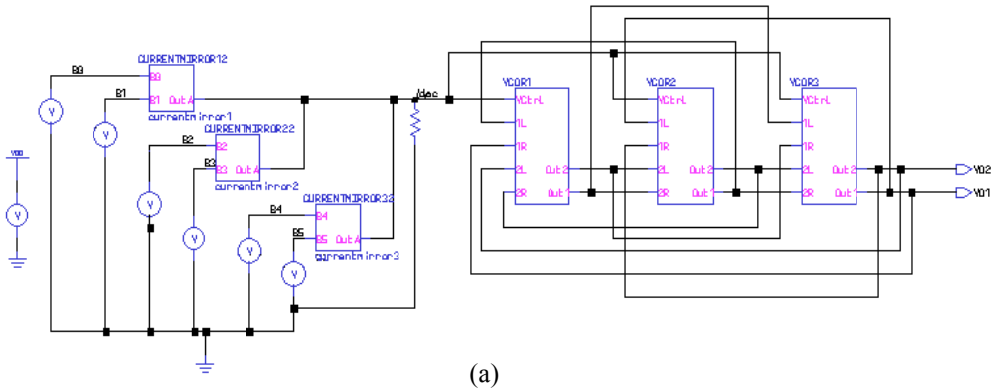
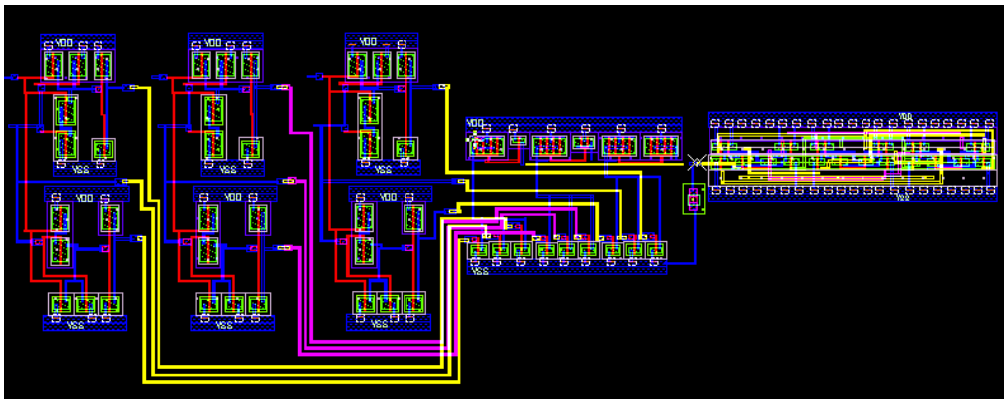


Figure 7. Phase noise at offset frequency.

Further down, it shows Figure 8 (a) the complete circuit for ring-based DCO in schematic and Figure 8 (b) shows the layout of DCO. The size of DCO core cell is approximately 6000 μm^2 (130.02 μm X 46.21 μm). The performance Comparisons with earlier reported circuits in terms of power consumption, phase noise and frequency range are presented in Table 1. It has been observed that the proposed circuits show considerable power saving, a sufficient tuning range and better phase noise.



(a)



(b)

Figure 8. The ring-based digitally controlled oscillator circuit (a) schematic diagram, (b) layout

Table 1. The ring-based DCO performance Comparison.

DCO structure	Power consumption (mW)	Output frequency (GHz)	Phase noise (dBc/Hz)	Technology (μm)
Ref. [19]	63.4	0.333–1.472	–106 @1 MHz	0.35
Ref. [20]	5.4	0.087–0.250	–	0.18
Ref. [21]	30	4.89–5.36	–114 @1 MHz	0.18
Ref. [22]	9	8.79–9.17	–105 @1 MHz	0.18
Present work	9.5764	0.033–3	-132@100 KHz	0.18

Conclusion

The structure of low power 6-bit ring-based DCO was proposed using a 0.18 μm CMOS process have been presented in this paper. This circuit is a combination of BT decoder, current DAC and three-stage ring-based VCO. Simulation results indicate the new 6-bit DCO is able to operate at low supply voltage of 2V and low power consumption is 9.5764 mW. The presented results demonstrate that the proposed design is feasible for various clock control systems for full digital implementations. The performance, flexibility, and robustness make the 6-bit ring-based DCO feasible for high performance fully digital PLL application.

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