Design of transparent a-IGZO thin film transistor for AMOLED display

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***Abstract*—Thin-film transistor(TFT) are key elements for next generation high resolution displays.Transparent amorphous oxide semiconductors especially a-InGaZnO are the most recent TFT materials of interest for driving active matrix displays.In this paper we designed indium-gallium-zinc oxide (a-IGZO) TFT with highly transparent and multilayered gate electrodes using SILVACO TCAD Software which results in reduced RC delay and reduce power consumption by controlling threshold voltage.we obtain threshold voltage of 0.5V and mobility of 11.57 cm2/(V·s).**

Keywords—Thin-film transistor,a-IGZO,RC delay,multilayered gate electrode.

I. INTRODUCTION

The Hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) has long been the workhorse in the active matrix liquid crystal display (AMLCD) industry. As the most critical element of the entire AMLCD the active matrix backplane commonly consists of a array of a-Si:H TFT pixel electrode circuits which directly drive each individual liquid crystal cell pixel. This approach significantly reduces the pixel crosstalk and allows the LCD display to have a high resolution. The typical a-Si:H TFT has field effect mobility (µeff) of 0.6 ~ 0.8cm2/Vs, sub-threshold swing of 0.3 ~ 0.4V/dec, off-state drain current (ID_off) below 10^{-13}A and on-to-off ratio about 10^{7}. These properties are suitable for liquid crystal cell switching but the µeff could become insufficient for the new requirements of next generation displays.

The other emerging area is active matrix organic light-emitting display (AMOLED) where the organic light emitting diode (OLED) is directly integrated with the TFT pixel electrode circuit. AMOLED avoids the need of backlight and the dynamic range of the AMOLED brightness can be controlled at the pixel level which is ideal for TV applications. In addition it can have an extremely high contrast ratio and delivers much better picture quality than the AMLCD. Despite all these attractive properties AMOLED actually poses more stringent requirement on TFT backplane. Unlike liquid crystal which only required external electrical field to change its phase OLED takes significant amount of current to produce light. The µeff of a-Si:H TFT unfortunately is not high enough to drive a large area AMOLED.

II. a-IGZO Thin Film Transistor

Popular semiconductor materials for flexible TFTS ,such as organic semiconductors and amorphous Silicon (a-Si) have been widely used. However, despite their popularity organic semiconductors exhibit low field effective mobilities in the order of ($0.1cm^{2}V.s^{-1}$) and Amorphous Silicon, a-Si exhibits electron mobilities in the order of ($2cm^{2}V.s^{-1}$). Therefore, these low electron mobility values can seriously limit the electrical performance and unit frequency of the device, since both are intimately related to the electron mobility (µ)of the channel under conduction.

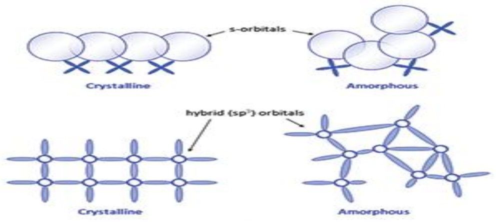

Figure.1 Electronic Structure of Amorphous Semiconductors

As an alternative for these materials, Amorphous Oxides semiconductors (AOSs) exhibit high electron mobilities, that are normally in the order of 10cm^{2}V s^{-1} ,making them suitable channel semiconductor for high performance TFTs.It can be easily seen that a-IGZO TFT is currently the only technology which can achieve a desired balance between high mobility and large area uniformity.Although poly-crystalline silicon (poly-Si) TFT has μeff close to 100 cm^2/Vs.

III. TFT STRCTURE AND OPERATION

A TFT is a field-effect transistor (FET) comprising three terminals (gate, source, and drain) and including semiconductive, dielectric, and conductive layers. The semiconductor is placed between source/drain electrodes and the dielectric is located between the gate electrode and the semiconductor. The main idea in this device is to control the current between drain and source (IDS) by varying the potential between gate and source (VGS) inducing free charge accumulation at the dielectric/semiconductor interface.

TFTs can be seen as a class of FETs where main emphasis is on large area and low temperature processing, while metal oxide semiconductor field-effect transistors (MOSFETs) are essentially focused in high performance, at the cost of considerably larger processing temperature. Figure.2, shows TFT structures depending on the positioning of layers.

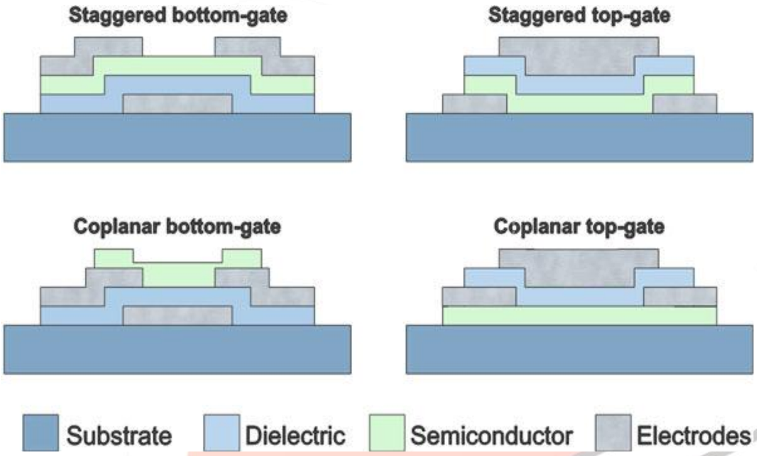

Figure.2 TFT structures depending on the positioning of layers.

Regarding operation and considering n-type TFTs, these can be designated by enhancement or depletion mode depending if threshold voltage (VT) is positive or negative. Enhancement mode is typically preferable because a gate voltage is not necessary to turn off the device. Still, depletion mode devices are also useful for circuit fabrication.

When VGS>VT a significant density of electrons is accumulated in dielectric/semiconductor interface and a large IDS starts flowing depending on the drain-to-source potential (VDS). This state is designated by On-state and involves two main regimes depending on the VDS value:

- If VDS < VGS _ VT, the TFT is in linear mode,
- If VDS >> VGS _ VT, the device is in saturation mode.

IV. DISCUSSION AND RESULTS

Figure 3 shows the mesh structure of a-IGZO thin film transistor.An important area for accuracy in modeling is mesh. It is imperative that there are several mesh points in the X and Y direction in this inversion region to model the drain current correctly.

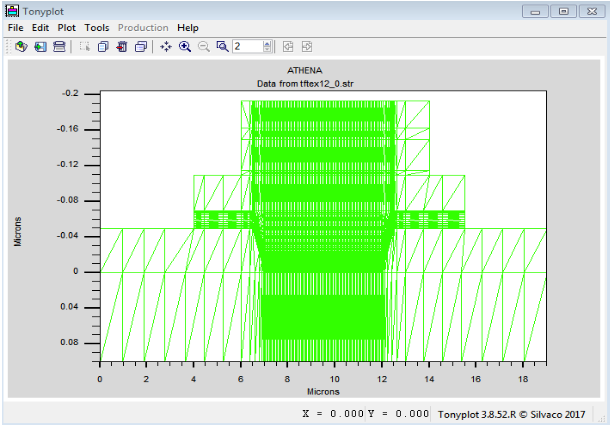

Figure 3. Meshing of TFT

Figure.4 shows the structure of a-IGZO thin film transistor modeled using Athena

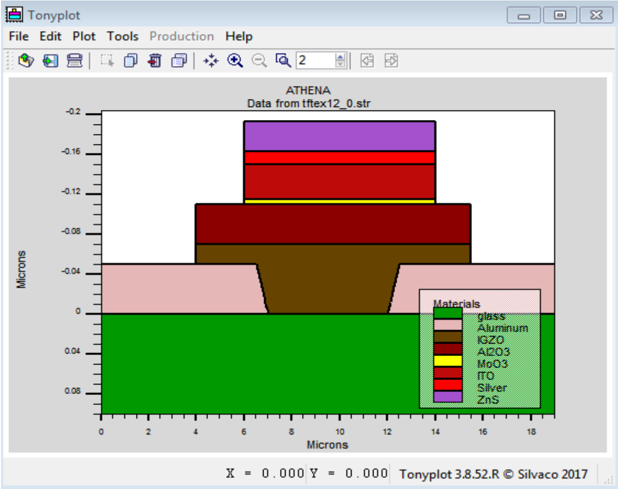

Figure 4. structure of a-IGZO thin film transistor

Figure.5 shows Id-vg Characterisics of a-IGZO thin film transistor which is obtained by setting the drain voltage to 0.1v and sweeping the gate voltage from 0 to 10v. It is observed that threshold voltage vth of designed a-IGZO thin film transistor reaches 0.5v.

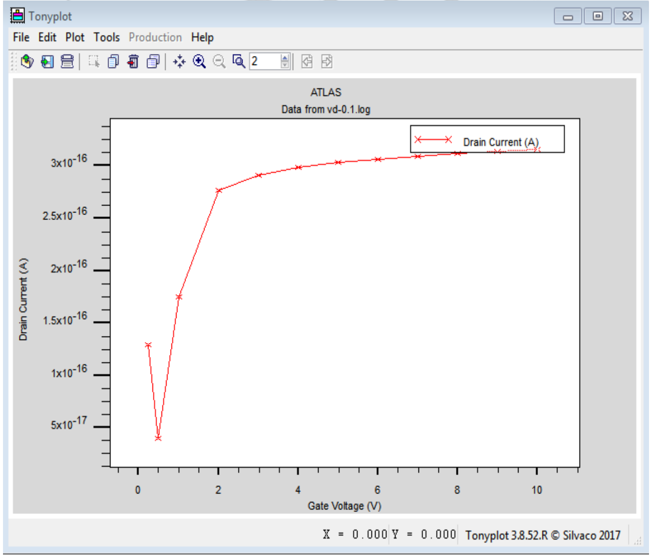

Figure 5. Id-Vg Characteristics

Figure.6 shows Id vs vd characteristics which is obtained by sweeping the gate potential from 4v to 20v with step size of 4v.

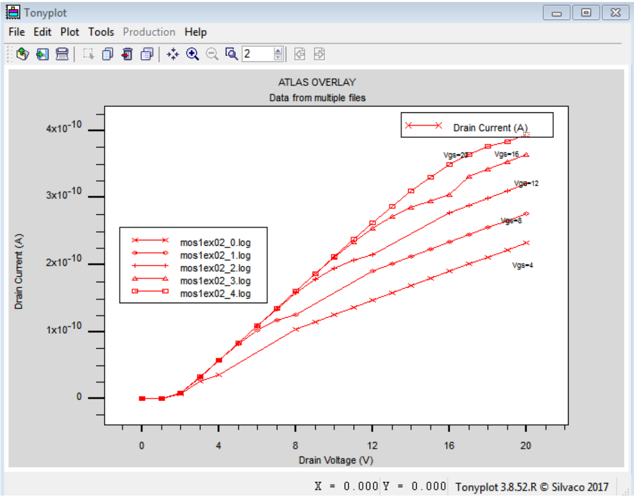

Figure 6. Id-vd Characteristics

Figure.7 shows transfer curves of varying ITO thickness range from 35nm to 100nm,which shows that performance of TFT depending on the ITO thickness. It was found that when the ITO thickness exceeded 35 nm, the TFT mobility was reduced. Therefore, the ITO thickness was set to less than 35 nm considering the device mobility.

ITO thickness (nm)	25	35	45	55	65
μ_{sat} (cm^2/(V·s))	11.84	11.46	10.27	10.09	9.48

Table 1. mobility according to thicknesses of ITO

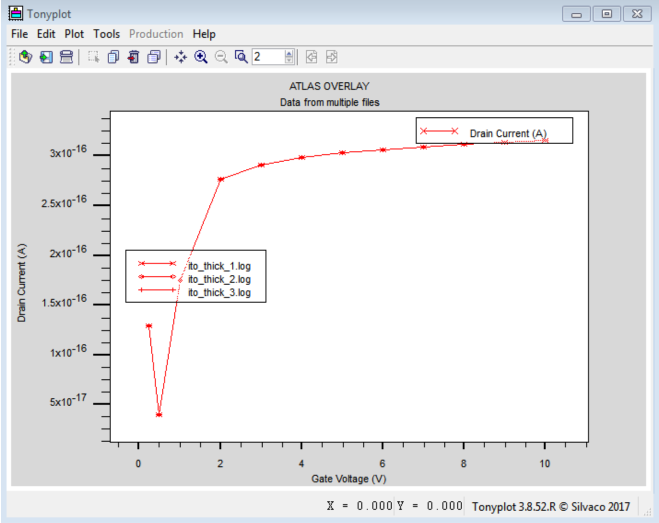

Figure.7 Transfer curves of varying ITO thickness

Figure.8 shows transfer curves with changing the MoO3 thickness from 5 to 10 nm. It was necessary to optimize the MoO3 thickness to yield threshold voltage shift without degradation of the device performance.

	MoO$_3$ thickness (nm)	μ_{sat} (cm^2/(V·s))
IGZO / Al$_2$O$_3$ / MoO$_3$(x) / ITO	5	10.86 (± 0.255)
	10	11.32 (± 0.235)
	15	9.48 (± 0.34)
	20	8.4 (± 0.32)
	25	8.86 (± 0.535)

Table 2. mobility according to thicknesses of MoO3

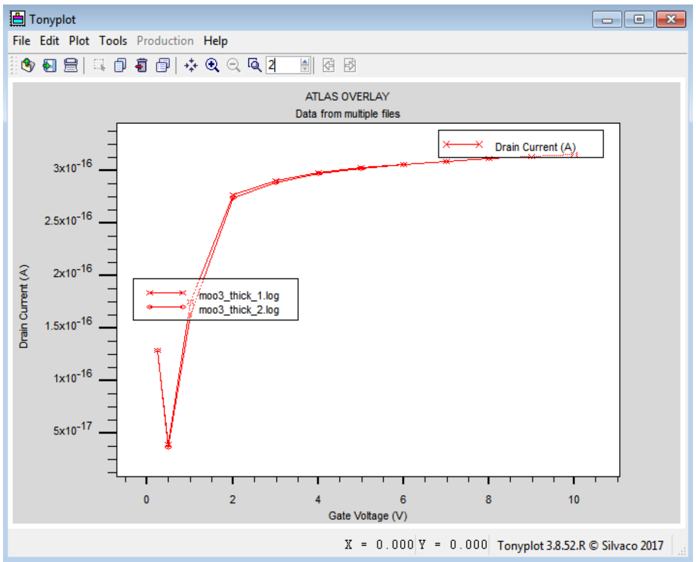

Figure.8 Transfer curves for varying MoO3 thickness

To assess the performance of the optimized electrode, we compared it with ITO gate electrode. The thickness of ITO is 83 nm, which is the same as optimized MIAZ electrode. It shows that threshold voltage of ITO was under 0 V, the threshold voltage of MIAZ exceeded 0 V. The mobility levels of the TFTs with the ITO gate and the MIAZ gate averaged 11.42 and 11.57 cm2/(V·s), respectively.

	ITO	MIAZ
Average V_{th}	-0.08673	0.5
SS (mV/decade)	73.90	70.21
On/off ratio (10^{12})	4.463	1.515
μ_{sat} (cm^2/(V·s))	11.42	11.57

Table 3. Properties of TFTs using ITO and MIAZ gate electrode

V. CONCLUSION

Transparent TFTs based on oxide semiconductors in addition to being transparent have high mobilities and low processing temperatures making them very competitive to existing organic/inorganic TFTs. Highly transparent and low resistive multilayered gate electrodes MoO3/indium–tin oxide (ITO)/Ag/ZnS (MIAZ) playing as the high work function layer, the nonreactive interface layer, the lateral conduction layer, and the index matching layer, respectively have been used for construction of a-IGZO TFT. It provide positive Vth of 0.5V compared with that with single ITO gate electrode of which *V*th is −0.086.

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