Development of a New Improved High Performance Flip Chip BGA Package

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Abstract

The recent advancement in high performance semiconductor packages has been driven by the need for higher pin count and superior heat dissipation. A one-piece cavity lid flip chip BGA package with high pin count and targeted reliability has recently been developed by UTAC. The flip chip technology can accommodate I/O count of more than five hundreds, and the die junction temperature can be reduced to a minimum level by a metal heat spreader attachment. Nonetheless, greater expectations on these high performance packages arose such as better substrate land estate utilization for multiple chips, ease in handling for thinner core substrates and improved board level solder joint reliability. A new design of the flip chip BGA package (patent pending) has been looked into for meeting such requirements. By encapsulating the flip chip with molding compound leaving the die top exposed, a planer top surface can be formed. And a flat lid can then be mounted on the planer mold/die top surface. In this manner the direct interaction of the metal lid with the substrate can be removed. The new package is thus less rigid under thermal loading and solder joint reliability enhancement is expected. This paper discusses the process development of the new package and its advantages for improved solder joint fatigue life, and being a multi-chip package and thin core substrate options. Finite element simulations have been employed for the study of its structural integrity, thermal and electrical performances. Detailed package and board level reliability test results will also be reported.

1. Introduction

The ever-increasing in capacity and power requirements of high-end computers and networks has driven the demand for fast data rate transfer and high speed computing. In meeting these requirements, a challenge is presented to the electronics packaging industry to develop high performance integrated circuit (IC) packages with high input/output (I/O) connections and superior thermal dissipation capabilities. The advancement in flip chip interconnect technology over the years has enabled flip chip devices to be produced more cost effectively (especially on low cost BT substrates). Quality and reliability of the flip chip packages have also been improved greatly. Due its area array interconnection, much higher circuit density can be achieved comparing to conventional peripheral wire-bonding technique. To ease the significant heat generation in the flip chip device, a metal heat spreader (or lid) can be attached on the top of the package for efficient heat dissipation. In this way, the die junction temperature can be maintained at a minimum level. The heat spreader also acts as an environmental protection to the die. In addition to high thermal performance, these devices must exhibit high level of package and solder interconnects reliability, and ease in assembly process. Multiple variations in the high performance semiconductor packages have been developed by the industries [1-5].

In conventional high performance flip chip BGA packages, a metal lid (either one-piece or two-piece structure) will be directly attached onto the substrate after the flip chip assembly process. A one-piece cavity lid flip chip BGA package with high pin count and targeted reliability has recently been developed by UTAC [6]. However it was found that with the one-piece cavity lid directly mounted onto the substrate, restricted flexing in the package has resulted in lower level of solder joints reliability during thermal cycling test.

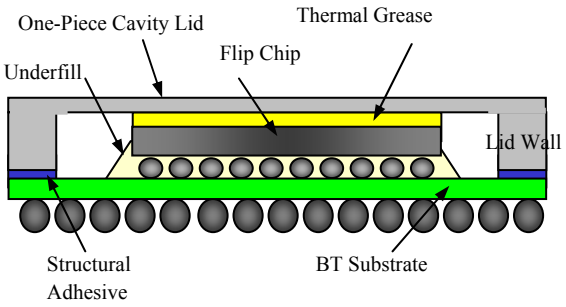


Fig 1. One-Piece Lid High Performance Flip Chip BGA (HP-fcBGA) Package.

A new design of flip chip BGA package (patent pending) has been looked into for improved board level performance. In this new design, the flip chip will be plastic encapsulated (with the die top surface exposed) after the flip chip attach process. A single flat lid will then be mounted onto the mold compound (instead of the substrate). With the elimination of the direct interaction between the metal lid and substrate, the package is expected to be less rigid under thermal loading. Hence solder joint integrity enhancement is anticipated. The ease in manufacturing of the flat lid in the new design is an added advantage, as compared to the powder injection molding of the one-piece cavity lid in the original design. Other advantages of the new design include maximum substrate utilization for multiple chips and passives, accommodating the flexibility in change of die size, and easy handling of thin core substrates during assembly as the overmold helps in making the overall structure more rigid.

This paper discusses the structural integrity of the new flip chip BGA design and the process development involved in its manufacturing. Test vehicles (BT substrate based) of size 40x40mm with pin count of 1521 are fabricated for the evaluation of package and board levels reliability. As heat dissipation capability plays an important role in the high performance IC packages, the thermal performance of the new design will also be analyzed. With the attraction of thinner substrates for minimizing via inductance, electrical simulations/analysis will be performed to investigate the effects of using thin cores on the power distribution impedance and crosstalk interference. Package and board level reliability tests results will also be presented.

2. New Package Construction and Assembly Flow

The HP-fcBGA package (BT substrate based) of size 40x40mm has been built and characterized by UTAC [6]. It is found that the direct interaction between the rigid lid and the substrate has restricted the flexing of the package after being mounted onto the printed circuit board (PCB). It thus induces higher stress and inelastic deformation in the solder joints which resulted in degradation of fatigue performance. Hence a design intent is explored to reduce the direct interference between the lid and substrate. The new Extra Performance flip chip BGA (XP-fcBGA) package is illustrated in Fig. 2. Both package designs share the same substrate consisting of a full array pin count of 1521 (39 x 39 rows), with a solder ball diameter of 0.6mm and a pitch of 1.0mm. The near eutectic solder composition is used in the package.

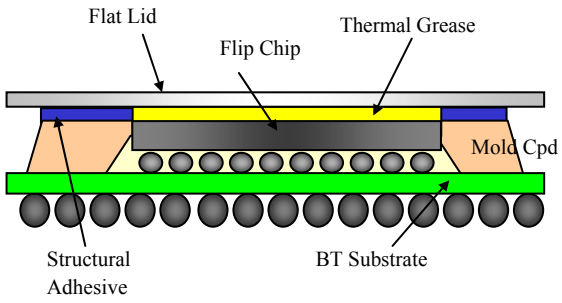


Fig 2. Schematic for Extra Performance Flip Chip BGA (XP-fcBGA) Package - Patent Pending.

In the XP-fcBGA design, the cavity type one-piece lid is being replaced by a flat lid. The assembly flow is as shown in Fig. 3. The flip chip is first mounted onto the BT substrate. After the flip chip underfill process, the silicon die will be encapsulated by a layer of mold compound leaving the chip surface exposed. A new mold chase has to be fabricated for the plastic encapsulation purpose. The spacing available at the substrate corner allows the clamping of substrate during molding process. The tapered edge also helps in relieving stress at the package corner. To provide good thermal interface with the heat spreader, thermal grease is being applied on the silicon top. And the structural adhesive is dispensed on the mold compound for adhesion with the heat spreader. The package would then be subjected to reflow at a temperature of 150^{o}C for the curing of the adhesive before solder ball mounting. With the new assembly process for XP-fcBGA, the immediate interference of the lid on the substrate is being removed. As such, the package is expected to be more flexible under temperature loading which eventually leads to better solder joints fatigue integrity.

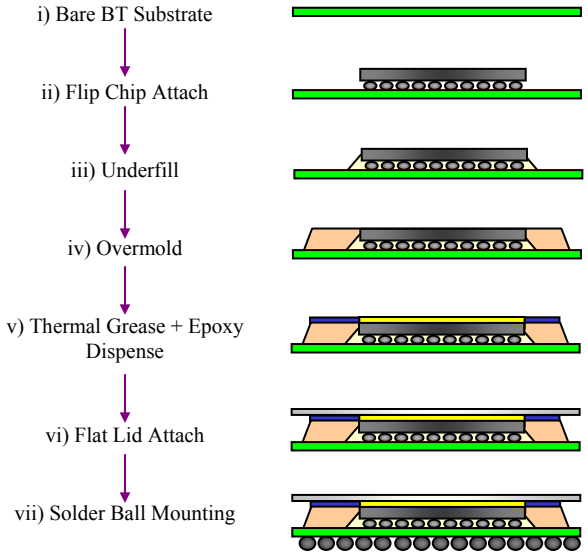
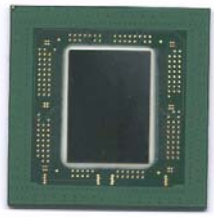


Fig 3. Assembly Flow for the "XP-fcBGA" Package.

The new design is termed "Extra Performance" for several reasons. Firstly, it allows maximum utilization of the substrate's land estate. With the footprint of the metal lid no longer needed on the substrate, extra space can be catered for multiple chips and passive component making it a system-in-package option. Secondly the heat spreader design for XP-fcBGA is independent of die size, making it easier to manufacture by means of photo-etching or metal stamping at a lower cost. The flat lid also enables the ease of attachment to the XP-fcBGA package top compared to HP-fcBGA which requires critical process control on the dispensing of epoxy and thermal grease. Thirdly, it enables the use of thin substrate for better electrical performance. Thin substrates are known to provide better electrical performance as via inductance can be reduced due to shorter interconnections through the substrate. However thin substrates are very difficult to handle during assembly processes, especially after chip attach. With the mold compound covering the top of the thin substrate, the entire structure becomes rigid and thus improving its ease in handling.

Fig. 4 shows the actual sample of the XP-fcBGA package. In the new design, the two-step process of adhesive and thermal grease dispense can be substituted by a single dispense of a thermally conductive adhesive (which is usually of a lower stress and modulus), due to the planar surface for lid placement. With this implementation, assembly cycle time can be shortened as a result.



Flip Chip on Substrate

After Molding

Final Product

Fig 4. Actual Samples of the XP-fcBGA Package.

3. Package Performance Assessments

Test vehicles of the XP-fcBGA package were built for detailed development study. It has a body size of 40x40mm with a nominal total height of 2.82mm. The package is made up of a 6-layer build-up BT substrate of 1.1mm, a flip chip of size 16x22mm backgrinded to 0.52mm thick, a mold block size of 39x39mm with thickness of 0.63mm, and a flat copper lid of 40x40x0.5mm in dimension. Various aspects of the package performance in structural integrity, solder joints fatigue assessment, thermal, electrical and reliability will be discussed. The Finite Element Analysis (FEA) technique is also employed to study the impact of temperature excursion on materials deformation. Three-dimensional (3D) FEA models were created using *ANSYS 7.0* for stress, warpage and solder joint fatigue analysis. The 3D quarter model was created along the cut-out section A-O-B for package related study, while the 3D slice model of the section O-C was used for board interconnects analysis (see Figs. 5 & 6). The first level of flip chip interconnects (solder bumps) was assumed to exhibit the behavior of the underfill layer, hence not included in both the FE models. Inelastic strain energy density representing the damage per cycle of the solder joint would be extracted from the solution for solder joint reliability study. Detailed material properties and FEA modeling have been reported in Chong et al's work [7].

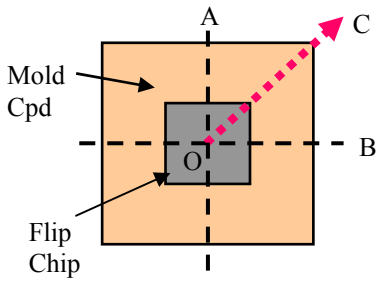
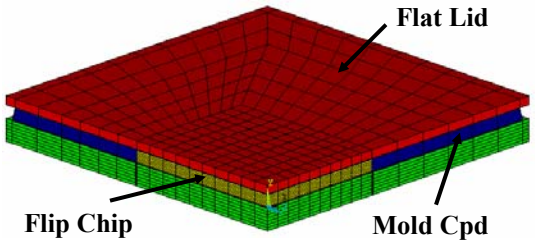
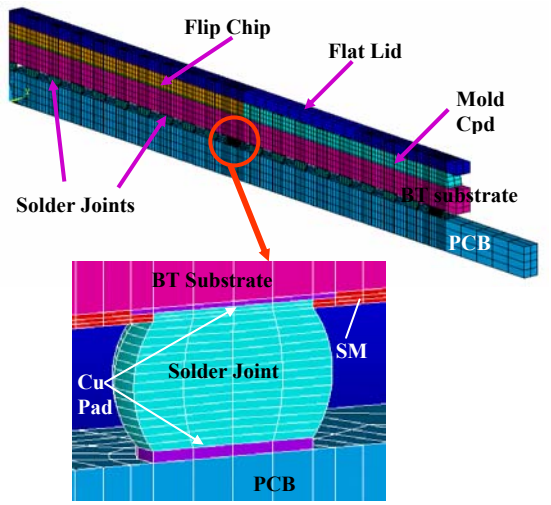


Fig 5. Package Cut-out for the 3D Quarter and 3D Slice Models.



a) 3D Quarter Model (Section A-O-B).



b) 3D Slice Model (Section O-C).

Fig 6. 3D Quarter and Slice FE Models for XP-fcBGA.

3.1. Structural Integrity

With package sizes large than 20x20mm, warpage will always pose many challenges to the assembly processes. For instance, high warpage in a package will cause great difficulty in solder ball mounting onto the substrate and the eventual board assembly. With the present package size of 40x40mm for the flip chip package, it is critical to keep package warpage to a minimum. The package warpage was extracted from the finite element models after a thermal loading from 150°C to 25°C and comparison made with actual substrate warpage measured by a RVSI machine (refer to Fig. 7). It could be seen that XP-fcBGA has generated a higher warpage than the HP-fcBGA (approx. 31% higher). However with the use of a low stress adhesive, a lower warpage could be achieved by the XP-fcBGA package. Good correlation trend has been observed between the finite element results and experimental values, with the exception on the low stress adhesive case. The reason can be attributed to the use of elastic material properties for the mold compound. As molding compound exhibits viscoelastic behavior in nature, warpage may not be accurately captured by simulation. Nonetheless, the warpage data is considerably low for all cases falling below 150um.

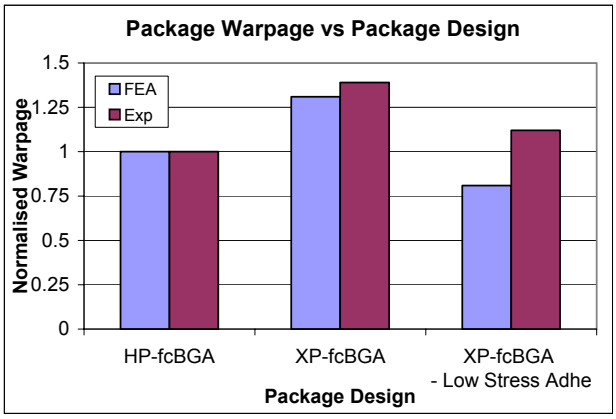


Fig 7. Package Warpage for Different Package Designs.

Due to the additional molding process in the XP-fcBGA design, the package will be subjected to post mold curing prior to lid attachment. When the mold compound cures and set permanently, chemical shrinkage and CTE mismatch will induce warpage to the package thereby increasing the difficulty in mounting the flat lid onto the flip chip and mold top surface. A parametric study was performed in aid to reduce package warpage after post mold curing (before lid is attached). From the results plotted in Fig. 8, it was discovered that an increase in substrate thickness has resulted in the decrease in warpage. The reason can be attributed to the thicker substrate that makes the structure more rigid, hence less susceptable to deformation. The use of a lower Tg mold compound can also help to reduce the package warpage. A reduction in Tg changes the effective CTE of the mold compound, giving a coupling effect on the overall CTE mismatch within the system. However, the varying in die thickness and modulus of mold compound does not have much influence on the warpage behavior.

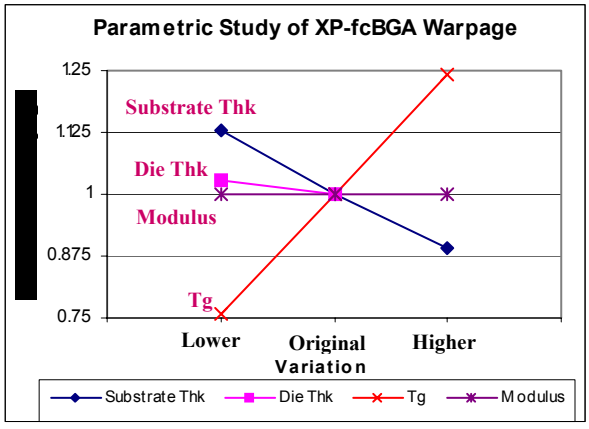


Fig 8. Parametric Effects on XP-fcBGA Structure Warpage (without lid).

Failures such as die cracking and interfacial delamination would render a package faulty and useless. Thus reliability of a new package under development has to be characterized effectively. The package stresses are being analyzed next, with focus on the flip chip and heat spreader. The silicon die being the heart and most vital part in the package, any damage to it will result in losing its electrical functionality. The heat spreader attached onto the package is able to dissipate large amount of heat away from the die and help to maintain a low junction temperature. Any failure in the heat spreader will lower its heat transfer efficiency and may result in over-heating of the silicon die. The die stress, as well as the interfacial shear stresses for die/underfill and heat spreader/mold compound are plotted in Fig. 9. With silicon being a brittle material, the maximum principal stress (S1) accumulated in the die will be extracted for analysis.

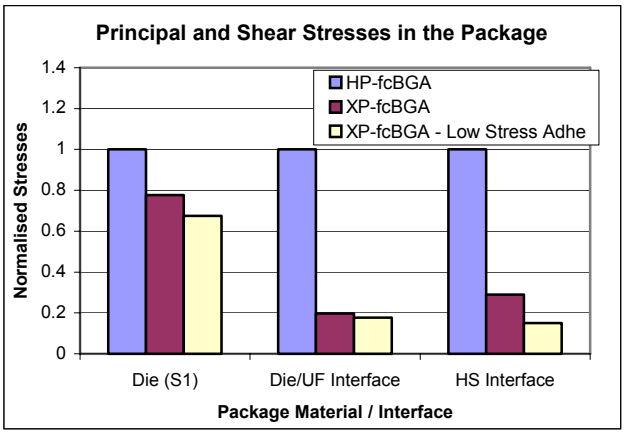
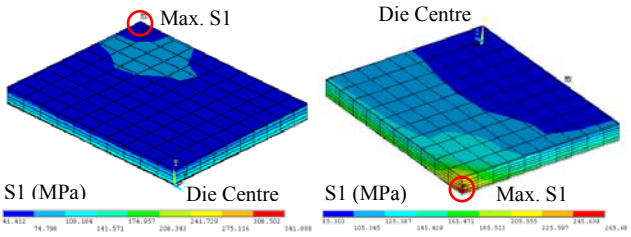


Fig 9. Stresses Experienced in Flip Chip BGA Packages.

In the die stress response, the XP-fcBGA design illustrated a lower die stress than the HP-fcBGA package. A reduction of 23% in die stress could be achieved by the XP-fcBGA, with a larger 33% difference by using the low stress adhesive. The stress distribution in the die is shown in Fig. 10, with the maximum stress located at the outermost corner of the active die side. The interfacial shear stress, where it is an indication of the adhesion strength between interface materials, is investigated next. At the die to underfill interface, XP-fcBGA has again constituted to a lower shear stress with a significant decrease of more than 80% compared to HP-fcBGA. It strongly indicates slimmer chances of delamination taking place at the die/underfill interface. In both cases, the mold compound serves as a buffer to absorb the residual stresses resulting from CTE mismatches under temperature loading. Without the mold compound, the die and underfill would have to absorb the bulk of residual stress which may eventually lead to potential failure such as die cracking or interfacial delamination.



a) HP-fcBGA b) XP-fcBGA

Fig 10. Principal Stress Distribution Within the Die.

With attention moving to the heat spreader interface, a lower shear stress of more than 70% decrement is being observed in XP-fcBGA over HP-fcBGA. With a larger adhesion area of the flat lid to the mold compound in the XP-fcBGA package than the cavity lid to the substrate in HP-fcBGA, the flat lid is able to experience a lesser shear impact. This also shows a much lower interaction force between the lid and the mold compound than the lid with the BT substrate. Thus the potential of delamination at lid interface is reduced to a minimum for the XP-fcBGA package, enhancing the lid's capability in dissipating heat.

3.2. Solder Joint Reliability Assessments

Solder joints fatigue performance has always been a critical concern in new package development. General industrial standard requires the solder joint's fatigue life of a package to surpass 1000 cycles. Board level solder joint reliability of the XP-fcBGA package will be tested and analysed. When undergoing a temperature cycling test according to the test standard of IPC-SM-785 (-40°C to +125°C, 1 cycle/hr), the HP-fcBGA package reported a characteristic life (63.2% failure, θ) of 1777 cycles (with a β of 11.3) with the first failure occurring at 1430 cycles. The failure data is illustrated in the Weibull plot (2 parameters) of Fig. 11. Based on a 3D slice model FEA simulation, the widely accepted Darveaux's volume average strain energy density approach was used to calculate the solder joint fatigue lives [8]. A predicted fatigue life of 1425 cycles for HP-fcBGA was computed, with fairly good correlation of 1.25 times with the experimental value. The FEA model also predicted solder joint cracks occurring at the package side (due to solder-mask defined pad design), agreeing well with the cross-sectional failure analysis pictures (see Fig. 12).

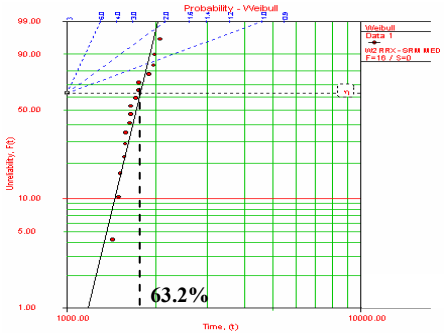


Fig 11. Weibull Reliability Data Plot for HP-fcBGA Package.

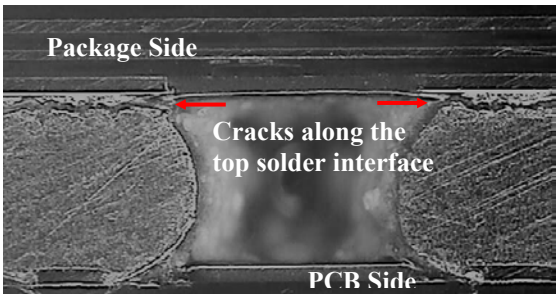


Fig 12. Cross-sectional View of Cracked Solder Joints in the HP-fcBGA Package.

Similar modeling and fatigue life predictions for the XP-fcBGA package were performed, with estimated improved fatigue life shown in Fig. 13. The XP-fcBGA design revealed a significant fatigue improvement of 2.62 times of the HP-fcBGA. It is thus anticipated that the actual characteristic life for XP-fcBGA can surpass 1777 cycles. The solder joint fatigue life can be further enhanced by the use of a low stress adhesive. The preceding section illustrated a significant reduction in the shear stress at the lid interface in XP-fcBGA design. Lesser interference is thus transmitted from the lid to the solder joints through the molding compound. Due to its low modulus, the low stress adhesive provides a large cushioning effect between the lid and the mold compound. The trend revealed that with the removal of the direct interaction between the lid and BT substrate, the new design is able to survive longer fatigue life cycles. This prediction is indeed very encouraging as high reliability solder joint performance is always desired for this package type and application. Test vehicles of the XP-fcBGA package is currently undergoing thermal cycling test with the same loading conditions. Test result up to the present stage stands at 2100 cycles with no solder joint failure. Complete failure data will be reported at a later stage and be correlated to modeling results.

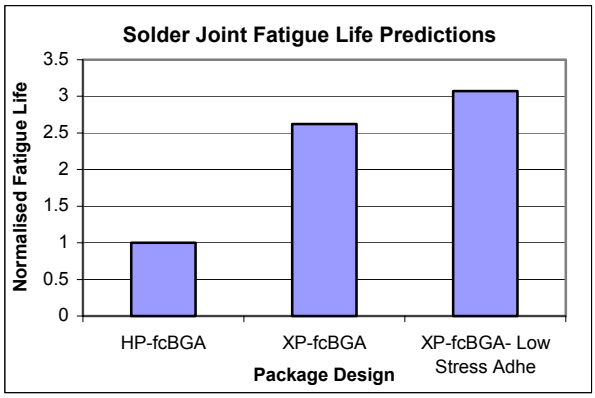


Fig 13. Solder Joint Fatigue Lives Comparison for Flip Chip BGA Packages.

In driving for higher solder joint reliability, further parametric studies have been performed on die and lid thickness. In both cases, a lower thickness has constituted to a better board level solder joints fatigue performance. It is due to the lower effective CTE mismatch with the PCB by the thinner die and lid.

3.3. Heat Dissipation and Thermal Performance

Superior heat dissipation and low thermal resistance is one of the main attractions for the development of this package type. It is therefore necessary to ensure the thermal performance of the XP-fcBGA package should not be compromised. Thermal simulations were carried out using Flotherm 4.1 to assess the heat dissipation capability of the XP-fcBGA design. Experimental thermal measurement conducted for HP-fcBGA package mounted onto a 4-layer PCB (based on JESD 51-9 standard) recorded a junction-to-ambient thermal resistance (θ_{JA}) of 8.89°C/W at zero

windspeed, achieving good correlation with the modeling results [7]. A device power of 3 watts was being used. Correlation within 10% range was also obtained for forced convection conditions of 1, 2, & 3m/s windspeeds. With the same power capacity, thermal simulation predictions for the XP-fcBGA package are shown in Table 1.

Table 1. Thermal Simulations Data of θ_{JA} (^{o}C/W) for HP-fcBGA and XP-fcBGA Packages.

Package	Windspeed (m/s)			
	0	1	2	3
HP-fcBGA	8.68	6.73	5.81	5.27
XP-fcBGA	8.83	6.23	4.86	4.4
XP-fcBGA*	8.82	5.69	4.79	4.29
XP-fcBGA with external heatsink	6.17	-	-	-

* Single dispense of thermally conductive adhesive

Through thermal simulations in the still air condition, only a slight increase in θ_{JA} of 1.62% to 1.73% for the XP-fcBGA package was observed. It thus reveals comparable heat dissipation strength with the HP-fcBGA package. However XP-fcBGA is able to perform better than HP-fcBGA thermally under forced convections. This is due to the extra thermal path from the die's side surfaces to the mold compound and eventually through the flat lid (where this path does not exist in the HP-fcBGA design). It results in a larger heat distribution area on the lid surface where air flow is able to remove the heat away. And results for all cases showed that thermal resistance can be reduced with assisted air flows. For further improvement of the thermal performance, an external heatsink can be attached to the XP-fcBGA package top for maximum heat removal. Modeling result showed that with a pin fin type heatsink (base area = 2"x2", overall height = 0.78", number of pins = 11x11) mounted, a 30% reduction in θ_{JA} can be achieved. Lastly thermal measurements will be conducted for the XP-fcBGA package with values to be correlated with modeling results.

3.4. Electrical Performance Considerations

The use of flip chip solder bumps interconnect has shortened the electrical path between the silicon chip and the chip carrier significantly, thus driving ultimate performances for higher speeds and frequencies. The possible use of thin core in BT substrates will provide a low impedance and high static capacitance for the power distribution network in an IC package. With decreased operating voltage and increased power demands, the current needed to run a system is increasing which requires low impedance for the power distribution network. In addition, the increased static capacitance between the power and ground plane is helpful in power supply decoupling.

There are several advantages for using a thin core substrate. Firstly, the thin core minimizes the loop inductance of power/ground as well as signal nets due to reduced via length. For a power/ground net with a parasitic inductance of L, the induced noise due to one signal switch is given by:

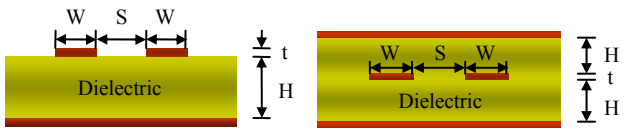
$$V = L\frac{di}{dt} \qquad (1)$$

where V is the induced voltage, and di is the transient current over the signal transition period of time dt. Thus, a reduced L results in lower simultaneous switching noise (SSN). For a signal net, lower inductance causes less impedance discontinuity resulting in higher signal transmission efficiency. Secondly, thin core can offer superior wiring densities due to smaller via diameters. This makes it possible for packing a shrunk die in a smaller package, or retaining the package size while allocating more I/Os for power/ground distribution. The increased power/ground I/Os will result in even lower parasitic inductances, higher current handling capability as well as better heat dissipation. Thirdly, thin core substrate is able to offer a thin profile package solution. If the thickness of a package's substrate is kept constant, thin core provides the possibility for more solid planes to be incorporated as power or ground plane. These solid power/ground planes have the advantage of providing more effective system power distributions. Furthermore, signal layers are usually sandwiched between the power and ground planes forming stripline structures (see Fig. 14) compared to a microstrip design. A 2-dimensional electrical simulation was preformed using Ansoft Spicelink, and the parasitics for microstrip and stripline designs were compared in Table 2. By virtue of a stripline structure, adjacent signal nets will have a lower near-end and a nearly zero far-end crosstalk for a better electrical performance and lower Electromagnetic Interference (EMI). Thus it could be seen that a thin core substrate provides several possibilities in improving a package electrical performance. The overmolded structure of XP-fcBGA will help in easy handling of the thin core substrates during assembly processes, and thus able to drive its popularity in the semiconductor industry.

Table 2. Electrical Performance Parameters for "Microstrip" and "Stripline" Structures.

Structure	Ls (nH/mm)	Lm (nH/mm)	Cs (fF/mm)	Cm (fF/mm)	Zo (Ohm)	X_talk (%)
Microstrip	0.53	0.22	58.36	17.75	100.00	18%
Stripline	0.30	0.04	148.90	18.90	45.00	6%

* Note: w/s = 35/45 um and dielectric thickness = 100um.



a) Microstrip b) Stripline

Fig 14. Schematic for "Microstrip" and "Stripline" Structures.

3.5. Package Level Reliability Tests Results

Reliability tests were conducted at the package level to assess its internal structural integrity. The flip chip solder bumps interconnection was monitored and check on possible interfacial delamination was carried out using CSAM technique. Three tests namely temperature cycling (TC), unbiased autoclave (also known as pressure cooker test, PCT) and high temperature storage (HTS) were conducted with a sample size of 22 units for each test. The moisture preconditioning was set at JEDEC level 4. Both the standard and low stress adhesive dispense types were studied. Table 3 shows the results of the reliability evaluation. The XP-fcBGA package with the low stress adhesive showed good reliability data with no solder bump crack or delamination failure. The standard adhesive XP-fcBGA tests are still in progress and results will be reported when completed.

Table 3. Package Reliability Test Results for the XP-fcBGA Package.

		Results	
Test	Condition (JEDEC Standard)	XP-fcBGA	XP-fcBGA (low stress adhe)
TC	-55°C to +125° 2 cycles/hr (JESD22-A104-B)	Test in progress	Passed 1000 cycles
PCT	121°C / 100% RH 2 atm (JESD22-A102-C)	Test in progress	Passed 168 hours
HTS	150 °C (JESD22-A103-B)	Test in progress	Passed 1000 hours

4. Conclusions

The new XP-fcBGA package has been successfully developed, with various aspects of the package performance in structural integrity, solder joints fatigue assessment, thermal, electrical and reliability being addressed. By encapsulating the flip chip with a molding compound exposing the die top surface, a flat lid can be mounted on the planer top surface for heat dissipation purpose. As such, the direct interaction of the metal lid with the substrate can be removed thus enhancing solder joint reliability.

The XP-fcBGA package shows clearly its strength over the original HP-fcBGA design with comparable package warpage, lower package stresses and higher solder joint fatigue lives. In board level reliability test, the XP-fcBGA solder joints have survived more than 2000 cycles with no observed failure. In package level reliability tests, the option of low stress adhesive is able to withstand stringent test conditions. In addition, the XP-fcBGA package is able to exhibit high heat dissipation capability with a low thermal resistance. With the overmolded structure which increases rigidity during process handling, thin core substrates can be used for improved electrical performances. Further developments of the XP-fcBGA design include expanding to different package sizes and thickness, and the evaluation of the new design as a multi-chip module.

5. Future Work

Experimental board level solder joint fatigue lives will be correlated with simulation results. Thermal measurements will also be conducted for the XP-fcBGA package to determine its thermal resistance. Lastly, package level reliability tests results will be reported when tests are completed.

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