Deliang Fan

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RESEARCH INTEREST

- Energy Efficient and High Performance In-Memory Computing Circuit, Architecture and Algorithm co-design, with applications in Deep Neural Network, Data Encryption, Graph Processing and Bioinformatics, etc.
- Hardware-Aware Deep Neural Network Compression and Optimization Algorithm
- Adversarial AI Security Algorithm and Hardware System
- Brain-inspired (Neuromorphic) and Boolean Computing Using Emerging Nanoscale Devices like Spintronics and Memristors
- Low Power Digital VLSI Circuit Design
- Cross-layer (Device/ Circuit/ Architecture) Co-Design for Ultra-low Power, High Performance System

EDUCATION

Purdue University West Lafayette, IN, USA Aug. 8, 2015
Ph.D. in Electrical and Computer Engineering
Thesis: Boolean and Brain Inspired Computing using Spin-Transfer Torque Devices
Advisor: Prof. **Kaushik Roy** (Edward G. Tiedemann Jr. Distinguished Professor of ECE)

Purdue University West Lafayette, IN, USA Dec.2012
Master of Science in Electrical and Computer Engineering GPA:3.66/4.0
Thesis: Cross Layer Design Exploration for OFDM Energy-Quality Trade-offs Advisor: Prof. K. Roy

Zhejiang University, College of Electrical Engineering Hangzhou, China Jun.2010
Bachelor of Electronic Information Engineering Major GPA:3.91/4.0 Overall GPA: 3.81/4.0
Thesis: Design of High Resolution DPWM in Digital Power Management Chip Advisor: Prof. Xiaobo Wu

PROFESSIONAL EXPERIENCE

- Tenure-Track Assistant Professor at School of Electrical, Computer and Energy Engineering
  Arizona State University (ASU), Tempe, AZ, USA Aug. 2019 - present

- Courtesy Professor at Department of Electrical and Computer Engineering
  University of Central Florida (UCF), Orlando, FL, USA Aug. 2019- 2021

- Tenure-Track Assistant Professor at Department of Electrical and Computer Engineering
  University of Central Florida (UCF), Orlando, FL, USA Aug. 2015-Aug. 2019

- Research Assistant at Nanoelectronics Research Lab
  Purdue University, West Lafayette, IN, USA Mar.2012-Aug. 2015

ACADEMIC AWARDS

- **Best Paper Award** in ACM Great Lakes Symposium on VLSI (*GLSVLSI*), Washington, D.C., USA, 2019 (My phd student, Shaahin Angizi, as the first author and I am the corresponding author)
- **Best Paper Award** in IEEE Computer Society Annual Symposium on VLSI *(ISVLSI)*, Hong Kong, China, 2018 (my phd student, Zhezhi He, as the first author and I am the corresponding author)
- **Best Paper Award** in IEEE Computer Society Annual Symposium on VLSI *(ISVLSI)*, Bochum, Germany, 2017 (my phd student, Farhana Parveen, as the first author and I am the corresponding author)
- **Best Poster Award (1st place)**, Ph.D. Forum at Design Automation Conference, San Francisco, CA, USA, 2018 (My phd student, Shaahin Angizi, as the first author and I am the corresponding author)
- **Best Paper Nomination** in Design Automation Conference (*DAC*), 2021 (My phd student, Fan Zhang, as the first author and I am the corresponding author)
- **Best Paper Candidate** in Asia and South Pacific Design Automation Conference (*ASPDAC*), Tokyo, Japan, 2019 (collaborative work with Dr. Ewetz)
- **Best Paper Candidate** in International Symposium on Quality Electronic Design (*ISQED*), Santa Clara, CA, 2019 (my phd student, Shaahin Angizi, as the co-author)
- **Schloss Dagstuhl - NSF** Award for Junior Researchers, 2019
- **Front Cover Paper** in *IEEE Transactions on Magnetics, Vol. 54, No.2, Feb. 2018*
- **Outstanding Faculty Mentor Award Nomination** of ASU Graduate College, 2020-21

FUNDED RESEARCH PROJECTS

- National Science Foundation (**NSF**): SaTC: CORE: Small: "Understanding and Taming Deterministic Model Bit Flip attacks in Deep Neural Networks", 10/01/2020 – 09/30/2023; Role: **PI**; $249,476); NSF Award number: 2019548
- National Science Foundation (**NSF**): FET: Small: "AlignMEM: Fast and Efficient DNA Sequence Alignment in Non-Volatile Magnetic RAM", 10/01/2019 - 09/30/2022; Role: **Leading-PI**, total: $491,298; personal share: $242,744; NSF Award number: 2003749
- National Science Foundation (**NSF**): CPS: Medium: "A Secure, Trustworthy, and Reliable Air Quality Monitoring System for Smart and Connected Communities", 10/01/2019 – 09/30/2022; Role: **Co-PI** of whole project, **PI of ASU**, total: $1,198,111; personal share: $221,112; NSF award number: 1931871
- National Science Foundation (**NSF**): E2CDA: "Non-Volatile In-Memory Processing Unit: Memory, In-Memory Logic and Deep Neural Network" 2017-2021; Role: **Sole-PI**, $184,470; NSF award number: 2005209/ 1740126
- Semiconductor Research Corporation (**SRC**): "Non-Volatile In-Memory Processing Unit: Memory, In-Memory Logic and Deep Neural Network" 2018-2020, Role: **Sole-PI**, $107,626
- **H Lee Moffitt Cancer Center and Research Institute, Inc.**: Development of a mathematically-based clinical decision support tool for multiple myeloma,", 2020 – 2021; Role: **Co-PI** of whole project, and **PI of ASU**; personal share: $25,000
- **Cyber Florida**: "Towards Robust Deep Learning Systems Against Adversarial Attacks," 2019-2020, total: $75,000; Role: **Leading-PI,** personal share: $37,500
- UCF NanoScience Technology Center (NSTC) Research Seed Award, "3D nanotubular metal-insulator-metal memristors for neuro-inspired artificial intelligence", 2019-2020, Role: **Co-PI**, total project: $30,000, personal share: $10,000
- Southeastern Center for Electrical Engineering Education (**SCEEE**), Research Initiation Grant,

"Ultra-Low Energy Brain-Inspired Computing using Nanoscale Emerging Spintronic Devices**,**" 2016-2017, Role: **Sole-PI**, $44,00 ($22,000 + $22,000 UCF matching fund)

- UCF In-House Award, "Self-Sustained Spin-Transfer Torque Devices based Brain-inspired Processor Powered by Energy Harvesting Technology for Internet of Things Applications," 2016-2017; Role: **Sole-PI**, $7,500

GRADUDATE STUDENTS ADVISING (as *Advisory Committee Chair*)

- Advisor of Ph.D. students:
    a) Zhezhi He (PhD awarded in Summer 2020 from ECEE of ASU, currently tenure track Assistant Professor in Shanghai Jiaotong University, China https://elliothe.github.io/)
    b) Shaahin Angizi (ASU, PhD defense scheduled in April 2021, accepted tenure-track assistant professor offer from department of Electrical and Computer Engineering, New Jersey Institute of Technology, starting from Fall 2021)
    c) Adnan Siraj Rakin (enrolled in ECEE of ASU)
    d) Li Yang (enrolled in ECEE of ASU)
    e) Fan Zhang (enrolled in ECEE of ASU)
    f) Amitesh Sridharan (enrolled in ECEE of ASU)
    g) Farhana Parveen (Aug. 2016 to Jan. 2018, was enrolled in ECE of UCF)

- Advisor of Master students with thesis:
    a) Kiju Kim (enrolled in ECEE of ASU)
    b) Li Yang (Aug. 2017 to Dec. 2018, graduated from ECE of UCF)

ADVISED STUDENTS' AWARDS

- Zhezhi He:

    a) Engineering Graduate Fellowship, Arizona State University, 2020
    b) University Graduate Fellowship (UGF), Arizona State University, 2020
    c) TECHCON travel grant, Semiconductor Research Corporation, 2019
    d) ACM SIGDA scholarship for Ph.D. forum, Design Automation Conference, 2019
    e) Best Paper Award, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2018,2017

- Shaahin Angizi:

    a) Outstanding Adjunct Instructor performance, EEL 4362 Post-CMOS Devices and Circuits, UCF, 2020
    b) David T. & Jane M. Donaldson Memorial Scholarship Award, UCF, 2019
    c) Best Paper Award, ACM GLSVLSI, Washington, D.C., USA, 2019
    d) Best Poster Award, Ph.D. Forum at DAC, San Francisco, CA, USA, 2018
    e) Best Paper Award, IEEE ISVLSI, Hong Kong, China, 2018
    f) IEEE/ACM DAC - Ph.D. Forum Travel Grant, San Francisco, CA, USA, 2018
    g) Paper of the month (October-December) of IEEE TETC, 2018
    h) Best Paper Award, IEEE ISVLSI, Bochum, Germany, 2017
    i) Two Most Cited Articles in Elsevier's Microelectronics Journal, 2017

j) Most Cited Article in Elsevier's Microprocessors and Microsystems, 2017
k) Outstanding Reviewer Award of Microelectronics Journal and Microprocessors and Microsystems, 2017
l) Doctoral Fellowship Award, UCF- Office of Research and Commercialization (ORC), 2016

- Fan Zhang :

a) Best Paper Nomination in Design Automation Conference (DAC), 2021

PUBLICATIONS

Journal (**35** in total, listed by publication date, **my phd students are labelled with '*'**)

J35. [TCAS-I'21] Honglan Jiang, Shaahin Angizi*, Deliang Fan, Jie Han and Leibo Liu, "Non-Volatile Approximate Arithmetic Circuits using Scalable Hybrid Spin-CMOS Majority Gates," *IEEE Transactions on Circuits and Systems (TCAS-I)* (accept)

J34. [TCAD'21] Han Xu, Ziwei Li, Ziru Li, Deliang Fan, Fei Qiao, Qi Wei, Li Luo, Xinjun Liu and Huazhong Yang, "Reducing SRAM Reading Power With Column Data Segment and Weights Correlation Enhancement for CNN," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*(accept)

J33. [JETC'21] Qutaiba Alasad, Jie Lin, Jiann-Shuin Yuan, Amro Awad, Deliang Fan, "Resilient and Secure Hardware Devices Using ASL," *ACM Journal on Emerging Technologies in Computing Systems* (accept)

J32. [TNNLS'21] Xiaolong Ma, Sheng Lin, Shaokai Ye, Zhezhi He, Linfeng Zhang, Geng Yuan, Sia Huat Tan, Zhenggang Li, Deliang Fan, Xuehai Qian, Xue Lin, Kaisheng Ma, and Yanzhi Wang, "Non-Structured DNN Weight Pruning – Is It Beneficial in Any Platform?," *IEEE Transactions on Neural Networks and Learning Systems (*TNNLS*)*, 2021 (accept)

J31. [EDL'20] Durjoy Dev, Adithi Krishnaprasad, Mashiyat S. Shawkat, Zhezhi He*, Sonali Das, Deliang Fan, Hee-Suk Chung, Yeonwoong Jung, and Tania Roy, "2D MoS2 Based Threshold Switching Memristor For Artificial Neuron," *IEEE Electron Device Letter (EDL)*, 2020 (accept)

J30. [TMAG'20] Shaahin Angizi*, Zhezhi He*, An Chen and Deliang Fan, "Hybrid Spin-CMOS Polymorphic Logic Gate with Application in In-Memory Computing," *IEEE Transactions on Magnetics (*TMAG*)*, Volume: 56 , Issue: 2 , Feb. 2020, DOI: 10.1109/TMAG.2019.2955626

J29. [JETC'20] Zhezhi He*, Li Yang*, Shaahin Angizi*, Adnan Siraj Rakin* and Deliang Fan, "Sparse BD-Net: A Multiplication-Less DNN with Sparse Binarized Depth-wise Separable Convolution," *ACM Journal on Emerging Technologies in Computing Systems,* January 2020 Article No.: 15 https://doi.org/10.1145/3369391

J28. [Bioinformatics'19] Zhibo Wang, Zhezhi He*, Milan Shah, Teng Zhang, Deliang Fan and Wei Zhang, "Network-based multi-task learning models for biomarker selection and cancer outcome prediction," *Bioinformatics*, 05 November 2019, btz809, https://doi.org/10.1093/bioinformatics/btz809 (9 pages)

J27. [TC'19] Arman Roohi, Shadi Sheikhfaal, Shaahin Angizi*, Deliang Fan, Ronald DeMara, "ApGAN: Approximate GAN for Robust Low Energy Learning from Imprecise Components," *IEEE Transactions on Computers*, 23 October 2019, DOI: 10.1109/TC.2019.2949042 (12 pages)

J26. [TCAD'19] Baogang Zhang, Necati Uysal, Deliang Fan, Rickard Ewetz, "Handling Stuck-at-fault Defects using Matrix Transformation for Robust Inference of DNNs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (TCAD), 30 September 2019, DOI:

10.1109/TCAD.2019.2944582 (13 pages)

J25. [TCAD'19] Shaahin Angizi*, Zhezhi He*, Amro Awad and Deliang Fan, "MRIMA: An MRAM-based In-Memory Accelerator," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (TCAD) 27 March 2019, DOI: 10.1109/TCAD.2019.2907886 (14 pages)

J24. [JETC'18] Farhana Parveen*, Shaahin Angizi* and Deliang Fan, "IMFlexCom: Energy Efficient In-memory Flexible Computing using Dual-mode SOT-MRAM," *ACM Journal on Emerging Technologies in Computing Systems*, vol. 14, no.3, October 2018, https://doi.org/10.1145/3223047

J23. [TNANO'18] Shaahin Angizi*, Honglan Jiang, Ronald Demara, Jie Han and Deliang Fan, "Majority-Based Spin-CMOS Primitives for Approximate Computing," IEEE Transactions on Nanotechnology, vol. 17, no. 4, July 2018

J22. [TMSCS'18] Zhezhi He*, Yang Zhang, Shaahin Angizi*, Boqing Gong and Deliang Fan, "Exploring A SOT-MRAM based In-Memory Computing for Data Processing," IEEE Transactions on Multi-Scale Computing Systems, vol. 4, no.4, pp. 676-685, Oct.-Dec.1, 2018

J21. [TMAG'18] Farhana Parveen*, Shaahin Angizi*, Zhezhi He* and Deliang Fan, "IMCS2: Novel Device-to-Architecture Co-design for Low Power In-memory Computing Platform using Coterminous Spin-Switch," *IEEE Transactions on Magnetics,* vol. 54, no.7, July 2018

J20. [TMAG'18] Steven Pyle, Deliang Fan, Ronald DeMara, "Compact Spintronic Muller C-Element with Near-Zero Standby Energy," *IEEE Transactions on Magnetics,* vol.54, no.2, Feb. 2018 (**Front Cover Paper**)

J19. [TMSCS'17] Yu Bai, Deliang Fan and Mingjie Lin, "Stochastic-Based Synapse and Soft-Limiting Neuron with Spintronic Devices for Low Power and Robust Artificial Neural Networks," *IEEE Transactions on Transactions on Multi-Scale Computing Systems,* vol.4, no.3, pp.463-476, Dec. 2017

J18. [TCAD'17] S. Angizi*, Z. He*, N. Bagherzadeh and D. Fan, "Design and Evaluation of a Spintronic In-Memory Processing Platform for Non-Volatile Data Encryption," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol.37, no.9, Sept. 2018

J17. [MAGL'17] Z. He*, S. Angizi*, and D. Fan, "Current Induced Dynamics of Multiple Skyrmions with Domain Wall Pair and Skyrmion-based Majority gate Design," *IEEE Magnetics Letters*, vol.8, March 30, 2017

J16. [TCAD'17] A. Roohi, R. Zand, D. Fan and R. DeMara, "Voltage-based Concatenatable Full Adder using Spin Hall Effect Switching," *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD),* vol.36, no.12, Dec. 2017

J15. [JETC'17] K. Yogendra, C. Liyanagedera, D. Fan, Y. Shim and K. Roy, "Coupled Spin-Torque Nano-Oscillator based Computation: A Simulation Study", *ACM Journal on Emerging Technologies in Computing Systems*, vol. 13, no.4, July 2017

J14. [TETC'17] Z. He* and D. Fan, "Energy Efficient Reconfigurable Threshold Logic Circuit with Spintronic Devices," *IEEE Transactions on Emerging Topics in Computing*, vol. 5, no. 2, pp.223-237, May 2017

J13. [JETCAS'17] S. Salehi, D. Fan, R. DeMara, "Survey of STT-MRAM Cell Design Strategies: Taxonomy and Sense Amplifier Tradeoffs for Resiliency," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems,* Vol.13, no.3, May 2017

J12. [TNANO'17] R. Zand, A. Roohi, D. Fan and R. DeMara, "Energy-Efficient Nonvolatile Reconfigurable Logic using Spin Hall Effect-based Lookup Tables," *IEEE Transactions on Nanotechnology,* Vol. 16, no. 1, pp. 32-43, Jan. 2017.

J11. [TCAD'16] X. Fong, Y. Kim, K. Yogendra, D. Fan, A. Sengupta, A. Raghunathan, and K. Roy, "Spin-Transfer Torque Devices: Prospects and Perspectives," *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 25, no. 1, pp.1-22, Jan 2016 (invited tutorial)

J10. [TED'16] K. Yogendra, D. Fan, B. Jung and K. Roy, "Magnetic Pattern Recognition using Injection Locked Spin Torque Nano-Oscillators", *IEEE Transactions on Electron Devices (TED)*, vol. 63, no. 4, pp. 1674-1680, Feb. 2016

J9. [TNANO'15] D. Fan, S. Maji, K. Yogendra, M. Sharad and K. Roy, "Injection Locked, Spin Hall Induced Coupled-Oscillators for Energy Efficient Associative Computing," *IEEE Transaction on Nanotechnology* (TNANO), Vol. 14, no.6, Aug. 2015.

J8. [TNNLS'15] D. Fan, M. Sharad, A. Sengupta and K. Roy, "Hierarchical Temporal Memory Based on Spin-Neurons and Resistive Memory for Energy-Efficient Brain-Inspired Computing," IEEE *Transaction on Neural Networks and Learning Systems* (TNNLS), Vol.27, no.9, Sept. 2016.

J7. [JETCAS'15] K. Roy, D. Fan, X. Fong, Y. Kim, M. Sharad, S. Paul, S. Chatterjee, S. Bhunia, and S. Mukhopadhyay "Exploring Spin Transfer Torque Devices for Unconventional Computing", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems* (JETCAS), Vol. 5, No. 1, March 2015

J6. [TNANO'15] D. Fan, Y. Shim, A. Raghunathan and K. Roy, "STT-SNN: A Spin-Transfer-Torque Based Non-Linear Soft-Limiting Neuron for Low-Power Artificial Neural Networks," *IEEE Transactions on Nanotechnology* (TNANO), vol. 14, no. 6, pp.1013-1023, June 2015.

J5. [TMAG'15] K Yogendra, D. Fan and K. Roy, "Coupled Spin Torque Nano Oscillators for Low Power Neural Computation", *IEEE Transactions on Magnetics*, Vol.51, no.10, June 2015

J4. [TMAG'15] M. Sharad, D. Fan and K. Roy, "Energy-Efficient and Robust Associative Computing with Injection-Locked Dual Pillar Spin-Torque Oscillators", *IEEE Transactions on Magnetics*, Vol. 51, No. 7, June 2015

J3. [TNANO'14] D. Fan, M. Sharad and K. Roy, "Design and Synthesis of Ultra Low Energy Spin-Memristor Threshold Logic," *IEEE Transaction on Nanotechnology* (TNANO) Vol. 13, No. 3, May, 2014.

J2. [TNANO'14] M. Sharad, D. Fan, and K. Roy, "Energy Efficient Non-Boolean Computing With Spin Neurons and Resistive Memory", *IEEE Transaction on Nanotechnology* (TNANO), vol. 13, No.1, 2014

J1. [JAP'13] M. Sharad, D. Fan and K. Roy, "Spin Neurons: A Possible Path to Energy-Efficient Neuromorphic Computers", *Journal of Applied Physics* (JAP), 114, 234906 (2013)

Conference Proceedings (**83** in total, listed by conference date, **my phd students are labelled with '*'**)

C83. [CVPR'21] Li Yang*, Zhezhi He*, Junshan Zhang and Deliang Fan, "KSM: Fast Multiple Task Adaption via Kernel-wise Soft Mask Learning". IEEE/CVF *Computer Vision and Pattern Recognition* (*CVPR*) June 19-25, 2021 (double blind peer-review, 27% acceptance rate)

C82. [DAC'21] Fan Zhang*, Shaahin Angizi* and Deliang Fan, "Max-PIM: Fast and Efficient Max/Min Searching in DRAM". In: 58th Design Automation Conference (DAC), San Francisco, CA, Dec. 5-9, 2021 (double blind peer-review, 23% acceptance rate) (**Best Paper Nomination**)

C81. [DAC'21] Fan Zhang*, Shaahin Angizi*, Naima Ahmed Fahmi, Wei Zhang and Deliang Fan, "PIM-Quantifier: A Processing-in-Memory Platform for Genome Quantification". In: 58th Design Automation Conference (DAC), San Francisco, CA, Dec. 5-9, 2021(double blind peer-review, 23% acceptance rate)

C80. [DAC'21] Sai Kiran Cherupally, Adnan Rakin*, Shihui Yin, Mingoo Seok, Deliang Fan and Jae-sun Seo. "Leveraging Variability and Aggressive Quantization of In-Memory Computing for Robustness

Improvement of Deep Neural Network Hardware Against Adversarial Input and Weight Attacks". In: 58th Design Automation Conference (DAC), San Francisco, CA, Dec. 5-9, 2021(double blind peer-review, 23% acceptance rate)

C79. [ISCAS'21] Jian Meng, Li Yang*, Xiaochen Peng, Shimeng Yu, Deliang Fan, Jae-Sun Seo, "Structured Pruning of RRAM Crossbars for Efficient In-Memory Computing Acceleration of Deep Neural Networks," IEEE International Symposium on Circuits and Systems (ISCAS), May, 2021

C78. [IRPS'21] Wangxi He, Wonbo Shim, Shihui Yin, Xiaoyu Sun, Deliang Fan, Shimeng Yu, Jae-sun Seo, "Characterization and Mitigation of Relaxation Effects on Multi-level RRAM based In-Memory Computing," IEEE International Reliability Physics Symposium (IRPS), March 21-25, 2021 (**Best Student Paper Candidate**)

C77. [DATE'21] Jingtao Li, Adnan Siraj Rakin*, Zhezhi He*, Deliang Fan and Chaitali Chakrabarti, "RADAR: Run-time Adversarial Weight Attack Detection and Accuracy Recovery," Design, Automation and Test in Europe (DATE), 01-05 Feb. 2021, ALPEXPO, Grenoble, France

C78. [ASPDAC'21] Li Yang* and Deliang Fan, "Dynamic Neural Network to Enable Run-Time Trade-off between Accuracy and Latency", 26th Asia and South Pacific Design Automation Conference (ASPDAC), Jan. 18-21, 2021 (invited special session)

C75. [SOCC'20] Li Yang*, Zhezhi He*, Shaahin Angizi* and Deliang Fan, "Processing-In-Memory Accelerator for Dynamic Neural Network with Run-Time Tuning of Accuracy, Power and Latency", 33rd IEEE International System-on-Chip Conference (SOCC), September 8-11, 2020 (invited)

C74. [USENIX Security'20] Fan Yao, Adnan Siraj Rakin* and Deliang Fan, "DeepHammer: Depleting the Intelligence of Deep Neural Networks through Targeted Chain of Bit Flips," In 29th USENIX Security Symposium (USENIX Security 20), August 12-14, 2020, Boston, MA, USA (double blind peer-review, 157/977=16.1% acceptance rate)

C73. [ISLPED'20] Mingyen Lee, Wenjun Tang, Bowen Xue, Juejian Wu, Mingyuan Ma, Yu Wang, Yongpan Liu, Deliang Fan, Vijaykrishnan Narayanan, Huazhong Yang and Xueqing Li, "FeFET-Based Low-Power Bitwise Logic-in-Memory with Direct Write-Back and Data-Adaptive Dynamic Sensing Interface", ACM/IEEE International Symposium on Low Power Electronics and Design, August 10-12, 2020 (double blind peer-review, 23% acceptance rate)

C72. [GLSVLSI'20] Shaahin Angizi*, Wei Zhang and Deliang Fan, "Exploring DNA Alignment-in-Memory Leveraging EmergingSOT-MRAM", 30th edition of the ACM Great Lakes Symposium on VLSI (*GLSVLSI*), September 7-9, 2020 (invited)

C71. [GLSVLSI'20] Adnan Siraj Rakin*, Zhezhi He*, Li Yang*, Yanzhi Wang, Liqiang Wang, Deliang Fan, "Robust Sparse Regularization: Simultaneously Optimizing Neural Network Robustness and Compactness", 30th edition of the ACM Great Lakes Symposium on VLSI (*GLSVLSI*), September 7-9, 2020 (invited)

C70. [GLSVLSI'20] Baogang Zhang, Necati Uysal, Deliang Fan and Rickard Ewetz, "Redundant Neurons and Shared Redundant Synapses for Robust Memristor-based DNNs with Reduced Overhead", 30th edition of the ACM Great Lakes Symposium on VLSI (*GLSVLSI*), September 7-9, 2020

C69. [GLSVLSI'20] Dayane Reis, Di Gao, Shaahin Angizi*, Xunzhao Yin, Deliang Fan, Michael Niemier, Cheng Zhuo and X. Sharon Hu, "Modeling and benchmarking computing-in-memory for design space exploration", 30th edition of the ACM Great Lakes Symposium on VLSI (*GLSVLSI*), September 7-9, 2020 (invited)

C68. [CVPR'20] Adnan Siraj Rakin*, Zhezhi He* and Deliang Fan, "TBT: Targeted Neural Network Attack

with Bit Trojan," 2020 IEEE/CVF Conference on Computer Vision and Pattern Recognition (*CVPR*), June 16-20, 2020, Seattle, Washington, USA (double blind peer-review, 22% acceptance rate)

C67. [CVPR'20] Zhezhi He*, Adnan Siraj Rakin*, Jingtao Li, Chaitali Chakrabarti and Deliang Fan, "Defending and Harnessing the Bit-Flip based Adversarial Weight Attack," 2020 IEEE/CVF Conference on Computer Vision and Pattern Recognition (*CVPR*), June 16-20, 2020, Seattle, Washington, USA (double blind peer-review, 22% acceptance rate)

C66. [DAC'20] Li Yang*, Zhezhi He*, Yu Cao and Deliang Fan. "Non-uniform DNN Structured Subnets Sampling for Dynamic Inference". In: 57th Design Automation Conference (DAC), San Francisco, CA, July 19-23, 2020 (double blind peer-review, 228/991=23.0% acceptance rate)

C65. [DAC'20] Shaahin Angizi*, Naima Ahmed Fahmi, Wei Zhang and Deliang Fan, "PIM-Assembler: A Processing-in-Memory Platform for Genome Assembly" In: 57th Design Automation Conference (DAC), San Francisco, CA, July 19-23, 2020 (double blind peer-review, 228/991=23.0% acceptance rate)

C64. [DAC'20] Jingtao Li, Adnan Siraj Rakin*, Yan Xiong, Liangliang Chang, Zhezhi He*, Deliang Fan, and Chaitali Chakrabarti. "Defending Bit-Flip Attack through DNN Weight Reconstruction". In: 57th Design Automation Conference (DAC), San Francisco, CA, July 19-23, 2020. (double blind peer-review, 228/991=23.0% acceptance rate)

C63. [AAAI'20] Li Yang*, Zhezhi He* and Deliang Fan, "Harmonious Coexistence of Structured Weight Pruning and Ternarization for Deep Neural Networks," *Thirty-Fourth AAAI Conference on Artificial Intelligence* (AAAI), Feb. 7-12 2020, New York, USA (double blind peer-review, 1591/7737=20.6% acceptance rate) (**Spotlight**)

C62. [DATE'20] Shaahin Angizi*, Jiao Sun, Wei Zhang and Deliang Fan, "PIM-Aligner: A Processing-in-MRAM Platform for Biological Sequence Alignment," *Design, Automation and Test in Europe* (DATE), 09-13 March 2020, ALPEXPO, Grenoble, France (6 pages) (double blind peer-review, 26% acceptance rate)

C61. [ASPDAC'20] Li Yang*, Shaahin Angizi*, Deliang Fan, "A Flexible Processing-in-Memory Accelerator for Dynamic Channel-Adaptive Deep Neural Networks," Asia and South Pacific Design Automation Conference (ASP-DAC), Jan. 13-16, 2020, Beijing, China (6 pages) (double blind peer-review, 86/279=30% acceptance rate)

C60. [ASPDAC'20] Baogang Zhang, Necati Uysal, Deliang Fan, Rickard Ewetz, "Representable Matrices: Enabling High Accuracy Analog Computation for Inference of DNNs using Memristors," Asia and South Pacific Design Automation Conference (ASP-DAC), Jan. 13-16, 2020, Beijing, China (6 pages) (double blind peer-review, 86/279=30% acceptance rate)

C59. [ICCV'19] Adnan Siraj Rakin*[$], Zhezhi He*[$], Deliang Fan, "Bit-Flip Attack: Crushing Neural Network with Progressive Bit Search," IEEE International Conference on Computer Vision, Seoul, Korea, Oct 27 - Nov 3, 2019 ([$]the first two authors contribute equally) (10 pages) (double blind peer-review, 1075/4303=25% acceptance rate)

C58. [ICCAD'19] Shaahin Angizi* and Deliang Fan, "ReDRAM: A Reconfigurable Processing-in-DRAM Platform for Accelerating Bulk Bit-Wise Operations," IEEE/ACM International Conference on Computer-Aided Design, 4-7 November 2019, Westminster, CO (8 pages) (double blind peer-review, 24% acceptance rate)

C57. [NANOARCH'19] Shaahin Angizi* and Deliang Fan, "Deep Neural Network Acceleration in Non-Volatile Memory: A Digital Approach?," IEEE/ACM International Symposium on Nanoscale

Architectures, 17-19 July 2019, Qingdao, CHINA (6 pages)

C56. [ISVLSI'19] Shaahin Angizi*, Zhezhi He*, Dayane Reis, Xiaobo Sharon Hu, Wilman Tsai, Shy Jay Lin and Deliang Fan, "Accelerating Deep Neural Networks in Processing-in-Memory Platforms: Analog or Digital Approach?," IEEE Computer Society Annual Symposium on VLSI, 15-17 July 2019, Miami, Florida, USA (6 pages) (double blind peer-review, 35% acceptance rate)

C55. [ISVLSI'19] Adnan Siraj Rakin* and Deliang Fan, "Defense-Net: Defend Against a Wide Range of Adversarial Attacks through Adversarial Detector," IEEE Computer Society Annual Symposium on VLSI, 15-17 July 2019, Miami, Florida, USA (6 pages) (double blind peer-review, 35% acceptance rate)

C54. [Dagstuhl Report'19] Deliang Fan, "Cognitive Computing-in-Memory: Circuit to Algorithm," Dagstuhl Seminar 19152, Emerging Hardware Techniques and EDA Methodologies for Neuromorphic Computing, Germany, 2019 (2 pages, invited)

C53. [DRC'19] Durjoy Dev, Adithi Krishnaprasad, Zhezhi He*, Sonali Das, Mashiyat Sumaiya Shawkat, Madison Manley, Olaleye Aina, Deliang Fan, Yeonwoong Jung and Tania Roy, "Artificial Neuron using Ag/2D-MoS2/Au Threshold Switching Memristor," 77th Device Research Conference, 23 - 26 June 2019, University of Michigan, Ann Arbor (2 pages)

C52. [CVOPS'19] Yifan Ding, Liqiang Wang, Huan Zhang, Jinfeng Yi, Deliang Fan, and Boqing Gong, "Defending Against Adversarial Attacks Using Random Forests" Workshop on The Bright and Dark Sides of Computer Vision: Challenges and Opportunities for Privacy and Security, Long Beach, CA, USA, 2019 (10 pages)

C51. [CVPR'19] Zhezhi He*$^{\$}$, Adnan Siraj Rakin*$^{\$}$ and Deliang Fan, "Parametric Noise Injection: Trainable Randomness to Improve Deep Neural Network Robustness against Adversarial Attack," Conference on Computer Vision and Pattern Recognition (CVPR), June 16-20, 2019, Long Beach, CA, USA ($^{\$}$the first two authors contribute equally) (double blind peer-review, 25% acceptance rate) (10 pages)

C50. [CVPR'19] Zhezhi He* and Deliang Fan, "Simultaneously Optimizing Weight and Quantizer of Ternary Neural Network using Truncated Gaussian Approximation," Conference on Computer Vision and Pattern Recognition (CVPR), June 16-20, 2019, Long Beach, CA, USA (double blind peer-review, 25% acceptance rate) (9 pages)

C49. [DAC'19] Shaahin Angizi*, Jiao Sun, Wei Zhang and Deliang Fan, "AlignS: A Processing-In-Memory Accelerator for DNA Short Read Alignment Leveraging SOT-MRAM," *Design Automation Conference* (DAC), June 2-6, 2019, Las Vegas, NV, USA (6 pages) (double blind peer-review, 202/815=24.8% acceptance rate)

C48. [DAC'19] Zhezhi He*, Jie Lin, Rickard Ewetz, Jiann-Shiun Yuan and Deliang Fan, "Noise Injection Adaption: End-to-End ReRAM Crossbar Non-ideal Effect Adaption for Neural Network Mapping," *Design Automation Conference* (DAC), June 2-6, 2019, Las Vegas, NV, USA (6 pages) (double blind peer-review, 202/815=24.8% acceptance rate)

C47. [GLSVLSI'19] Shaahin Angizi* and Deliang Fan, "GraphiDe: A Graph Processing Accelerator leveraging In-DRAM-Computing," ACM Great Lakes Symposium on VLSI (GLSVLSI), May 9-11, 2019, Washington, D.C. USA (double blind peer-review, 29% acceptance rate) (6 pages) (**Best Paper Award**)

C46. [GLSVLSI'19] Li Yang*, Zhezhi He* and Deliang Fan, "Binarized Depthwise Separable Neural Network for Object Tracking in FPGA," ACM Great Lakes Symposium on VLSI (GLSVLSI), May 9-11, 2019, Washington, D.C. USA (6 pages) (double blind peer-review, 29% acceptance rate)

C45. [ISQED'19] Arman Roohi, Shaahin Angizi*, Deliang Fan and Ronald F DeMara, "Processing-In-Memory Acceleration of Convolutional Neural Networks for Energy-Efficiency and Power-Intermittency Resilience," The 20th *International Symposium on Quality Electronic Design* (ISQED), March 6-7, 2019, Santa Clara, CA, USA (6 pages) (**Best Paper Candidate**)

C44. [DATE'19] Shaahin Angizi*, Jiao Sun, Wei Zhang and Deliang Fan, "GraphS: A Graph Processing Accelerator Leveraging SOT-MRAM," *Design, Automation and Test in Europe* (DATE), March 25-29, 2019, Florence, Italy (6 pages) (double blind peer-review, 24% acceptance rate)

C43. [WACV'19] Zhezhi He*, Boqing Gong, Deliang Fan, "Optimize Deep Convolutional Neural Network with Ternarized Weights and High Accuracy," *IEEE Winter Conference on Applications of Computer Vision*, January 7-11, 2019, Hawaii, USA (9 pages)

C42. [ASPDAC'19] Shaahin Angizi*, Zhezhi He* and Deliang Fan, "ParaPIM: a parallel processing-in-memory accelerator for binary-weight deep neural networks," Asia and South Pacific Design Automation Conference (ASP-DAC), Jan. 21-23, 2019, Tokyo, Japan (6 pages) (double blind peer-review, 35% acceptance rate)

C41. [ASPDAC'19] Baogang Zhang, Necati Uysal, Deliang Fan and Rickard Ewetz, "Handling Stuck-at-faults in Memristor Crossbar Arrays using Matrix Transformations," Asia and South Pacific Design Automation Conference (ASP-DAC), Jan. 21-24, 2019, Tokyo, Japan (**Best Paper Candidate**) (6 pages) (double blind peer-review, 35% acceptance rate)

C40. [ICCD'18] Adnan Siraj Rakin*, Shaahin Angizi*, Zhezhi He* and Deliang Fan, "PIM-TGAN: A Processing-in-Memory Accelerator for Ternary Generative Adversarial Networks," *IEEE International Conference on Computer Design* (ICCD), Oct. 7-10, 2018, Orlando, FL, USA

C39. [ICCAD'18] Shaahin Angizi*, Zhezhi He* and Deliang Fan, "DIMA: A Depthwise CNN In-Memory Accelerator," *IEEE/ACM International Conference on Computer Aided Design* (ICCAD), Nov. 5-8, 2018, San Diego, CA, USA (double blind peer-review, 98/396=25% acceptance rate)

C38. [ISLPED'18] Li Yang*, Zhezhi He* and Deliang Fan, "A Fully Onchip Binarized Convolutional Neural Network FPGA Implementation with Accurate Inference," ACM/IEEE International Symposium on Low Power Electronics and Design, July 23-25, 2018, Bellevue, Washington, USA (double blind peer-review, 23.3% acceptance rate)

C37. [ISVLSI'18] Zhezhi He*, Shaahin Angizi*, Adnan Siraj Rakin* and Deliang Fan, "BD-NET: A Multiplication-less DNN with Binarized Depthwise Separable Convolution," *IEEE Computer Society Annual Symposium on VLSI*, July 9-11, 2018, Hong Kong, CHINA (double blind peer-review, 57/192=29% acceptance rate) (**Best Paper Award,** one out of 57 accepted papers)

C36. [ISVLSI'18] Zhezhi He*, Shaahin Angizi* and Deliang Fan, "Accelerating Low Bit-Width Deep Convolution Neural Network in MRAM," *IEEE Computer Society Annual Symposium on VLSI*, July 9-11, 2018, Hong Kong, CHINA (invited special session)

C35. [GLSVLSI'18] Shaahin Angizi*, Zhezhi He*, Yu Bai, Jie Han, Mingjie Lin and Deliang Fan, "Leveraging Spintronic Devices for Efficient Approximate Logic and Stochastic Neural Network," *ACM Great Lakes Symposium on VLSI*, Chicago, IL, USA, May 23-25, 2018 (invited)

C34. [DAC'18] Shaahin Angizi*[$], Zhezhi He*[$], Adnan Siraj Rakin and Deliang Fan, "CMP-PIM: An Energy-Efficient Comparator-based Processing-In-Memory Neural Network Accelerator," IEEE/ACM *Design Automation Conference*, June 24-28, 2018, San Francisco, CA, USA ([$] The first two authors contributed equally) (double blind peer-review, 168/691=24.3% acceptance rate)

C33. [DAC'18] Shaahin Angizi*, Zhezhi He* and Deliang Fan, "PIMA-Logic: A Novel

Processing-in-Memory Architecture for Highly Flexible and Energy-Efficient Logic Computation," IEEE/ACM *Design Automation Conference*, June 24-28, 2018, San Francisco, CA, USA (double blind peer-review, 168/691=24.3% acceptance rate)

C32. [WACV'18] Y. Ding, L. Wang, D. Fan and B. Gong "A Semi-Supervised Two-Stage Approach to Learning from Noisy Labels," *IEEE Winter Conference on Applications of Computer Vision*, March 12-14, 2018, Stateline, NV, USA

C31. [ASPDAC'18] F. Parveen*, Z. He*, S. Angizi* and D. Fan, "HieIM: Highly Flexible In-Memory Computing using STT MRAM," Asia and South Pacific Design Automation Conference, Jan. 22-25, 2018, Jeju Island, Korea (double blind peer-review, 31% acceptance rate)

C30. [ASPDAC'18] S. Angizi*, Z. He*, F. Parveen* and D. Fan, "IMCE: Energy-Efficient Bit-Wise In-Memory Convolution Engine for Deep Neural Network," Asia and South Pacific Design Automation Conference, Jan. 22-25, 2018, Jeju Island, Korea (double blind peer-review, 31% acceptance rate)

C29. [ICCD'17] Z. He*, S. Angizi* and D. Fan, "Exploring STT-MRAM based In-Memory Computing Paradigm with Application of Image Edge Extraction," IEEE International Conference on Computer Design, Nov. 5-8, 2017, Boston, MA (double blind peer-review, 29% acceptance rate)

C28. [ICCD'17] D. Fan and S. Angizi* "Energy Efficient In-Memory Binary Deep Neural Network Accelerator with Dual-Mode SOT-MRAM," *IEEE International Conference on Computer Design*, Nov. 5-8, 2017, Boston, MA (double blind peer-review, 29% acceptance rate)

C27. [ICCAD'17] M. Yang, J. Hayes, D. Fan, W. Qian, "Design of Accurate Stochastic Number Generators with Noisy Emerging Devices for Stochastic Computing," IEEE/ACM International Conference on Computer Aided Design, Nov 13-16, 2017, Irvin, CA (double blind peer-review, 105/399=26% acceptance rate)

C26. [NCAMA'17] S. Angizi* and D. Fan, "IMC: Energy-Efficient In-Memory Convolver for Accelerating Binarized Deep Neural Network," *Neuromorphic Computing Symposium: Architectures, Models, and Applications*, July 17-19, 2017, Knoxville, Tennessee

C25. [NANOARCH'17] Z. He*, S. Angizi*, F. Parveen* and D. Fan, "High Performance and Energy-Efficient In-Memory Computing Architecture based on SOT-MRAM," *IEEE/ACM International Symposium on Nanoscale Architectures*, July 25-26, 2017, Newport, USA

C24. [ISVLSI'17] D. Fan, S. Angizi*, and Z. He*, "In-Memory Computing with Spintronic Devices," *IEEE Computer Society Annual Symposium on VLSI*, July 3-5, 2017, Bochum, Germany (invited)

C23. [ISVLSI'17] S. Angizi*, Z. He* and D. Fan, "RIMPA: A New Reconfigurable Dual-Mode In-Memory Processing Architecture with Spin Hall Effect-Driven Domain Wall Motion Device," *IEEE Computer Society Annual Symposium on VLSI*, July 3-5, 2017, Bochum, Germany

C22. [ISVLSI'17] F. Parveen*, Z. He*, S. Angizi*, and D. Fan, "Hybrid Polymorphic Logic Gate with 5-Terminal Magnetic Domain Wall Motion Device," *IEEE Computer Society Annual Symposium on VLSI*, July 3-5, 2017, Bochum, Germany (**Best Paper Award**)

C21. [ISLPED'17] F. Parveen*, S. Angizi*, Z. He* and D. Fan "Low Power In-Memory Computing based on Dual-Mode SOT-MRAM," *IEEE/ACM International Symposium on Low Power Electronics and Design*, July 24-26, 2017, Taipei, Taiwan (double blind peer-review, 24% acceptance rate)

C20. [MWSCAS'17] D. Fan, Z. He* and S. Angizi*, "Leveraging Spintronic Devices for Ultra-Low Power In-Memory Computing: Logic and Neural Network," *60th IEEE International Midwest Symposium on Circuits and Systems, Aug.* 6-9, 2017, Boston, MA, USA (invited)

C19. [ISCAS'17] F. Parveen*, S. Angizi*, Z. He* and D. Fan, "Hybrid Polymorphic Logic Gate Using 6

Terminal Magnetic Domain Wall Motion Device," *IEEE International Symposium on Circuits & Systems*, Baltimore, MD, USA, May 28-31, 2017

C18. [DATE'17] Z. He*, D. Fan, "A Tunable Magnetic Skyrmion Neuron Cluster for Energy Efficient Artificial Neural Network," *Design, Automation and Test in Europe*, Lausanne, Switzerland, 27-31, March, 2017 (double blind peer-review, 23% acceptance rate)

C17. [GLSVLSI'17] Z. He*, S. Angizi*, F. Parveen*, and D. Fan, "Leveraging Dual-Mode Magnetic Crossbar for Ultra-low Energy In-Memory Data Encryption", *27th ACM Great Lakes Symposium on VLSI*, Banff, Alberta, Canada, May 10-12, 2017 (double blind peer-review, 48/197=24.4% acceptance rate)

C16. [GLSVLSI'17] S. Angizi*, Z. He*, and D. Fan, "Energy Efficient In-Memory Computing Platform Based on 4-Terminal Spin Hall Effect-Driven Domain Wall Motion Devices", *27th ACM Great Lakes Symposium on VLSI*, Banff, Alberta, Canada, May 10-12, 2017 (double blind peer-review, 48/197=24.4% acceptance rate)

C15. [GLSVLSI'17] Q. Alasad, J. Yuan, and D. Fan, "Leveraging All-Spin Logic to Improve Hardware Security", 27th *ACM Great Lakes Symposium on VLSI*, Banff, Alberta, Canada, May 10-12, 2017 (double blind peer-review, 48/197=24.4% acceptance rate)

C14. [ISQED'17] S. Angizi*, Z. He*, R. DeMara and D. Fan, "Composite Spintronic Accuracy-Configurable Adder for Low Power Digital Signal Processing," *18th International Symposium on Quality Electronic Design*, Santa Clara, CA, USA, 13-15 March, 2017

C13. [ISLPED'16] Z. He*, D. Fan, "A Low Power Current-Mode Flash ADC with Spin Hall Effect based Multi-Threshold Comparator," *International Symposium on Low Power Electronics and Design*, San Francisco, CA, Aug. 8-10, 2016 (double blind peer-review, 23% acceptance rate)

C12. [NANOARCH'16] D. Fan, "Low Power In-Memory Computing Platform with Four Terminal Magnetic Domain Wall Motion Devices," *IEEE/ ACM International Symposium on Nanoscale Architectures*, Beijing, China, July 18-20, 2016

C11. [GLSVLSI'16] D. Fan, "Ultra-Low Energy Reconfigurable Spintronic Threshold Logic Gate", *26th ACM Great Lakes Symposium on VLSI*, Boston, Massachusetts, May 18-20, 2016

C10. [IJCNN'16] C. Liyanagedera, K. Yogendra, K. Roy and D. Fan, "Spin Torque Nano-Oscillator based Oscillatory Neural Network," *2016 IEEE International Joint Conference on Neural Network*, Vancouver, Canada, July 24-29, 2016

C9. [ASPDAC'16] K. Yogendra, D. Fan, Y. Shim, M. Koo, and K. Roy, "Computing with Coupled Spin Torque Nano Oscillators", *21st Asia and South Pacific Design Automation Conference*, pp.312-317, Macao, China, Jan. 25-28, 2016 (double blind peer-review, 94/274=34.3% acceptance rate)

C8. [ASPDAC'16] Abhronil Sengupta, Karthik Yogendra, Deliang Fan, Kaushik Roy, "Prospects of efficient neural computing with arrays of magneto-metallic neurons and synapses," *21st Asia and South Pacific Design Automation Conference*, Macao, China, pp. 115-120, Jan. 25-28, 2016 (double blind peer-review, 94/274=34.3% acceptance rate)

C7. [DATE'14] K. Roy, M. Sharad, D. Fan and K. Yogendra, "Brain-inspired computing with spin torque devices", *Design, Automation & Test in Europe*, Dresden, Germany, March 24-28, 2014. (invited tutorial)

C6. [ISVLSI'14] K. Roy, M. Sharad, D. Fan and K. Yogendra, "Computing with Spin-Transfer-Torque Devices: Prospects and Perspectives," IEEE Computer Society Annual Symposium on VLSI, Tampa, FL, July 9-11, 2014

C5. [DAC'13] M. Sharad, D. Fan, and K. Roy, "Ultra Low Power Associative Computing With Spin Neurons and Resistive Crossbar Memory," IEEE/ACM *Design Automation Conference*, Austin, TX, June 2-6, 2013

C4. [ISLPED'13] K. Roy, M. Sharad, D. Fan, and K. Yogendra, "Beyond Charge-Base Computing: Boolean and Non Boolean computing Using spin Devices", *International Symposium on Low Power and Design* (ISLPED), Beijing, China, Sept.4-6, 2013.

C3. [ICCAD'13] K. Roy, M. Sharad, D. Fan, and K. Yogendra, "Exploring Boolean and Non Boolean Computing Using Spin torque Switches", *International Conference on Computer-Aided Design* (ICCAD), San Jose, CA, Nov. 18-21, 2013. (invited tutorial)

C2. [ISQED'13] M. Sharad, D. Fan, and K. Roy, "Low Power and Compact Mixed-Mode Signal Processing Hardware using Spin-Neurons," IEEE *International Symposium on Quality Electronic Design*, Santa Clara, CA, March 4-6, 2013

C1. [E3S'13] M. Sharad, D. Fan, K. Yogendra, and K. Roy, "Ultra-Low Power Neuromorphic Computing with Spin-Torque Devices", *3rd Berkeley Symposium on Energy Efficient Electronic Systems*, Berkeley, CA, Oct.28-29, 2013

RESEARCH PRESENTATIONS AND INVITED TALKS

44. "Secure and Efficient Deep Learning Computing System -A Software and Hardware Co-Design Perspective", Invited talk by Rutgers University, March 11, 2021
43. "Energy Efficient and Intelligent Processing-in-Memory for Data-Intensive Applications - From Device to Algorithm", Invited talk in The *State University of New York*, Feb. 19, 2021
42. "Energy Efficient and Intelligent Processing-in-Memory for Data-Intensive Applications - From Device to Algorithm", Invited talk by Samsung, December 17, 2020
41. "Secure and Efficient Deep Learning Computing System -A Software and Hardware Co-Design Perspective", Invited talk by Mitsubishi Electric Research Laboratories, Nov. 02, 2020
40. "Energy Efficient Processing-in-Memory, From Circuits to Algorithms", Workshop on Computing with Unconventional Technologies, Oct. 19, 2020
39. "Toward New Era of Compute-in-Memory: Software-Hardware Co-Design for Data-Intensive Applications", In: 57th Design Automation Conference (DAC) Tutorial, July 20, 2020
38. "Non-uniform DNN Structured Subnets Sampling for Dynamic Inference". In: 57th Design Automation Conference (DAC), San Francisco, CA, July 19-23, 2020
37. "PIM-Assembler: A Processing-in-Memory Platform for Genome Assembly" In: 57th Design Automation Conference (DAC), San Francisco, CA, July 19-23, 2020
36. "PIM-Aligner: A Processing-in-MRAM Platform for Biological Sequence Alignment," *Design, Automation and Test in Europe* (DATE), 09-13 March 2020, ALPEXPO, Grenoble, France
35. "A Flexible Processing-in-Memory Accelerator for Dynamic Channel-Adaptive Deep Neural Networks," *Asia and South Pacific Design Automation Conference* (ASP-DAC), Jan. 13-16, 2020, Beijing, China
35. "Energy Efficient Deep Neural Network Processing-In-MRAM: From Device to Algorithm," *Emerging Memory and Artificial Intelligence Workshop*, 29, August, 2019, Stanford University, CA
34. "Deep Neural Network Acceleration in Non-Volatile Memory: A Digital Approach?," IEEE/ACM International Symposium on Nanoscale Architectures, 17-19 July 2019, Qingdao, CHINA
33. "Accelerating Deep Neural Networks in Processing-in-Memory Platforms: Analog or Digital Approach?," IEEE Computer Society Annual Symposium on VLSI, 15-17 July 2019, Miami, Florida,

USA

32. "GraphiDe: A Graph Processing Accelerator leveraging In-DRAM-Computing," ACM Great Lakes Symposium on VLSI (GLSVLSI), May 9-11, 2019, Washington, D.C. USA
31. "Neuromorphic/Cognitive Computing-in-Memory: Circuit and Algorithm," Dagstuhl Neuromorphic Computing Seminar, April 8-10, Warden, Germany, 2019
30. "GraphS: A Graph Processing Accelerator Leveraging SOT-MRAM," *Design, Automation and Test in Europe* (DATE), March 25-29, 2019, Florence, Italy
29. "Intelligent and Energy Efficient Big Data Processing-in-Memory: From Device to Algorithm," SRC nCore eWorkShop, February 12, 2019
28. "PIM-TGAN: A Processing-in-Memory Accelerator for Ternary Generative Adversarial Networks," *IEEE International Conference on Computer Design* (ICCD) , Oct. 7-10, 2018, Orlando, FL, USA
27. "BD-NET: A Multiplication-less DNN with Binarized Depthwise Separable Convolution," *IEEE Computer Society Annual Symposium on VLSI*, July 9-11, 2018, Hong Kong, CHINA
26. Accelerating Low Bit-Width Deep Convolution Neural Network in MRAM," *IEEE Computer Society Annual Symposium on VLSI*, July 9-11, 2018, Hong Kong, CHINA (invited talk)
25. "CMP-PIM: An Energy-Efficient Comparator-based Processing-In-Memory Neural Network Accelerator," IEEE/ACM Design Automation Conference (DAC), June 24-28, 2018, San Francisco, CA, USA
24. "HieIM: Highly Flexible In-Memory Computing using STT MRAM," Asia and South Pacific Design Automation Conference (ASP-DAC), Jan. 22-25, 2018, Jeju Island, Korea
23. "MCE: Energy-Efficient Bit-Wise In-Memory Convolution Engine for Deep Neural Network," Asia and South Pacific Design Automation Conference (ASP-DAC), Jan. 22-25, 2018, Jeju Island, Korea
22. "Exploring STT-MRAM based In-Memory Computing Paradigm with Application of Image Edge Extraction," IEEE International Conference on Computer Design (ICCD), Nov. 5-8, 2017, Boston, MA
21. "Energy Efficient In-Memory Binary Deep Neural Network Accelerator with Dual-Mode SOT-MRAM," *IEEE International Conference on Computer Design (ICCD)* , Nov. 5-8, 2017, Boston, MA
20. "Leveraging Spintronic Devices for Ultra-Low Power In-Memory Computing: Logic and Neural Network," *60th IEEE International Midwest Symposium on Circuits and Systems, Aug.* 6-9, 2017, Boston, MA, USA
19. "Leveraging Spintronic Devices for Ultra-Low Power In-Memory Computing: Non-Volatile Memory, Logic and Neural Network," Ningbo University, Ningbo, CHINA, July 29th, 2017
18. "Leveraging Spintronic Devices for Ultra-Low Power In-Memory Computing: Non-Volatile Memory, Logic and Neural Network," Shanghai Jiaotong University, Shanghai, CHINA, July 28th, 2017
17. "Leveraging Spintronic Devices for Ultra-Low Power In-Memory Computing: Non-Volatile Memory, Logic and Neural Network," Zhejiang University, Hangzhou, CHINA, July 27th, 2017
16. "IMC: Energy-Efficient In-Memory Convolver for Accelerating Binarized Deep Neural Network," *Neuromorphic Computing Symposium: Architectures, Models, and Applications* , July 17-19, 2017, Knoxville, Tennessee
15. "From Biological Spike to Topological Skyrmion: Developing All-Skyrmion Spiking Neural Network," *Neuromorphic Computing Symposium: Architectures, Models, and Applications* , July 17-19, 2017, Knoxville, Tennessee
14. "In-Memory Computing with Spintronic Devices," *IEEE Computer Society Annual Symposium on VLSI*,

July 3-5, 2017, Bochum, Germany

13. "RIMPA: A New Reconfigurable Dual-Mode In-Memory Processing Architecture with Spin Hall Effect-Driven Domain Wall Motion Device," *IEEE Computer Society Annual Symposium on VLSI,* July 3-5, 2017, Bochum, Germany
12. "Hybrid Polymorphic Logic Gate with 5-Terminal Magnetic Domain Wall Motion Device," *IEEE Computer Society Annual Symposium on VLSI,* July 3-5, 2017, Bochum, Germany
11. "Neuromorphic Computing With Spintronic Devices: From Device to Architecture", ACM/IEEE System Level Interconnect Prediction 2017 workshop, Austin, TX, June 17, 2017
10. "Energy Efficient In-Memory Computing Platform Based on 4-Terminal Spin Hall Effect-Driven Domain Wall Motion Devices", 27th GLSVLSI, Banff, Alberta, Canada, May 10-12, 2017
9. "Leveraging Dual-Mode Magnetic Crossbar for Ultra-low Energy In-Memory Data Encryption", 27th GLSVLSI, Banff, Alberta, Canada, May 10-12, 2017
8. "A Tunable Magnetic Skyrmion Neuron Cluster for Energy Efficient Artificial Neural Network," Design, Automation and Test in Europe (DATE), Lausanne, Switzerland, 27-31 March, 2017
7. "Composite Spintronic Accuracy-Configurable Adder for Low Power Digital Signal Processing", International Symposium on Quality Electronic Design, Santa Clara, CA, USA, 13-15 March, 2017
6. "Low Power In-Memory Computing Platform with Four Terminal Magnetic Domain Wall Motion Devices," *IEEE/ ACM International Symposium on Nanoscale Architectures,* Beijing, China, July 18-20, 2016
5. "Brain Inspired And Non-Boolean Computing with Spin-Transfer Torque Devices," University of Central Florida, Orlando, FL, February 19, 2015
4. "Brain Inspired And Non-Boolean Computing with Spin-Transfer Torque Devices," Shanghai Tech University, Shanghai, China, April 14, 2015
3. "Computing With Spin-Transfer-Torque Devices: Prospects and Perspectives," IEEE Computer Society Annual Symposium on VLSI, University of South Florida, Tampa, FL, July 9, 2014
2. "Nano-Oscillators and CMOS Interface Circuits for Associative Computing Module," DARPA-UPSIDE Project Review, HRL Laboratories, Malibu, CA, April/ Aug/ Sept - 2014, March – 2015
1. "Ultra-Low Power Neuromorphic Computing With Spin-Torque Devices," 3rd Berkeley Symposium on Energy Efficient Electronic Systems, University of California, Berkeley, CA, Oct. 28, 2013

RESEARCH POSTERS

18. Li Yang, Zhezhi He and Deliang Fan, "Harmonious Coexistence of Structured Weight Pruning and Ternarization for Deep Neural Networks," *Thirty-Fourth AAAI Conference on Artificial Intelligence* (AAAI), Feb. 7-12 2020, New York, USA
17. Adnan Siraj Rakin, Zhezhi He, Deliang Fan, "Bit-Flip Attack: Crushing Neural Network with Progressive Bit Search," IEEE International Conference on Computer Vision, Seoul, Korea, Oct 27 - Nov 3, 2019
16. "Defense-Net: Defend Against a Wide Range of Adversarial Attacks through Adversarial Detector," IEEE Computer Society Annual Symposium on VLSI, 15-17 July 2019, Miami, Florida, USA
15. "Parametric Noise Injection: Trainable Randomness to Improve Deep Neural Network Robustness against Adversarial Attack," Conference on Computer Vision and Pattern Recognition (CVPR), June 16-20, 2019, Long Beach, CA, USA
14. "Simultaneously Optimizing Weight and Quantizer of Ternary Neural Network using Truncated

Gaussian Approximation," Conference on Computer Vision and Pattern Recognition (CVPR), June 16-20, 2019, Long Beach, CA, USA

13. "Binarized Depthwise Separable Neural Network for Object Tracking in FPGA," ACM Great Lakes Symposium on VLSI (GLSVLSI), May 9-11, 2019, Washington, D.C. USA
12. "Optimize Deep Convolutional Neural Network with Ternarized Weights and High Accuracy," *IEEE Winter Conference on Applications of Computer Vision*, January 7-11, 2019, Hawaii, USA
11. "A Fully Onchip Binarized Convolutional Neural Network FPGA Implementation with Accurate Inference," *ACM/IEEE International Symposium on Low Power Electronics and Design*, July 23-25, 2018, Bellevue, Washington, USA
10. "CMP-PIM: An Energy-Efficient Comparator-based Processing-In-Memory Neural Network Accelerator," IEEE/ACM Design Automation Conference (DAC), June 24-28, 2018, San Francisco, CA, USA
9. "PIMA-Logic: A Novel Processing-in-Memory Architecture for Highly Flexible and Energy-Efficient Logic Computation," IEEE/ACM Design Automation Conference (DAC), June 24-28, 2018, San Francisco, CA, USA
8. "Accelerating Binarized Convolutional Neural Network Using Spin-based In-Memory Processing," IBM CAS Emerging Technology symposium, IBM T.J. Watson Research Center, Yorktown, New York, Oct. 5th, 2017
7. "Low Power In-Memory Computing based on Dual-Mode SOT-MRAM," *IEEE/ACM International Symposium on Low Power Electronics and Design*, July 24-26, 2017, Taipei, Taiwan
6. "Hybrid Polymorphic Logic Gate with 5-Terminal Magnetic Domain Wall Motion Device for Hardware Security," Design Automation Conference, Austin, TX, June 18-22, 2017
5. "RIMPA: A New Reconfigurable In-Memory Processing Architecture with Spin Hall Effect Driven Domain Wall Motion Device," Design Automation Conference, Austin, TX, June 18-22, 2017
4. "A Low Power Current-Mode Flash ADC with Spin Hall Effect based Multi-Threshold Comparator," *International Symposium on Low Power Electronics and Design (ISLPED)*, San Francisco, CA, Aug. 8-10, 2016
3. "Low Power In-Memory Computing Platform with Four Terminal Magnetic Domain Wall Motion Devices," ShanghaiTech Workshop on Emerging Devices, Circuits and Systems (SWEDCS'2016), Shanghai, China, June 30th to July 1st, 2016
2. D. Fan, "Ultra-Low Energy Reconfigurable Spintronic Threshold Logic Gate", *26th GLSVLSI*, Boston, Massachusetts, May 18-20, 2016
1. M. Sharad, D. Fan, K. Roy, "Ultra Low Power Brain-Inspired Computing with Spin-Torque Devices," University of Minnesota, Minneapolis, C-SPIN Annual Review, Sept 27, 2013

NEWS

1. https://www.ucf.edu/news/new-ucf-project-will-put-downtown-orlando-air-quality-data-in-residents-hands/
2. SRC Newsletter May 2019 to report best paper award of GLSVLSI 2019

TEACHING EXPERIENCE

- **Instructor**, EEE 334 (Spring 2021), "*Circuit II*", Arizona State University, Tempe, AZ
- **Instructor**, EEE 425 (Fall 2019/2020), "*Digital Systems and Circuits*", Arizona State University, Tempe, AZ

- **Instructor**, EEL6364 (created by me, Fall 2016/2017/2018), "*Neuromorphic Computing Architecture, Circuit and Device*", University of Central Florida, Orlando, FL
- **Instructor**, EEL4362 (created by me, Fall 2017/2018), "*Post-CMOS Device and Circuit*", University of Central Florida, Orlando, FL
- **Instructor**, EEL4781 (Summer 2019), "*Computer Communication Networks*", University of Central Florida, Orlando, FL
- **Instructor**, EEE4768 (Spring 2016/2017/2018/2019), "*Computer Architecture*", University of Central Florida, Orlando, FL
- **Instructor**, EEE6338 (Fall 2015), "*Advanced Topics in Microelectronics*", University of Central Florida, Orlando, FL
- **Mentor**, ECE peer mentoring program, Purdue University, West Lafayette, IN, 2014

INSTITUTIONAL SERVICE

Arizona State University

- Ph.D. Thesis Committee (**Arizona State University**):
    a) Tao Li, school of ECEE, ASU, advisor; Dr. Yanchao Zhang (Ph.D. awarded in Summer 2020)
    b) Xiaocong Du, school of ECEE, ASU, advisor; Dr. Yu Cao (Ph.D. awarded in Fall 2020)
    c) Zheng Li, school of ECEE, ASU, advisor; Dr. Yu Cao (Ph.D. awarded in Fall 2020)
    d) Xin Ye, school of Computer Science, ASU, advisor; Dr. Yezhou Yang
    e) Wangxin He, school of ECEE, ASU, advisor; Dr. Jae-Sun Seo
    f) Mehmet Dedeoglu, School of ECEE, ASU, Advisor: Dr. Junshan Zhang

- Master Thesis Committee (**Arizona State University**):
    a) Shiva Bandyopadhyay, school of ECEE, ASU, advisor; Dr. Umit Ograss (graduated in Summer 2020)

- Senior Design Committee in School of ECEE, ASU for academic year 2020-2021
- Piazza Replacement Committee in Fulton Schools of Engineering, Spring 2021

University of Central Florida

- Ph.D. Thesis Committee (**University of Central Florida**):
    a) Soheil Salehi Mobarakeh, Ph.D. degree awarded in Spring 2020, advisor: Dr. Ronald DeMara
    b) Ramtin Mohammadi-Zand, Ph.D. awarded in Spring 2019, advisor: Dr. Ronald DeMara
    c) Arman Roohi, Ph.D. awarded in Spring 2019, advisor: Dr. Ronald DeMara
    d) Steven Pyle, Ph.D. awarded in Spring 2019, advisor: Dr. Ronald DeMara
    e) Amad Hassen, Ph.D. awarded in Spring 2019, advisor: Sumit Jha
    f) Hang Li, Ph.D. awarded in Spring 2019, Advisor: Dr. KALPATHY B. SUNDARAM
    g) Lingfeng He, Ph.D. awarded in Spring 2019, Advisor: Dr. KALPATHY B. SUNDARAM
    h) Jian Zhou, Ph.D. awarded in Summer 2018, Advisor: Dr. Jun Wang
    i) Wei Liang, Ph.D. awarded in Spring 2017, advisor; Dr. KALPATHY SUNDARAM
    j) Xunchao Chen, Ph.D. awarded in Fall 2017, advisor: Dr. Jun Wang
    k) Xuhong Zhang, Ph.D. awarded in Fall 2017, advisor: Dr. Jun Wang

l) Baogang Zhang (Advisor: Dr. Rickard Ewert)
m) Shayan Taheri (Advisor: Dr. Jiann-Shiun Yuan);
n) Qutaiba Alasad (Advisor: Dr. Jiann-Shiun Yuan);
o) Aihua Dong (Advisor; Dr. KALPATHY B. SUNDARAM);
p) Liheng Zhang (Advisor; Dr. Liqiang Wang);
q) Juan Escobedo Contreras (Advisor; Dr. Mingjie Lin);

- Master Thesis Committee (University of Central Florida):
  a) Soheil Salehi Mobarakeh, master degree awarded in Fall 2016, advisor: Dr. Ronald DeMara

- Computer Engineering faculty search committee at UCF, academic year of 2015-2016
- Computer Engineering Curriculum Oversight and Review Committee at UCF, academic year of 2018-2019
- ECE Department Undergraduate Curriculum Revision Subcommittee at UCF (Digital Logic and Secure Circuit Design Track, Software and Middleware Engineering Track), academic year of 2016-2017
- Senior Design Committee in ECE and CS departments at UCF for 2016 Fall, 2017 Spring, 2017 Fall, 2018 Spring, 2018 Fall

PROFESIONAL SERVICE

Technical Program Committee (TPC) of International Conference

- Design Automation Conference (DAC) 2018/2019/2020
- International Conference on Computer Aided Design (ICCAD) 2018/2019/2020
- IEEE International Symposium on High-Performance Computer Architecture (HPCA) 2020
- IEEE/ACM International Symposium on Microarchitecture (Micro) 2020
- Design, Automation and Test in Europe (DATE) 2020
- IEEE Winter Conference on Applications of Computer Vision (WACV), 2021
- ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED) 2020/2021
- Asia and South Pacific Design Automation Conference (ASP-DAC) 2018/2019/2020
- Design Automation Conference (DAC) Late Breaking Results 2020
- Great Lakes Symposium on VLSI (GLSVLSI) 2017/2018/2019
- IEEE Computer Society Annual Symposium on VLSI (ISVLSI) 2017/2018/2019
- IEEE International Symposium on Circuits and Systems (ISCAS) 2019
- International Conference on VLSI Design (VLSID) 2020/2021
- SIGDA PhD Forum at Design Automation Conference (DAC) 2016/2017/2018
- Student Research Contest Program Committee at ICCAD 2018
- Student Research Forum at IEEE/ACM ASP-DAC 2019
- IEEE International Symposium on Intelligent Signal Processing and Communication Systems 2017

Award Review Panel

- *National Science Foundation* Review Panel, 2016/2019/2020
- *Army Research Office* Research Fund/Award Review Panel, 2018
- *Defense Threat Reduction Agency* Review Panel, 2016
- *Ralph E. Powe Junior Faculty Award* of Oak Ridge Associated Universities Review Panel, 2016

- *Hong Kong Research Grant Council*, 2018/2019/2020
- *Dutch Research Council* (NWO) Award Review, 2020
- Best paper select committee of GLSVLSI 2017
- Best Paper select committee of ASP DAC 2018

Conference Service

- **Technical Area Chair** of Machine Learning System, Design Automation Conference (DAC) 2021
- **Technical Area Chair** of Emerging Computing & Post-CMOS Technologies, ACM Great Lakes Symposium on VLSI (GLSVLSI) 2019/2020/2021
- **Technical Area Chair** of Cognitive Computing Hardware, International Symposium on Quality Electronic Design (ISQED) 2019/2020/2021
- **Publicity Chair**, IEEE Computer Society Annual Symposium on VLSI (ISVLSI) 2021
- **Financial Chair**, IEEE Computer Society Annual Symposium on VLSI (ISVLSI) 2019
- **Local Arrangement Chair**, IEEE CyberSciTech/DASC/PICom/DataCom, Orlando, FL, 2017
- **Tutorial Session Organizer:** "Toward New Era of Compute-in-Memory: From Memory Devices to Applications" in Design Automation Conference, Austin (DAC) 2020.
- *Session Chair*, Design Automation Conference, Austin (DAC), 2017/2018/2019
- *Session Chair*, Design, Automation and Test in Europe Conference (DATE) 2020
- *Session Chair*, IEEE International Conference On Computer Aided Design (ICCAD), 2018/2019
- *Session Chair*, IEEE International Conference on Computer Design (ICCD), 2017/2018
- *Session Chair*, *IEEE Computer Society Annual Symposium on VLSI* (ISVLSI), 2017/ 2018/ 2019
- *Session Chair*, Asia and South Pacific Design Automation Conference (ASP DAC), 2018
- *Session Chair*, Great Lakes Symposium on VLSI (GLSVLSI), 2017/2018/2019
- *Panelist* in Neuromorphic Computing and Deep Learning, ACM/IEEE System Level Interconnect Prediction 2017 workshop, Austin, TX, 2017
- *Panelist*, ACM/IEEE System Level Interconnect Prediction 2019 workshop, Las Vegas, NV, 2019

Editors of Journals

- Guest editor of *Special Issue – 'Physical phenomena for Future Electronics', Frontiers in Physics*
- Guest editor of *Special Issue – 'Hardware-Aware Deep Learning', Applied Sciences*
- Guest editor of *CCF THPC Special Issue on 'Disruptive Computing Technologies'*
- Topic Editor of *Micromachines (ISSN 2072-666X)*
- Topic Editor in *Frontiers in Neuroscience-Neuromorphic Engineering*

Journal Technical Reviewer

- Reviewer of *Nature Electronics*
- Reviewer of *IEEE Transactions on Neural Networks and Learning Systems (TNNLS)*
- Reviewer of *IEEE Transactions on Very Large Scale Integrated Systems (TVLSI)*
- Reviewer of *IEEE Transactions on Nanotechnology*
- Reviewer of *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*
- Reviewer of *IEEE Transactions on Computers*
- Reviewer of *IEEE Transactions on Emerging Topics in Computing (TETC)*
- Reviewer of *IEEE Transactions on Emerging Topics in Computational Intelligence (TETCI)*

- Reviewer of *IEEE Transactions on Electronic Device (TED)*
- Reviewer of *IEEE Transactions on Circuits and Systems I (TCAS-I)*
- Reviewer of *IEEE Transactions on Multi-Scale Computing Systems (TMSCS)*
- Reviewer of *IEEE Transactions on Circuits and Systems for Video Technology (TCSVT)*
- Reviewer of *IEEE Transactions on Aerospace & Electronic Systems*
- Reviewer of *IEEE Transactions on Medical Imaging*
- Reviewer of *IEEE Electron Device Letters (EDL)*
- Reviewer of *IEEE Magnetics Letters*
- Reviewer of *IEEE Journal on of Solid-State Circuits (JSSC)*
- Reviewer of *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*
- Reviewer of *IEEE Design & Test*
- Reviewer of *IEEE Journal of Exploratory Solid-State Computational Devices and Circuits*
- Reviewer of *IEEE Embedded Systems Letters*
- Reviewer of *IEEE Access*
- Reviewer of *IEEE Circuit and Systems Magazine*
- Reviewer of *ACM Journal on Emerging Technologies in Computing Systems*
- Reviewer of *ACM Transactions on Modeling and Performance Evaluation of Computing Systems*
- Reviewer of *IET Cyber-Physical Systems: Theory & Applications*
- Reviewer of *Journal of Applied Physics*
- Reviewers of *Royal Society of Chemistry, Nanoscale*
- Reviewers of *Applied Sciences*
- Reviewers of *Applied Physics Letter*
- Reviewer of *ELSEVIER Nano Communication Networks*
- Reviewer of *ELSEVIER Neurocomputing*
- Reviewer of *ELSEVIER Engineering Science and Technology*
- Reviewer of *ELSEVIER Integration, The VLSI Journal*
- Reviewer of *ELSEVIER Physics Letters A*
- Reviewer of *Journal of Computational Electronics*
- Reviewer of *Journal of Systems Architecture*
- Reviewer of *Electronics (ISSN 2079-9292)*
- Reviewer of AEU-*International Journal of Electronics and Communications*
- Reviewer of *Sensors* (ISSN 1424-8220)
- Reviewer of MDPI *Molecules*
- Reviewer of *SCIENCE CHINA Information Sciences*

Conference Technical Reviewer

- Reviewer of *International Conference on Machine Learning* (ICML) 2021
- Reviewer of *International Conference on Computer Vision* (ICCV) 2021
- Reviewer of *34th Conference on Neural Information Processing Systems* (NeurIPS) 2020
- Reviewer of 53rd *IEEE/ACM International Symposium on Microarchitecture* (MICRO), 2020
- Reviewer of *Design Automation Conference* (DAC) 2018/2019
- Reviewer of *Asia Conference on Computer Vision* (ACCV) 2020
- Reviewer of *Asia and South Pacific Design Automation Conference* (ASP-DAC) 2018/2019/2020

- Reviewer of *Great Lakes Symposium on VLSI* (GLSVLSI) 2017, 2018
- Reviewer of *IEEE Computer Society Annual Symposium on VLSI* (ISVLSI) 2017,2018
- Reviewer of SIGDA PhD Forum at Design Automation Conference (DAC) 2016, 2017
- Reviewer of *IEEE International Symposium on Intelligent Signal Processing and Communication Systems* (ISPACS) 2017
- Reviewer of *International Symposium on Quality Electronic Design* (ISQED), 2017
- Reviewer of *International Symposium on Circuits & Systems* (ISCAS), 2017/2019
- Reviewer of IEEE *International Conference on Nanotechnology*, 2017
- Reviewer of *International Symposium on Low Power Electronics and Design* (ISLPED), 2015
- Reviewer of *International Midwest Symposium on Circuits and Systems* (MWSCAS), 2012

Others

- Member of *Institute of Electrical and Electronics Engineers* (*IEEE)*
- Member of *Association for Computing Machinery* (*ACM)*
- Member of *ACM Special Interest Group in Design Automation (SIGDA)*
- Member of *IEEE Council on Electronic Design Automation (CEDA)*