Digital Circuit Applications of Resonant Tunneling Devices

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Many semiconductor quantum devices utilize a novel tunneling transport mechanism that allows picosecond device switching speeds. The negative differential resistance characteristic of these devices, achieved due to resonant tunneling, is also ideally suited for the design of highly compact, self-latching logic circuits. As a result, quantum device technology is a promising emerging alternative for high-performance very-large-scale-integration design. The bistable nature of the basic logic gates implemented using resonant tunneling devices has been utilized in the development of a gate-level pipelining technique, called nanopipelining, that significantly improves the throughput and speed of pipelined systems. The advent of multiple-peak resonant tunneling diodes provides a viable means for efficient design of multiple-valued circuits with decreased interconnect complexity and reduced device count as compared to multiple-valued circuits in conventional technologies.

This paper details various circuit design accomplishments in the area of binary and multiple-valued logic using resonant tunneling diodes (RTD's) in conjunction with high-performance III–V devices such as heterojunction bipolar transistors (HBT's) and modulation doped field-effect transistors (MODFET's). New bistable logic families using RTD + HBT and RTD + MODFET gates are described that provide a single-gate, self-latching MAJORITY function in addition to basic NAND, NOR, and inverter gates. This forms the basis for design of high-speed nanopipelined 32- and 64-bit adders using only a single 4-bit adder block. A 32-bit nanopipelined correlator, designed using RTD + HBT logic, demonstrates a simulated power-delay product of 32 pJ while achieving a simulated throughput of one 32-bit correlation every 100 ps. Examples of multiple-valued logic circuits using resonant tunneling devices are presented, which achieve significant compaction in terms of device count over comparable binary logic circuits in conventional technologies. These include a four-valued 4 : 1 multiplexer using four RTD's and 21 HBT's, a mask programmable four-valued, single-input gate using four RTD's and 14 HBT's, and a four-step countdown circuit using one RTD and three HBT's.

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I. INTRODUCTION

Growing high-performance computing needs of end users are constantly pushing circuit and device technology to improve in terms of speed and power. Over the past few decades, scaling of device dimensions has proved to be an effective ploy in meeting circuit performance requirements and in decreasing power consumption. As device dimensions in integrated circuits (IC's) shrink from the micrometer to submicrometer levels and below, quantum effects become more prominent. When these device dimensions go down to a few nanometers, quantum effects such as resonant tunneling lead to interesting new device characteristics, which can be exploited to create extremely fast and compact circuits [1]. State-of-the-art commercial process technologies such as complementary metal–oxide–semiconductor (CMOS) rely largely on device scaling for performance improvement of integrated circuits. While this trend has been responsible for rapid advancement of very-large-scale-integration (VLSI) technology in the present era, the physical limits of the conventional device transport phenomenon will likely be reached in the early part of the next century, thus necessitating alternative device concepts to continue fueling the growth of the VLSI industry. The resonant tunneling properties of quantum devices seemingly promise a dramatic improvement in circuit performance as a result of picosecond device switching speeds and reduction in device counts per circuit function. While the properties of resonant tunneling diodes (RTD's) were predicted almost 20 years ago [2], recent developments in growth techniques such as molecular-beam epitaxy have made it possible actually to build and use these devices. Also, to achieve the resonant tunneling phenomenon, it is necessary to scale devices only along a single dimension. This nanometric scaling can be achieved by nonlithographic processes in order to form critical dimensions required for the tunneling effect [3]. This implies that resonant tunneling devices can be integrated with conventional transistors.

Table 1 Comparison of Process Technologies

Parameter (per gate)	CMOS	GaAs CHFET	RTD+ HBT	RTD+ MODFET
Power (mW)	0.2	0.1	0.5	0.3
Delay (ps)	500	250	40	200
Device count	Large *due to regular I-V curves*	Large	Small *due to NDR I-V curves*	Small

The cointegration of resonant tunneling devices and GaAs transistors [4], [5] has made feasible several novel, high-performance digital logic families. Table 1 compares some conventional silicon and GaAs-based technologies with RTD-based technologies that use similar feature sizes and device dimensions. The entries for power per gate in Table 1 are for circuits operating at the maximum speed corresponding to the entry for delay per gate for that circuit.

Several novel memory and logic circuits using RTD's have been proposed over the past few years. These circuits have one or more of the following advantages over conventional logic circuits:

1) reduced circuit complexity for implementing a given function;
2) low power operation;
3) high-speed operation.

Circuits using one or two RTD's or resonant tunneling transistors (RTT's) were described by Capasso *et al.* [6], [7]. The main focus of this work was on fabricating these novel device structures; a few interesting circuit applications based on their negative differential resistance (NDR) characteristics were built to demonstrate the possibilities of these devices. Multistate memories, multivalued logic, and compact circuits for parity generation were described. Each circuit contained just one or two quantum devices; a three-state memory cell consisted of two RTD's and a couple of resistors, a parity generator consisted of just one RTT, and so on. These circuits demonstrated reduced circuit complexity (component count) due to the use of the new quantum devices. More recently, device fabrication techniques for multiple-peak RTD's have been developed, and various authors have proposed multistate memories using RTD's [8]–[10]. Typically, a single memory cell consists of one or more RTD's in series with a load, as well as access lines and transistors. A multidimensional memory cell [10] consisting of m single-peak RTD's with a current source load stores m bits of information at a cost of one RTD, $1+1/m$ transistors, and $1+1/m$ access lines per bit, as compared to six transistors and two access lines per bit in a conventional static random access memory (SRAM) cell (without the bit-bar line) and one transistor, one capacitor, and two access lines in a dynamic RAM cell. Seabaugh *et al.* [11] describe a nine-state memory cell using a single multipeak RTD. While a conventional SRAM cell contains six transistors and stores 1 bit of information, this memory cell contains just one multipeak RTD and one load transistor and stores $\log_2(9) = 3.2$ bits of information (nine states).

While the RTD is the basic two-terminal NDR device, it is also now possible to introduce tunneling at the base-emitter junctions of high-performance bipolar GaAs devices such as hot-electron transistors (HET's) and heterojunction bipolar transistors (HBT's) to form three-terminal NDR devices such as resonant hot-electron transistors (RHET's) and resonant tunneling bipolar transistors (RTBT's). RHET's have been built, and extremely compact circuits have been demonstrated using these devices [12]–[16]. RHET's and RTT's, being three-terminal devices with NDR characteristics, offer more possibilities to the circuit designer than two-terminal devices. An adder circuit described in [13] uses RHET's to perform complex operations such as XOR with a single device (the most compact XOR in CMOS technology requires at least six transistors). A full adder that requires 45 transistors and several resistors in a conventional bipolar technology, such as transistor–transistor logic requires only seven RHET's and a few resistors. Apart from RHET's [12], we have designed and fabricated the bound-state (BS)RTT [17], [18]. Using the predicted properties of the RTT, extremely compact, self-latching logic circuits were designed [19]; two new types of logic families, called true-bistable and pseudo-bistable logic, were developed with the property that each gate not only performed a specific logic function such as AND or OR but also latched the output automatically, without the need for extra storage latches. A pipelined adder designed using this form of logic is extremely compact because:

1) the NDR characteristic of the RTT allows a single gate to perform the 1-bit CARRY function, as opposed to the five gates required in a canonical implementation in conventional MOS or bipolar technologies;
2) the self-latching property reduces the pipeline storage and speed overhead to zero.

Table 2 Device Counts for Function Implementation in Various Technologies

Circuit	TTL	CMOS	ECL	NDR
Bistable XOR	33	16	11	4
Bistable Majority	36	18	29	5
Muller C-element	45	8	44	4
9-state memory	24	24	24	5
NOR2+flipflop	14	12	33	4
NAND2+flipflop	14	12	33	4

More recently, another self-latching gate using a different quantum electronic device has been demonstrated elsewhere; this device is a combination of an RTD and a modulation doped field-effect transistor (MODFET), and it realizes a self-latching threshold function of three inputs [20], [21]. The circuit size compaction afforded by the use of NDR logic is illustrated in Table 2, which shows the comparison of the device counts of NDR logic circuits with similar implementations in conventional technologies.

Since the publication of the initial papers on the subject of circuit applications of RTD's by Capasso and coworkers [1], [8], RTD-based circuit design has been receiving wider attention, and various authors have published novel logic circuits using resonant tunneling devices. Some recent

circuit efforts using resonant tunneling devices are documented in [22]–[27]. The multistate nature of multiple-peak (M)RTD's has always made them attractive for application in building memory cells. Van der Wagt *et al.* [28] and Shieh *et al.* [29] describe recent work in this area. Multiple-valued logic applications of RTD's, other than memories, were first described by Micheel and Paulus [30], and several RTD-based multiple-valued logic circuits have been described by various authors since then [31]–[34]. Low-power binary logic using RTD's has been proposed by Chang *et al.* [35]. Seabaugh *et al.* [36] have designed a full-adder circuit using cointegrated RTD's and bipolar transistors, with just 11 active devices and a few resistors. Device count is reduced through the application of the RTD's folded I–V characteristic to design a two-input XOR gate with just three active devices.

RTD's have also been used widely in analog circuits such as analog-to-digital converters [37] and microwave circuits, but these circuits are not in the scope of this paper. Interested readers are referred to [38] for further information and references. In the 1990's, many researchers have recognized the important potential contributions of resonant tunneling devices to state-of-the-art circuit design and have periodically documented the progress made in this area [39]–[42].

This paper is organized as follows. In Section II, we present the design and analysis of basic bistable logic gates that use RTD's in conjunction with HBT's and MODFET's. We also discuss related RTD-based circuit design activities pursued by other researchers in the field. RTD + transistor logic has many advantages over RTD-only logic, such as better fanout, improved isolation between input and output, higher noise margins, greater component tolerance, larger circuit gain, and a more extensive basic function library resulting in better applicability to larger systems. In Section III, we discuss the concept of nanopipelining, made possible by the self-latching nature of the basic gates, and its application to the design of high-speed and high-throughput adders and correlators. In Section IV, we review multiple-valued applications of RTD-based circuits. We present examples of RTD-based multiple-valued logic circuits that provide substantial circuit size compaction over conventional implementations while also reducing interconnect complexity and thus further improving circuit performance. These circuits—a four-valued 4 : 1 multiplexer, a four-valued mask-programmable multiple-valued logic (MVL) gate array and a four-step countdown circuit—demonstrate the viability of MVL using the novel quantum-effect devices.

A summary of basic quantum circuit designs discussed in this paper is presented in Table 3. The entries for power in Table 3 are for circuits operating at the maximum speed corresponding to the entry for speed/delay for that circuit.

Table 3 Summary of Basic Self-Latching NDR Circuits

Circuit	Technology	Power (mW)	Speed/ Delay	Noise Margin
AND3	RTBT	10	40 ps	0.3 V
OR3		10	37 ps	0.3 V
CARRY		10	34 ps	0.3 V
NOR3	RTD+	0.48	5 GHz	I_h=90 mA
MINORITY	MODFET	0.6		I_l=0
NAND3	(dep.)			NM_l=9 mA
				NM_h=17 mA
NOR3	RTD+	0.3	5 GHz	same as
MINORITY	MODFET			above
	(enh.)			
NOR3	RTD+HBT	0.5	25 GHz	0.3 V
MINORITY				
Adder		10	800 ps	
(32-bit)				
Correlator	RTD+HBT	320	10 GHz	
(32-bit)	RTD+	250	3 GHz	
	MODFET			
T-gate	RTD+HBT	327	2.87 ns	0.3 V
		3.2	33.3 ns	
MVL Gate		500	2 GHz	
Array				

II. Compact Binary Logic Using RTD's

A binary logic circuit is said to operate in the bistable mode when its output is latched, and any change in the input is reflected in the output only when a clock or other evaluation signal is applied. The bistable mode has been used in several earlier technologies, notably in superconducting logic [43]. Superconducting logic typically uses a multiphase AC power source to reset/evaluate each gate periodically. Similar logic using resonant tunneling devices has been proposed by several authors [20], [44], [45]. The chief disadvantage of these circuits is the requirement of an AC power source whose frequency determines the maximum switching frequency. The logic circuits described herein use a DC power supply and multiphase clocks, but the clock signals are not required to supply large amounts of power, as in the case of the earlier circuits.

In the following subsections, we introduce the current–voltage characteristics of an RTD and its associated device parameters, followed by the design, analysis, and fabrication of RTD-based bistable logic gates and a discussion of the unique properties that make them attractive for circuit design.

A. RTD Device Characteristics

An RTD is composed of alternate layers of heterogeneous semiconductors [46], which facilitate the tunneling mechanism that results in folded device I–V characteristics, as illustrated in Fig. 1. As the voltage applied across the RTD terminals is increased from zero, the current increases due to tunneling until V_p, the peak voltage of the RTD. The corresponding current is called the peak current I_p. As the voltage across the RTD is increased beyond V_p, the current through the device drops due to reduction in tunneling until the voltage reaches V_v, the valley voltage. The current at this voltage is the valley current I_v. Beyond V_v, the current through the RTD starts increasing again in accordance with conventional diode behavior. For a current in [I_v, I_p], there are two possible stable voltages: $V_1 < V_p$ or $V_3 > V_v$. The voltage across the RTD when it is operating in the first positive differential-resistance region and the current through it equals I_v is called the first voltage V_f.

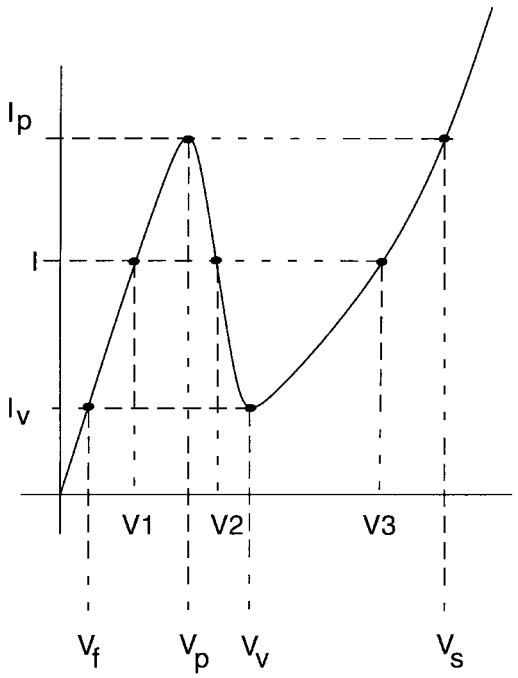

Fig. 1. RTD current–voltage characteristics.

Similarly, the voltage across the RTD when it is operating in the second positive differential-resistance region and the current through it equals I_p is called the second voltage V_s.

Other important derived RTD parameters used in this paper are as follows:

$$R_{p1} = \frac{V_p}{I_p} \tag{1}$$

$$R_{p2} = \frac{V_s - V_v}{I_p - I_v} \tag{2}$$

$$|R_n| = \frac{V_v - V_p}{I_p - I_v} \tag{3}$$

$$PVVR = \frac{V_p}{V_v} \tag{4}$$

$$PVCR = \frac{I_p}{I_v}. \tag{5}$$

Here, R_{p1} is the first positive differential resistance, R_{p2} is the second positive differential resistance, R_n is the negative differential resistance, $PVVR$ is the peak-to-valley voltage ratio, and $PVCR$ is the peak-to-valley current ratio of the RTD.

The folded characteristic of the RTD makes it a useful load device that, when properly biased, draws very low currents for both high and low outputs. Although tunnel diodes have been in existence for many decades, they have relatively low switching speeds and a protracted valley region that is not conducive for high-performance circuit design. Resonant tunneling allows picosecond switching and sharp transitions, which result in improved performance of circuits designed using RTD's.

B. RTD + HBT Bistable Logic

The operating principle of the new bistable element, using RTD's in conjunction with HBT's, may be understood by considering the simplified circuit shown in Fig. 2. There are m input transistors and one clock transistor driving a single RTD load. The input transistors can be in either of two states: ON, with a collector current of I_h, or OFF with no collector current. The clock transistor can be in one of two states: HIGH, with collector current I_{clkh}, and *quiescent*, with collector current I_{clkq}. In addition, there is a global reset state where all the collector currents are zero. When the clock transistor current is at I_{clkq}, the load lines in Fig. 2 show that the circuit has two possible stable operating points for every possible input combination. When the clock current is I_{clkh}, there is exactly one stable operating point for the circuit when n or more inputs are high and the sum of the collector currents is $nI_h + I_{clkh}$. This operating point corresponds to a logic zero output voltage. Hence, this circuit can be operated sequentially to implement any nonweighted threshold logic function $f(x_1, x_2, \cdots, x_m; n)$, where $f(x_1, x_2, \cdots, x_m)$ is one if and only if $(x_1 + x_2 + \cdots x_m) < n$ and where $x_1, x_2, \cdots, x_m$ take on values of either zero or one.

The operating sequence is as follows.

1) Reset all collector currents to zero, causing the output voltage to go high.
2) Remove the reset signal and make the clock high so that the clock current is I_{clkh} and the inputs have their normal stable values. If n or more inputs are high, the output goes to the logic low state corresponding to the second positive differential resistance (PDR) region of the RTD characteristic corresponding to $V_{rtd} > V_v$, where V_{rtd} is the voltage across the RTD. Otherwise, if fewer than n inputs are high, the operating point remains in the first PDR region of the RTD, where $V_{rtd} < V_p$.
3) Bring the clock signal to its quiescent state so that the current through the clock transistor is I_{clkq}. The output voltage reaches the stable level corresponding to whether the RTD was in the first PDR region or the second PDR region in the previous step of the sequence.

As long as the clock remains at its quiescent state and the reset signal is not applied, the output does not change with the inputs. Once the inputs are stable, however, the correct output can be set by the above evaluation sequence. Hence, this circuit operates as a clocked, self-latching threshold element. Thus, system design using RTD-based gates eliminates the area and delay overhead associated with the use of separate latches in a pipelined system. This results in a pipelining scheme, called nanopipelining, that converts each level of a multilevel logic circuit into a pipeline stage.

For a three-input circuit, three nontrivial threshold functions can be implemented for the cases where $n = 1, 2, 3$. For $n = 1$, $f1(x_1, x_2, x_3) = 0$ if and only if one or more inputs are high. This corresponds to a NOR function. For $n = 3$, $f3(x_1, x_2, x_3) = 0$ if and only if all three inputs are high. This corresponds to a NAND function.

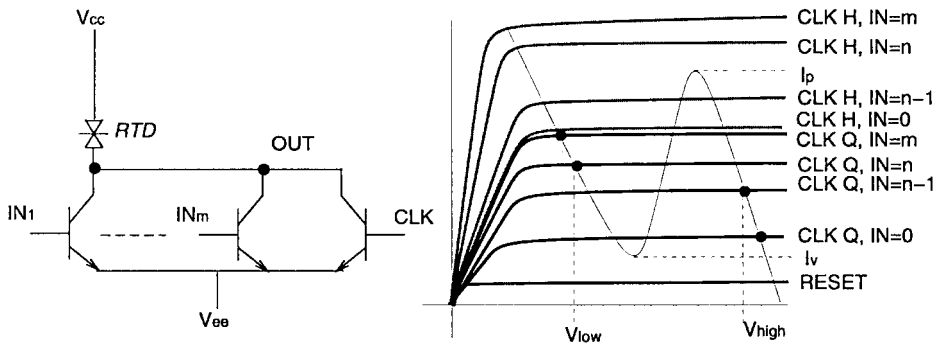

Fig. 2. Operating principle of a bistable RTD + HBT logic gate.

For $n = 2$, $f2(x_1, x_2, x_3) = 0$ if and only if two or more inputs are high. This corresponds to an inverted majority or inverted CARRY function. Considering the single gate implementation of the CARRY function, and given the picosecond switching speed of RTD, it is clear that these logic gates can be well used to speed up addition chains, which invariably fall on the critical path in a computing system. This scheme can easily be extended to implement weighted threshold logic elements by simply assigning different areas to the input transistors. A weighted threshold logic element with m inputs $x_1, x_2, \cdots, x_m$ and weights $w_1, w_2, \cdots, w_m$ has a low output if and only if $w_1x_1 + w_2x_2 + \cdots w_mx_m > n$, where n is the threshold. It can be seen that the above circuit implements this function when the collector currents of the input transistors are weighted by the factors $w_1, w_2, \cdots, w_m$ and the peak current I_p of the RTD is chosen so that the total current through the input transistors exceeds $I_p - I_{clkh}$ exactly when the weighted sum of the logic inputs exceeds the threshold n.

1) Implementation Issues: The implementation of the above circuit requires precise control over the RTD and transistor circuits in fabrication. Since the cointegration of RTD's and HBT's is still an active area of research, a prototype version of the above circuit was fabricated. This version 1) places very few constraints on the HBT gain and collector current, as well as on the RTD peak and valley currents, and 2) allows the same integrated circuit to be used in testing the functionality of different logic circuits by changing some external voltages. To account for possible mismatches between RTD and HBT parameters due to immaturity of process technology, large base resistances were used, which limit the high-frequency operation of the circuit. The RTD's and HBT's were integrated on the same wafer, and Fig. 3 shows a photomicrograph of the integrated circuit. The IC was fabricated using InP/InGaAs HBT's and AlAs/InGaAs/AlAs RTD's grown by chemical-beam epitaxy. Conventional photolithography and liftoff techniques were used to process the active devices and thin-film Ti resistors. The HBT's show maximum DC current gain around 50, and the RTD's have a peak-to-valley current ratio of six and peak voltage of 0.3 V.

Fig. 4 shows the load lines for a three-input bistable inverted MAJORITY gate and the sequence of operations

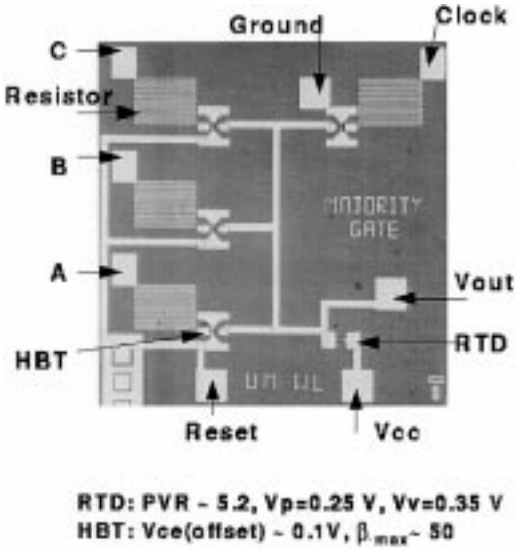

Fig. 3. Photomicrograph of integrated circuit.

corresponding to the observed traces from the testing of the fabricated circuit. It can be seen that the output switches to logic zero when two or more inputs are at logic one and the clock is high. Thereafter, the output stays at zero even when the clock goes back to its quiescent/low level. The output levels are indicated by 1, 0, x, and 11. Eleven and x correspond to the levels seen when the reset and clock, respectively, are active. Hysteresis in the RTD characteristics may make the x level look like a one level, as seen in the observed traces. Hysteresis does not, however, change the design equations or the logic function. The inverted self-latching MAJORITY gate operated at 1.5 V with an average static current of 3.85 mA, showing a static power consumption of approximately 5.5 mW.

The simulated power-delay characteristics of RTD + HBT circuits compare well with the best ECL/CML technologies using silicon or HBT technologies. While this scheme consumes more static power than CMOS circuits, where the static power consumption is zero, it does provide a means to reduce power consumption in high-speed bipolar circuits. When the RTD load was used in an I^2L type of configuration, total power savings of 50% over conventional HBT I^2L were observed in simulations of divide-by-two frequency dividers. Unloaded gate delays of

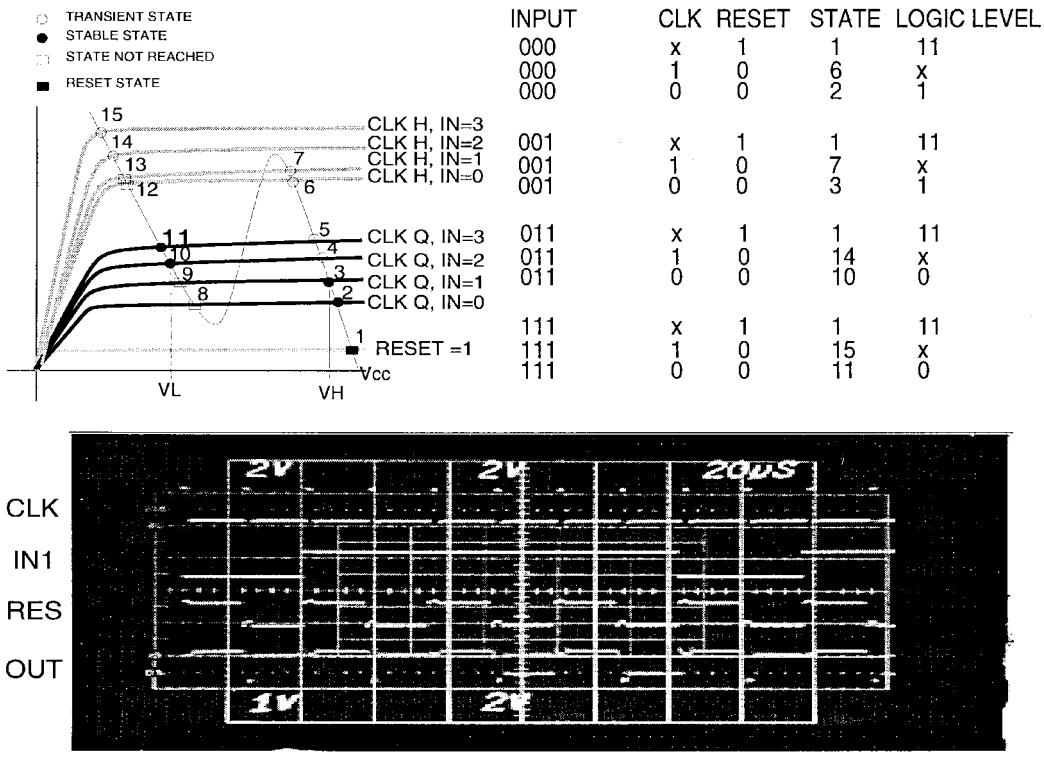

Fig. 4. Bistable inverted MAJORITY circuit operation.

less than 40 ps were obtained with a power dissipation of 0.4 mW/gate and a logic swing of 0.8 V. In addition, advantages of RTD + HBT logic such as self-latching gates and single gate CARRY circuit implementation make them a potential candidate for ultrafast and ultradense VLSI circuit design. A concern of these logic circuits is their reduced noise margin due to operation in the threshold mode. In the next subsection, we present noise-margin analysis of RTD + HBT logic gates, quantifying important RTD parameters that affect circuit noise margins while presenting guidelines for design of more robust circuits.

C. Noise Margins of RTD + HBT Threshold Logic Gates

Bhattacharya *et al.* [47] have developed a noise-margin measurement technique for RTD + HBT logic gates adapted from the simple but accurate method of fitting a maximum area rectangle between the normal and mirrored transfer characteristics of an RTD + HBT inverter. This method is very general and precise for characterizing noise margins. Additionally, due to the nature of the transfer characteristic of an RTD + HBT inverter, this method can be applied very simply, with some modifications. Based on the transfer characteristics of an RTD + HBT inverter, operating at a supply voltage of V_{cc}, the sum of the noise margins of the circuit can be written as follows:

$$\begin{aligned} NM_H + NM_L &= V_{cc} - V_p + (I_{clkh} - I_{clkq})R_{p1} \\ &\quad - V_{cc} + V_s - (I_{clkh} - I_{clkq})R_{p2} \\ &= (I_{clkh} - I_{clkq})(R_{p1} - R_{p2}) \\ &\quad + (V_s - V_p). \end{aligned} \tag{6}$$

From (2) and (3), we can write $(V_s - V_p) = (R_{p2} + |R_n|)(I_p - I_v)$.

Therefore

$$\begin{aligned} NM_H + NM_L &= (I_{clkh} - I_{clkq})(R_{p1} - R_{p2}) \\ &\quad + (R_{p2} + |R_n|)(I_p - I_v). \end{aligned} \tag{7}$$

For proper operation of the gate, $I_{clkh} < I_p$ and $I_{clkq} > I_v$, implying $I_{clkh} - I_{clkq} < I_p - I_v$.

Therefore, if $R_{p1} >= R_{p2}$

$$\begin{aligned} NM_H + NM_L &< (R_{p2} + |R_n|)(I_p - I_v) \\ &\quad + (R_{p1} - R_{p2})(I_p - I_v) \\ &< V_v\left(1 - \frac{PVVR}{PVCR}\right). \end{aligned} \tag{8}$$

Otherwise, if $R_{p1} \leq R_{p2}$

$$\begin{aligned} NM_H + NM_L &< (R_{p2} + |R_n|)(I_p - I_v) \\ &< V_s - V_p. \end{aligned} \tag{9}$$

The individual noise margins are given by

$$\begin{aligned} NM_H &= (V_{cc} - V_p) + (I_{clkh} - I_{clkq})\,R_{p1} \\ &\quad - V_T \ln\left(\frac{I_p - I_{clkh}}{I_s\{1 - e^{-[(V_{cc} - V_p)/V_T]}\}}\right) \end{aligned} \tag{10}$$

$$\begin{aligned} NM_L &= V_T \ln\left(\frac{I_p - I_{clkh}}{I_s\{1 - e^{-[(V_{cc} - V_p)/V_T]}\}}\right) \\ &\quad - (V_{cc} - V_s) - (I_{clk} - I_{clkq})\,R_{p2}. \end{aligned} \tag{11}$$

Thus, (8) and (9) give us important upper bounds for the sum of the two noise margins. On one hand, they provide us with a simple way to estimate the maximum noise margin

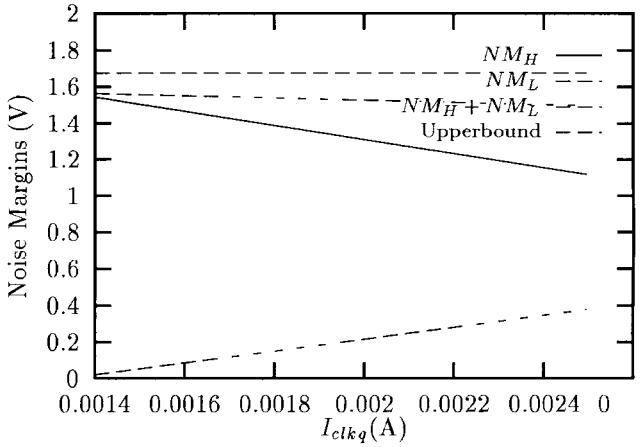

Fig. 5. Noise margins versus quiescent clock current ($V_{cc} = 3$ V).

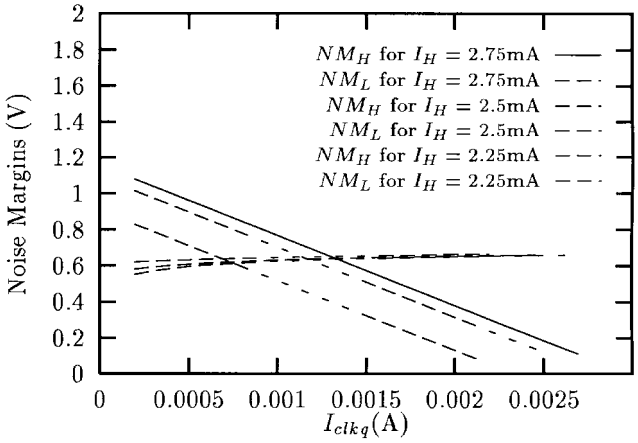

Fig. 6. Noise margins versus I_{clkq} for different I_{clkh}.

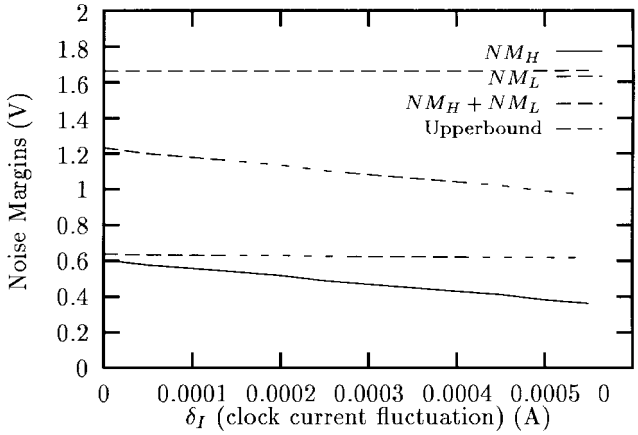

Fig. 7. Noise margins versus δ_I.

that can be harnessed from a given RTD, while on the other hand, they can be used by device engineers as a guideline for designing RTD's for digital logic applications.

1) Noise Margin with Noise on the Clock Signal: Noise on the clock line lowers the previously estimated signal noise margins. To study the worst case noise margins on the signal lines by introducing noise on the clock lines, it is assumed in [47] that noise on the clock lines can cause $\pm\delta_I$ fluctuations in the quiescent and high clock currents. That is, instead of a steady value of I_{clkq}, the quiescent clock can vary from $I_{clkq} - \delta_I$ to $I_{clkq} + \delta_I$. Similarly, the high clock current can vary from $I_{clkh} - \delta_I$ to $I_{clkh} + \delta_I$. Based on the effect of these variations on the transfer characteristic of the RTD + HBT inverter, the new noise margins can be written as

$$NM_H = (V_{cc} - V_p) + (I_{clkh} - I_{clkq} - \delta_I) R_{p1} - V_T \ln\left(\frac{I_p - I_{clkh} + \delta_I}{I_s\{1 - e^{-[(V_{cc}-V_p)/V_T]}\}}\right) \quad (12)$$

$$NM_L = V_T \ln\left(\frac{I_p - I_{clkh} - \delta_I}{I_s\{1 - e^{-[(V_{cc}-V_p)/V_T]}\}}\right) - (V_{cc} - V_s) - (I_{clkh} - I_{clkq} + \delta_I) R_{p2}. \quad (13)$$

2) Computer Simulation of Noise Margins: Fig. 5 shows the variation of an RTD + HBT inverter's noise margins as a function of the quiescent clock current I_{clkq}. As seen before, the upper bound of the sum of the noise margins that can be extracted from an RTD is given by (8). Practically, this upper bound can never be reached because I_{clkh} has to be less than I_p, and I_{clkq} has to be greater than I_v for proper operation. We see in Fig. 5 that for a constant clock high current of 2.5 mA ($I_p = 3.08$ mA) operating at $V_{cc} = 3$ V, as I_{clkq} is increased from I_v to I_{clkh}, NM_H decreases while NM_L increases in accordance with the predictions in (10). It should be noted, though, that the derivation of (10) assumes $(V_{cc} - V_s)$ to be positive; hence, if $V_{cc} < V_s$, load lines drawn will show that the operating point after switching (from one to zero) has to be such that the transistor will be in saturation. From this observation, it is clear that (10) cannot be used when $V_{cc} < V_s$.

The dependence of noise margin on the value of I_{clkh} is seen in Fig. 6. While NM_H increases with I_{clkh}, NM_L decreases with it, for a given value of I_{clkq}. When $NM_L = NM_H$, however, the value of the noise margins ≈600 mV (30% of V_{cc}), independent of I_{clkh}.

The presence of noise on the clock line will have an effect of reducing the overall noise margin on the signal lines. Fig. 7 shows this effect. Interestingly, NM_L does not seem to be affected at all by the clock noise. This, in conjunction with the fact that NM_H decreases with increasing δ_I, tells us that the choice of I_{clkh} and I_{clkq} should not be such that $NM_H = NM_L$. In fact, a robust design that can tolerate a larger amount of noise in the clock line should have I_{clkh} and I_{clkq} that make $NM_H > NM_L$.

Since RTD + HBT circuits operate at extremely high speeds, it is imperative to account for the ΔI-noise generated by the sharp clock edges coupled with the inductances of interconnects. Also, from the discussion above, it can be seen that the upper bound on the sum of the noise margins $(NM_H + NM_L)$ that can be extracted from a given RTD, irrespective of the type of transistors used, given by (8), can never exceed the valley voltage V_v of the RTD. To maintain consistent output of high and low voltage levels in order to have reliable operation of cascaded gates, it is necessary to have small values of positive differential resistances R_{p1} and R_{p2}. This, combined with the need to have high $PVCR$

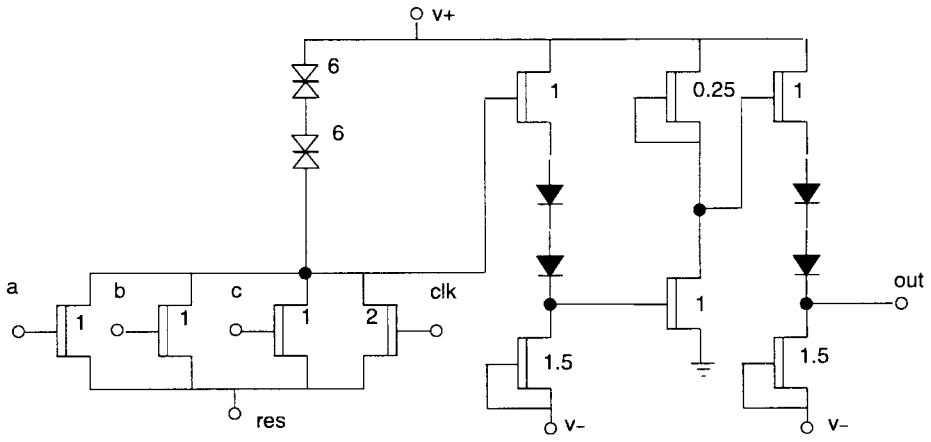

Fig. 8. Three-input MAJORITY/MINORITY circuit.

and low PVR [as dictated by (8)], indicates that the ideal RTD characteristic would have a sharp "N" shape.

D. RTD + MODFET Bistable Logic

Along the same principles as RTD + HBT logic, RTD's have been used in conjunction with MODFET's to develop a new logic family. In the absence of enhancement-mode MODFET's, positive and negative supply voltages and level-shifting stages are used. Two-peak RTD's are used to obtain a large enough voltage separation between the peak and valley points, but either one-peak or three-peak RTD's could be used instead, with a corresponding change in the voltage margins. The circuit diagram for a three-input, self-latching MAJORITY gate is shown in Fig. 8. The circuit consists of two stages; the first stage is a three-input bistable minority gate. The second stage is a combinational inverter that produces the majority function. The combinational inverter has a depletion MODFET load instead of an RTD load. When the input to the inverter is low, the bottom transistor (driver) is turned off and the output is high. When the input to the inverter is high, the driver is turned on and the output is pulled low. The inverter is very similar to an inverter in buffered FET logic. The depletion-mode MODFET's have a threshold voltage of approximately -0.6 V. The supply voltages are 1.5 and -2.0 V. The input and output logic levels are -0.2 and -0.7 V. The RTD's have a peak voltage of approximately 0.1 V and a valley voltage of approximately 0.4 V. The peak and valley currents of a 1×1-μm RTD are 100 and 25 μA, respectively. The numbers by the side of the RTD's indicate the area factor. Two level-shifting diodes are used. The operating principle of the self-latching MAJORITY gate, unique to NDR logic, is analogous to the bistable RTD + HBT gate operation discussed earlier. The simulated operation of the self-latching minority and majority functions is illustrated in Fig. 9. Basic RTD + MODFET bistable logic gates (NAND, NOR, MINORITY) have been fabricated in collaboration with Texas Instruments Incorporated. Fig. 10 shows a photomicrograph of the fabricated die.

RTD + MODFET logic will potentially have very low power dissipation, comparable to CMOS circuits, and high speed of operation due to compact logic circuit implementations as well as very high RTD tunneling speed. Hence, with improvements in processing technology, RTD + MODFET logic can be a viable alternative for systems with stringent power budgets that require high performance circuits such as portable computing.

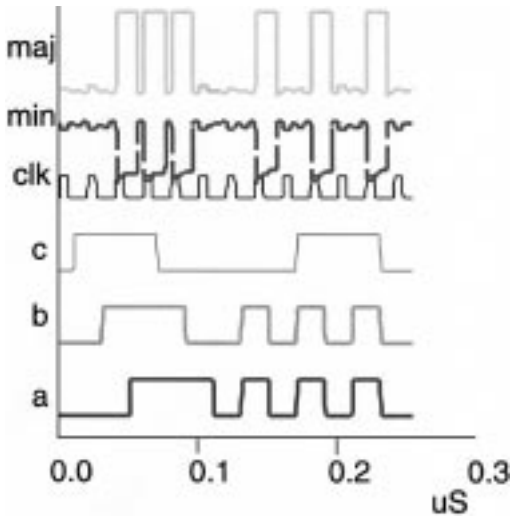

Fig. 9. Three-input MAJORITY/MINORITY simulation.

E. RTD-Only and Three-Terminal RT-Device Logic Circuits

Thus far, we have discussed RTD-based logic gate configurations that are constructed using cointegrated but separate RTD and HBT/MODFET devices. Two other approaches are commonly used in designing circuits that contain resonant tunneling devices. The first approach uses RTD's as the only active elements in the circuit, whereas the second approach introduces tunneling within conventional bipolar devices, such as HBT's, and field-effect devices, such as MODFET's, to achieve three-terminal resonant tunneling devices that are used for circuit applications. In the latter approach, resonant tunneling is introduced at the base-emitter (gate-source) junction of an HBT (MODFET) to obtain a resonant tunneling transistor, or an integrated RTD + MODFET device is built that is equivalent to an RTD

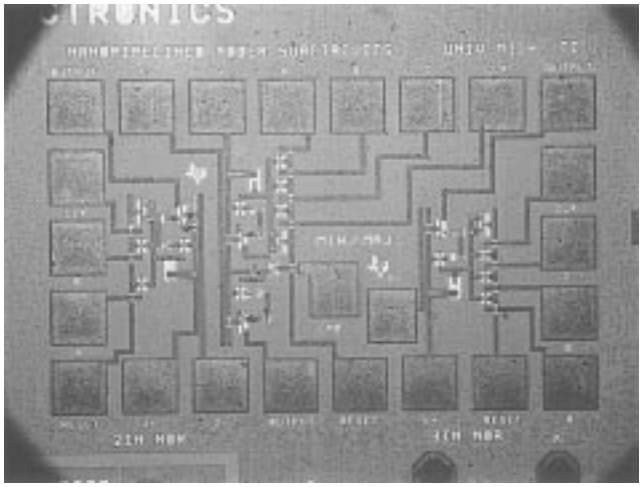

Fig. 10. Photomicrograph of RTD + MODFET logic circuits chip.

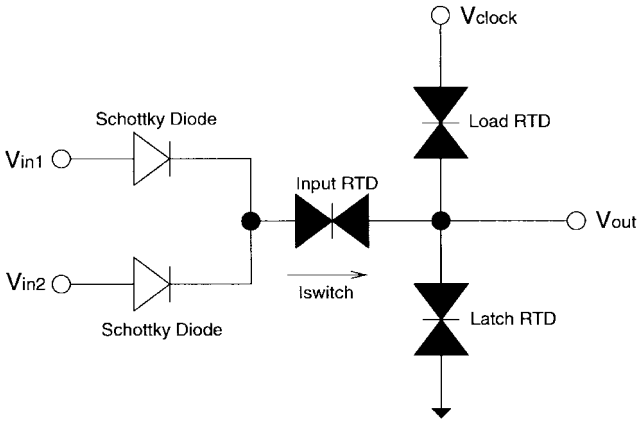

Fig. 11. Generic logic gate using RITD's.

and a MODFET connected in parallel. In this subsection, we present three examples that illustrate logic circuits built using these approaches.

1) Pipelined Logic Gates Using Interband RTD's [48]: Williamson *et al.* [48] report the demonstration of a functionally complete set of logic gates using resonant interband tunneling diodes (RITD's) and Schottky diodes, operating at a frequency of 12 GHz. The RITD is structurally similar to an RTD; however, it has a different bandgap alignment than an RTD. The device design of an RITD is described by Chow *et al.* [22]. From the circuit design point of view, RITD's demonstrate similar NDR I–V characteristics as RTD's. A common circuit topology, illustrated in Fig. 11, is used to generate different logic gate operations such as AND, OR, XOR, and INVERSION. The basic gate is composed of a logic element consisting of two Schottky diodes and an RTD and a latch consisting of two series-connected RTD's. The gate inputs are in the form of currents flowing through the parallel Schottky diodes and the series RTD. The logic output is the voltage level stored by the latch, which is clocked using a two-phase overlapping clock between adjacent pipelined gates. The latching mechanism is achieved by the two series RTD's forming a bistable pair. After the logic is evaluated, the clock signal is applied. If the evaluated logic is low, the sum of the input logic current and the load RTD current is such that the peak of current of the combined characteristic is less than the latch RTD peak current, and hence the stable operating point found by the intersection of the two mirrored characteristics is in $PDR1$ of the latch RTD. Thus, the output voltage is low. If the evaluated logic is high, the combined characteristic of the input logic and the load RTD has a peak current greater than the latch RTD, resulting in a stable operating point being found in $PDR2$ of the latch RTD. Thus, the output voltage is high. As long as the clock voltage is maintained high, the output is latched to the evaluated value, irrespective of changes in the input. Fig. 12 shows representative load lines of low, high, and quiescent states of the output latch. The logic functions are designed by using the device area to control the amount of current flowing trough the latch. Fig. 13 shows the load lines of the Schottky diodes and series RTD that form OR, AND, and XOR functions. The RTD-only circuit design approach alleviates problems related to device matching that hamper RTD + transistor designs. However, the lack of current gain in RTD-only circuits limits the logic fanout of the gates. In this instance, the fanout limitation is offset by using a two-stage pipelining scheme for the gates.

2) XNOR Gate Using RTBT's [36]: Seabaugh *et al.* [36] have designed a compact XNOR logic gate using one RTBT and two HBT's. In the XNOR circuit shown in Fig. 14, the RTBT at the output is such that it is turned off for an input voltage (at the base of the RTBT) between 0 and 0.8 V (i.e., both gate inputs are logic high), resulting in the output's remaining high. As the input voltage increases beyond 0.8 V, the RTBT is turned on, and it reaches its resonant peak for an input voltage of 1.7 V (i.e., only one gate input is logic high). This causes the output to go low. Beyond the resonant peak voltage of the RTBT, for an input voltage greater than 2 V (i.e., both inputs are logic low), the RTBT is in the off resonance condition, resulting in the output voltage's being high again. Thus, the XNOR operation is achieved. The circuit uses three transistors and four resistors, as compared to an emitter-coupled logic (ECL) XNOR, which requires three times as many active devices as well as multiple power supplies. By appropriately biasing the output RTBT, bistable operation of the gate can be achieved.

3) Monostable–Bistable Transition Logic Elements [21]: Chen *et al.* [21] have developed a new device structure in which an RTD and a MODFET are connected in parallel. This potentially allows highly compact circuit implementations while also enabling flexible circuit design due to separate optimization of the MODFET and RTD. A logic circuit consisting of an RTD in series with the aforementioned RTD-MODFET structure is called a monostable–bistable transition logic element (MOBILE). Its operating principle is graphically illustrated in Fig. 15. When the bias voltage V_{bias} is less than twice the peak voltage ($2V_p$), there is one stable point (monostable). When V_{bias} increases beyond $2V_p$, there are two stable points in

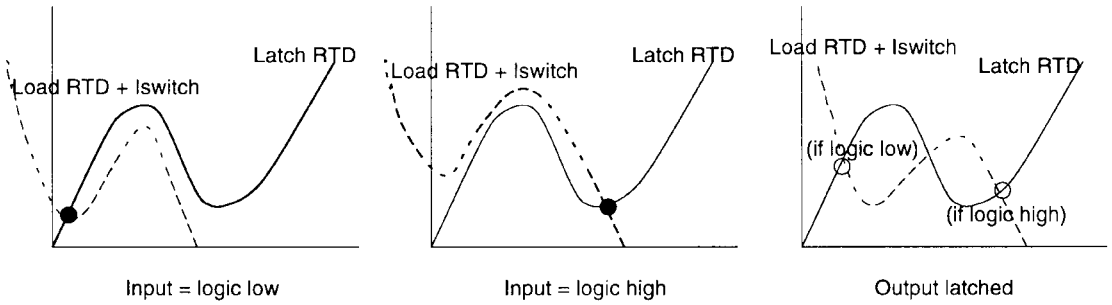

Fig. 12. Load lines for RITD-based latch circuit.

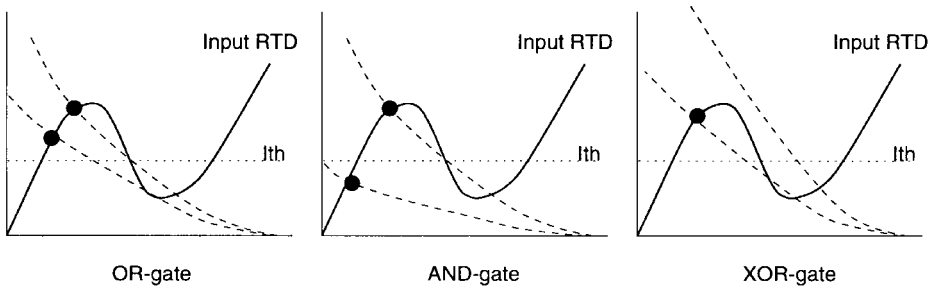

Fig. 13. Load lines for RITD-based logic function circuit.

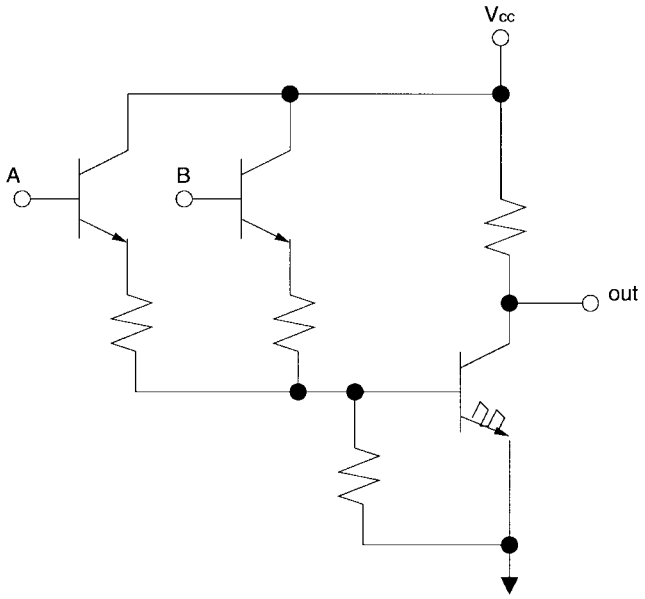

Fig. 14. XNOR gate using RTBT.

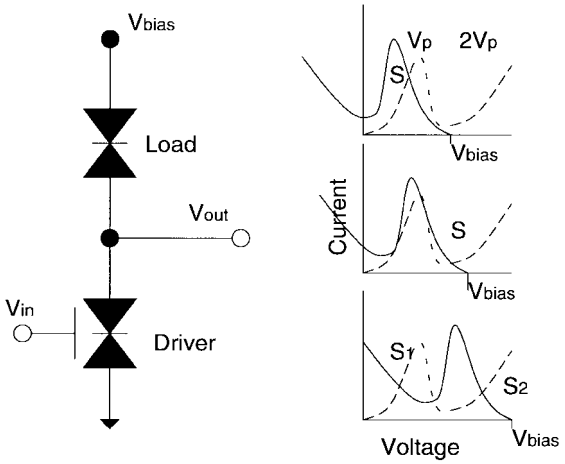

Fig. 15. Operating principle of MOBILE's.

the circuit corresponding to logic zero and logic one. The circuit state after the monostable-to-bistable transition is determined by the difference in the peak currents of the driver and load devices, and hence logic operations can be achieved by controlling the magnitude of the peak current of the RTD in the RTD-MODFET structure with the gate voltage of the MODFET. Thus, by using multiple RTD-MODFET structures along with a suitably biased RTD load, multiple-input logic gates can be formed using MOBILE's. While RTT's have existed for a long time prior to the development of MOBILE structures, the new MOBILE gates offer use of MODFET's and RTD's in a variety of monolithic integrated schemes in which they could be used in conjunction or separately to improve design flexibility.

Maezawa *et al.* [49] have demonstrated a data flip-flop (D-FF) circuit using MOBILE's that operates at 12.5 Gb/s at room temperature. Fig. 16 shows the circuit diagram of this D-FF. It consists of two MOBILE's whose outputs drive a set/reset flip-flop (SR-FF). The SR-FF configuration is similar to the MOBILE elements discussed above except that the RTD areas are relatively small, such that the MODFET's can switch the circuit state without requiring an oscillating bias voltage. At the positive edge of the clock pulse, in accordance with the data input, a MOBILE with a gate input attached to the lower RTD generates a reset pulse, or the other MOBILE with a gate input attached to the upper RTD generates a set pulse. These pulses then switch the SR-FF, and the data are stored at the flip-flop

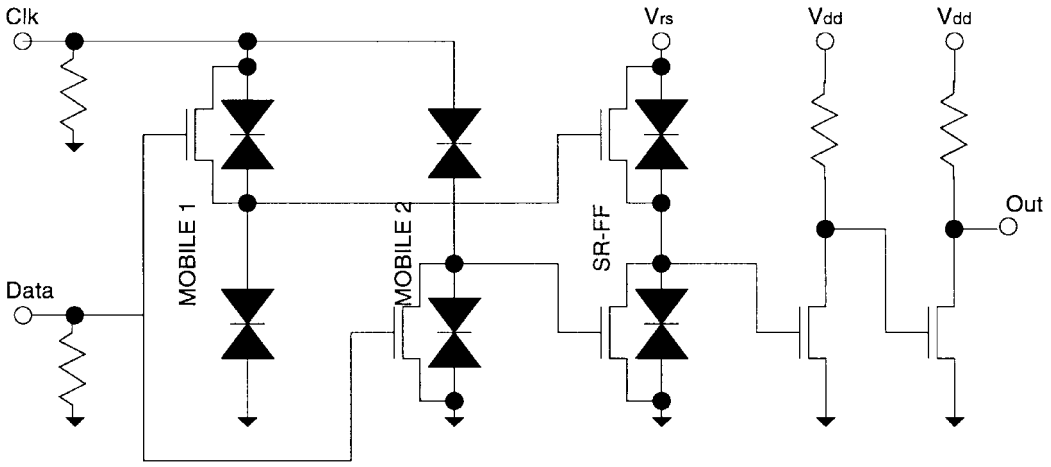

Fig. 16. Circuit configuration of a MOBILE-based D-FF.

output, thus achieving D-FF operation. The circuit uses only ten devices in the core of the D-FF, which is about one-third that of conventional D-FF's. The 12.5 Gb/s operation of the D-FF was achieved using MODFET's of gate length 0.7 μm. Hence, with improvement in process technology and reduction in feature sizes, there is the possibility of achieving further improvement in speed of MOBILE-based digital logic gates.

III. Nanopipelined Computation

The self-latching nature of basic NDR gates, and the ability to implement extremely compact MAJORITY gates in NDR logic, leads to new possibilities for fast adder designs that utilize gate-level pipelining to provide very high addition throughput. Thus, a new system design technique, called nanopipelining, is made possible in which primitive logic gates also perform the latching function without the necessity for external latches. This eliminates delay and area overhead in pipelined systems, thus further improving speed and throughput of deeply pipelined systems over what can be gained as a result of the picosecond switching speeds of RTD's. The block diagram of a 1-bit nanopipelined adder is shown in Fig. 17. The blocks represent bistable logic circuits described in the previous section. BI is a bistable inverter, BNOR2 is a bistable two-input NOR, BNOR3 is a bistable three-input NOR, and BMAJ is a bistable MINORITY/MAJORITY circuit. A two-phase nonoverlapping clocking scheme is used. When Phase 2 (clk/res) is active, Phase 1 (clk/res) is quiescent; and when Phase 1 is active, Phase 2 is quiescent. The sequence of operations in evaluating the SUM and CARRY functions is as follows.

1) Inputs a, b, and c are stable; phase 1 quiescent.
2) Phase 1 becomes active and the outputs $ab, \cdots, carry$ are evaluated.
3) Phase 1 becomes quiescent and the inputs to the second stage are now valid.
4) Phase 2 becomes active and the outputs of the second stage are evaluated.
5) Phase 2 becomes quiescent, Phase 1 becomes active, and SUMB is evaluated. At the same time, new inputs a, b, and c are available. The first stage evaluates these inputs, while the third stage of the adder computes SUMB for the previous set of primary inputs a, b, and c.
6) Phase 1 becomes quiescent and Phase 2 becomes active, evaluating the SUM output and also the outputs of the second stage.

In this circuit, two computations can be active concurrently, and this is how nanopipelining improves the throughput of the system. The use of nanopipelined 1-bit adders in designing fast, larger computing subsystems such as multibit adders and parallel correlators is discussed in the following subsections.

A. Efficient Multibit Adder Design

A multibit adder is an essential part of any general-purpose computer, and a tradeoff is normally made between the speed and area of the adder, since fast adders usually require more hardware [50]. A simple *ripple and carry* adder requires the least number of gates, but the time required to perform a single addition is a linear function of the number of bits in the numbers being added. A *carry lookahead* adder requires more logic but its speed is, ideally, independent of the number of bits being added. However, practical considerations, such as fan-in and fan-out limitations, cause the carry lookahead scheme to be slower than in the ideal case. Variations on this theme, such as the Ling adder [51], seek to overcome the fan-in limitations by using WIRE-OR properties of certain logic families along with some algebraic manipulation of the terms in the carry lookahead expressions. Another type of fast adder makes use of chains of CMOS transmission gates to form the SUM and CARRY, in effect replacing multiple gates with a single complex gate. These adder architectures are technology specific, however, and cannot be used if the technology does not permit WIRE-OR or the chaining together of a large number of transistors in series.

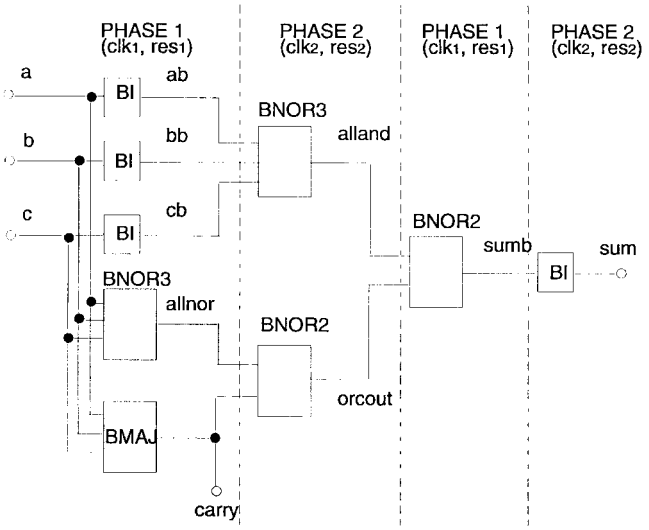

Fig. 17. A 1-bit nanopipelined adder with four stages and a two-phase clock.

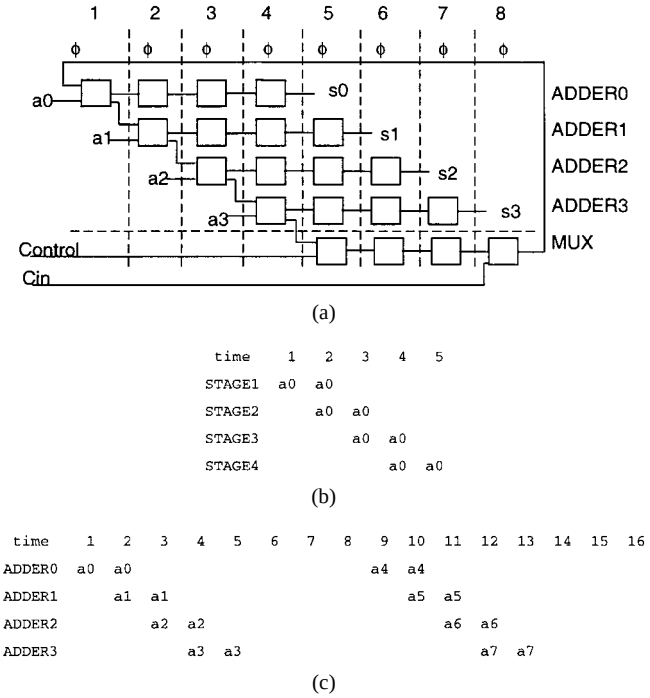

Fig. 18. (a) A 4-bit nanopipelined adder schematic. (b) Data flow through adder pipeline stages. (c) Timing for multibit addition.

The nanopipelining concept can be used to design fast multibit adders using only a small number of cyclically connected bistable full adders. A 64-bit adder is chosen as the vehicle to explore the design problem. Fig. 18(a) shows a 4-bit ripple CARRY adder using NDR devices. Each adder has four stages corresponding to the four levels of the true-bistable SUM circuit. The CARRY output is generated in the first stage, while the SUM output is generated in the fourth stage. Fig. 18(b) shows how the data flow through one stage of the pipeline. Since two-phase clocking is used, the data at the input change once every two time periods, where a time period in this context is one-half the period of either of the two-phase clocks. Fig. 18(c) shows the data at the input of the first stage of each of the four 1-bit adders as a function of time. It may be noted that the name a_i refers to the two input bits to be summed and that the least significant bits are a_0. The feedback scheme shown in the figure feeds the CARRY bit from the fourth adder back to the input of the first adder. Since the CARRY bit is delayed by four clocks, the bits a_4 can enter the adder only at time $t = 9$. Hence, the adder utilization is low, as can be seen from Fig. 18(b) and (c). This situation can be remedied by interleaving four different additions. The interleaved serial-parallel data format allows four different additions to proceed simultaneously. A 64-bit addition has a latency of 63 time units, but the throughput of the adder is increased to one 64-bit addition every 16 time units.

A conventional serial-parallel ripple carry adder that performs 4-bit ripple carry addition on a series of 4-bit-wide inputs, with the carry from the most significant bit being clocked and fed back, has a latency of 63 t_c, where t_c is the time required to generate the bit-wise carry (at least three gate delays for each bit) and a throughput of one 64-bit addition every 64 t_c time units. The nanopipelined NDR adder architecture improves the throughput to one 64-bit addition every 16 t_{cndr} units, where t_{cndr} is the bit-wise carry generation delay and is equal to one gate delay instead of three gate delays in conventional logic. Hence, the nanopipelined architecture increases the throughput by a factor of 12 without any significant increase in area, as compared to the conventional serial-parallel pipelined addition scheme.

The number of gates required is about 30, compared to the 600 required for carry lookahead addition. The complete 64-bit pipelined adder uses four identical single-bit adders with the carry-out of each adder being connected to the carry-in of the next adder in a cyclic fashion. The 64-bit numbers are fed to this adder in a bit-serial fashion, and four different additions are carried on simultaneously in the four pipeline stages. The effective throughput of the pipeline system is thus one new 64-bit addition for every 16 time units or one new 32-bit addition every eight time units. With a clock period of 100 ps, this gives an effective throughput of one 32-bit addition every 0.8 ns or one 64-bit addition every 1.6 ns. Since the entire adder contains only about 30 gates, with an area of 26 $\times$ 36 μm per gate, the maximum interconnect length is around 300 μm. Using a capacitance factor of 4 fF/100 μm for GaAs [52], the total line capacitance is only 12 fF, or about a third of the input capacitance of a single HBT. Therefore, the effect of interconnect delay is minimal in this design. The effect of line inductance for such line lengths is also negligible.

Hence, we see that nanopipelining can improve the throughput of multibit adders due to elimination of area and delay overhead of pipeline latches that are present in conventional designs. In particular, the speedup proffered by nanopipelining is highly evident in circuit systems that use long, cascaded adder trees. In the following subsection, we discuss the implementation of a 32-bit parallel correlator, an important constituent block of a code division

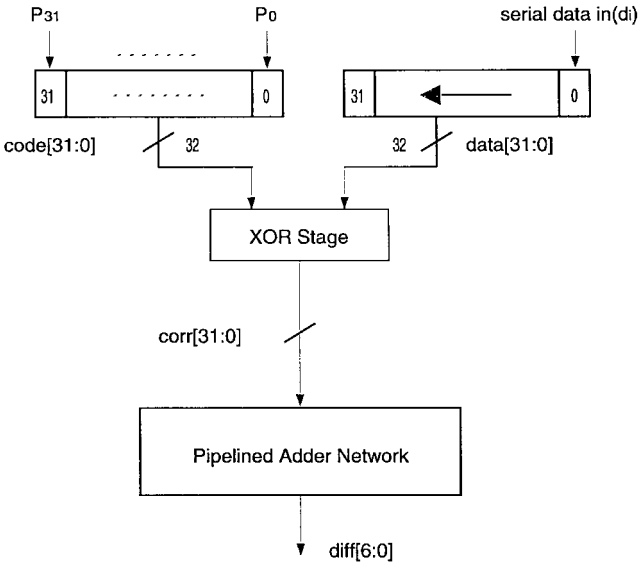

Fig. 19. Block diagram of nanopipelined correlator.

multiple access (CDMA) system, that exploits the system-level advantages of RTD-based nanopipelined adders.

B. System Application: Nanopipelined 32-Bit Parallel Correlator

CDMA systems [53] provide highly secure, reliable, and noise-free transmission between two transceivers. However, CDMA systems typically use very long pseudo-noise (PN) sequences (>1000 chips) and thereby require a tremendous amount of bandwidth since each transmitted bit is encoded into as many chips as the PN code length. Thus, to achieve reasonable speed of transmission and reception, it is imperative that high-performance circuits be used that maximize the symbol transmission rate. Quantum effect circuits can play a vital role in improving the speed of CDMA systems. High-throughput CDMA systems that use long PN sequences require very high-speed parallel correlators. Kulkarni *et al.* [54] have designed an RTD + HBT-based 32-bit correlator consisting of a nanopipelined adder network that has a simulated effective throughput of one 32-bit correlation every 100 ps. The correlator is an ideal vehicle for demonstrating the advantages of NDR logic since it utilizes long adder trees that can efficiently be implemented using nanopipelining logic of RTD-based circuits.

The block diagram of the pipelined correlator is illustrated in Fig. 19. A 32-bit latch holds the PN sequence. The input is a serial bit stream that is fed to a 32-bit shift register. The 32-bit latch and 32-bit shift register are each composed of 64 bistable RTD + HBT inverters. A pair of cascaded bistable inverters, each operating on single, separate phases of the two-phase clock, form the basic 1-bit latch. The 32-bit raw correlation vector is generated by performing a bit-wise XOR operation on the PN sequence latch output and the most recent 32 bits of the sampled signal available at the shift register output. The raw correlation vector is automatically latched at the output of the XOR network due to the use of self-latching gates. This vector forms the input to the pipelined adder network that determines the difference between the number of ones and zeroes in the raw correlation vector. The result of this operation is the correlation value between the incoming signal and the resident PN sequence and is determined for the 32 most recent data bits at every clock cycle. This value ranges from −32 to +32. The functional description of the correlator is illustrated in (14)–(18)

$$data[31:0] = \{D^{32}(d_i),\, D^{31}(d_i),\, \cdots,\, D^{1}(d_i)\} \tag{14}$$

$$code[31:0] = \{D^{1}(P_{31}),\, D^{1}(P_{30}),\, \cdots,\, D^{1}(P_0)\} \tag{15}$$

$$corr[31:0] = code[31:0] \oplus data[31:0] \tag{16}$$

$$sum[5:0] = \sum_{i=0}^{31} corr[i] \tag{17}$$

$$diff[6:0] = 32_d - 2 \times sum[5:0]. \tag{18}$$

Here, $D^i(s)$ represents the value of signal s at i clock cycles prior to the current input.

1) Pipelined Adder Network: The adder network consisting of 26 nanopipelined full adders, 11 nanopipelined half adders, and 36 bistable inverters is illustrated in Fig. 20. The adders used in the design have complemented SUM and CARRY outputs in order to reduce pipeline latency. The input to the adder network is the raw correlation vector generated by the 32-bit bistable XOR network. The circuit performs 18 stages of addition to generate a 7-bit result, which is the difference between the number of ones and number of zeroes in the correlation vector. Since each stage is nanopipelined, the throughput of the circuit is one 32-bit correlation every cycle. Since the seven bits of the adder network output are not simultaneously generated, however, bistable inverters are required to synchronize the bits such that all seven bits of a correlation appear in order at the output of the correlator. The least significant bit of the correlation value is always zero since the difference between the number of ones and number of zeroes in a 32-bit vector is always even. The pipelined adder network essentially sums up the number of ones in the correlation vector. Bits zero, one, two, three, and four of the sum of ones directly translate to bits one, two, three, four, and five of the difference between number of ones and number of zeros. Bit six of the correlation value is computed while bit five of the sum of ones is being generated by connecting the CARRY input of the final full adder to V_{cc}. This achieves the twos complement subtraction required for computing the difference between the number of ones and number of zeroes in the correlation vector. No additional pipeline stages are required for this conversion. The functional simulation of the 32-bit parallel correlator is shown in Fig. 21. The PN sequence for this simulation is chosen to be AAAAAAAA Hex. The input is a pattern of alternating ones and zeroes, which results in the 32-bit shift register output's toggling between AAAAAAAA Hex and 55 555 555 Hex at each cycle. This causes the raw correlation vector to alternate between all ones (FFFFFFFF Hex) and all zeroes (00 000 000 Hex) with each cycle. Thus, the desired correlation difference is +32 decimal and −32

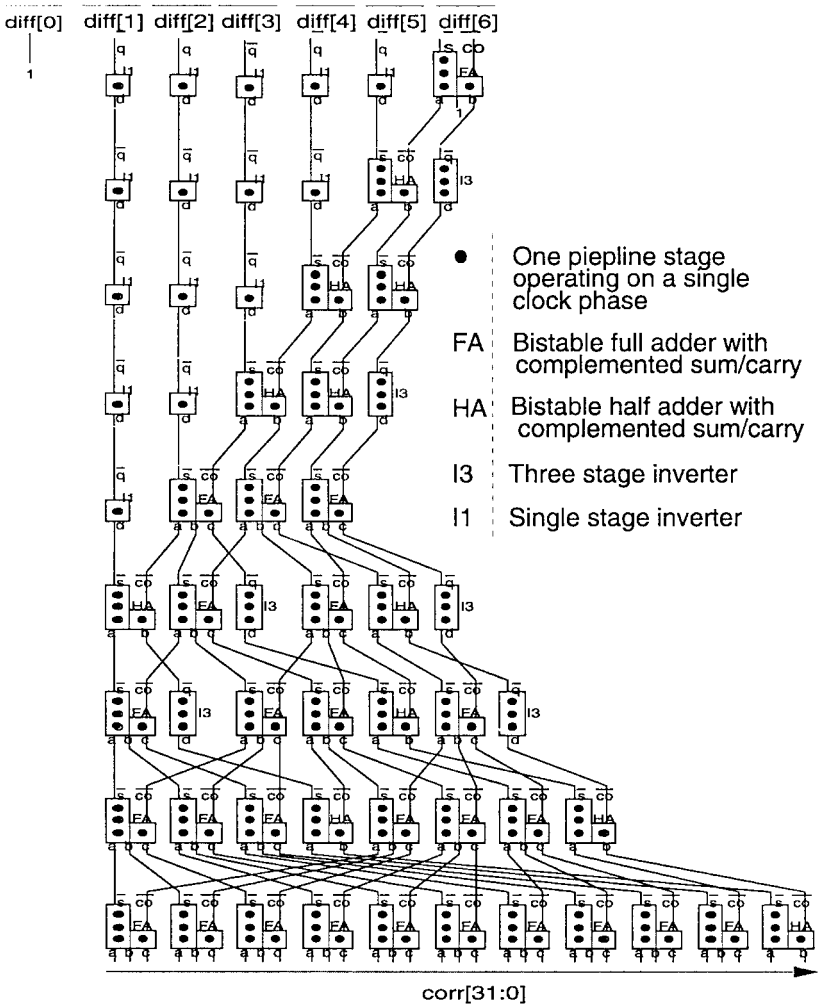

Fig. 20. 32-bit pipelined adder network.

decimal, respectively, for the two cases above, as seen in the simulation.

2) Qualitative Comparison with Conventional Technology: Since RTD + HBT/MODFET logic circuits are at present unable to achieve the same integration levels as CMOS IC's, their potential benefits at the system level can only be qualitatively assessed.

Two well-known schemes for speeding up evaluation of arithmetic functions are pipelining and parallelization. Parallelization increases the throughput of a system by using extra hardware to perform several operations simultaneously, while pipelining increases the throughput by splitting the combinational logic into several sequential stages separated by latches so that each stage can carry out a different computation. The main disadvantages of pipelining are the fact that any single computation still takes the same or more time as the nonpipelined version, while the extra area required for the latches limits the number of pipeline stages and the total throughput.

Consider, for instance, a combinational logic block that has n stages for a total delay of $n \cdot t_c$ time units. Assuming that this logic block can be split into any number of stages i from one through n, with equal stage delays $n \cdot t_c/i$ with i latches separating the stages, the total delay per stage is $t_L + n \cdot t_c/i$, where t_L is the latch delay. The computational throughput improves from $1/(n \cdot t_c)$ to $1/(t_L + n \cdot t_c/i)$ but the latency of the computation deteriorates from $n \cdot t_c$ to $n \cdot (t_c + t_L)$. The area increases from a_c (area of combinational logic alone) to $a_c + k \cdot i \cdot a_L$, where a_L is the area of a single latch, i is the number of latch stages, and k is a constant representing the number of latches per stage. In the limit where $n = i$, the ideal throughput is $1/t_c$, but the best achievable actual throughput is $1/(b \cdot t_c + t_L)$, where $b \cdot t_c$ is the longest stage delay, assuming the total combinational delay cannot be divided equally among the stages. There is a direct tradeoff between the achievable throughput and the extra area of the latches. Further, the latch delay factor t_L creates an absolute upper bound on the throughput whenever $t_L \gg b \cdot t_c$. Latching schemes such as the Earle latch [55] seek to avoid the extra delay due to the latch by incorporating two levels of logic into the latch itself. However, this results in an enormous increase in area. Hence, pipeline designs with conventional logic seek tradeoffs between space and time and seek to optimize the design corresponding to some metric, such as the AT^2 metric [56]. The use of true-bistable NDR logic results in

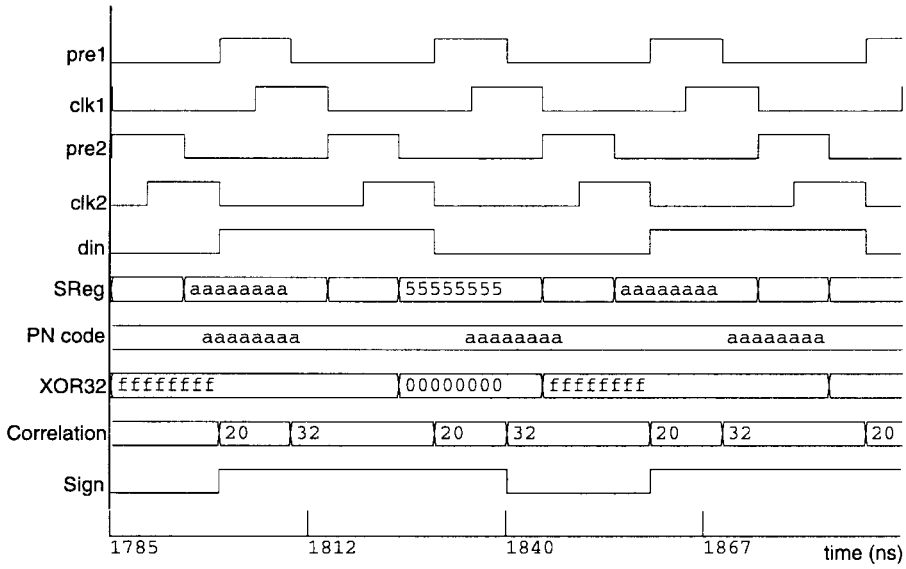

Fig. 21. Functional simulation of correlator in verilog.

Table 4 Circuit Compaction—RTD + HBT Versus CMOS

Circuits	CMOS	RTD +HBT
Bistable Majority	18	5
Bistable Full Adder	68	34
32-bit Pipelined Correlator	6000	2000

Table 5 RTD + HBT Circuit Parameters (Simulation Results)

	Bistable Majority Gate	Bistable Full Adder	32-bit Parallel Correlator
Power	0.5 mW	5 mW	320 mW
Speed	20 GHz	10 GHz	10 GHz
Power-delay	0.025 pJ	0.5 pJ	32 pJ

improved pipeline performance since the extra latch delay t_L is zero. This results in almost ideal pipeline throughput. Further, the area cost of latches is zero since every logic element is self-latching. Thus, RTD-based circuits promise considerable improvement in system speed, especially for deeply pipelined circuits. Table 4 compares the device counts of CMOS and RTD + HBT implementations of digital logic circuits discussed earlier. Note that the bistable logic mode is being used, and therefore for CMOS circuits, additional latches are required to achieve bistable operation in basic circuits such as the MAJORITY gate and the full adder.

Table 5 shows the simulated speed and power (at the operating frequency mentioned in the table) values for some RTD + HBT circuits. These statistics are only intended to outline the promise of RTD-based circuits, since medium- or large-scale cointegration of RTD's and HBT's is not feasible as yet.

The nanopipelined 32-bit correlator serves as an example of the potentially dramatic improvement in power-delay products of system-level designs that might utilize RTD + HBT circuits. The fewer number of devices used in the RTD + HBT correlator also implies a reduction in wiring lengths, translating to smaller parasitics and hence lower interconnect delays at the system level as compared to a conventional implementation.

In this section, we have seen the utility of bistable-mode RTD-based circuits in efficient implementation of high-throughput pipelined computing systems. Another significant advantage of resonant tunneling devices is the multistate nature of MRTD's, which can provide compact and high-speed multivalued circuit alternatives for conventional binary circuits. In the following section, we discuss novel multiple-valued circuit applications of resonant tunneling devices that have some demonstrable advantages over their binary counterparts.

IV. Multiple-Valued Logic Using Resonant-Tunneling Devices

MVL has been shown to effectively reduce the number of interconnects in digital circuits [57]. Interconnection length and complexity will be the dominant limiting factor of integrated circuit performance as device dimensions continue to shrink while chip areas continue to grow. The enhanced signal encoding efficiency of MVL results in a factor of $\log_2 r$ reduction in the number of wires for a radix-r number system as compared to an equivalent binary logic circuit. This in turn facilitates increased speed of operation and decreased power consumption in a logic circuit. However, implementation of MVL systems using conventional technologies such as CMOS has yet to provide a viable alternative to binary logic because the individual MVL building blocks tend to use a large number of devices. They also operate in the threshold mode, as a result of which such circuits have poor operating speeds and noise margins. To reduce device counts of MVL circuits using MOS devices [58], transistors with varying threshold voltages need to be implemented on the same die so as to vary switching points of the devices. This requires different levels of doping across the chip and hence

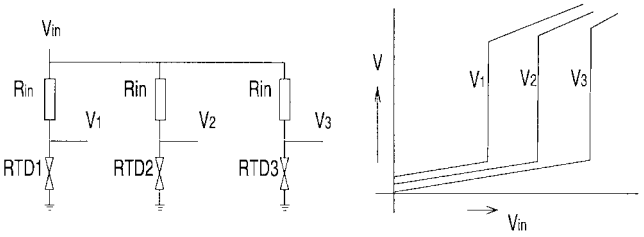

Fig. 22. RTD switches.

imposes severe constraints on the process technology. The advent of MRTD's has revived interest in MVL systems due not only to the multiple-folded nature of the I–V characteristics of MRTD's, which facilitates compact MVL circuit implementation, but also to the picosecond switching speed of MRTD's, which vastly improves performance of hitherto slow MVL circuits.

With the successful application of RTD's in building multiple-valued memories [8], [9], it is natural to seek applications of RTD's in multiple-valued logic systems. Micheel and Paulus [30] designed a generic single-input, single-output quaternary logic gate using tailored RTD's and current switches. The basic RTD subsystem consists of an RTD in series with a resistor R_{in}. When the applied voltage increases above a certain threshold ($V_p + I_p R_{in}$) determined by the RTD peak current (I_p) and voltage (V_p) and the value of R_{in}, the voltage across the RTD switches abruptly. The peak voltage of an RTD is determined by the process/material parameters, as is the peak current density, but the peak current itself can be varied by varying the area of the RTD. Hence, the same input voltage is applied to three different RTD-resistor combinations (same R_{in}, different I_p), and each RTD switches at a different voltage (see Fig. 22). To implement a gate such as $g(1, 0, 3, 1)$, which has outputs of one, zero, three, and one for inputs of zero, one, two, and three, respectively, the RTD branch voltages are connected to different current switches whose currents are then summed. Similar ideas are used in a more recent paper by Micheel [59] to implement some functions used in MVL addition.

In [31], Hanyu *et al.* describe a novel approach to building programmable logic arrays (PLA's) using RTD's. A four-valued RTD literal circuit, in which the peak position of the RTD is adjusted by varying the quantum well width, forms the basis of the multiple-valued PLA. Two four-valued literal circuits are combined to implement a universal literal circuit, illustrated in Fig. 23. Together with the universal literal circuit, an AND circuit and a linear summation circuit, implemented using wired logic or current-mode wired linear summation, can form any n-variable, four-valued PLA, shown in Fig. 24. The four-valued RTD-based PLA requires half as many input lines and devices as compared to an equivalent current-mode CMOS four-valued PLA implemented using variable transistor thresholds as the programming method. The difference arises due to the fact that the CMOS PLA implementation requires four input lines per variable in order to generate four kinds of literals, which, as mentioned earlier, can be accomplished by a combination of just two different RTD-based literal circuits.

Tang *et al.* [32] present a multiple-valued RTD-based decoder circuit that operates in the current tapping mode. In MVL circuit applications, a decoder can be used to implement a multiplexer/demultiplexer or transmission gate. The decoder circuit consists of the literal function, whose outputs are transmitted by a pass gate circuit according to the decoder function. The decoder circuit of [32] is illustrated in Fig. 25. The design uses two RTD's with different peak values and three n-channel (N)MOS transistors to generate three literals. The NMOS transistors bleed the bias current I_{bias}. The current through these transistors is determined by the reference voltages V_{r1} and V_{r2} and the state of the RTD's, i.e., whether they are operating in PDR region 1 or PDR region 2. Op-amps are used at the circuit output for current-to-voltage conversion. The input select pulse has three levels—zero, one, and two. When the select pulse is at level 0, an inverter is used to control the gate voltage of NMOS transistor $M0$, allowing maximum current flow for the level 0 input, which causes V_0 to be the largest among the output voltages. When the select pulse is at level 1, RTD1 switches to PDR region 2, thus slightly raising the gate voltage of transistor $M1$ due to which $M1$ carries a larger current as compared to $M2$. Hence, V_1 is the maximum output voltage. On application of the level 2 select pulse, both $RTD1$ and $RTD2$ switch to PDR region 2. In this situation, the reference voltages V_{r1} and V_{r2} are such that $I_1 < I_2$, and most of the current I_{bias} flows through $M2$, causing V_2 to be the largest output voltage. Thus, for every select level, there being only one output voltage that is the largest, the decoder function is achieved.

Baba and Uemura [60] introduce a new GaAs-based device called the multiple-junction surface tunneling transistor (MJ-STT) that is well suited for MVL circuit design. It combines the multiple stable states found in MRTD's with the flexibility of a third device terminal that acts as a controlling gate input. Fig. 26 shows a tristable circuit designed using an MJ-STT connected in series with a load resistor, as well as the corresponding load lines. For an applied gate bias voltage of 0.3 V, three stable operating points are observed in the PDR regions intersected by the load line. Circuit operation requires an initial low-going reset pulse applied to the gate input, which causes the output to go high. The circuit operating point is in PDR 3. Following the reset pulse, a set pulse is applied to the gate input of the MJ-STT. The set pulse has three possible logic values—zero, one, and two—corresponding to voltage levels of −0.05, 0.1, and 0.25 V with respect to the bias voltage. Depending on whether the set pulse is at logic zero, one, or two, the operating point of circuit is in PDR 3, PDR 2, or PDR 1, respectively, corresponding to output voltage levels of 0.45, 0.3, or 0.15 V. When the set pulse is turned off, the bias voltage on the gate input maintains the evaluated output state, thus achieving tristable circuit operation.

A good use of the multistate nature of MRTD + transistor logic is in implementing fast adder circuits that use internal

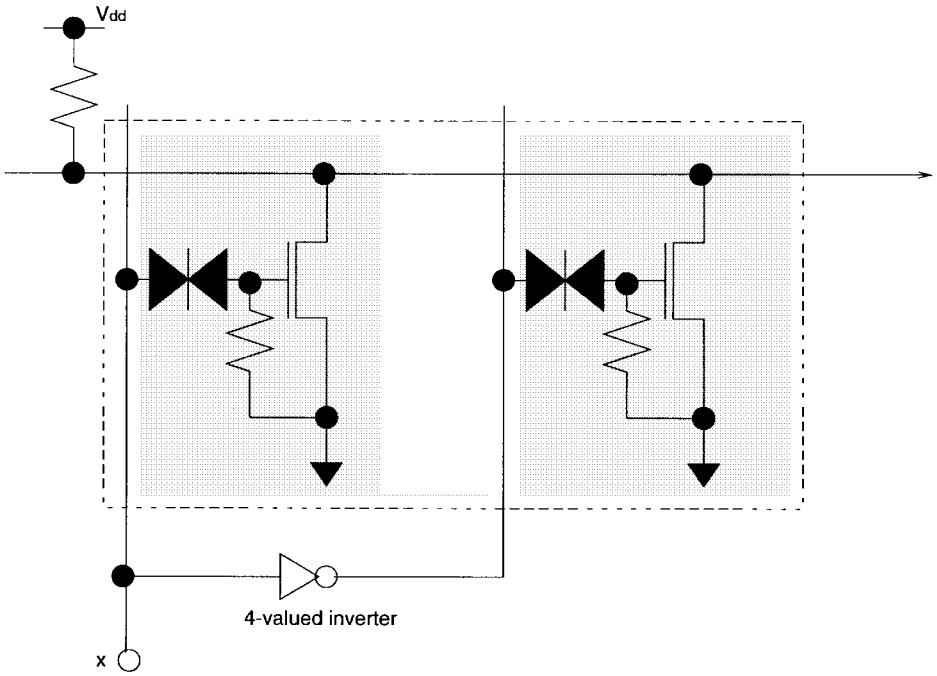

Fig. 23. Four-valued universal literal circuit.

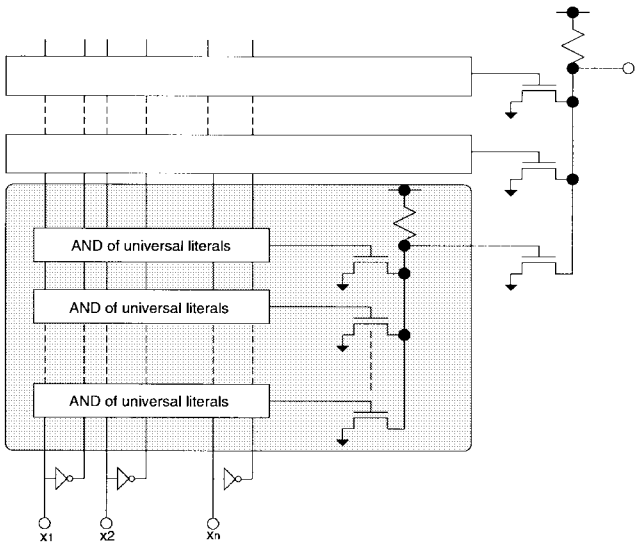

Fig. 24. Block diagram of a multiple-valued PLA using RTD's.

multivalued redundant number systems [61], [62]. Such number systems offer a means of adding numbers where there is no delay due to carry ripple regardless of word length. This has the potential of tremendously speeding up arithmetic computation. In [63], Lin discusses numerous other applications of resonant tunneling devices for multivalued applications.

In the following subsections, we discuss a multiple-valued multiplexer, a mask-programmable MVL gate, and a step-down counter that have been designed using RTD's in conjunction with high-performance transistors. These circuits demonstrate the feasibility of MVL using resonant tunneling devices and offer considerable improvement in performance and circuit size as compared to conventional MVL circuit implementations.

A. Multiple-Valued Multiplexer

The MVL gate designed by Micheel and Paulus [30] is based mainly on current switches and uses RTD's only to provide sharp switching points. A similar effect could be achieved by using conventional transistor inverters with varying thresholds. Chan *et al.* [64] describe a multiple-valued logic multiplexer that uses the RTD characteristic to pick specific ranges in the input voltage. Although this design uses RTD + resistor branches, as in the previous gate, the RTD branches are all coupled so that when one switches on, the others switch off. Furthermore, this circuit is a multiple-input circuit, unlike the previous circuit, which is single input.

Fig. 27 shows the RTD selector and its operating principle. When the input voltage to the RTD is in a specific narrow range, the HBT is turned on and the output voltage goes low. In the complete multiplexer circuit (see Fig. 28), four such RTD selectors are coupled together through the use of resistors R_2, R_3, and R_4. The input voltage to each successive stage is a diminished version of the *select* input voltage, due to the voltage drop in the resistors R_2, R_3, and R_4. These resistors are chosen so that each HBT connected to the RTD branches turns on at different ranges of the input voltage. Further, when one RTD switches abruptly to the lower base voltage state, the current in the next RTD branch increases suddenly, causing the corresponding HBT to switch *on* immediately. The outputs of all the RTD branches are connected to current switches, whose *on* currents are proportional to the input voltages. The currents are all summed to produce the output voltage dropped

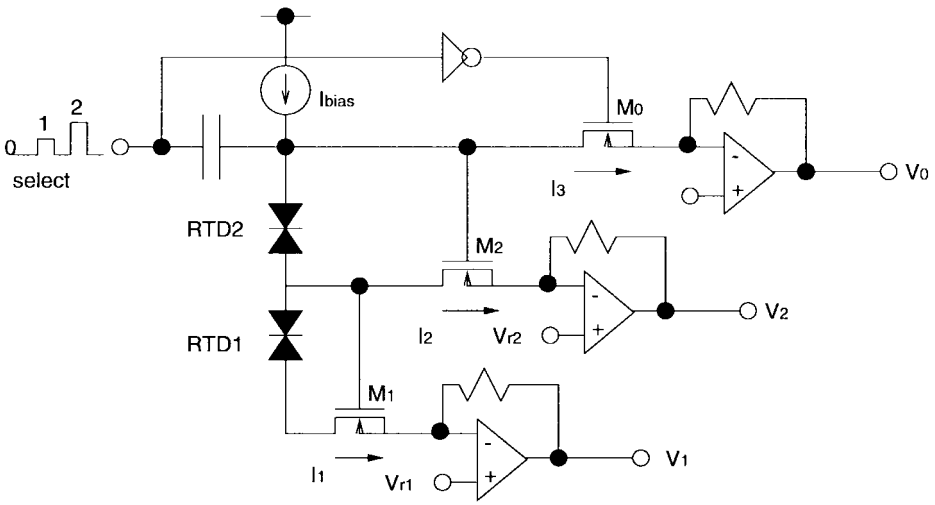

Fig. 25. RTD-based multiple-valued decoder circuit.

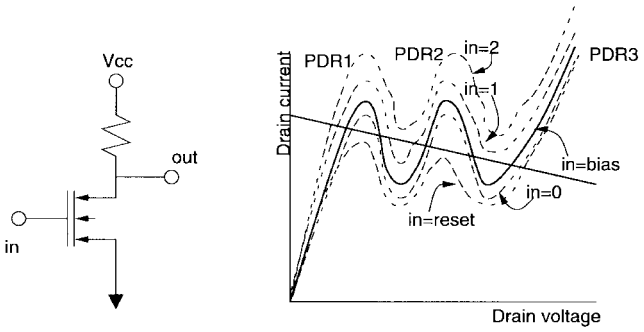

Fig. 26. MJ-STT tristable circuit and load lines.

across the resistor R_{out} in Fig. 28. The RTD branches ensure that all but one of the summed currents are zero and the other summed current is proportional to the selected input voltage. By properly choosing the output resistance, the output voltage is made equal to the selected input voltage.

The RTD multiplexer is thus a four-input analog multiplexer with a single multiple-valued select line. When the input signals are restricted to four different logic levels, the multiplexer becomes a four-valued T-gate [65]. The T-gate is an extremely versatile building block for multiple-valued logic, and any multiple-valued function can be implemented using T-gates alone (along with constants).

Experimental results for a bread-boarded multiplexer acting as an analog channel selector are shown in Fig. 29. Only two input channels and the output are shown in the trace. Note that a fast asynchronous pulse (not shown) is also being applied to the reset input in order to eliminate hysteresis.

The RTD + HBT multiplexer uses four RTD's, 21 HBT's, and 16 resistors, while a CMOS circuit with equivalent functionality (binary, 2-bit, 4 : 1 multiplexer) would require 44 transistors (MOSFET's). The savings in area increase with higher valued logics. For an eight-valued T-gate (8 : 1 multiplexer), the multiplexer design described above can be extended by using eight literal-pass gates with tighter margins on input voltages. Such a multiplexer would use 25 transistors and 32 resistors as against 118 MOSFET's for an equivalent CMOS implementation (binary, 3-bit 8 : 1 multiplexer).

B. Mask Programmable MVL Gate

A promising niche application of high-functionality MVL circuits is in the area of programmable logic [66] and synthesized logic. Chan *et al.* [67] describe a compact one- and two-input multiple-valued logic gate, which can be mask programmed or synthesized following simple rules. The mask programmable design is ideal for use in gate arrays not only because its MVL input and output lines require less space to route than its binary counterparts but also because even the functionality of these gates can be changed at the last mask levels. This provides tremendous design flexibility while vastly reducing design turnaround times. The design can be implemented with fewer transistors than other reported methods because of the use of RTD's.

An r-valued, n-variable function $f(X)$, where $X = \{x_0, x_1, \cdots, x_{n-1}\}$ with x taking on values from $R = \{0, 1, 2, \cdots, r-1\}$, is a function $f: R^n \Rightarrow R$, which maps n-inputs of radix-r numbers into one output of radix-r number. The one-input, four-valued logic gate described in this section is a circuit that realizes such a function in the voltage domain.

Another function $g(Y)$ is used to describe each individual gate. A gate $g(Y)$, where $Y = \{y_0, y_1, \cdots, y_{r-1}\}$, is a gate that maps $i \Rightarrow y_i$. For example, a four-valued cycle gate can be described by $g(1, 2, 3, 0)$ (Fig. 30).

The decoder generates a logic high in one of its four outputs (L-lines) based on the input's logic level. It is made up of four literal circuits, each turning on at a different nonoverlapping voltage range. Literals can be implemented very efficiently using a vertical integrated structure of an RTD and an HBT that forms an RTBT. The literal circuit consists of an RTBT inverter whose output is connected to a normal inverter. R_{out} has to satisfy the following

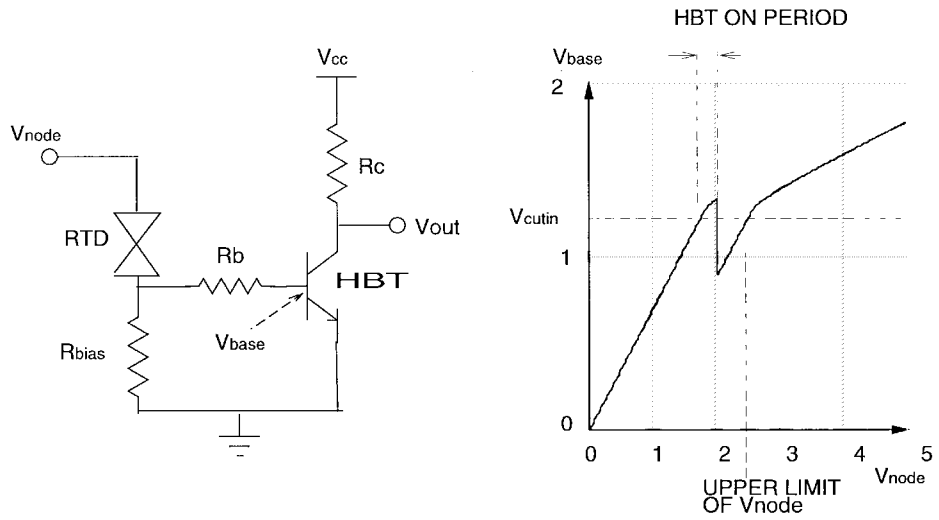

Fig. 27. RTD selector circuit and operating principle.

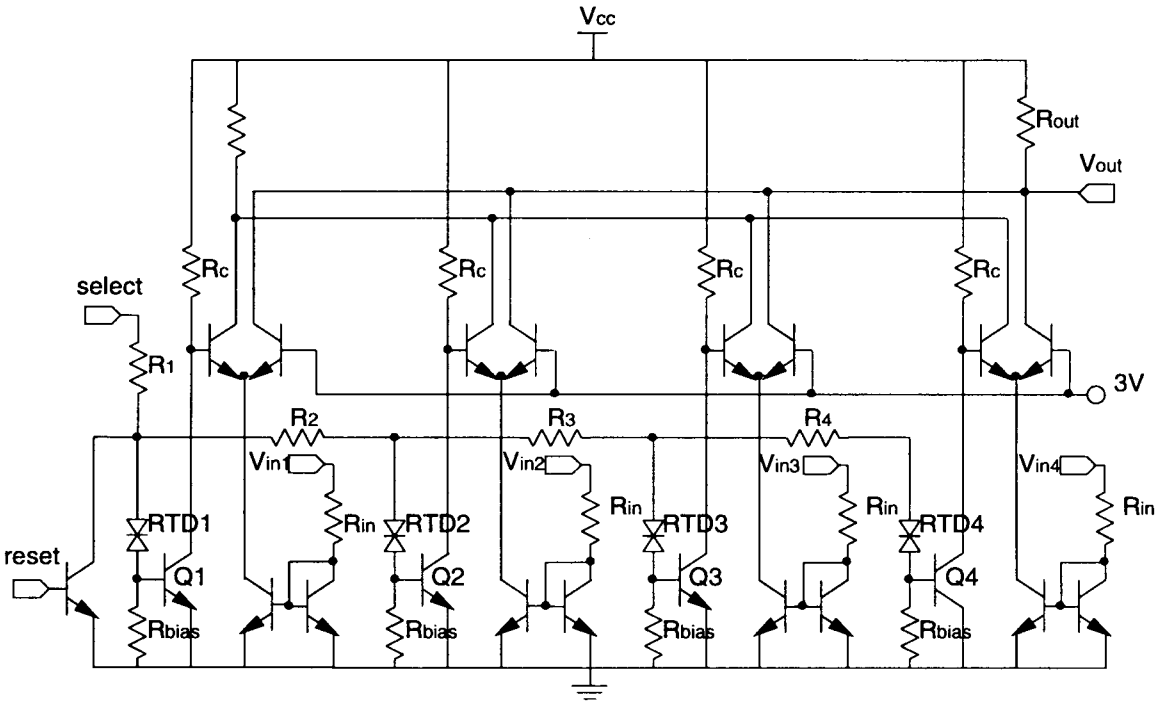

Fig. 28. Four-input RTD multiplexer.

inequality:

$$R_{out} > \frac{V_{cc}}{I_{peak}(\text{of RTD})}$$

to allow V_{out} to drop below the turn-on voltage of the next stage inverter before going into region 3, described above. It is also important that $R_{emitter}$ be large enough to prevent a second literal from being generated at V_{out}. Transistors connected to the output of the literal circuit in an emitter follower configuration not only improve the current drive of the output but also act as a MAX circuit to allow multiple L-lines to connect to a single Q-node (e.g., $L0$ and $L2$ in Fig. 30). A decoder is formed when the literal circuits are connected together at their inputs through a chain of diodes. The diode chain separates the node voltages by intervals of V_d. Identical literals connected to different nodes thus turn on at different applied voltage intervals. The quantizer converts a logic high on one of its inputs (Q-nodes) to a predefined voltage level. Together, the gate can be mask programmed by connecting each L-line to some Q-node. It is designed as a current mirror with multiple input resistors of different values. The fact that only one decoder output is high and all the others are reverse biased at any one time simplifies the design of the quantizer.

A one-input MVL programmable gate has been breadboarded with discrete NPN transistors and RTD's fabricated at the University of Michigan (UM1174). The input and output traces of the MVL gate are shown in Fig. 31.

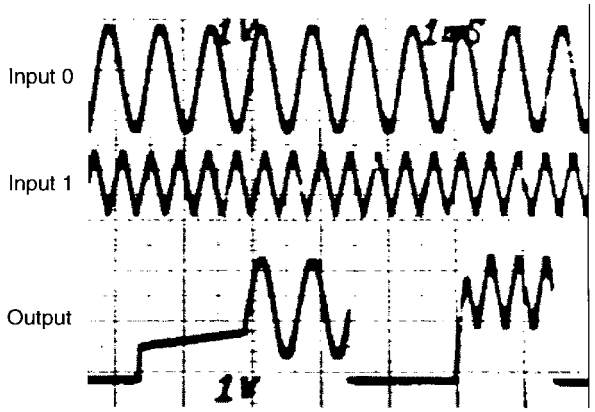

Fig. 29. Experimental results of the bread-boarded RTD multiplexer.

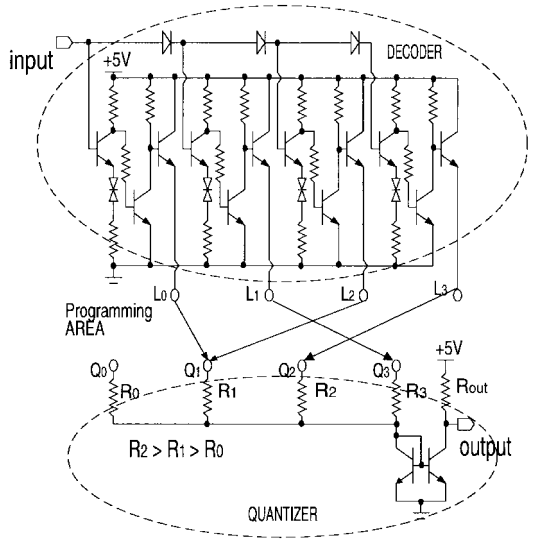

Fig. 30. One-input, four-valued logic gate.

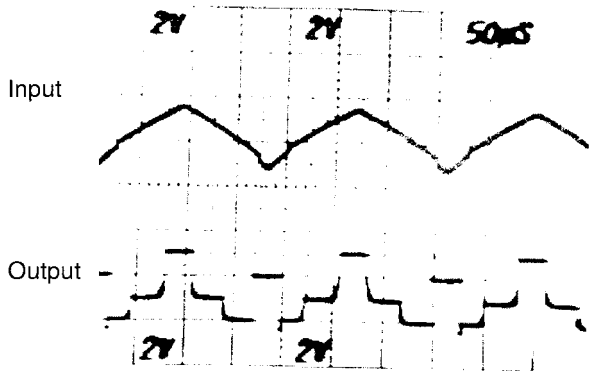

Fig. 31. Experimental result of MVL programmable gate.

C. Multivalued Step-Down Counter

Counters are an integral part of most digital systems, and RTD + HBT MVL circuits allow extremely compact counter circuit implementation, which ultimately translates into improved functional density of VLSI circuits. Bhattacharya *et al.* [68] describe a compact four-valued down counter using RTD's and HBT's. A similar RTD-based

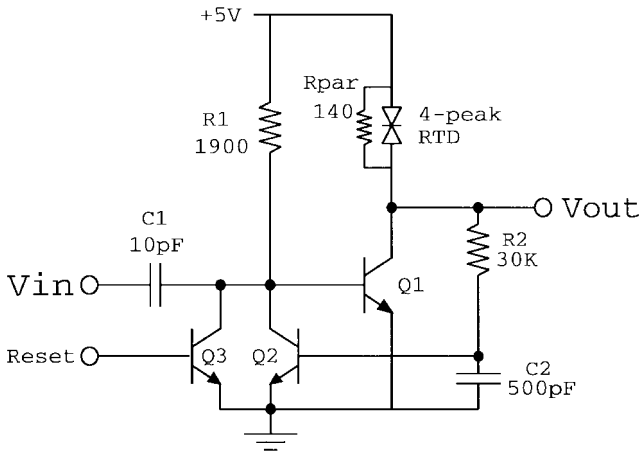

Fig. 32. Circuit diagram of multivalued counter.

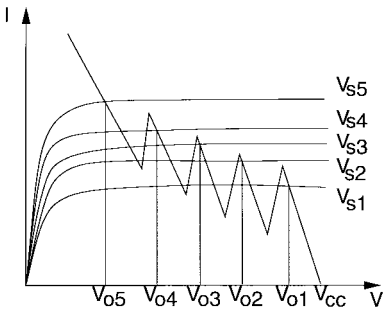

Fig. 33. Load lines for the multivalued counter.

multiple-valued counter has also been implemented by Kuo *et al.* [69]. It, however, uses seven transistors, as compared to the three-transistor design in [68].

The circuit diagram for the step-down counter is shown in Fig. 32. The input capacitor $C1$ acts as a high-pass filter and generates spikes at the positive and negative going transitions of the input clock signal. Transistor $Q3$ is used to reset the circuit after the full count has been completed. The four-peak RTD in conjunction with the transistor $Q1$ form the portion of the circuit that generates the output count. As the node voltage at the base of $Q1$ is gradually increased at each clock pulse, the collector current of $Q1$ increases as the MRTD jumps one peak at each clock pulse. As a result, the output voltage of the circuit decreases, step by step, through as many levels as the number of peaks in the MRTD I–V characteristic. The operation is illustrated through the load lines in Fig. 33, which also shows the desired current pulses through the RTD at different base voltages for $Q1$.

$R2$, $C2$, and $Q2$ form a feedback circuit that provides an output state dependent voltage feedback, which, when superimposed on the input spike, will produce a progressively increasing voltage at the base of $Q1$, which causes the counter output transitions. The level of the reset input should be in between the lowest and the second lowest output voltage levels. As soon as the output falls below this value, the latched comparator (clocked by the input clock) generates a "high" pulse that turns on $Q3$ and causes the voltage at the base of $Q1$ to go low, thus turning it off and

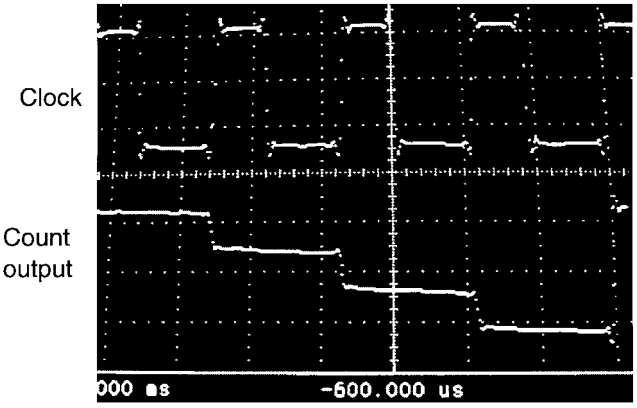

Fig. 34. Oscilloscope traces for multivalued counter.

returning the output to its highest voltage level, from which the circuit begins the countdown operation.

The functionality of the counter circuit was tested by bread-boarding a circuit composed of tunnel diodes and discrete NPN transistors. The low-frequency experimental results, which validate the functionality of the design, are presented in Fig. 34.

An equivalent counter implemented in CMOS would require 30 transistors. Thus, considerable area and circuit component count reduction arise as a result of RTD-based implementation of MVL circuits. With improvement in process technology and packing densities of RTD + HBT circuits, a significant thrust can be sustained by quantum devices in developing high-performance alternatives to conventional state-of-the-art technologies.

V. Conclusions

Various circuit design techniques using RTD's, and RTD's in conjunction with high-performance GaAs HBT's and MODFET's, have been presented. Although widely varying approaches toward building RTD-based circuits are being pursued by different researchers, they all have a common objective of utilizing the RTD characteristics to build ultrafast and ultradense digital circuits. Noise-margin analysis techniques for RTD-based circuits have been introduced, and effects of RTD characteristics on circuit noise margins have been quantified. Such analyses are important in developing formal methods for design of RTD-based circuits. Bistable-mode RTD-based circuits that have been designed using cointegrated RTD's and HBT's/MODFET's have the potential for very high switching speeds coupled with increased logic density when compared with conventional technologies. RTD-based circuits make possible novel self-latching binary logic families that allow high speed and compact implementation of deeply pipelined systems with no pipeline delay/area overhead. A gate-level pipelining scheme, called nanopipelining, has been successfully used to demonstrate greatly improved speed of multibit adders while requiring fewer circuit components than conventional implementations. This promises a tremendous improvement in system performance since carry propagation in adders often lies on the critical path of a system design. System design of an RTD + HBT ultrafast correlator serves as an example of the possibility of several-fold improvement in power-delay product of RTD-based system designs over conventional CMOS implementations.

MVL circuits have been designed using multiple-peak RTD's that allow the efficient implementation of literal circuits. The design of compact MVL multiplexers and mask programmable MVL gates presented here lays the foundation for a compact and flexible way of implementing combinational logic or a basic structure for logic synthesis. The savings in area increase dramatically with higher valued logics for RTD-based circuits due to the multistable characteristics of a single MRTD. The design principle of the programmable multivalued gates described here can be applied in general to other n-input, r-valued logic gates as well. These gate arrays provide a compact and flexible way of implementing combinational logic or a basic structure for logic synthesis. Adopting this design in gate arrays is especially promising not only because of the fact that the gate's multiple-valued input and output signals can reduce the number of interconnections needed for intergate routing but also because the functionality of each gate can be changed even until the final metal mask layers. The design of an ultracompact multiple-valued counter has been presented.

Quantum circuit technology is thus a promising emerging alternative VLSI circuit technology. The tunneling transport phenomenon of quantum devices offers picosecond switching speeds and hence the possibility of designing very-high-speed circuits. Compact, self-latching binary logic implementations and efficient MVL circuits arising due to the conjunction of RTD's and high-performance GaAs devices such as HBT's and MODFET's promise a viable means of dramatically improving the performance and density of future VLSI circuits. Based on the continuing improvements in process technology for resonant tunneling devices and integration of such devices with conventional devices, it is possible that these novel circuits might establish themselves in niche commercial applications even before the scaling limits of conventional CMOS technology are reached.

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