Digital Design for Low Power Systems

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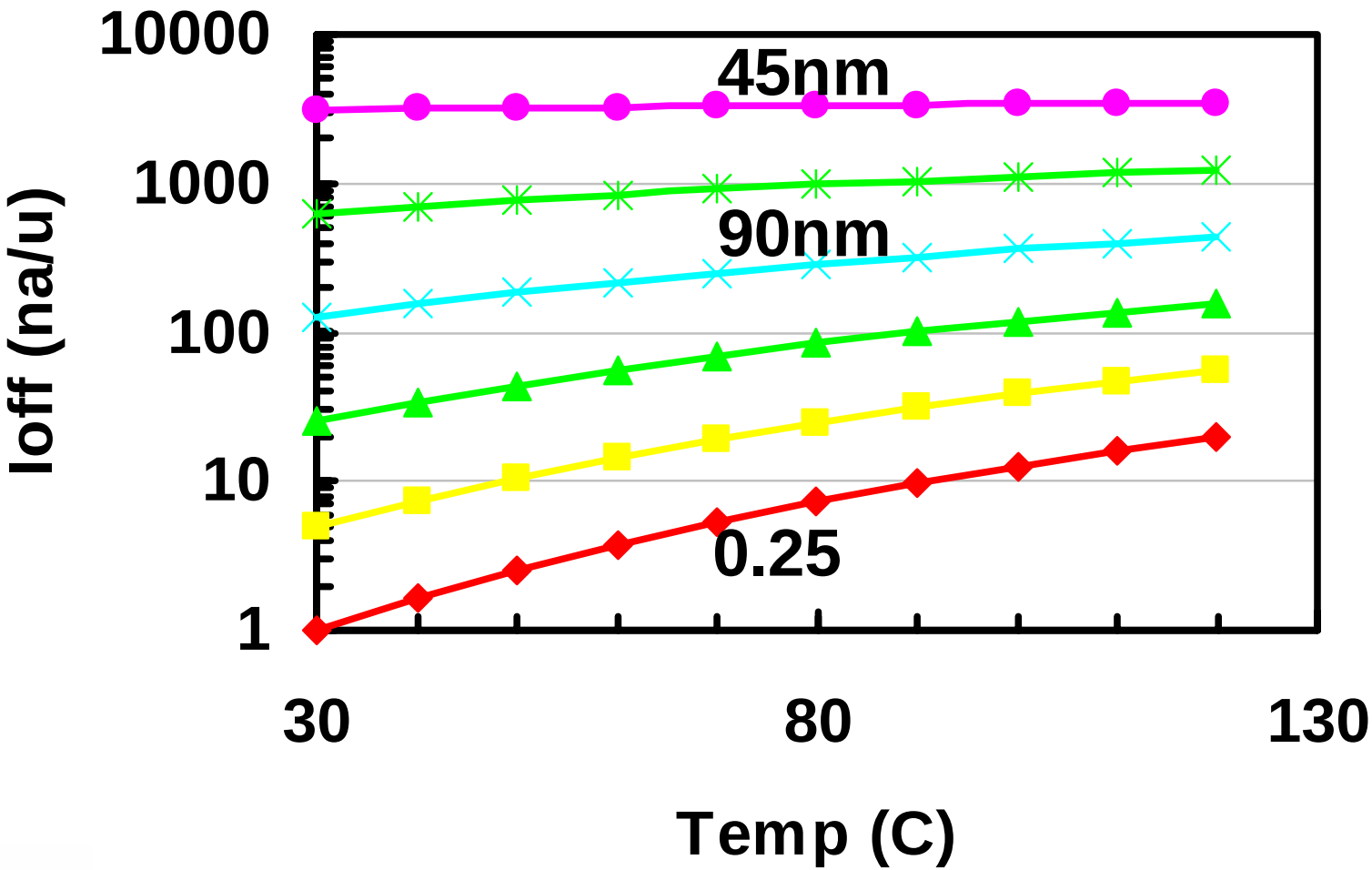
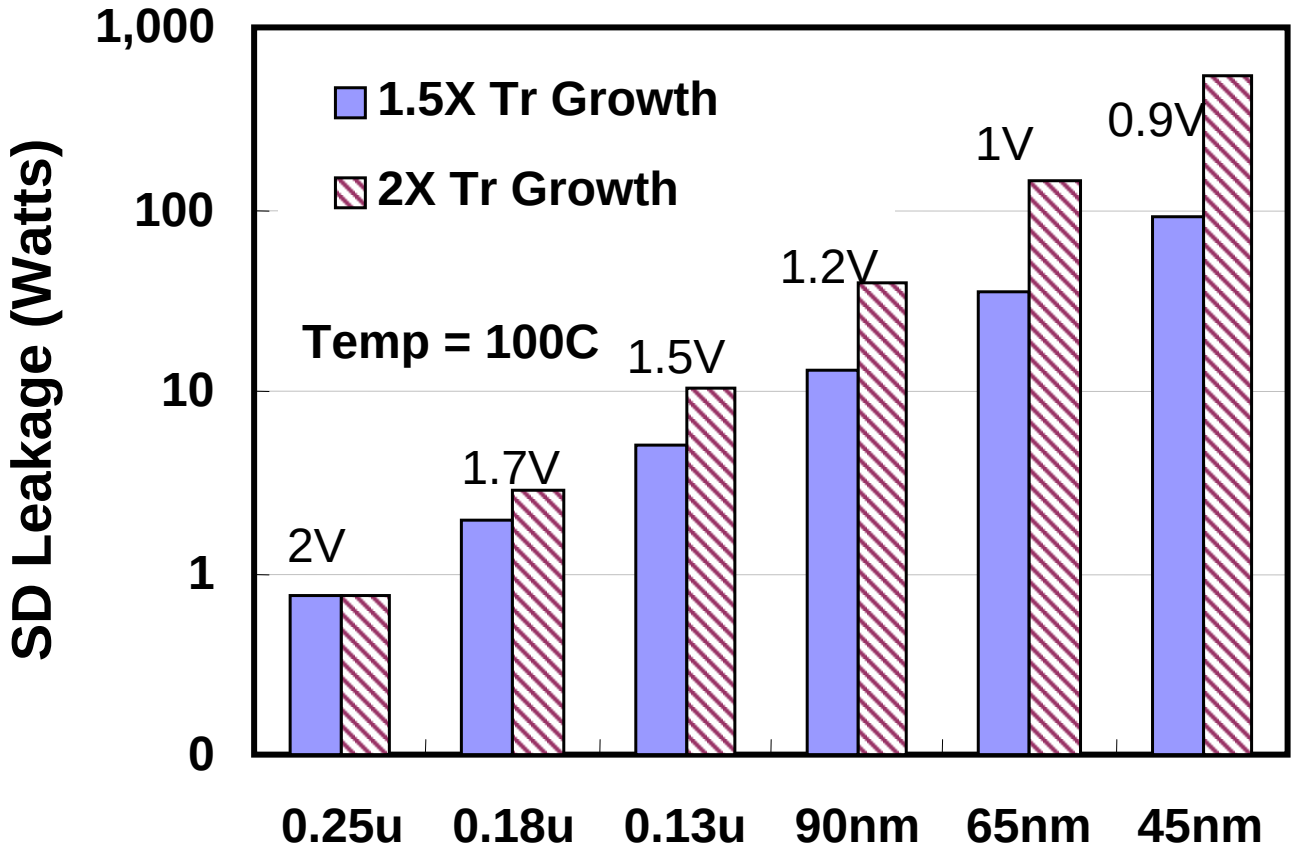
Outline

- **Low Power—Outlook & Challenges**
- **Circuit solutions for leakage avoidance, control, & tolerance**
- **Microarchitecture for Low Power**
- **System considerations**
- **Technology, Circuits, Architecture, and System co-optimization**

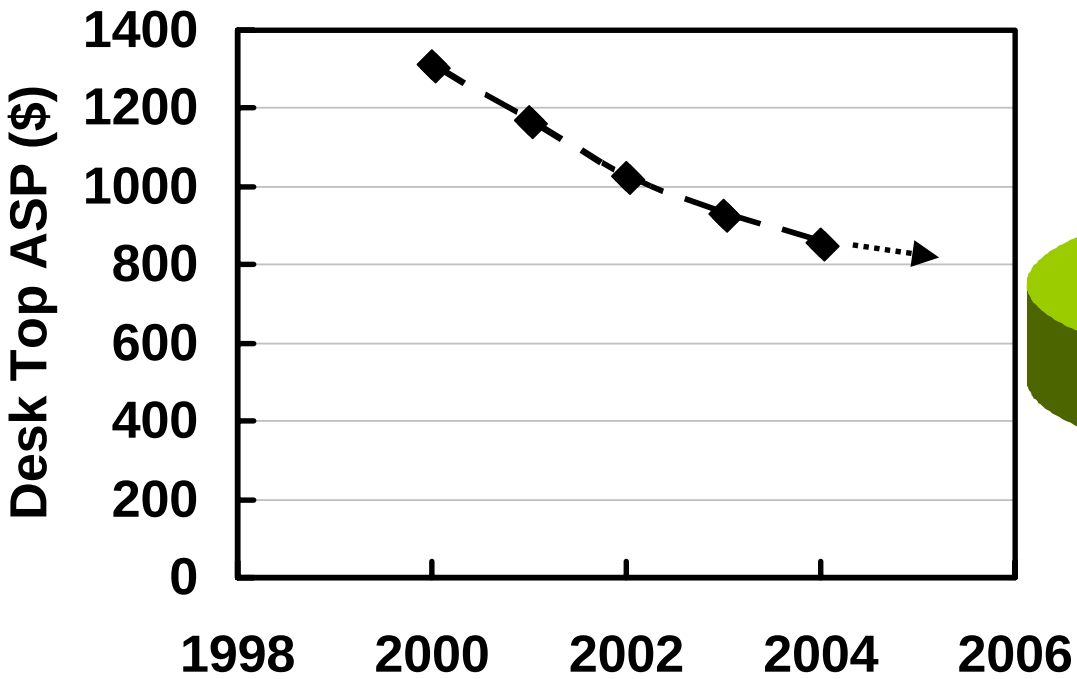
Unconstrained SD Leakage

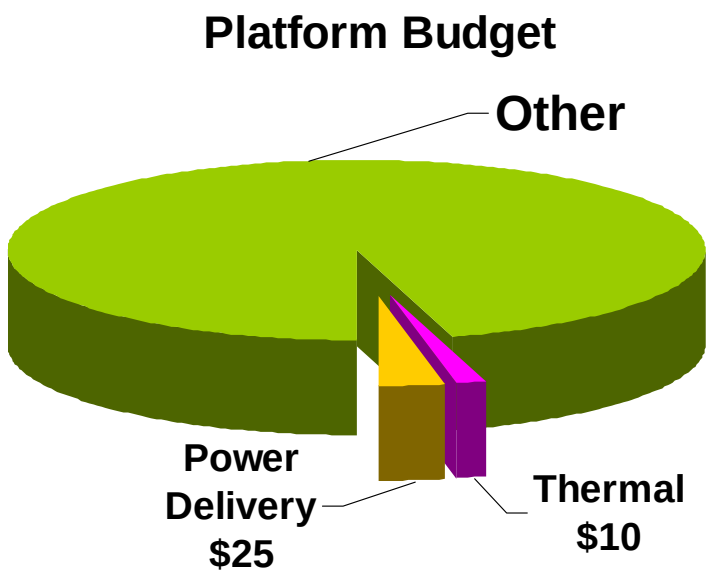


Unconstrained SD Leakage Power



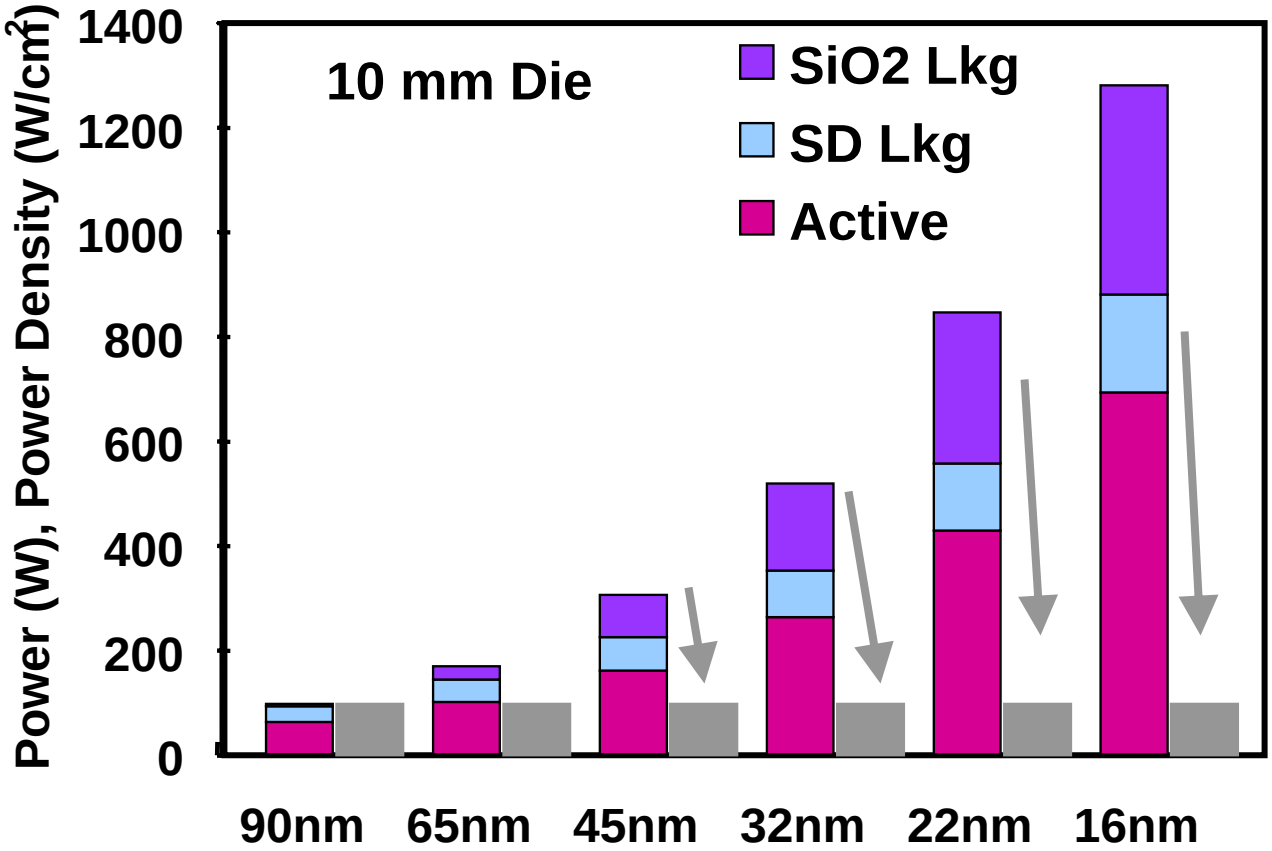
Product Cost Pressure





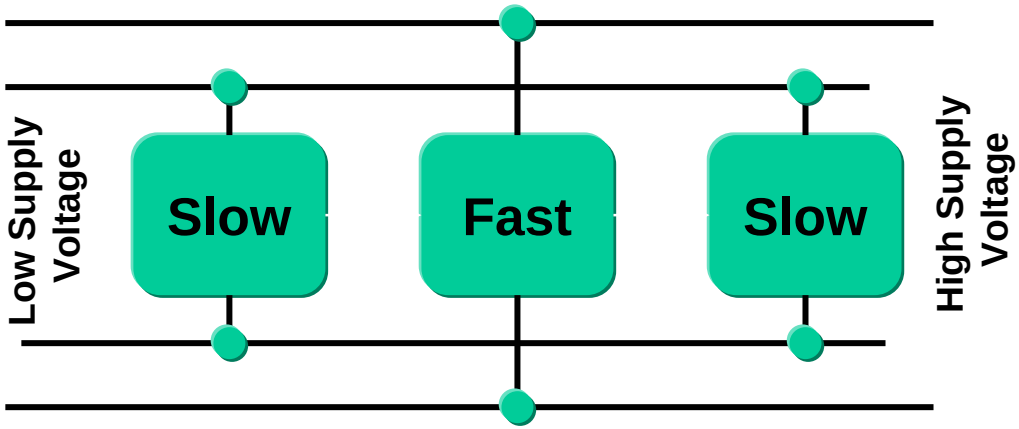
Shrinking ASP & budget for power

Unconstrained Total Power



Technology, Circuits, & Architecture to constrain power

Active Power Reduction



Multiple Supply Voltages

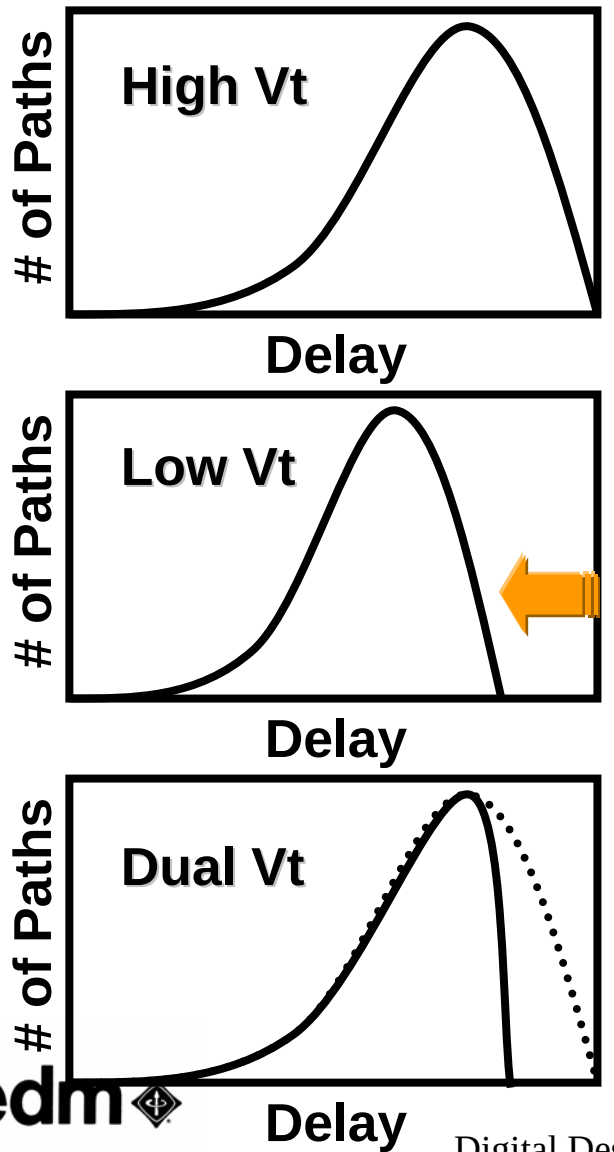
Multiple supply voltages mimic Vdd scaling

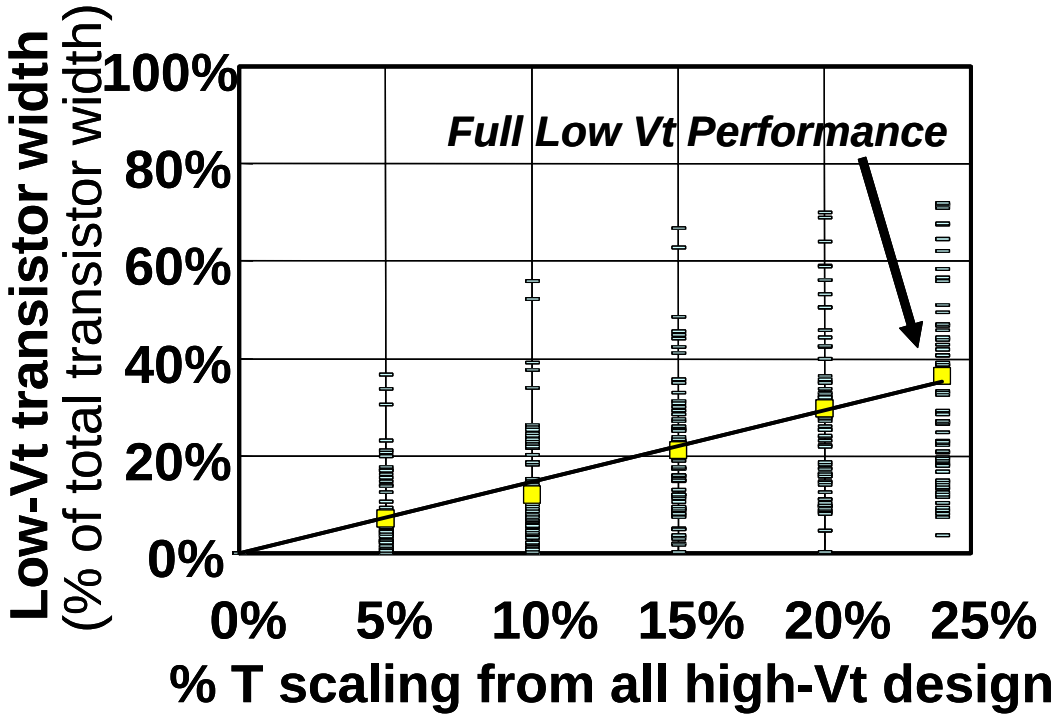
Issues:

Performance loss due to interface circuits

Multiple Vdd routing overhead

SD Leakage Avoidance—Dual Vt

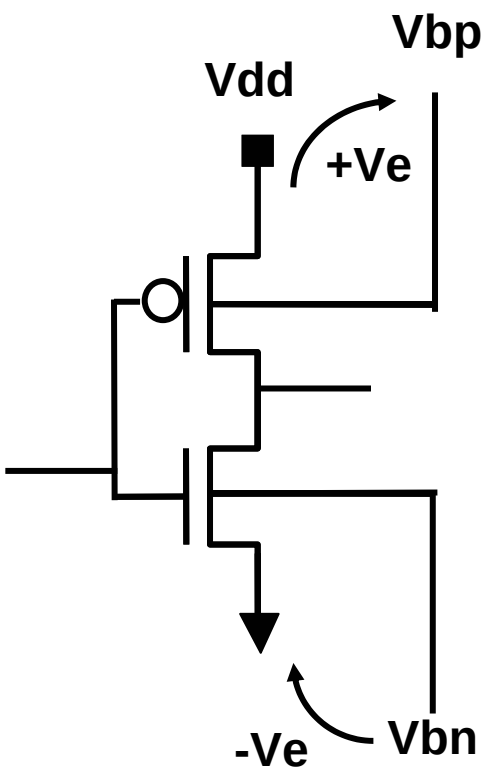




Leakage 3X smaller
(Active & Standby)
No performance loss

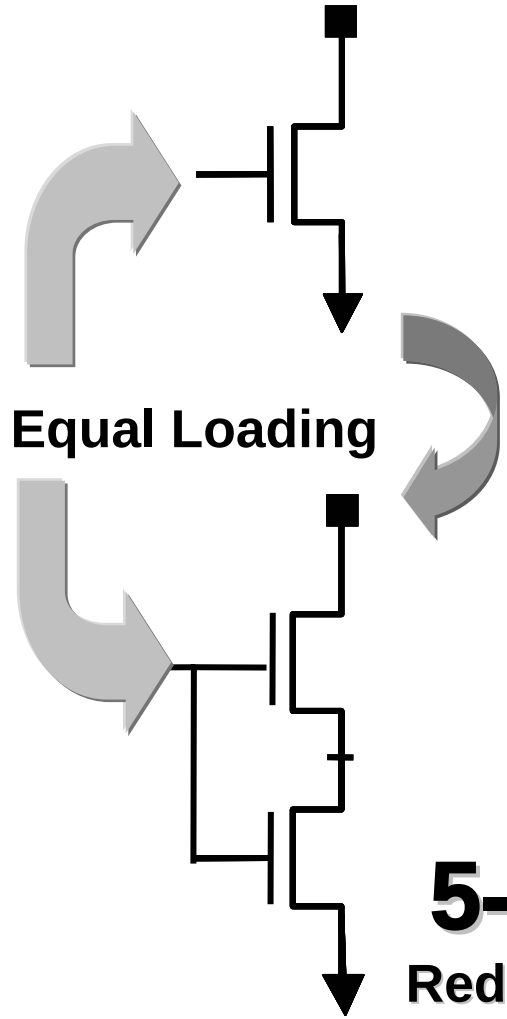
Leakage Control Circuits

Body Bias



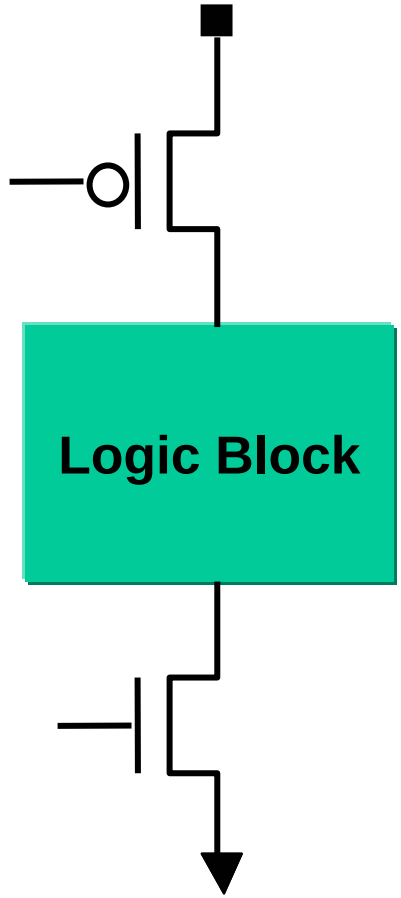
2-10X
Reduction

Stack Effect



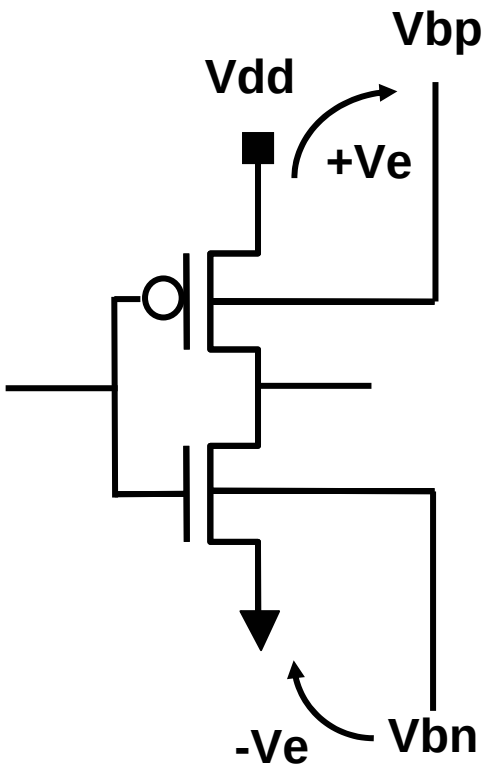
5-10X
Reduction

Sleep Transistor



2-1000X
Reduction

Body Bias

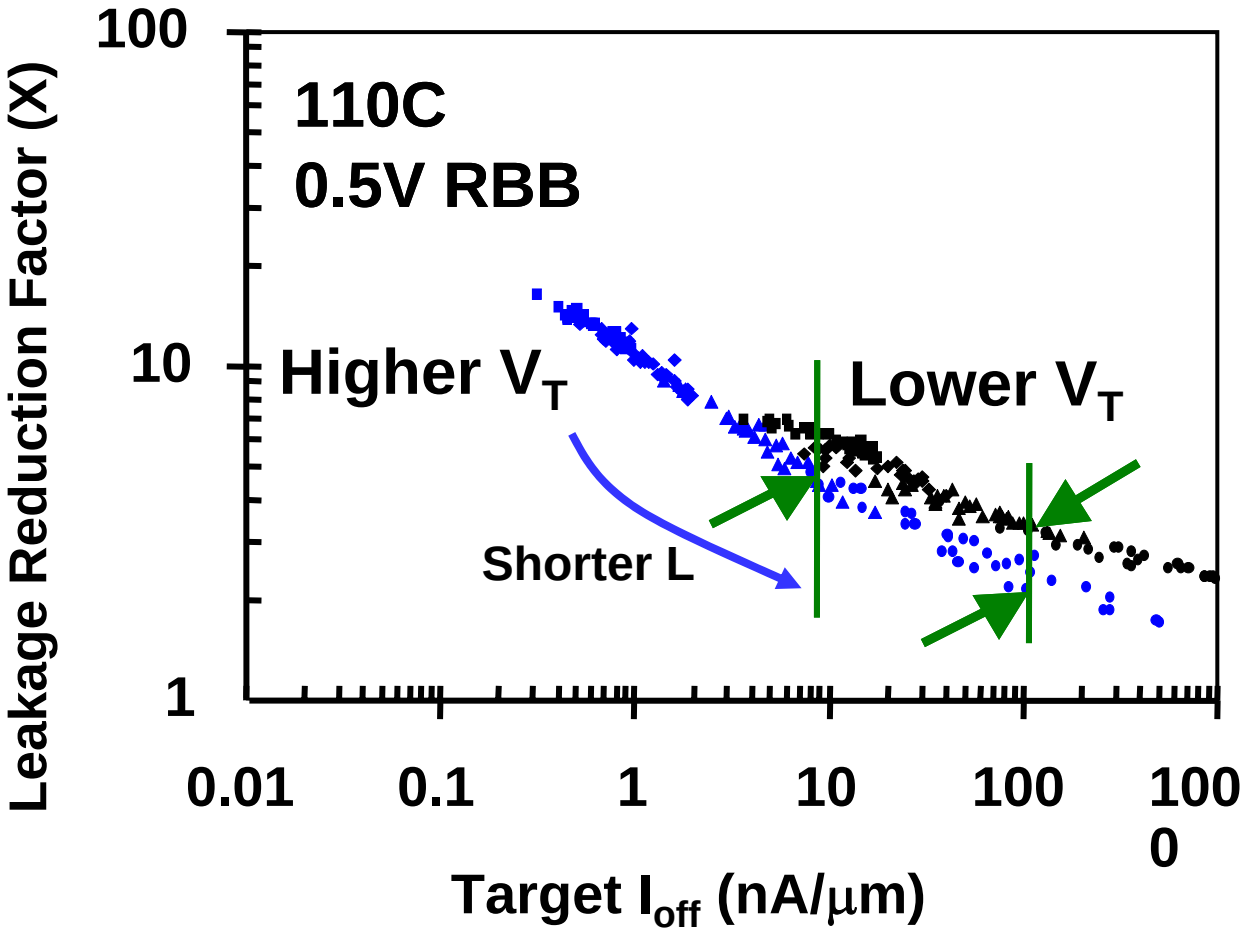


Reverse BB	Forward BB
Increases V_t Reduces I_{off}	Reduces V_t Increases I_{off}
To inactive circuits to reduce leakage	To active circuits to improve performance

Tradeoff & analysis required

- **Applying BB consumes active power**
- **Switching delay between body bias**

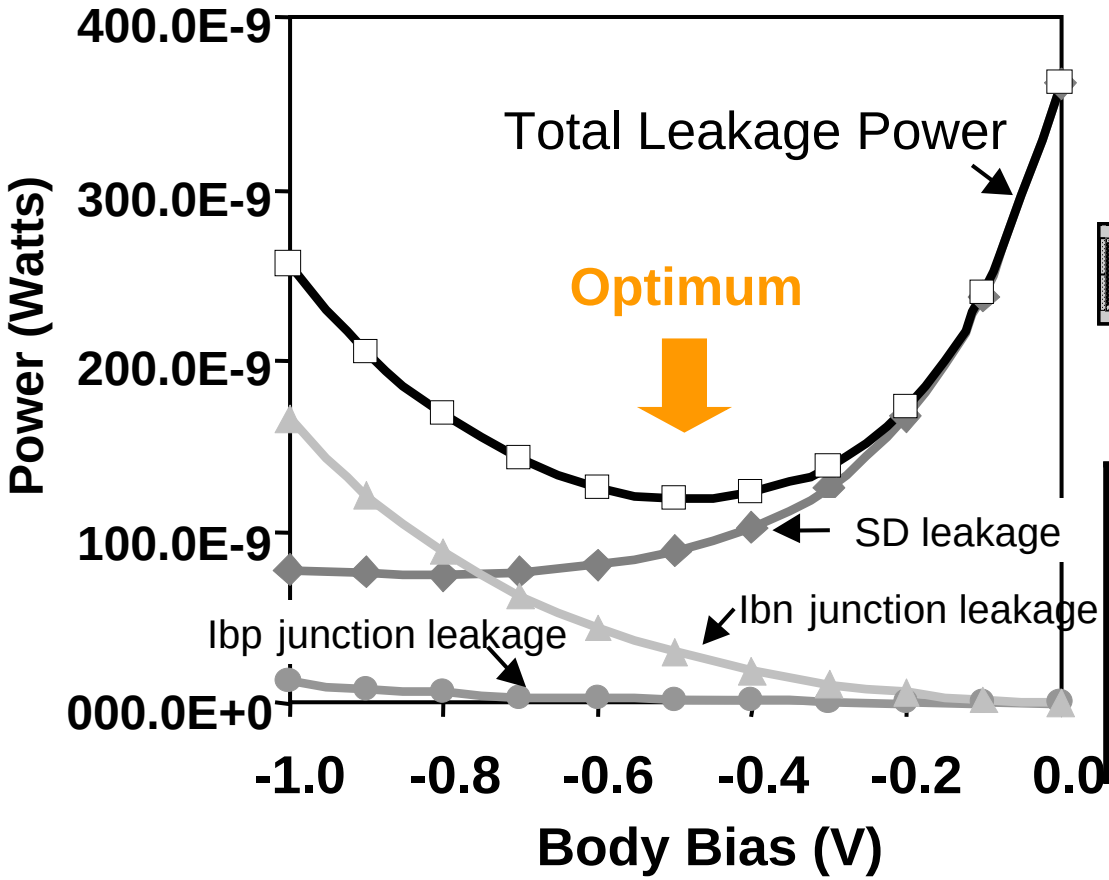
Reverse Body Bias



RBB less effective at shorter L and lower Vt

* A. Keshavarzi et. al., 2001 Int. Symp. Low Power Electronics & Design (ISLPED)

Scalability of RBB



Total Leakage Power Measured on Test Chip

0.18 μm

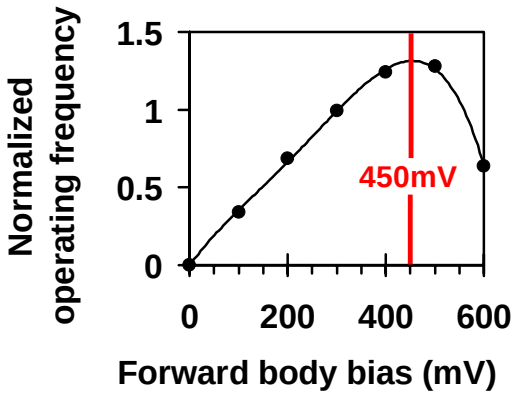
	0.35 μm	0.18 μm
Optimum RBB	2V	0.5V
Ioff Red.	1000X	10X

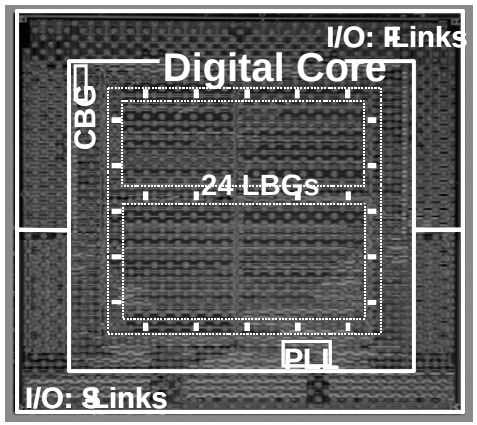
RBB Less effective with technology scaling

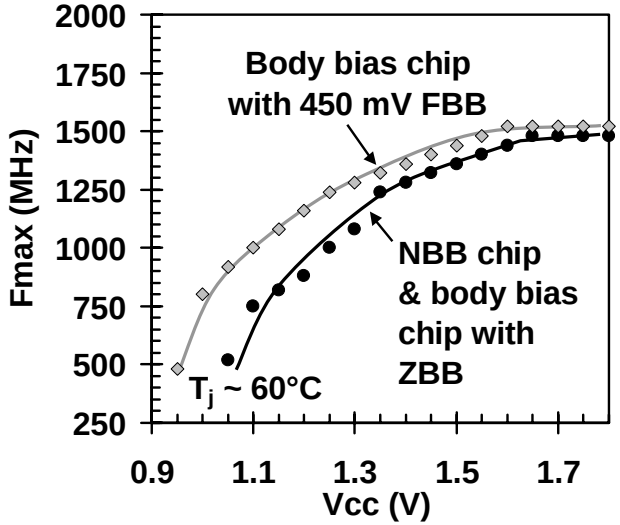
* A. Keshavarzi et. al., 1999 Int. Symp. Low Power Electronics & Design (ISLPED)

Forward Body Bias

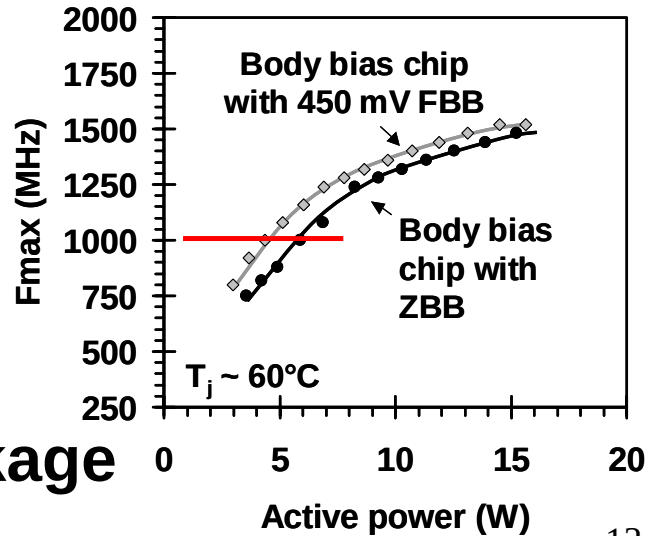
Router chip with body bias







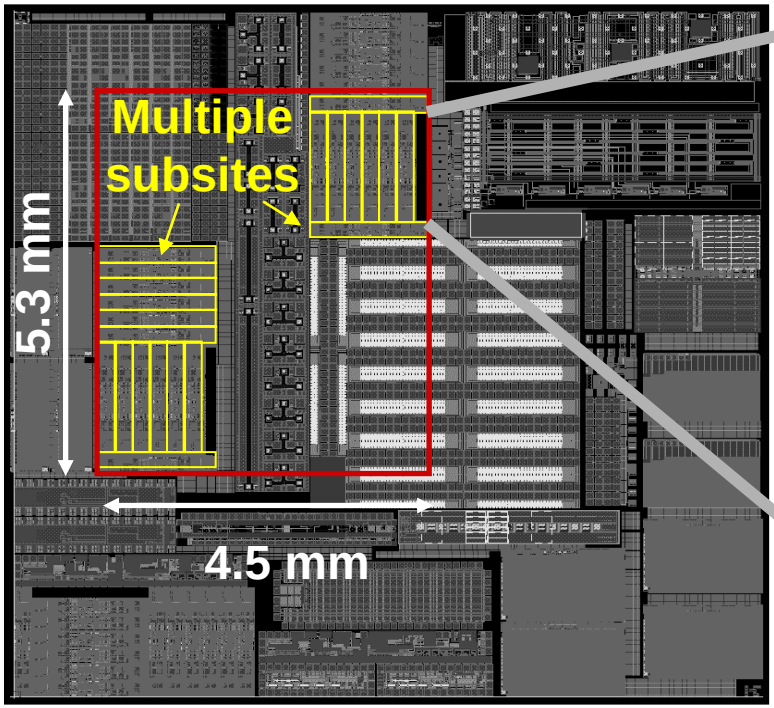
Die size	10.1 X 10.1 mm2
Technology	150nm CMOS
Transistors	6.6 million
Area overhead	2%
Power overhead	1%

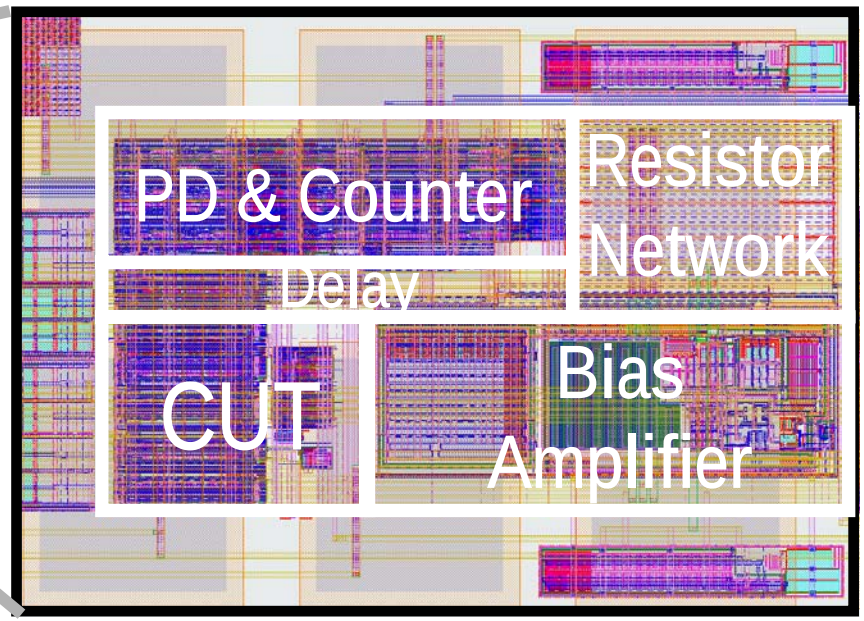


FBB increases frequency & SD leakage

* S. Narendra et al, ISSCC 2002, 16.4

Adaptive Body Bias Experiment





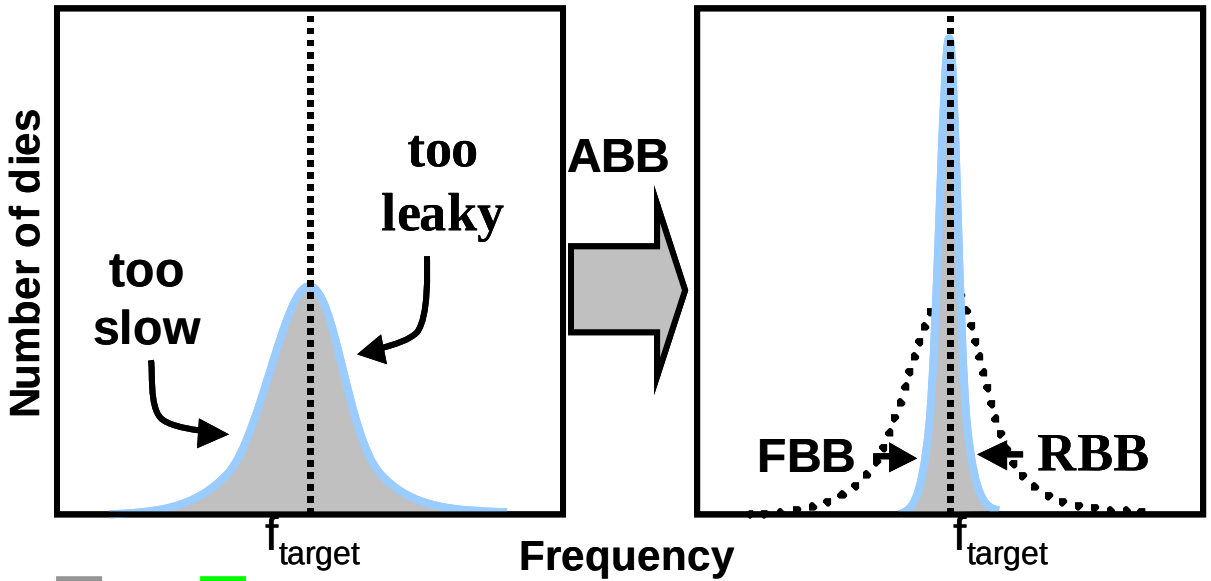
1.6 X 0.24 mm, 21 sites per die
150nm CMOS

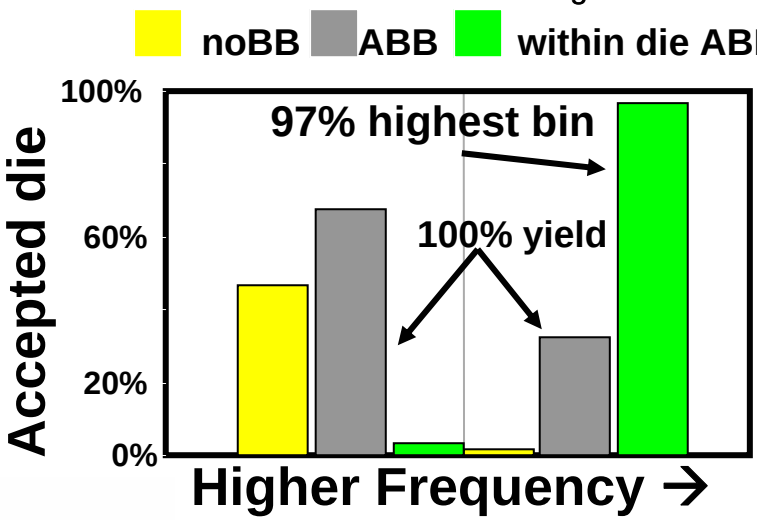
Technology	150nm CMOS
Number of subsites per die	21
Body bias range	0.5V FBB to 0.5V RBB
Bias resolution	32 mV

Die frequency: Min(F_1..F_{21})

Die power: Sum(P_1..P_{21})

Adaptive Body Bias Results

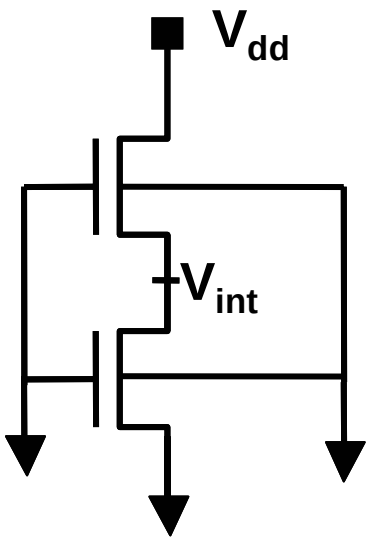


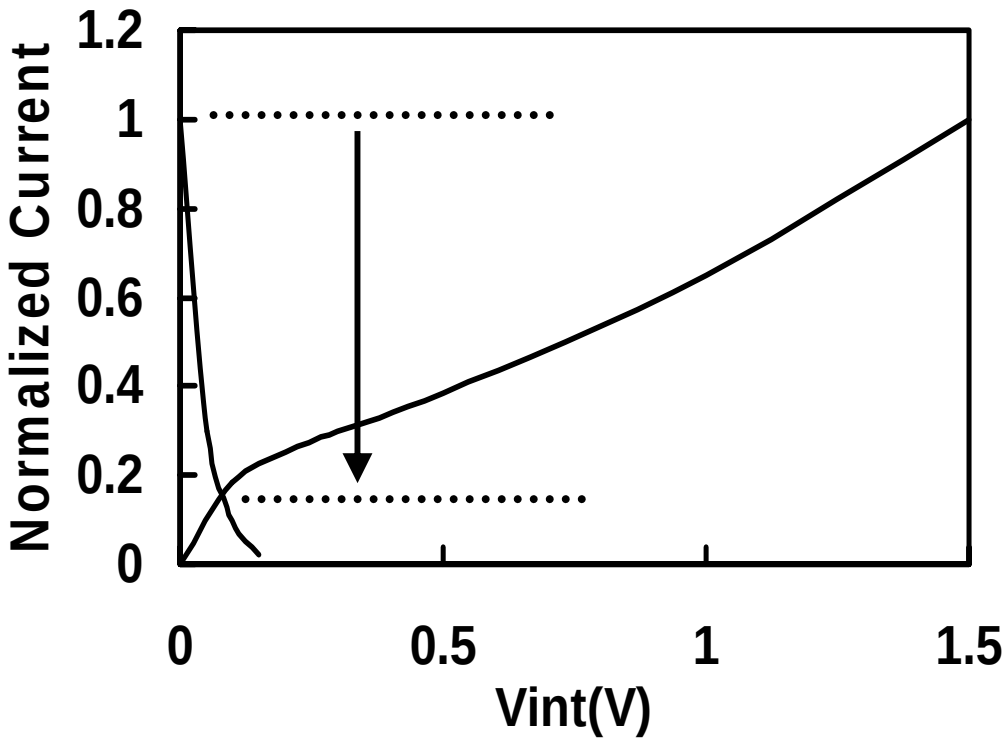


For given Freq and Power density

- 100% yield with ABB
- 97% highest freq bin with ABB for within die variability

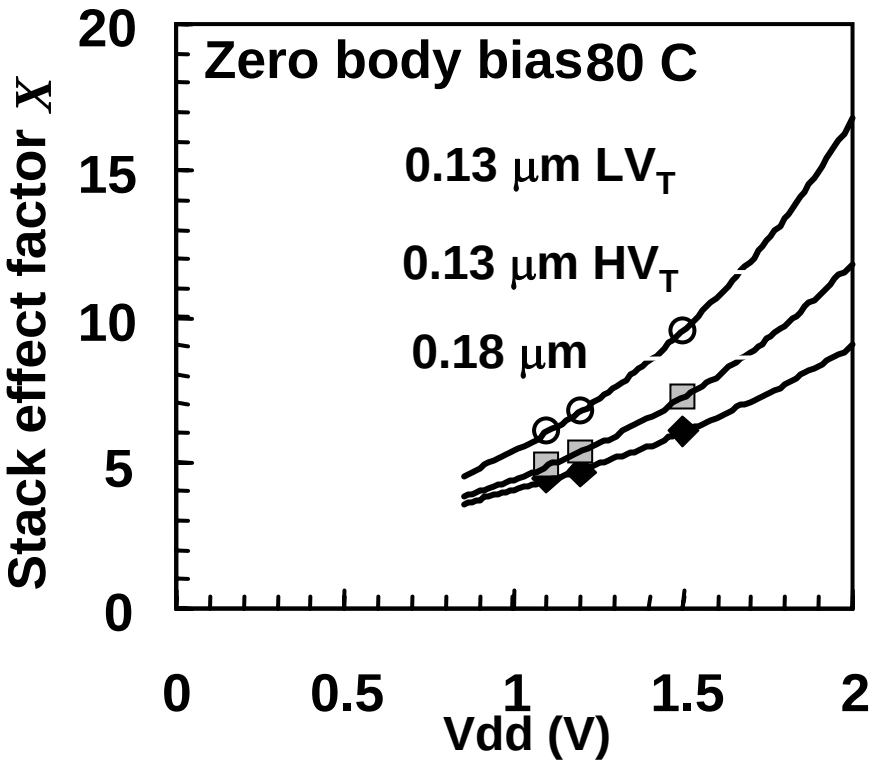
Transistor Stack

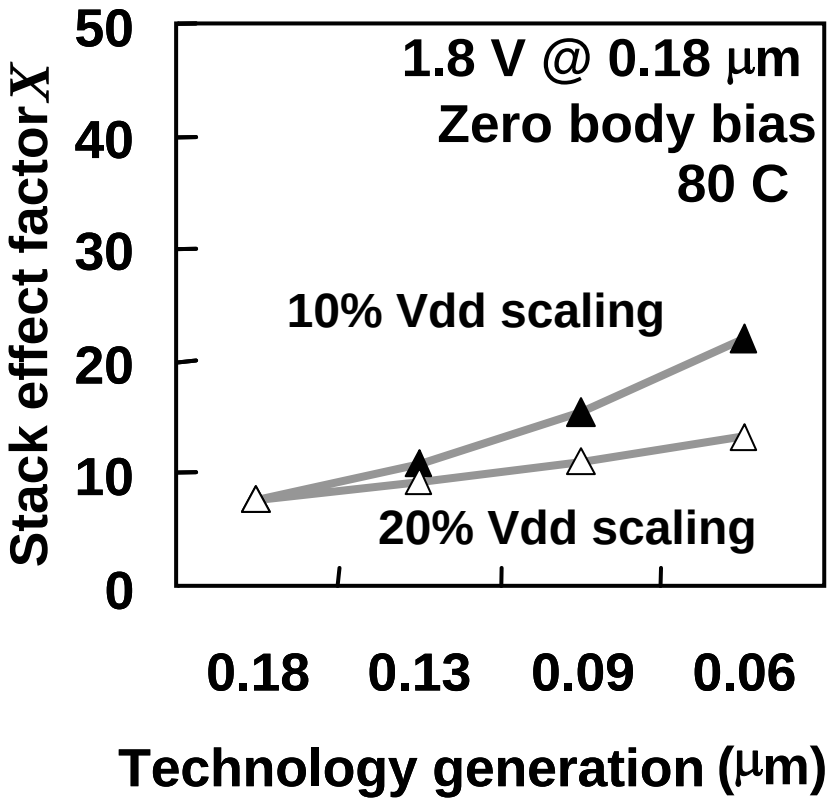




Stack leakage is ~5-10X smaller

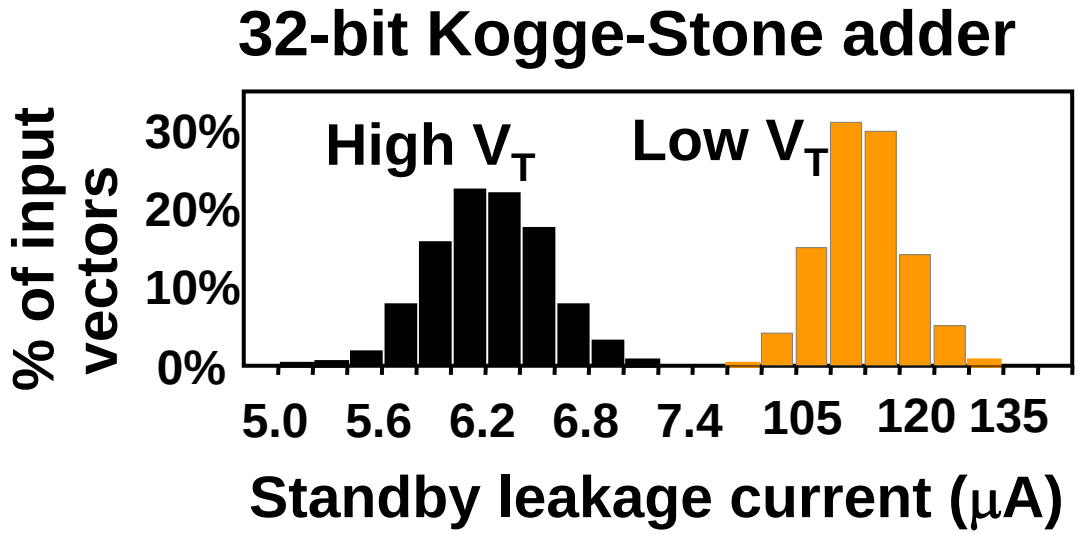
Scalability of Stack Effect





Stack effects becomes stronger with scaling

Exploiting Natural Stacks



Reduction	Avg	Worst
High V_T	**1.5X**	**2.5X**
Low V_T	**1.5X**	**2X**

	High V_T	Low V_T
Energy Overhead	**1.64 nJ**	**1.84 nJ**
Savings	**2.2 μA**	**38.4 μA**
Min time in Standby	**84 μS**	**5.4 μS**

* Y. Ye et. al., 1998 Symp. VLSI Circuits

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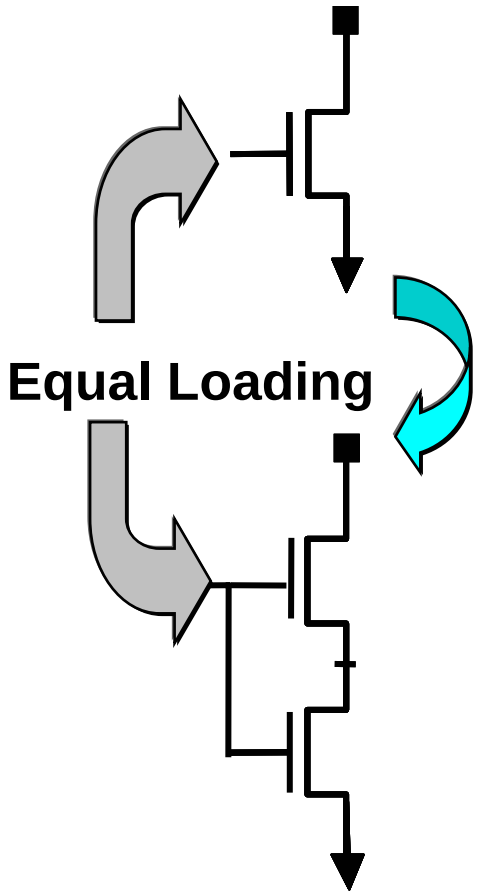
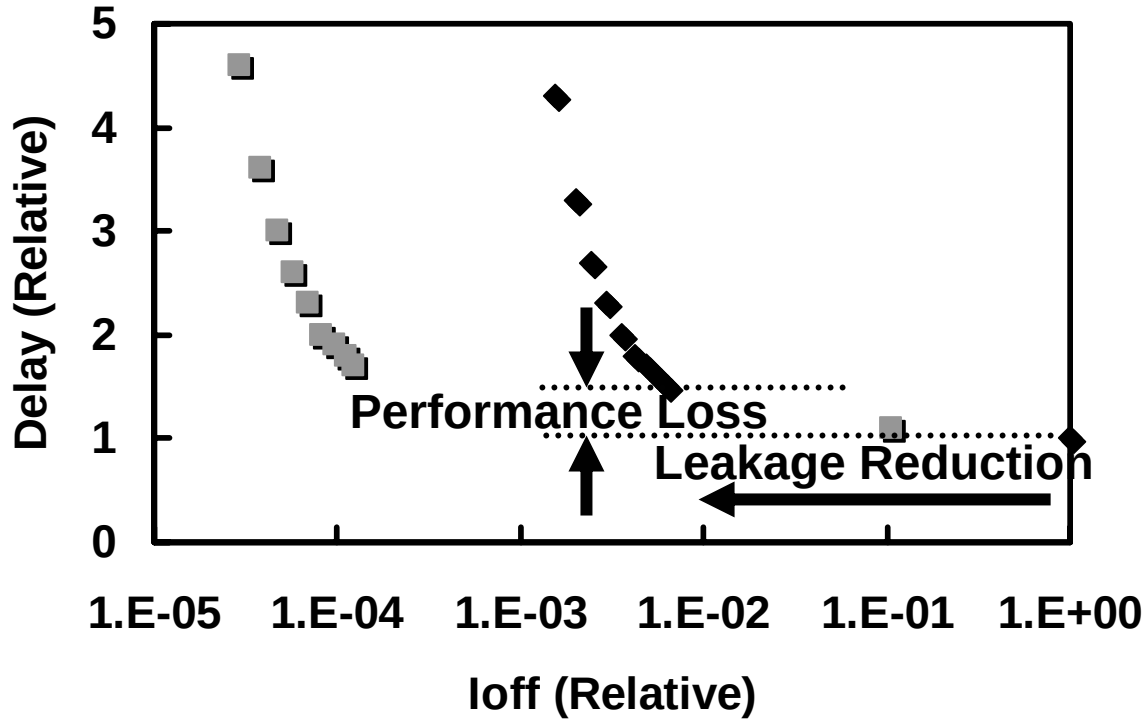
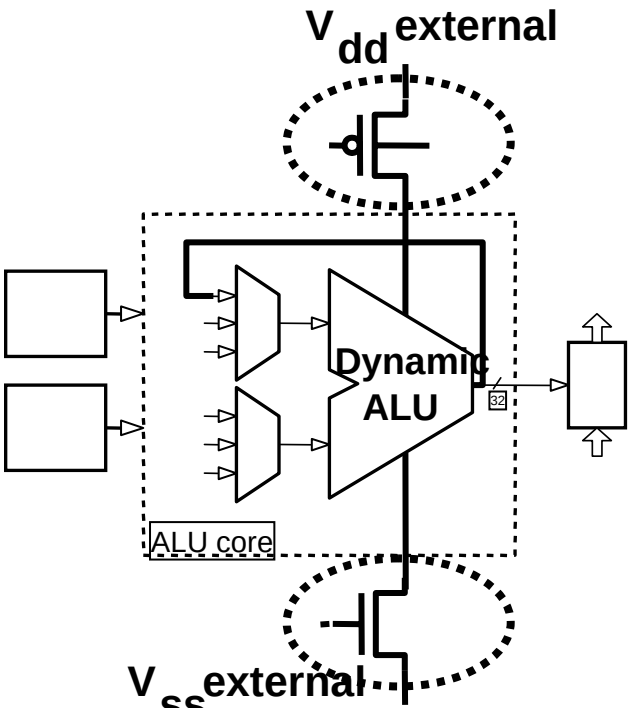
Stack Forcing

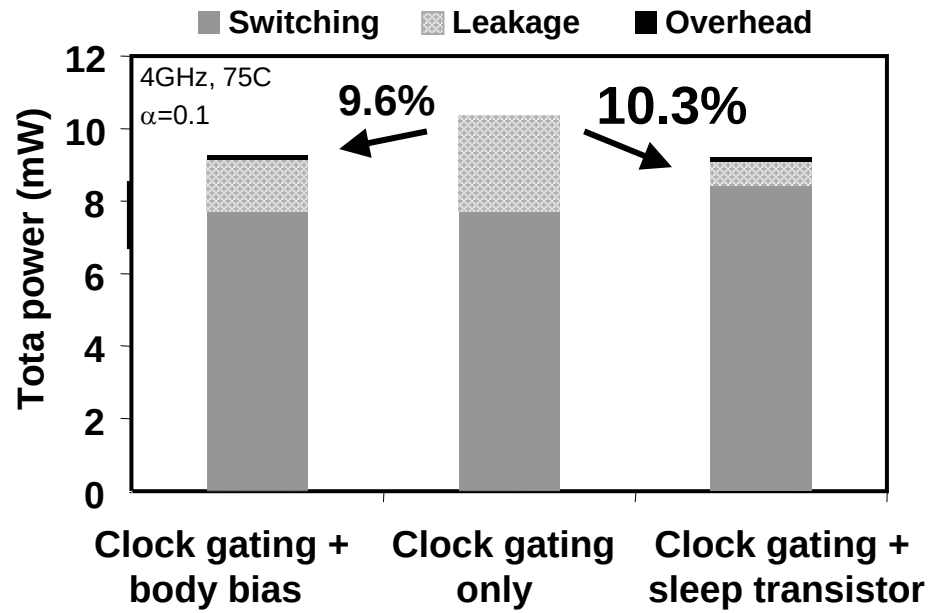


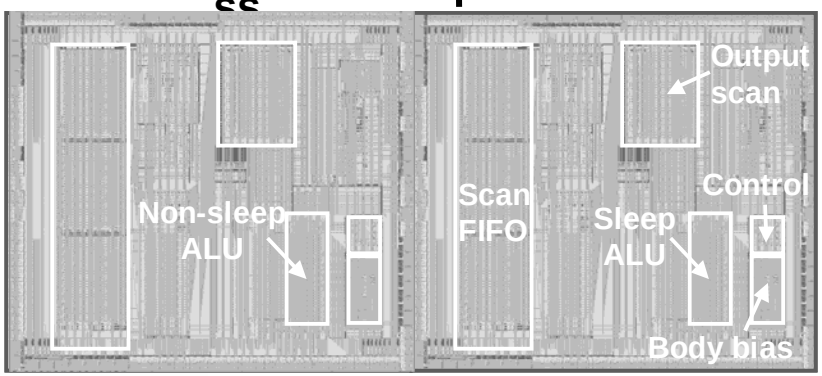


Circuit technique provides additional Vt's

Sleep Transistor Technique







	Frequency change	Leakage savings	Area over-head
PMOS sleep transistor	-2%	13X	11%
PMOS body bias	0%	2X	2%

J. Tschanz et al, ISSCC 2003, 6.1

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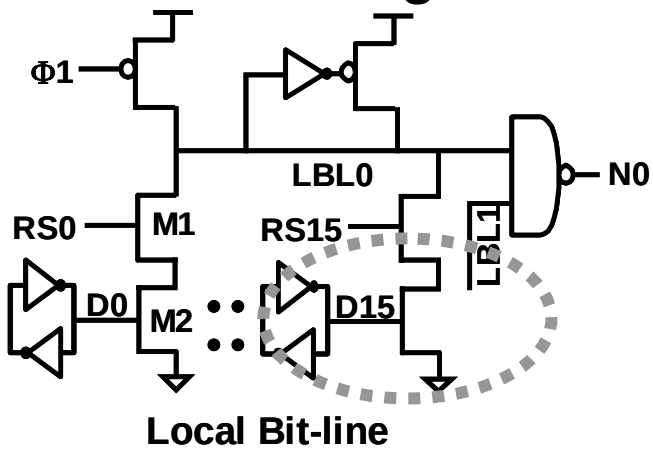
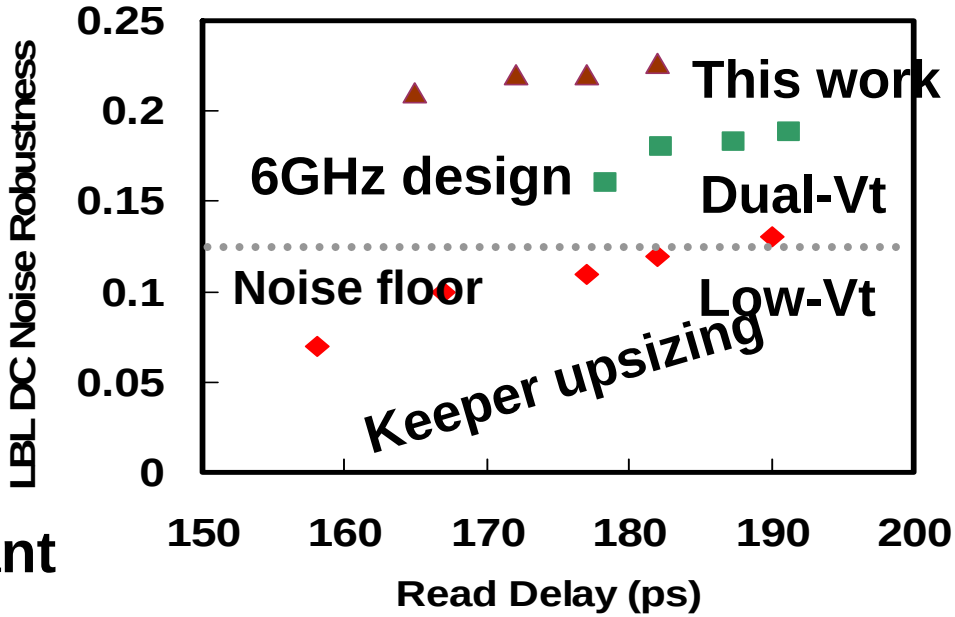
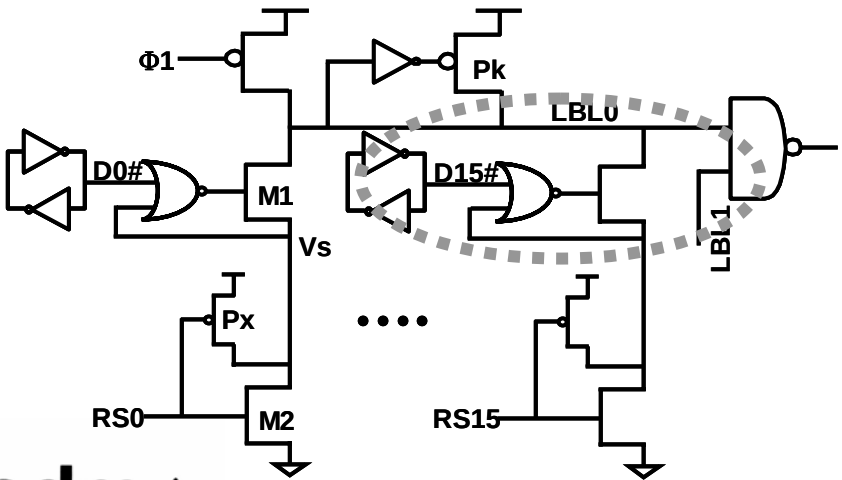
Leakage Tolerant Register File

Domino: leakage-sensitive





Pseudo-static: leakage-tolerant



Improves delay

Improves noise margin

Leakage tolerant

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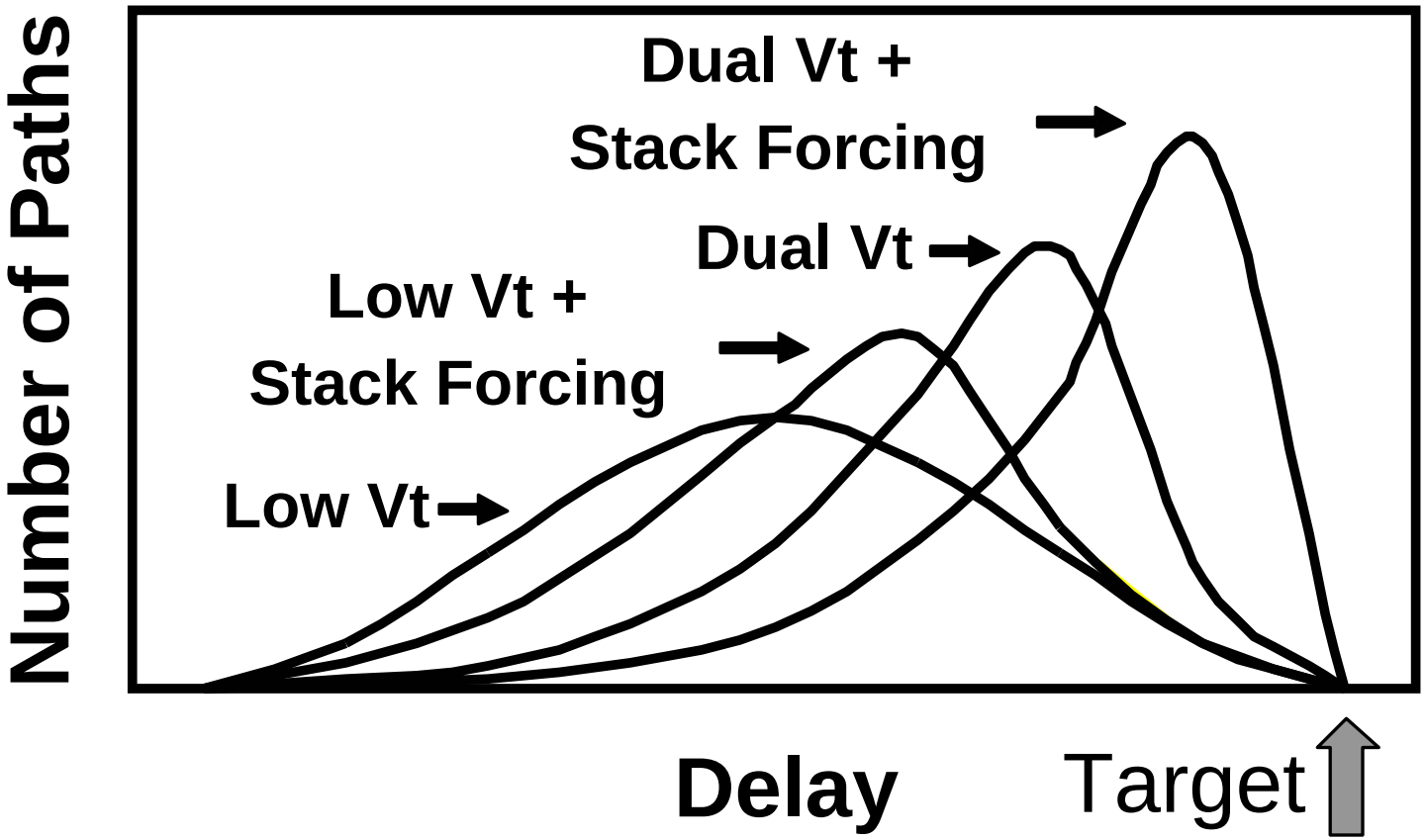
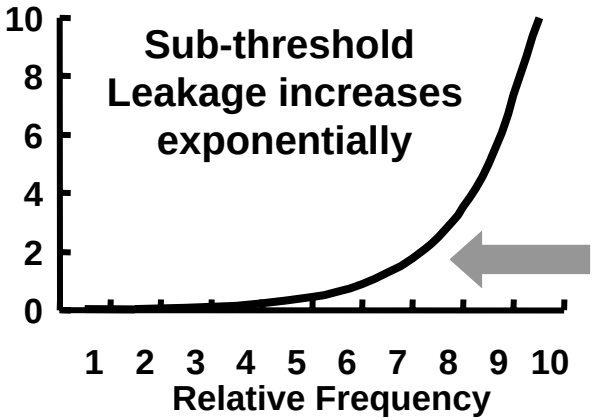
* R. Krishnamurthy et. al., 2001 Symp. VLSI Circuits

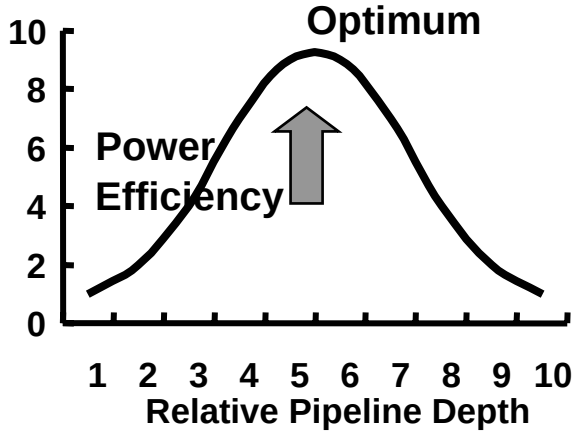
Employing Leakage Control



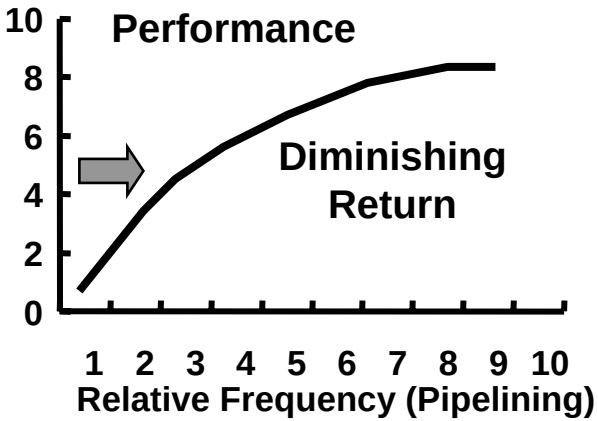
Optimum Frequency



Process Technology



Pipeline Depth

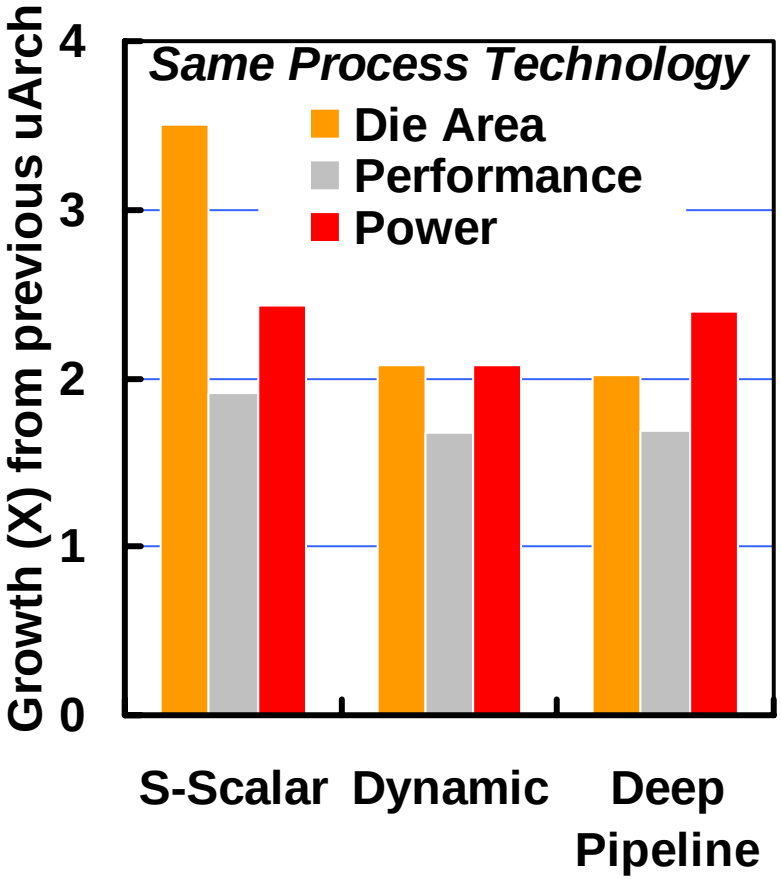


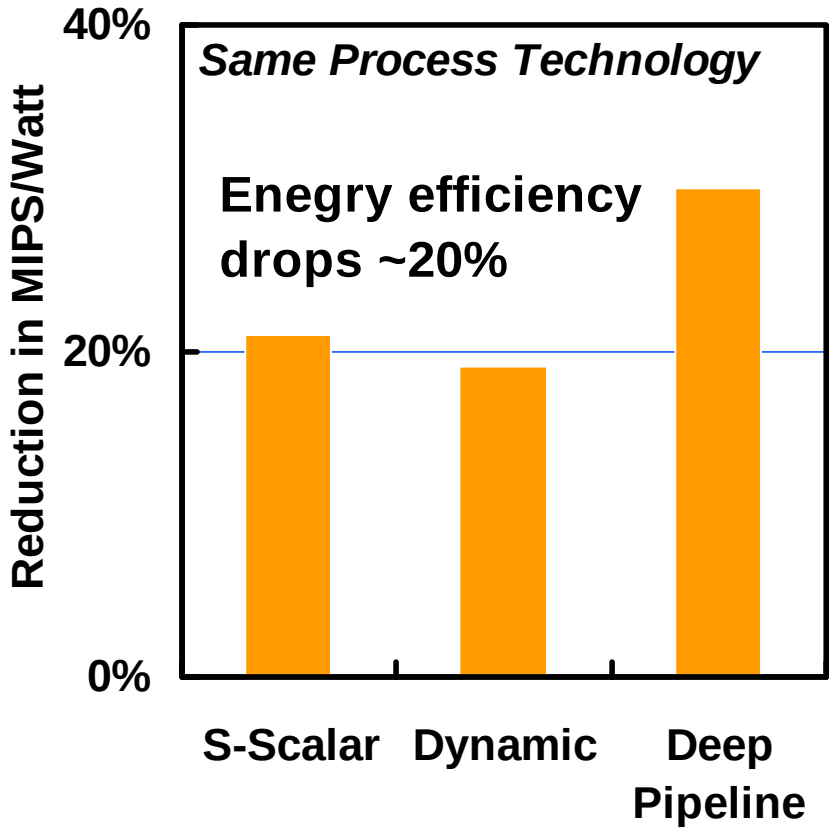
Pipeline & Performance

Maximum performance with

- **Optimum pipeline depth**
- **Optimum frequency**

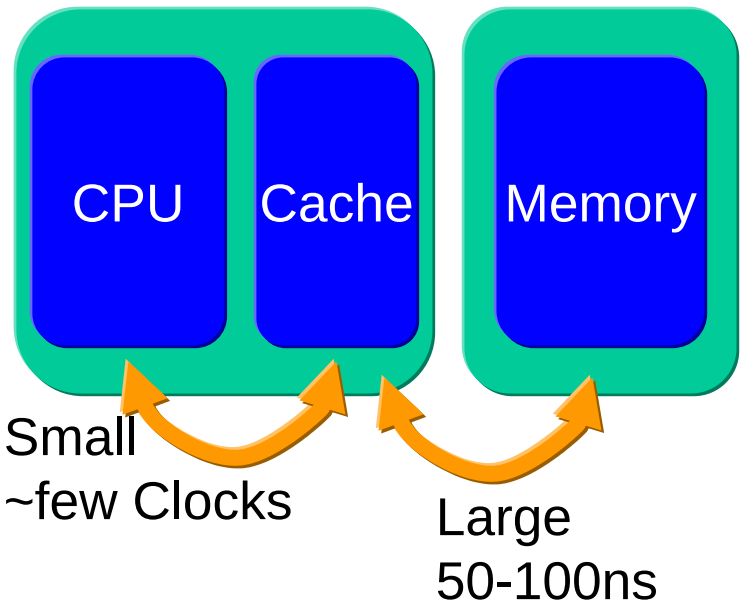
Efficiency of Microarchitectures

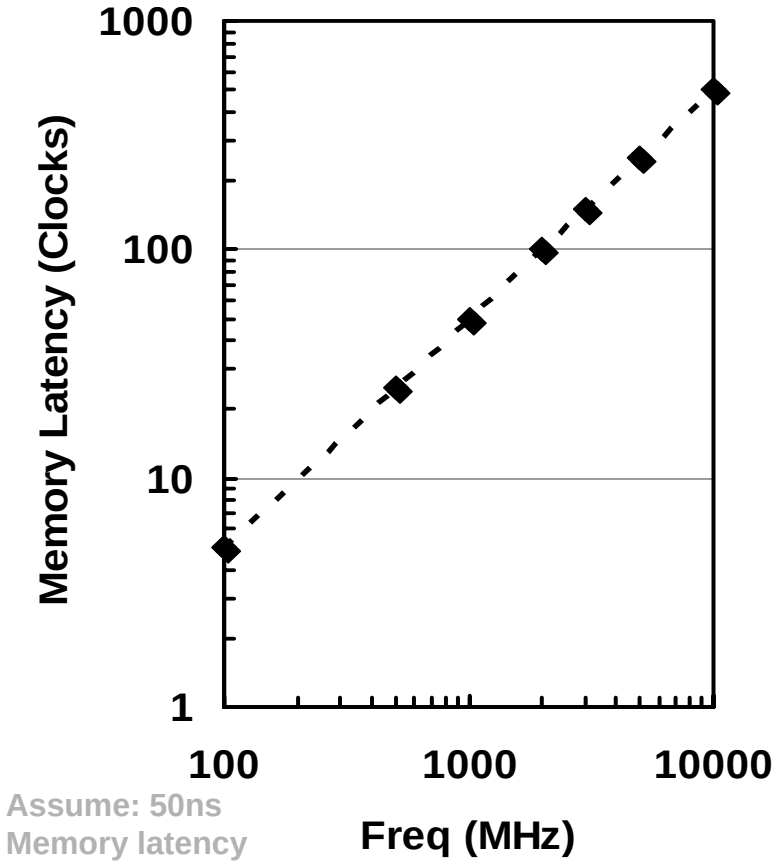




Employ efficient microarchitecture and design

Memory Latency

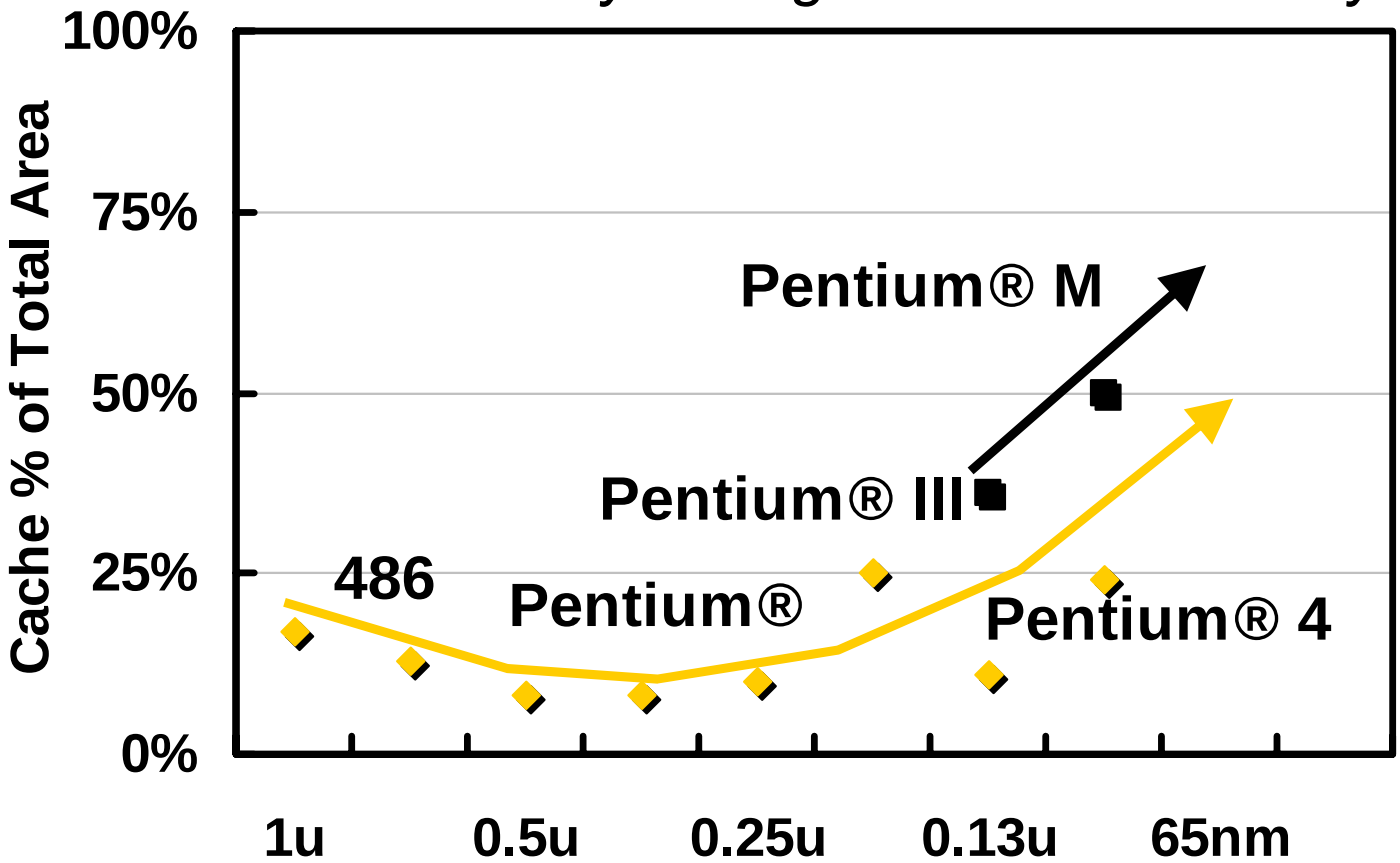




Cache miss hurts performance
Worse at higher frequency

Increase on-die Memory

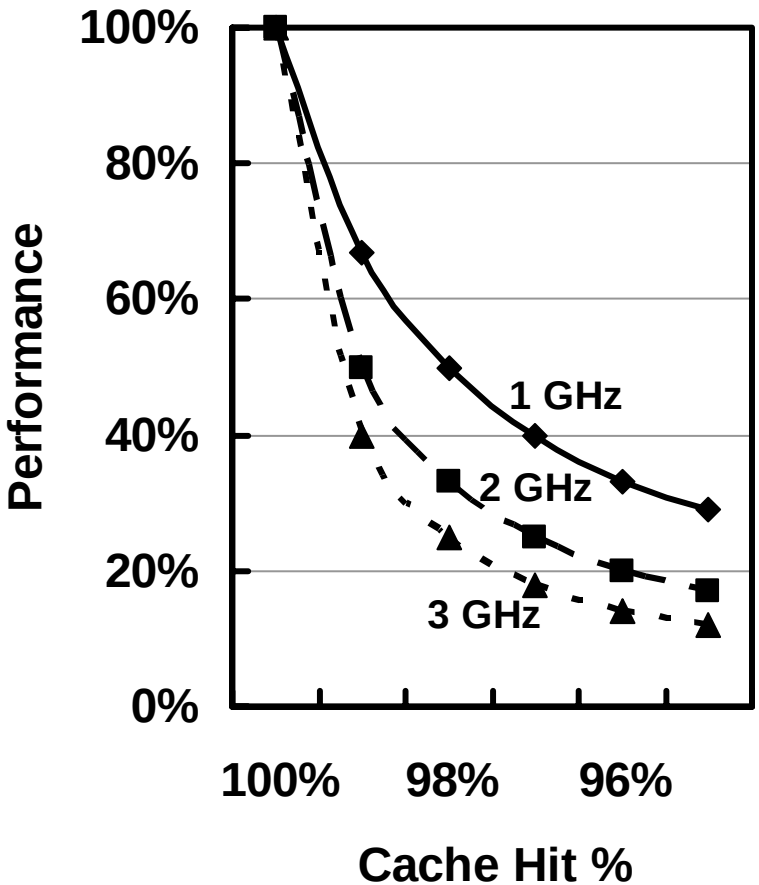
Power Density of Logic ≈ 10X of Memory



Increased Data Bandwidth & Reduced Latency

Hence, higher performance for much lower power

Multi-threading



Thermals & Power Delivery designed for full HW utilization

Single Thread

Full HW Utilization

ST | **Wait for Mem**

Multi-Threading

MT1 | **Wait for Mem**

MT2 | **Wait**

MT3

Multi-threading improves performance without impacting thermals & power delivery

Throughput Oriented Design

Vdd

Logic Block → Freq = 1
Throughput = 1
Active Power = 1
SD Lkg Power = 1

0.7 x Vdd

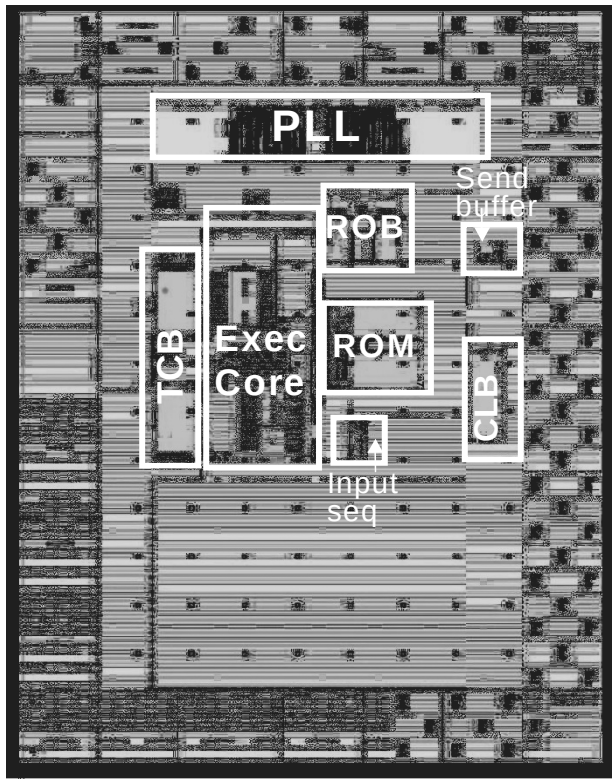
Logic Block → Freq = 0.7
Throughput = 1.4

Logic Block → Active Power = 0.7
SD Lkg Power = 0.7

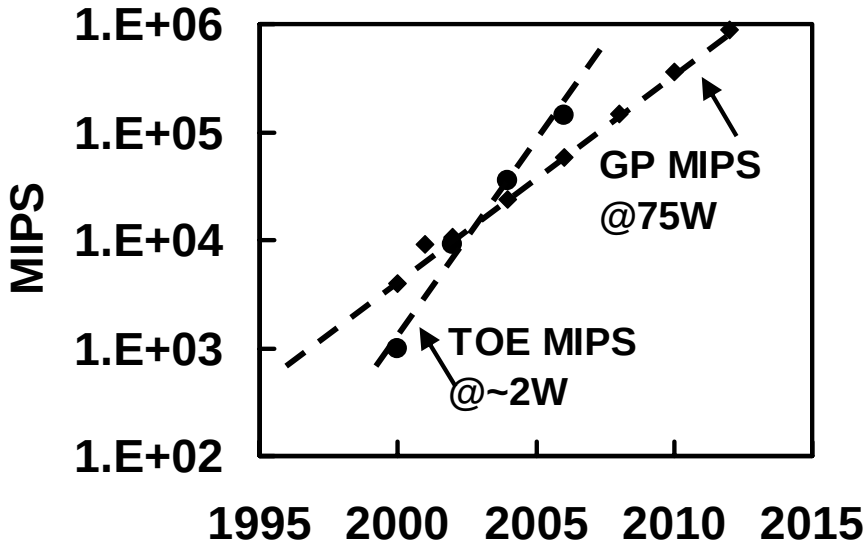
Higher logic throughput, yet lower power

Special Purpose Hardware

TCP Offload Engine



2.23 mm X 3.54 mm, 260K transistors



Opportunities:
Network processing engines
MPEG Encode/Decode engines
Speech engines

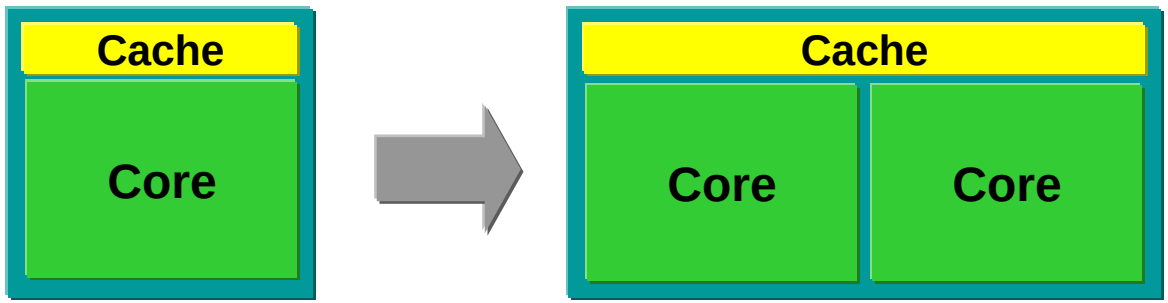
Special Purpose HW—Best Mips/Watt

Chip Level Multi-processing

Rule of thumb:

Voltage	Frequency	Power	Performance
1%	1%	3%	0.66%

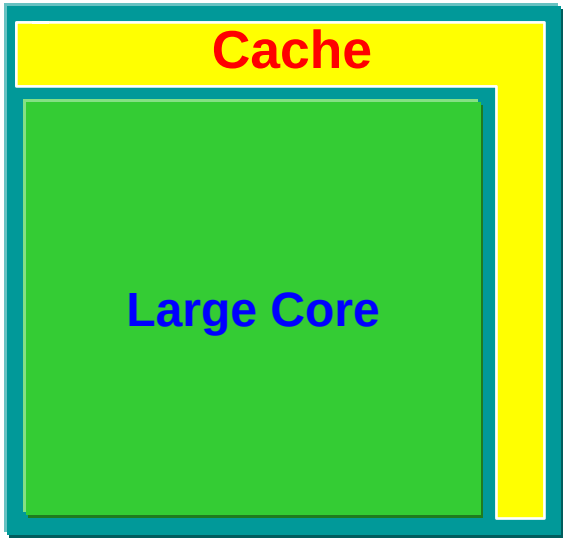
In the same process technology…

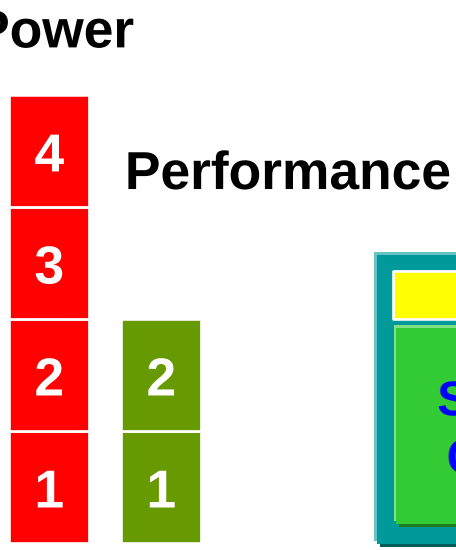


Voltage = 1
Freq = 1
Area = 1
Power = 1
Perf = 1

Voltage = -15%
Freq = -15%
Area = 2
Power = 1
Perf = ~1.8

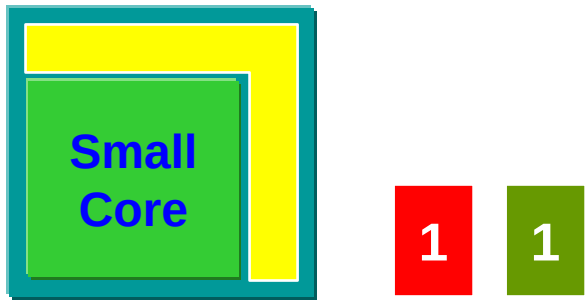
Multi-Core

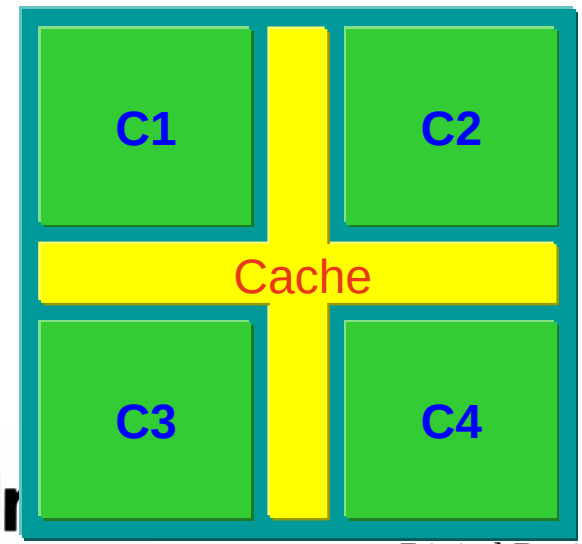


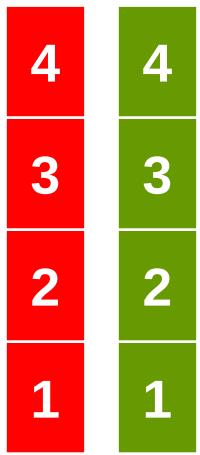


Power = 1/4

Performance = 1/2





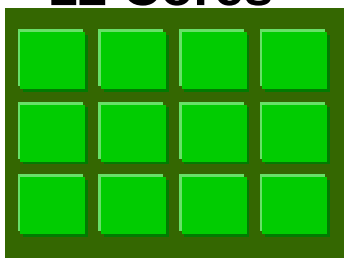


Multi-Core:
Power efficient
Better power and thermal management

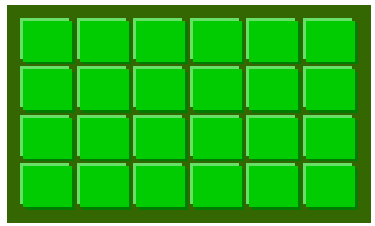
From Multi to Many…

13mm, 100W, 48MB Cache, 4B Transistors, in 22nm

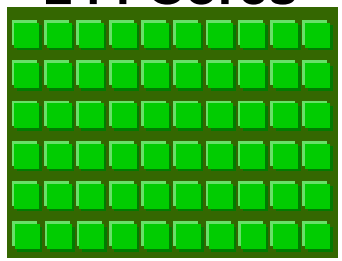
12 Cores



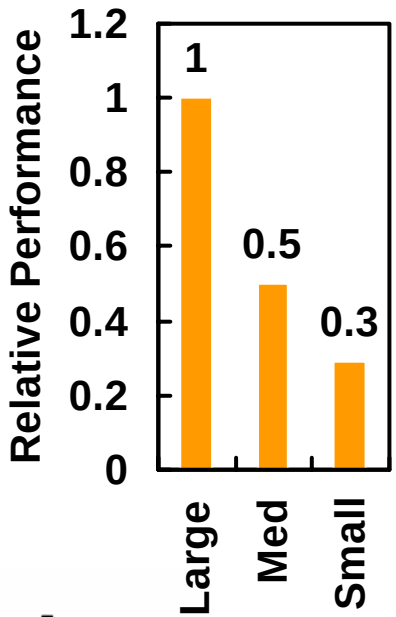
48 Cores

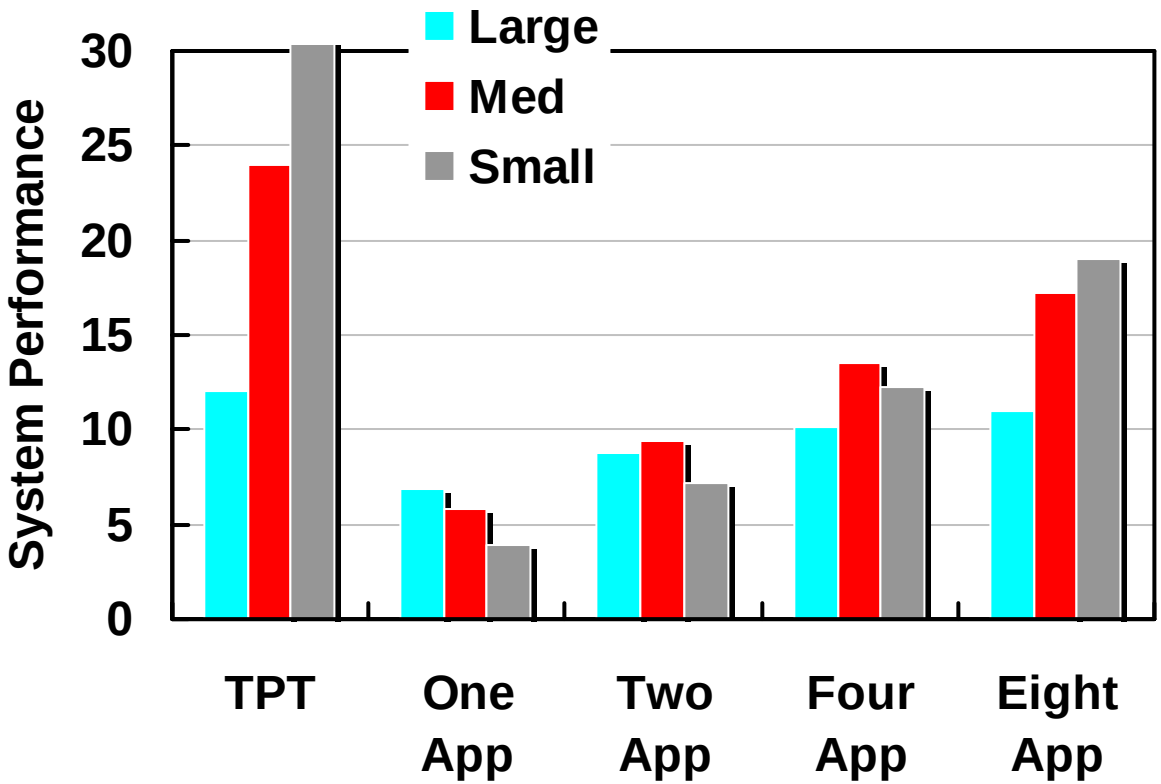


144 Cores



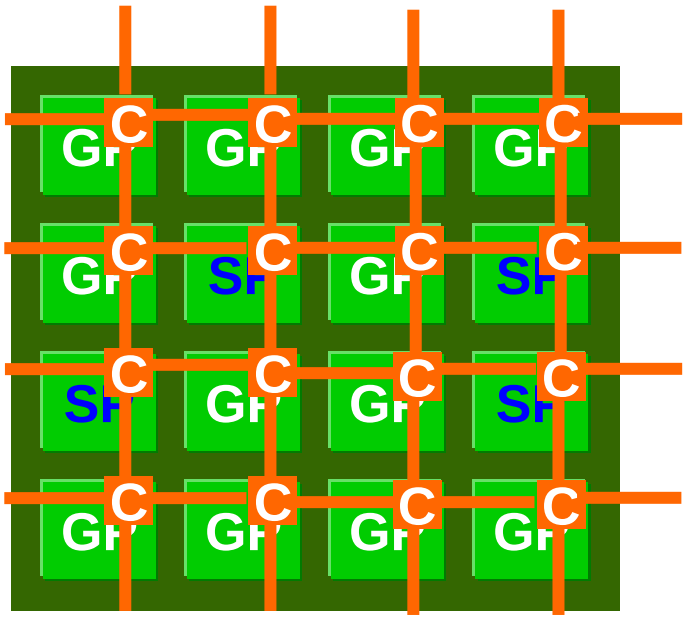
Single Core Performance





iedm

Future Multi-core Platform



General Purpose Cores

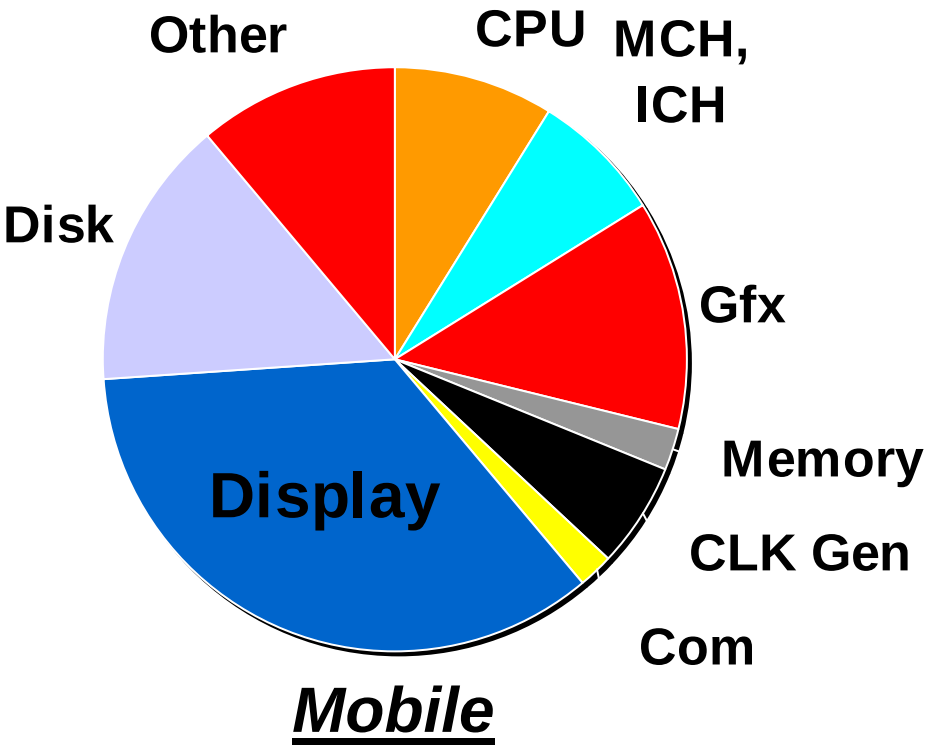
Special Purpose HW

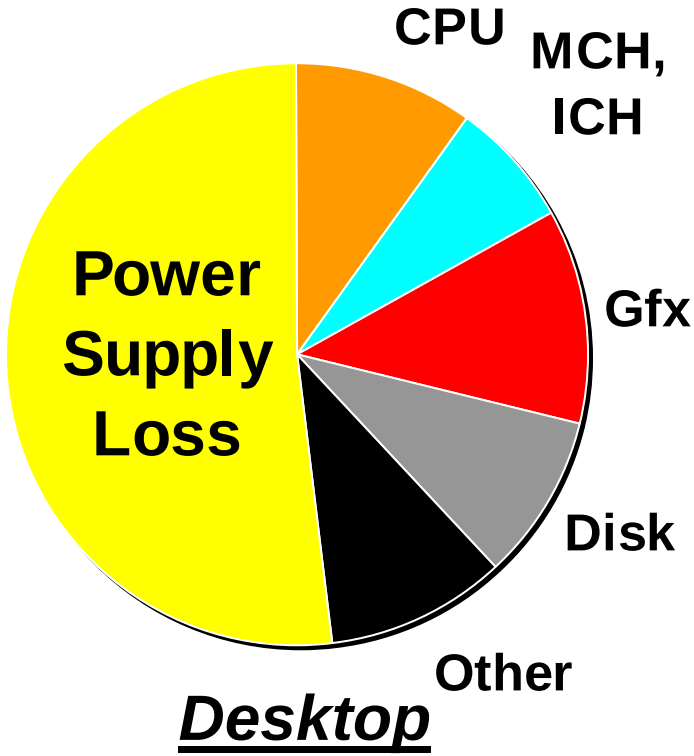
Interconnect fabric

Heterogeneous Multi-Core Platform

Low Power & Platform

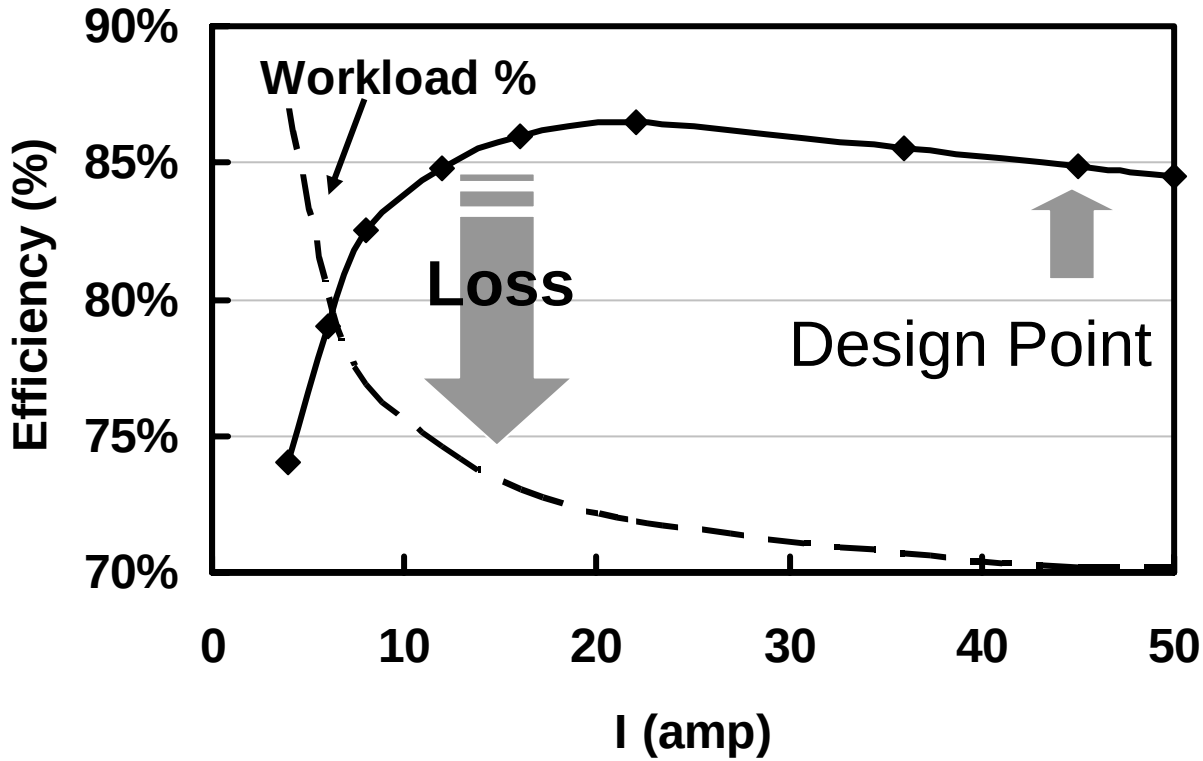
Breakdown of Platform Power





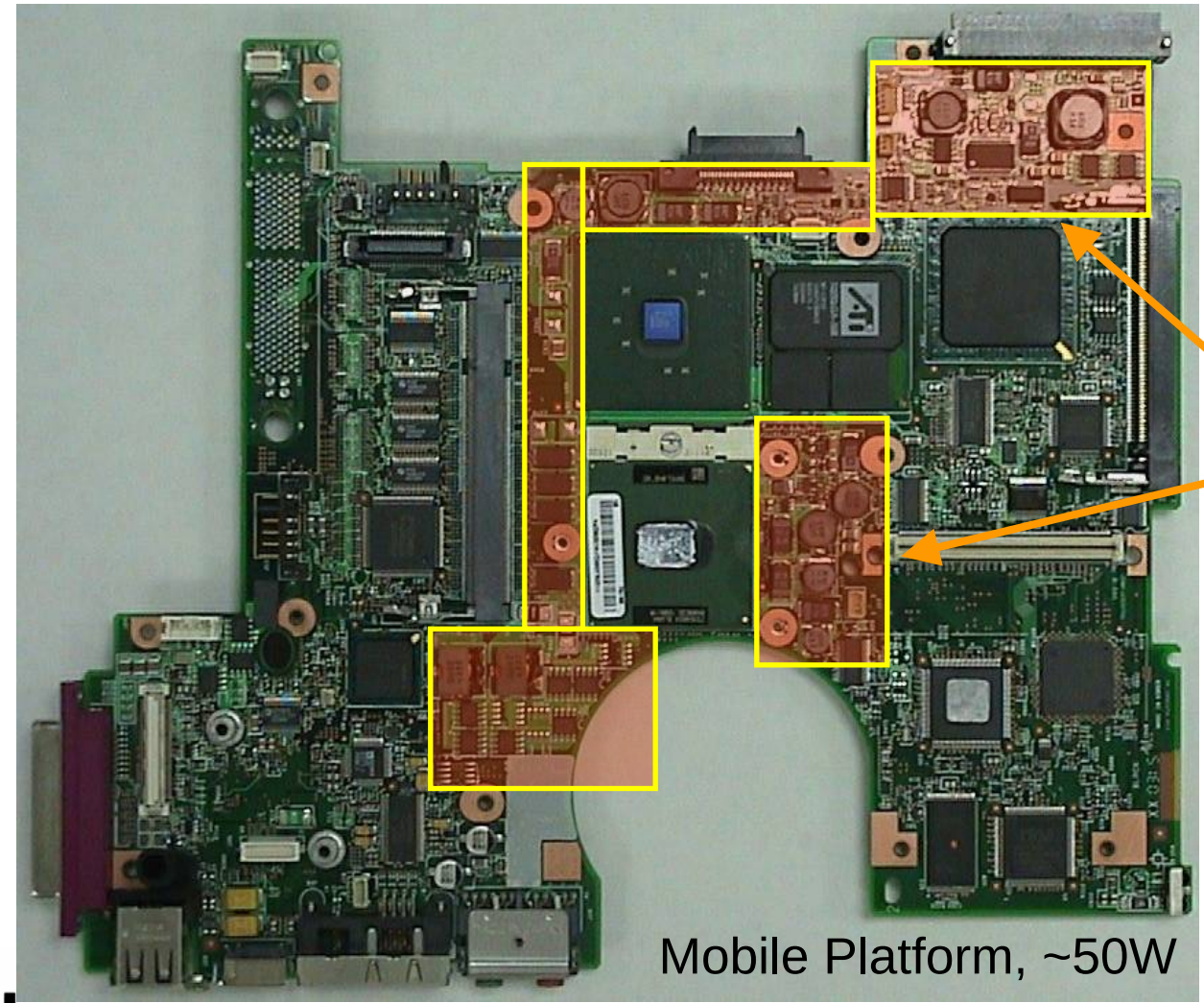
CPU & electronics power in a platform is low
Must reduce power of other platform ingredients

Efficiency of Power Delivery



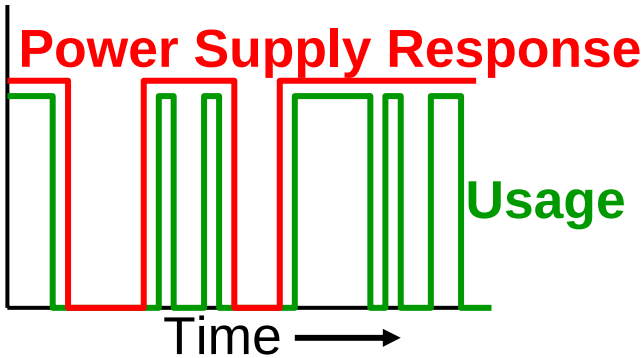
Difficult to maintain high efficiency across workloads
Power supply design needs to exploit new technologies

Typical Power Delivery System

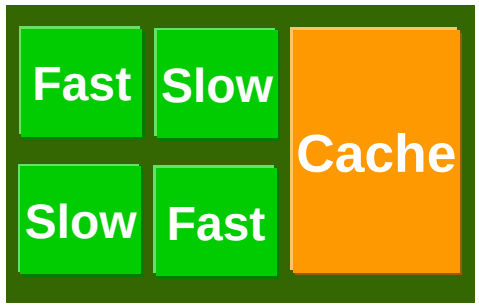


Power
Delivery
Electronics

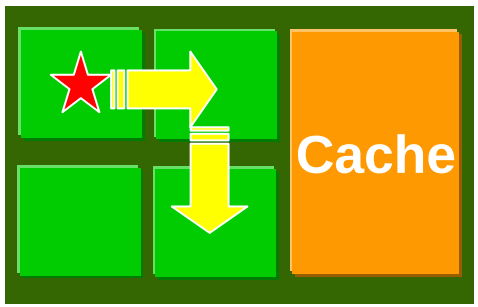
Fine-grain Power Management



Improve response time
Bring power supply closer



Provide multiple supply voltages
Fine grain Vdd and Freq scaling



Core Hopping for hot spot & power density management

Software & Low Power

Applications	Provide guidance to compilers and operating system through policy
Compilers	Add hooks for fine grain power management, and assist OS by providing checkpoints
Operating System	Fine grain power management algorithm Control HW through firmware
Firmware	Hardware control Detect conditions, take action, notify OS

Fine grain power management is possible only by cooperation of the entire software stack

Co-optimization

Technology	Circuits	μArch	Platform	Software
SD Leakage (Ioff) Number of Vt's	Leakage avoidance, control & tolerance	Optimal pipeline Throughput oriented micro-architecture	Fine grain power management hardware & software	
Gate dielectric (Tox)				
Supply voltage (Vdd)	Multiple Vdd circuits	Partitioning of logic Error correction	Efficient power delivery & management of multiple Vdd's	
Transistor density	Tradeoff frequency for transistors	Throughput oriented micro-architecture	Software and applications to utilize logic throughput	
Interconnect	RC delay tolerance		Interconnect cost vs efficiency of power delivery	

Summary

- **Power and energy will limit integration**
- **Employ circuit techniques for SD leakage avoidance, control, & tolerance**
- **Microarchitecture for Low Power**
- **Opportunities to save power at the platform level—Hardware & Software**
- **Technology, Circuits, Architecture, and System co-optimization will be key**