LAB MANUAL

Digital Electronics Lab
(EE-224-F)

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STUDENTS GUIDELINES

There is 1Hr 40 Minutes allocated to a laboratory session in Digital Electronics. It is a necessary part of the course at which attendance is compulsory.
Here are some guidelines to help you perform the experiments and to submit the reports:

1 Read all instructions carefully and carry them all out.

2 Ask a demonstrator if you are unsure of anything.

3 Record actual results (comment on them if they are unexpected!)

4 Write up full and suitable conclusions for each experiment.

5 If you have any doubt about the safety of any procedure, contact the demonstrator beforehand.

6 **THINK** about what you are doing!

CONTENTS

Experiment No:1

AIM: Introduction to Digital Laboratory Equipments & IC's

The Breadboard

The breadboard consists of two terminal strips and two bus strips (often broken in the centre). Each bus strip has two rows of contacts. Each of the two rows of contacts are a node. That is, each contact along a row on a bus strip is connected together (inside the breadboard). Bus strips are used primarily for power supply connections, but are also used for any node requiring a large number of connections. Each terminal strip has 60 rows and 5 columns of contacts on each side of the centre gap. Each row of 5 contacts is a node.

You will build your circuits on the terminal strips by inserting the leads of circuit components into the contact receptacles and making connections with 22-26 gauge wire. There are wire cutter/strippers and a spool of wire in the lab. It is a good practice to wire +5V and 0V power supply connections to separate bus strips.

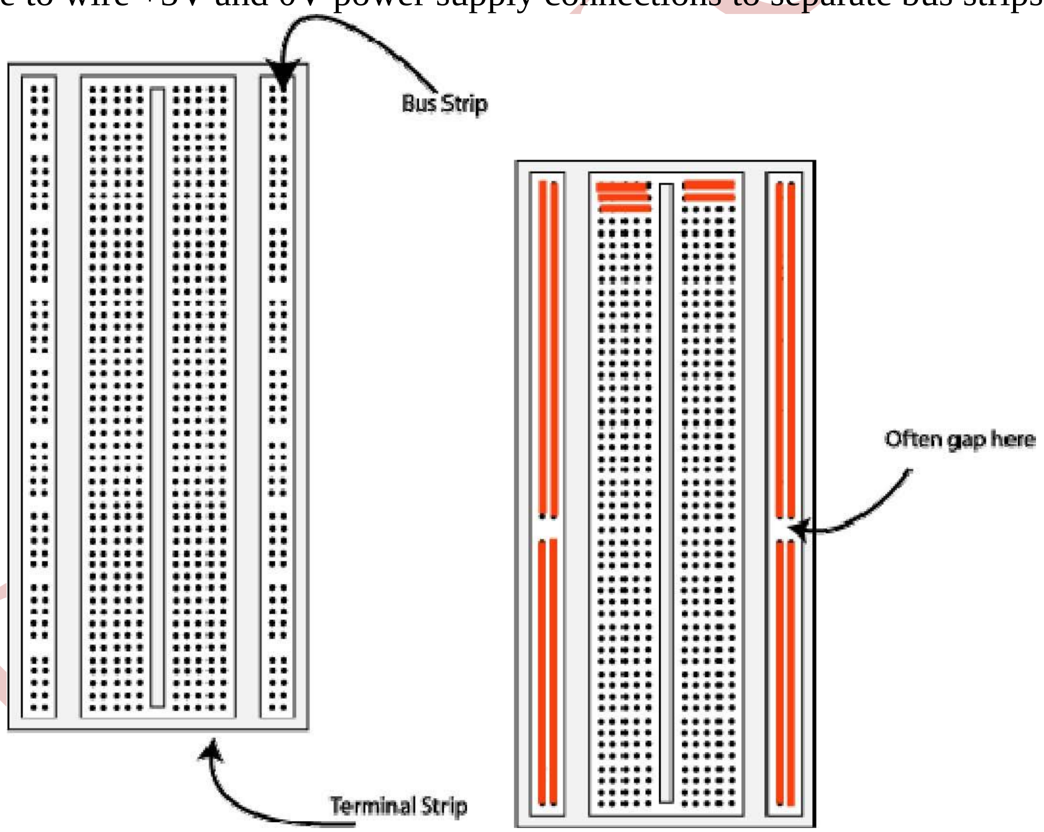


Fig 1. The breadboard. The lines indicate connected holes.

The 5V supply **MUST NOT BE EXCEEDED** since this will damage the ICs (Integrated circuits) used during the experiments. Incorrect connection of power to the ICs could result in them exploding or becoming very hot - with the **possible**

serious injury occurring to the people working on the experiment! Ensure that the power supply polarity and all components and connections are correct <u>before</u> switching on power.

Building the Circuit:

Throughout these experiments we will use TTL chips to build circuits. The steps for wiring a circuit should be completed in the order described below:

1. Turn the power (Trainer Kit) off before you build anything!
2. Make sure the power is off before you build anything!
3. Connect the +5V and ground (GND) leads of the power supply to the power and ground bus strips on your breadboard.
4. Plug the chips you will be using into the breadboard. Point all the chips in the same direction with pin 1 at the upper-left corner. (Pin 1 is often identified by a dot or a notch next to it on the chip package)
5. Connect +5V and GND pins of each chip to the power and ground bus strips on the breadboard.
6. Select a connection on your schematic and place a piece of hook-up wire between corresponding pins of the chips on your breadboard. It is better to make the short connections before the longer ones. Mark each connection on your schematic as you go, so as not to try to make the same connection again at a later stage.
7. Get one of your group members to check the connections, **before you turn the power on**.
8. If an error is made and is not spotted before you turn the power on. Turn the power off immediately before you begin to rewire the circuit.
9. At the end of the laboratory session, collect you hook-up wires, chips and all equipment and return them to the demonstrator.
10. Tidy the area that you were working in and leave it in the same condition as it was before you started.

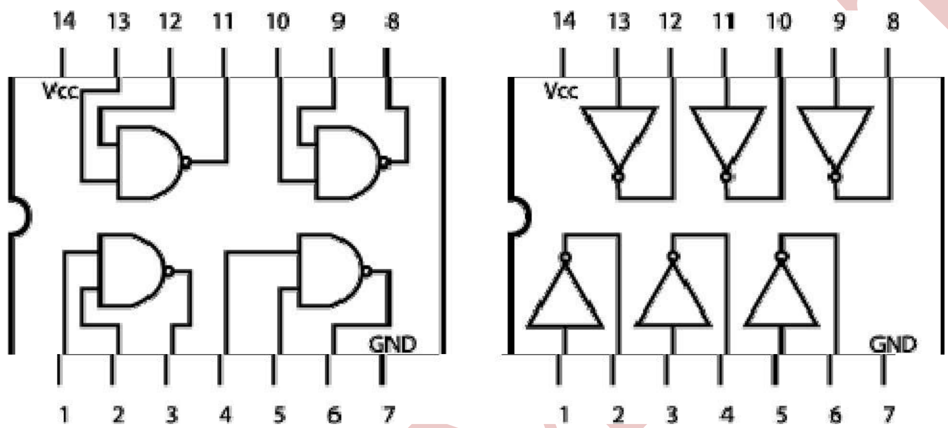
Common Causes of Problems:

1. Not connecting the ground and/or power pins for all chips.
2. Not turning on the power supply before checking the operation of the circuit.
3. Leaving out wires.
4. Plugging wires into the wrong holes.
5. Driving a single gate input with the outputs of two or more gates
6. Modifying the circuit with the power on.

In all experiments, you will be expected to obtain all instruments, leads, components at the start of the experiment and return them to their proper place after you have finished the experiment. Please inform the demonstrator or technician if you locate faulty equipment. If you damage a chip, inform a demonstrator, don't put it back in the box of chips for somebody else to use.

Example Implementation of a Logic Circuit:

Build a circuit to implement the Boolean function F = /(/A./B), please note that the notation **/A** refers to $\bar{A}$. You should use that notation during the write-up of your laboratory experiments.



Quad 2 Input 7400 Hex 7404 Inverter

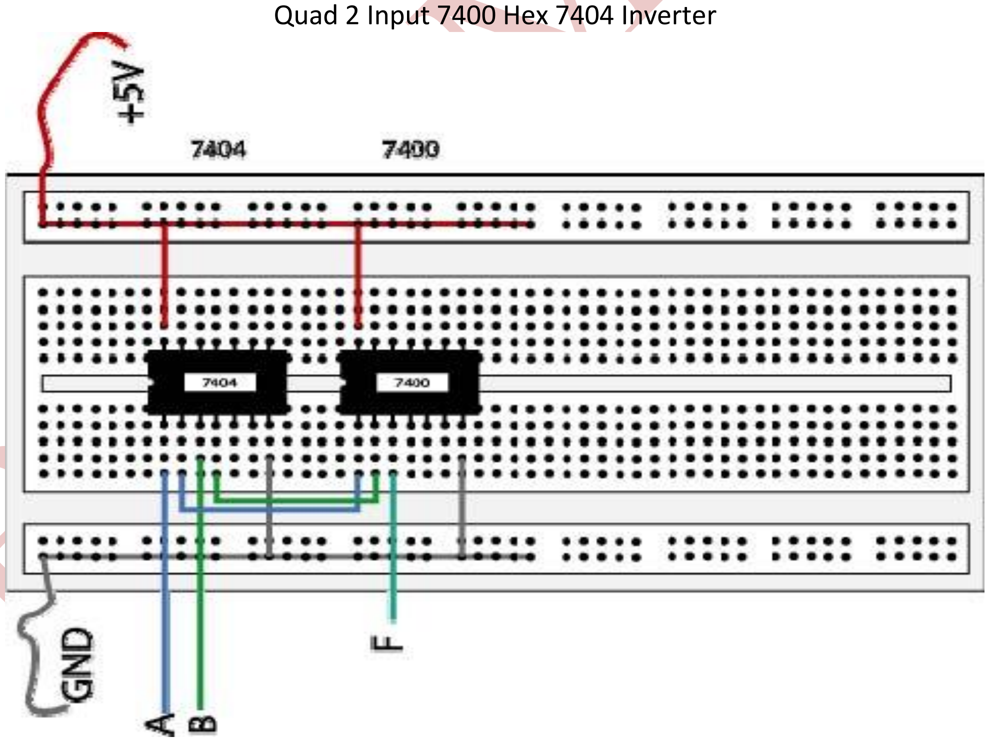


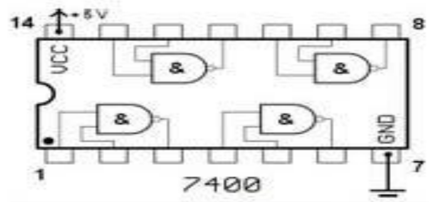
Fig 2. The complete designed and connected circuit

Sometimes the chip manufacturer may denote the first pin by a small indented circle above the first pin of the chip. Place your chips in the same direction, to save confusion at a later stage. Remember that you must connect power to the chips to get them to work.

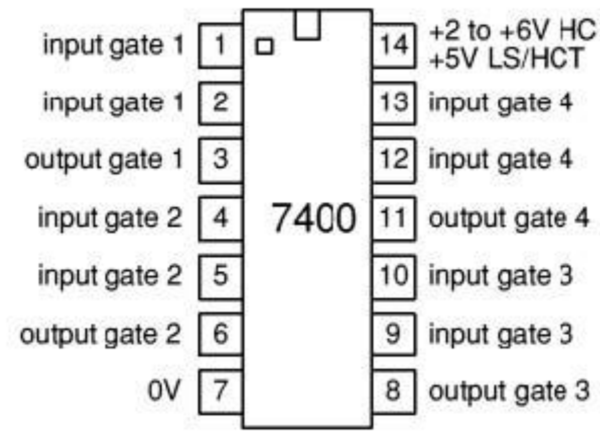
Useful IC Pin details

IC NUMBER	Description of IC
7400	Quad2inputNANDGATE
7401	Quad2inputNANDGate(opencollector)
7402	Quad 2 input NOR Gate
7403	Quad2inputNORGates(opencollector)
7404	Hex Inverts
7421	Dual 4 input AND Gates
7430	8 input NAND Gate
7432	Quad 2 input OR Gates
7486	Quad 2 input EX-OR Gate
74107	Dual j-k Flip Flop
74109	Dual j-k Flip Flop
74174	Hex D Flip Flop
74173	Quad D Flip Flop
7473	Dual j-k Flip Flop
7474	Dual D Flip Flop
7475	Quad Bi-stable latch

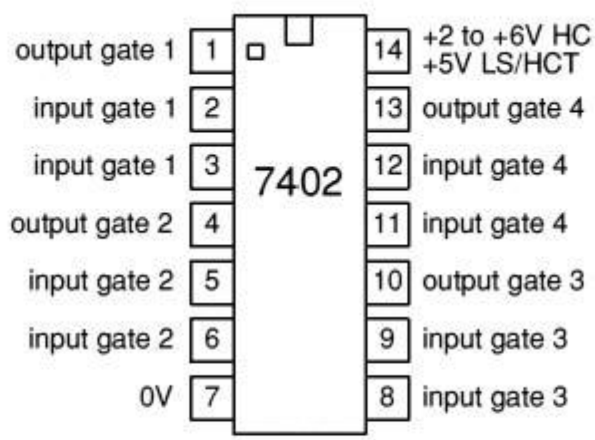
7476	Dual j-k Flip Flop



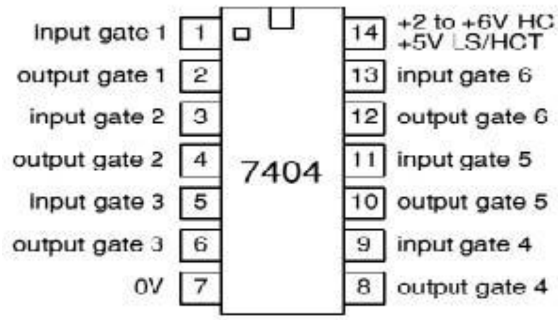
7400(NAND)



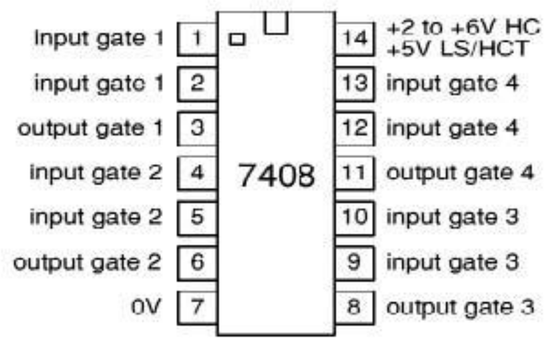
7402(NOR)



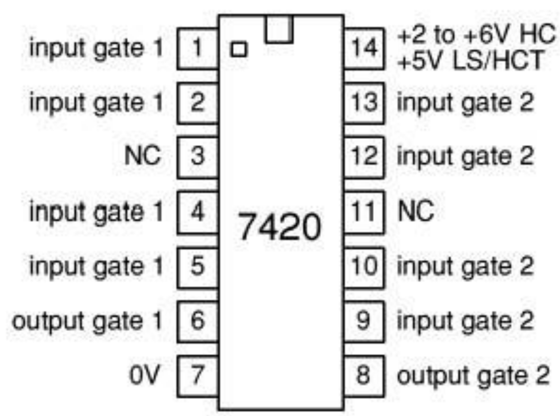
7404(NOT)



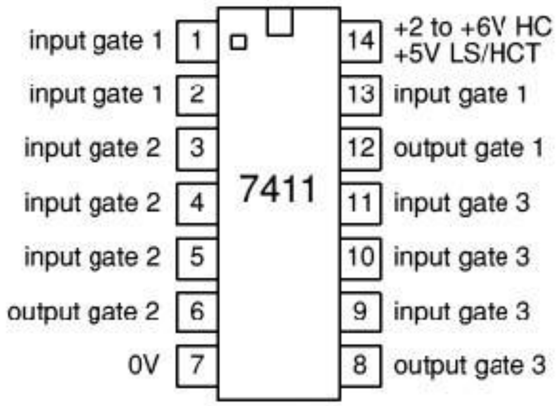
7408(AND)



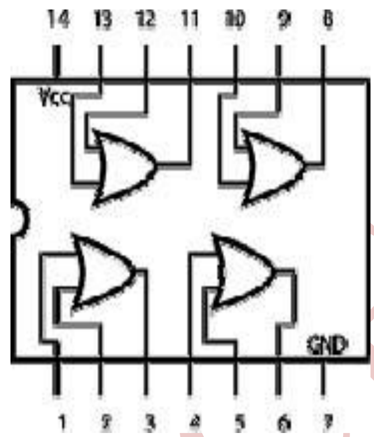
7420(4-i/pNAND)



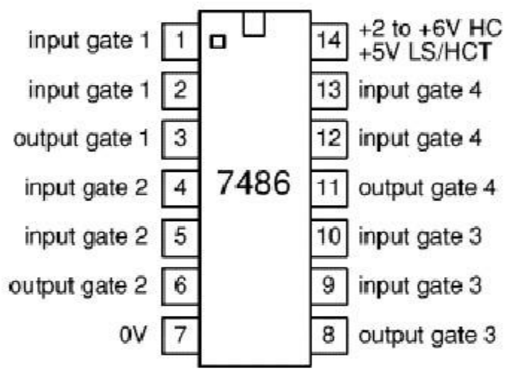
7411(3-i/p AND)

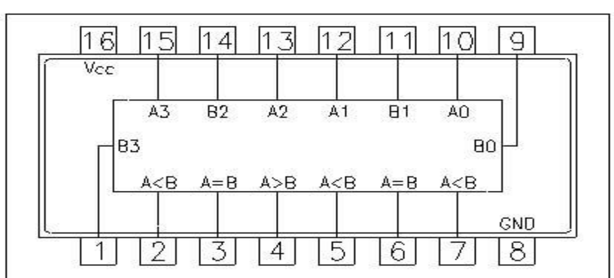


7432(OR)



7486(EX- R)





7485
4-Bit Magnitude Comparator

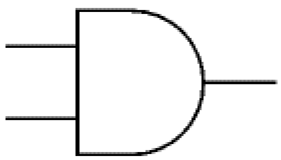
Experiment No:2

AIM:- To study basic gates (AND , OR , NOT) and verify their truth tables.

APPARATUS:- LED, IC's , Wires , 5 volt DC supply, Bread Board etc.

THEORY:-

AND Gate



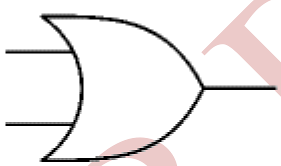
Input A	Input B	Output Q
0	0	0
0	1	0
1	0	0
1	1	1

Traditional symbol Truth Table

In AND gate circuit it has n input and only one output. Digital signals are applied in input terminal. In the AND gate operation is 't' if and only if all the input are '1' otherwise zero.

Mathematically :The output Q is true if input A AND input B are both true: **Q = A AND B** An AND gate can have two or more inputs, its output is true if all inputs are true.

OR Gate



Traditional symbol Truth Table

Input A	Input B	Output Q
0	0	0
0	1	1
1	0	1
1	1	1

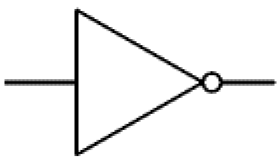
In OR-Gate operation it has also n input and only one output. In OR operation output is one if and only if one or more input are '1'.

Mathematically

The output Q is true if input A OR input B is true (or both of them are true): ***Q = A OR B***

An OR gate can have two or more inputs, its output is true if at least one input is true.

NOT Gate (Inverter)



Input A	Output Q
0	1
1	0

Traditional symbol Truth Table

It is also known as inverter. It has only one input and one output.Mathematically

*The output Q is true when the input A is NOT true, the output is the inverse of the input:**Q = NOT A**. A NOT gate can only have one input. A NOT gate is also called an inverter.*

RESULT:- *Corresponding truth tables of logic gates are verified.*

PRECAUTIONS:-

1. *Supply should not exceed 5v.*
2. *Connections should be tight and easy to inspect.*
3. *Use L.E.D. with proper sign convention and check it before conneting in circuit.*

Experiment No:3

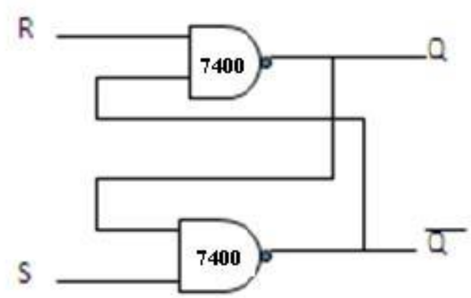
Aim: -To design and construct basic flip-flops R-S ,J-K,J-K Master slave flip-flops using gates and verify their truth tables

Apparatus: -

1 IC's - 7404, 7402, 7400
2 Electronic circuit designer
3 Connecting patch chords

Circuit Diagrams:-

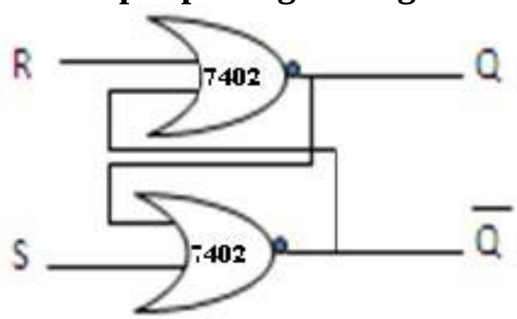
Basic flipflop using NAND gates



Truth Table

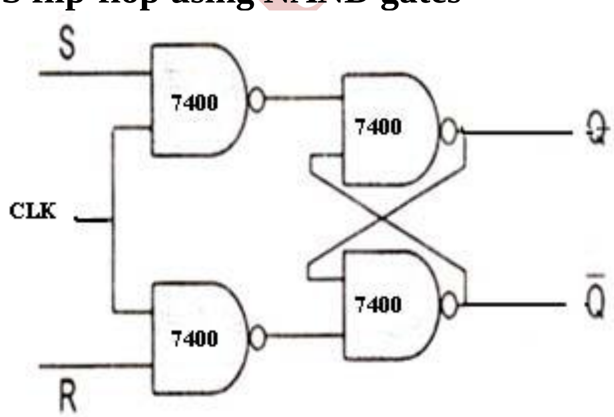
S	R	Q
0	0	Forbidden
0	1	1
1	0	0
1	1	No Change

Basic flipflop using NOR gates



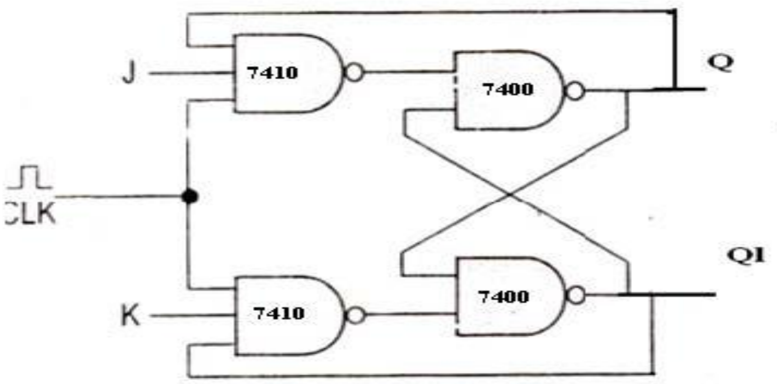
S	R	Q
0	0	No Change
0	1	0
1	0	1
1	1	Forbidden

R-S flip-flop using NAND gates



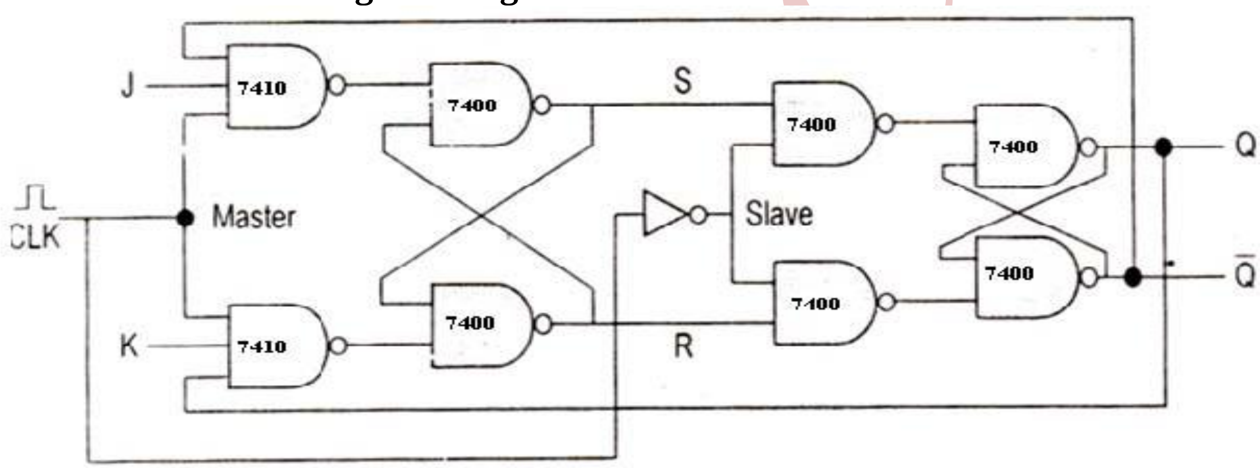
S	R	Q
0	0	No Change
0	1	0
1	0	1
1	1	Forbidden

J-k flip-flop using NAND gates



J	K	Q
0	0	No Change
0	1	0
1	0	1
1	1	Race around

J-K Master Slave using NAND gates



J	K	Q
0	0	
0	1	0
1	0	1
1	1	

Procedure:

1. Connect the Flip-flop circuits as shown above.
2. Apply different combinations of inputs and observe the outputs .

Precautions: All the connections should be made properly.

Result: Different Flip-flops using gates are constructed and their truth tables are verified

Experiment No:4

AIM: To design and implement encoder and decoder using logic gates and study of IC 7445 and IC 74147.

APPARATUS REQUIRED:

Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	3 I/P NAND GATE	IC 7410	2
2.	OR GATE	IC 7432	3
3.	NOT GATE	IC 7404	1
2.	IC TRAINER KIT	-	1
3.	PATCH CORDS	-	27

THEORY:

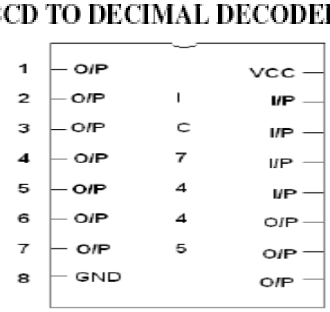
ENCODER:
An encoder is a digital circuit that performs inverse operation of a decoder. An encoder has 2^n input lines and n output lines. In encoder the output lines generates the binary code corresponding to the input value. In octal to binary encoder it has eight inputs, one for each octal digit and three output that generate the corresponding binary code. In encoder it is assumed that only one input has a value of one at any given time otherwise the circuit is meaningless. It has an ambiguila that when all inputs are zero the outputs are zero. The zero outputs can also be generated when D0 = 1.

DECODER:

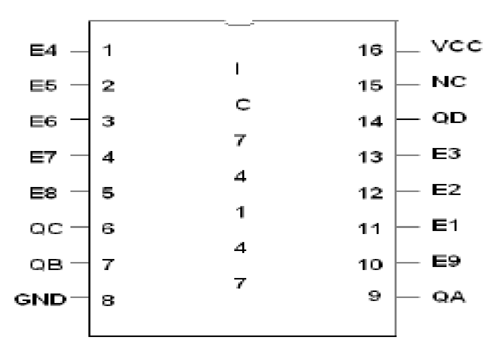
A decoder is a multiple input multiple output logic circuit which converts coded input into coded output where input and output codes are different. The input code generally has fewer bits than the output code. Each input code word produces a different output code word i.e there is one to one mapping can be expressed in truth table. In the block diagram of decoder circuit the encoded information is present as n input producing 2^n possible outputs. 2^n output values are from 0 through output 2^n-1

PIN DIAGRAM FOR IC 7445:

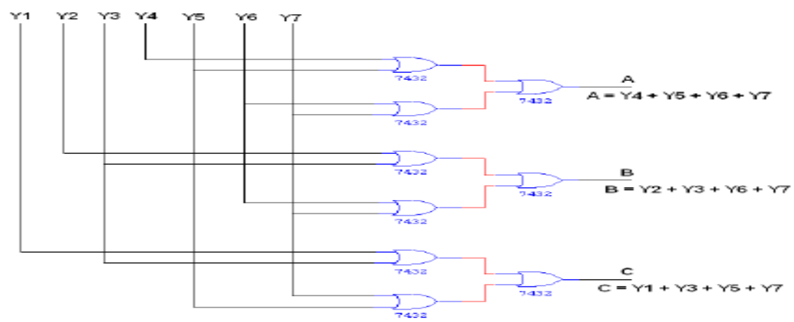
BCD TO DECIMAL DECODER:



PIN DIAGRAM FOR IC 74147:

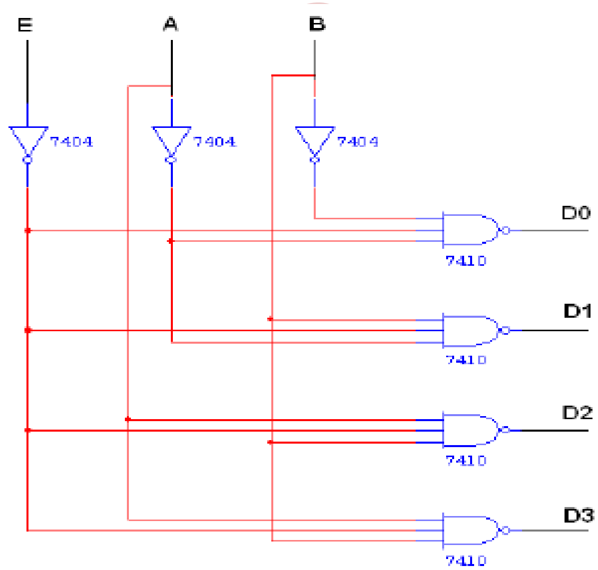


LOGIC DIAGRAM FOR ENCODER



INPUT							OUTPUT		
Y1	**Y2**	**Y3**	**Y4**	**Y5**	**Y6**	**Y7**	**A**	**B**	**C**
1	0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	1	1
0	0	0	1	0	0	0	1	0	0
0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	1	1	1	1

LOGIC DIAGRAM FOR DECODER:



TRUTH TABLE:

INPUT			OUTPUT			
E	A	B	D0	D1	D2	D3
1	0	0	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

PROCEDURE:

(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table.

RESULT:

Thus the design and implementation of encoder and decoder using logic gates and study of IC 7445 and IC 74147 were done.

Experiment No: 5 & 6

AIM: To design and implement Multiplexer and Demultiplexer using logic gates and study of IC 74150 and IC 74154.

APPARATUS REQUIRED:

Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	3 I/P AND GATE	IC 7411	2
2.	OR GATE	IC 7432	1
3.	NOT GATE	IC 7404	1
4.	IC TRAINER KIT -		1
5.	PATCH CORDS -		

THEORY:

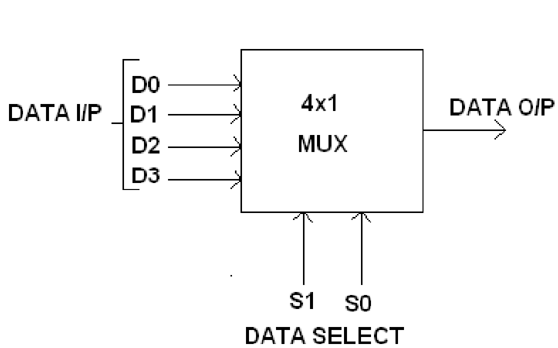
MULTIPLEXER:

Multiplexer means transmitting a large number of information units over a smaller number of channels or lines. A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally there are 2n input line and n selection lines whose bit combination determine which input is selected.

DEMULTIPLEXER:

The function of Demultiplexer is in contrast to multiplexer function. It takes information from one line and distributes it to a given number of output lines. For this reason, the demultiplexer is also known as a data distributor. Decoder can also be used as demultiplexer. In the 1: 4 demultiplexer circuit, the data input line goes to all of the AND gates. The data select lines enable only one gate at a time and the data on the data input line will pass through the selected gate to the associated data output line.

BLOCK DIAGRAM FOR 4:1 MULTIPLEXER:

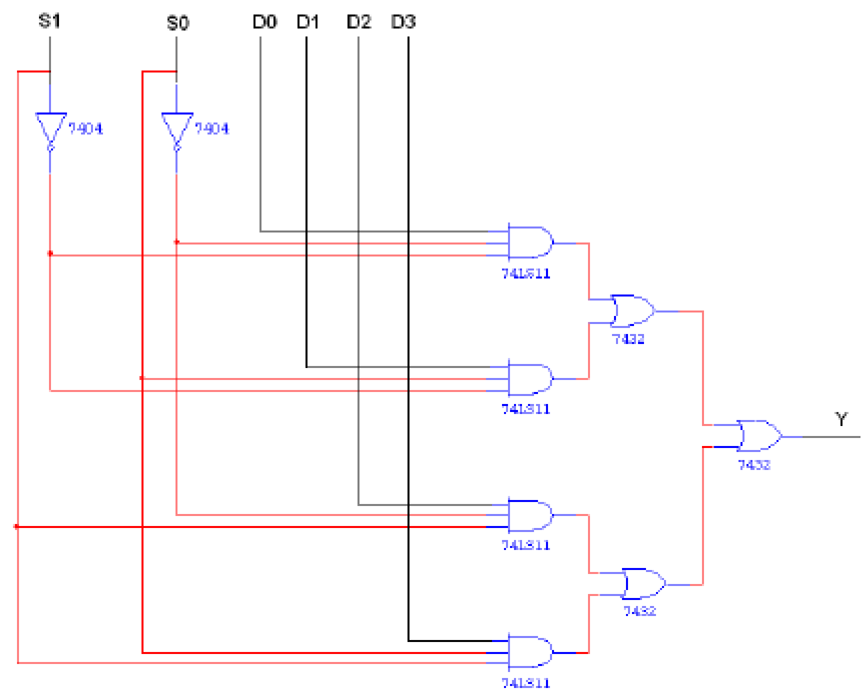


FUNCTION TABLE:

S1	S0	INPUTS Y
0	0	D0 → D0 S1' S0'
0	1	D1 → D1 S1' S0
1	0	D2 → D2 S1 S0'
1	1	D3 → D3 S1 S0

Y = D0 S1' S0' + D1 S1' S0 + D2 S1 S0' + D3 S1 S0

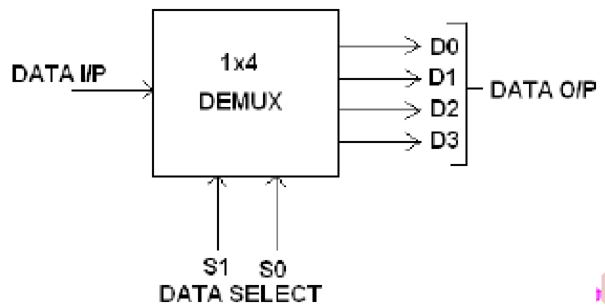
CIRCUIT DIAGRAM FOR MULTIPLEXER:



TRUTH TABLE:

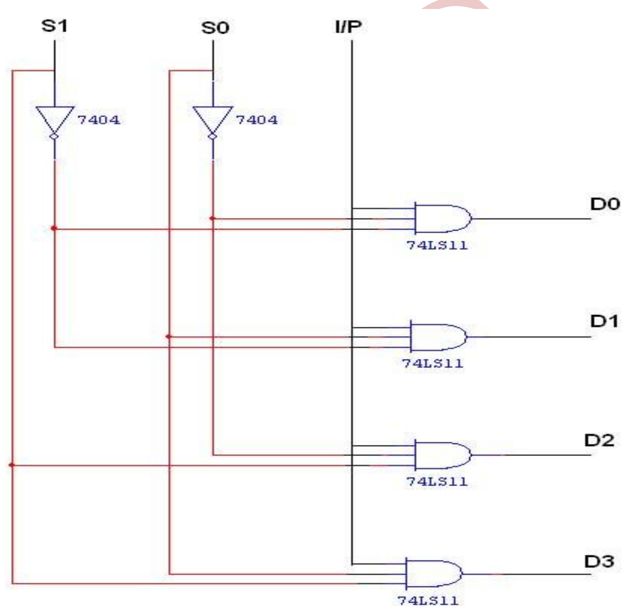
S1	S0	Y = OUTPUT
0	0	D0
0	1	D1
1	0	D2
1	1	D3

BLOCK DIAGRAM FOR 1:4 DEMULTIPLEXER:



S1	S0	INPUT
0	0	X → D0 = X S1' S0'
0	1	X → D1 = X S1' S0
1	0	X → D2 = X S1 S0'
1	1	X → D3 = X S1 S0

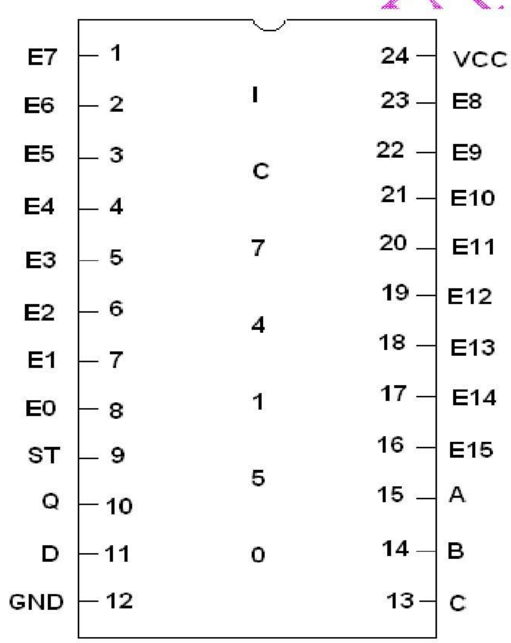
Y = X S1' S0' + X S1' S0 + X S1 S0' + X S1 S0



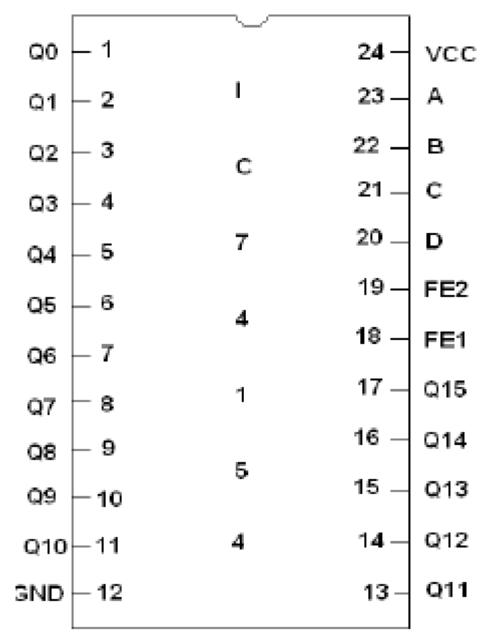
TRUTH TABLE:

INPUT			OUTPUT			
S1	**S0**	**I/P**	**D0**	**D1**	**D2**	**D3**
0	0	0	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	1	0	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	1	0
1	1	0	0	0	0	0
1	1	1	0	0	0	1

PIN DIAGRAM FOR IC 74150:



PIN DIAGRAM FOR IC 74154:



PROCEDURE:

(i) Connections are given as per circuit diagram.

(ii) Logical inputs are given as per circuit diagram.

(iii) Observe the output and verify the truth table.

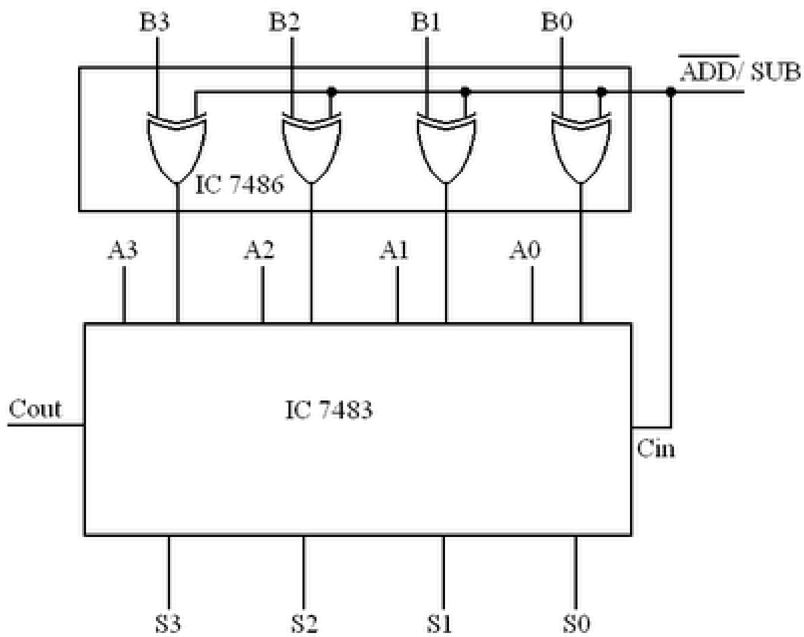
RESULT:
Thus the design and implementation of Multiplexer and Demultiplexer using logic gates and study of IC 74150 and IC 74154 were done

Experiment No:7

AIM: To verify the truth table of 4- bit adder and 2's compliment subtractor circuit using a 4-bit adder IC(7483) are verified

Apparatus: Logic trainer kit, 4-bit adder (IC 7483), X-OR gates (IC 7486), wires

Theory: IC 7483 is a 4 bit adder. In binary, subtraction can be performed by using 2's complement method. In this method negative number is converted into its 2's complement and it is added to the other number. The result of this addition is the subtraction of origin numbers.
If we modify the adder circuit, such that 2's complement and simple representation are presented, we can perform addition subtraction as required. X-OR gate is used as a controlled inverter/ buffer for this purpose. Use it as buffer for addition and inverter for subtraction.



Procedure:
1. Connect the IC 7483 and IC 7486 as per diagram.
2. Connect all A's and all B's to logic sources, S's to logic indicators.
3. Connect Cin to logic 0, this will set the circuit for addition.
4. Give various input combinations, verify adder operation. Here Cout is MSB of addition.
5. Connect Cin to logic 1, this will set the circuit for subtraction by 2's complement method.
6. Give various input combinations and observe outputs. Here Cout is neglected (2's complement subtraction)
7. Switch off power supply

Precautions: All the connections should be made properly.

Result: The truth table of 4- bit adder, 2's compliment subtractor circuit using a 4-bit adder IC are verified.

Experiment No:8

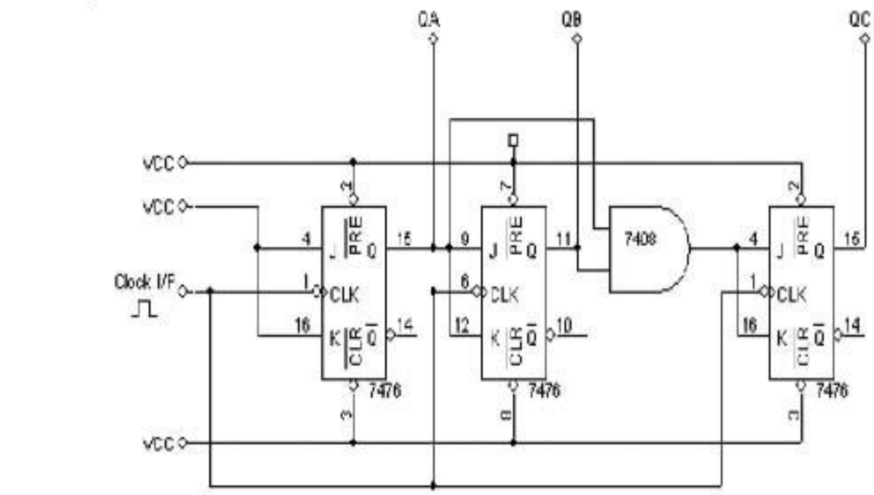
Aim:- To design and construct of 3-bit Synchronous up and down counters,2-bit up/down counter.

Apparatus:

1 IC's - 7408,7476,7400,7432
2 Electronic circuit designer
3 Connecting patch chords

Circuit Diagram:

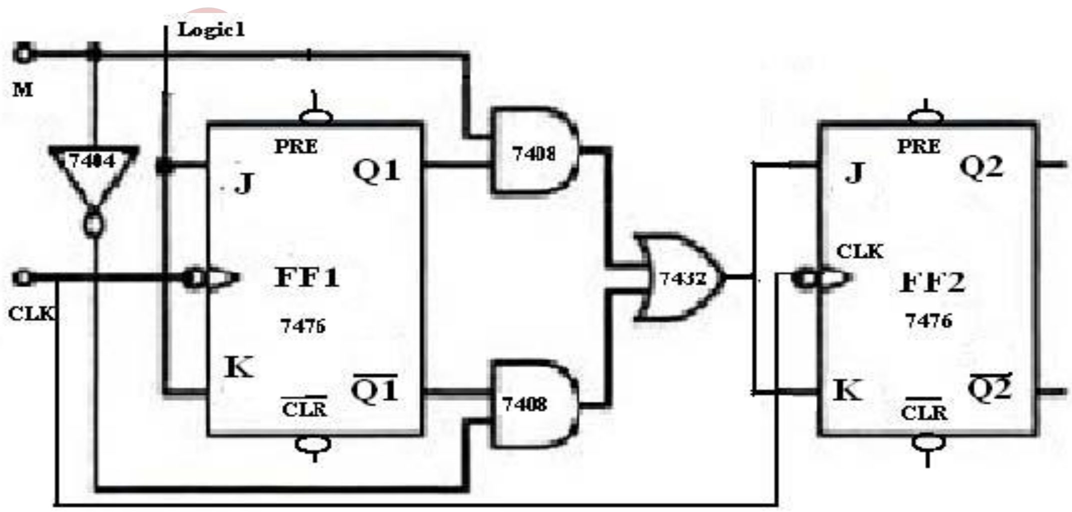
3-bit Synchronous Counter:-



Truth Table

3-bit synchronous up counter			
Clock	QC	QB	QA
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

Two Bit up/Down Counter using negative edge-triggered flip-flops



WHEN M=1

CLK	Q2	Q1
0	0	0
1	0	1
2	1	0
3	1	1

WHEN M=0

CLK	Q2	Q1
0	1	1
1	1	0
2	0	1
3	0	0

Procedure:

1 Connections are made as per the circuit diagram
2 Switch on the power supply.
3 Apply clock pulses and note the outputs after each clock pulse and note done the out puts.

Result: 3-bit Synchronous up and down counters,2-bit up/down counter are designed and truth tables are verified.

Precautions:

1 All the connections should be made properly.
2 IC should not be reversed.

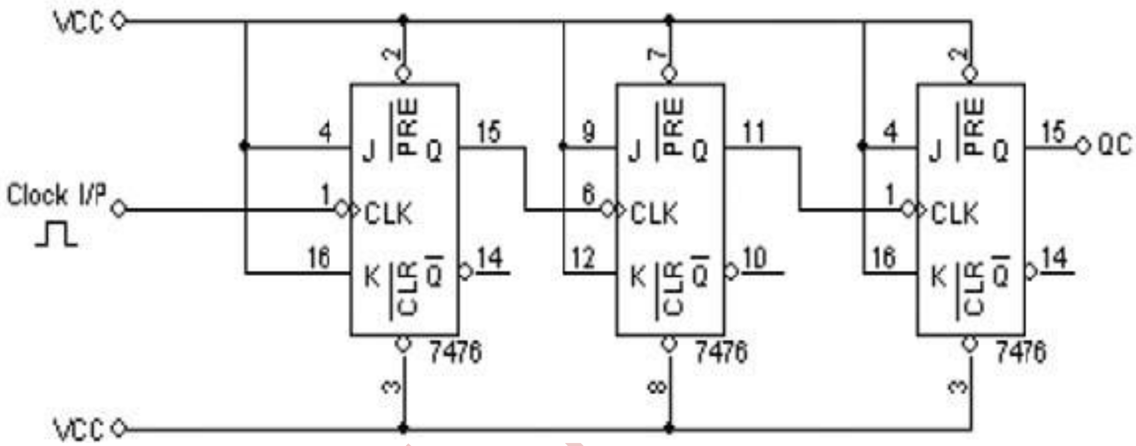
Experiment No:9

AIM: To design and construct of Asynchronous up and down counters, 2-bit up/down counter.

Apparatus:

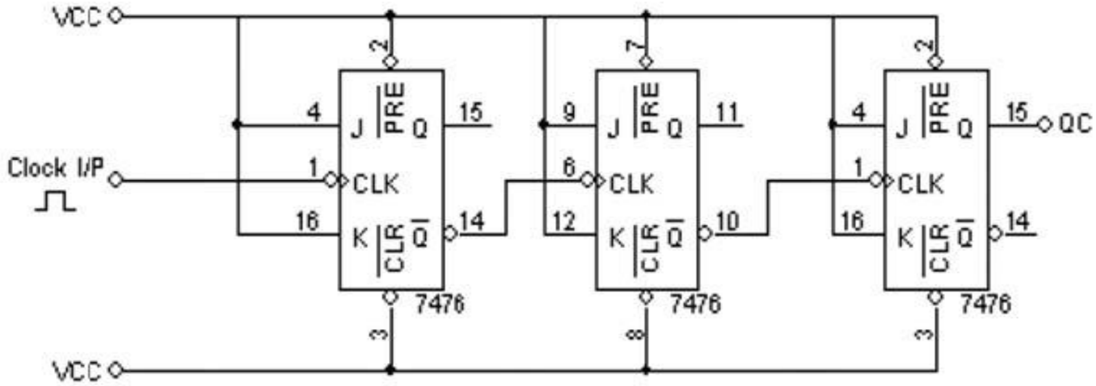
1 IC's - 7408,7476,7400,7432
2 Electronic circuit designer
3 Connecting patch chords

Circuit Diagram: 3-bit Asynchronous up counter:



3-bit Asynchronous up counter			
Clock	QC	QB	QA
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

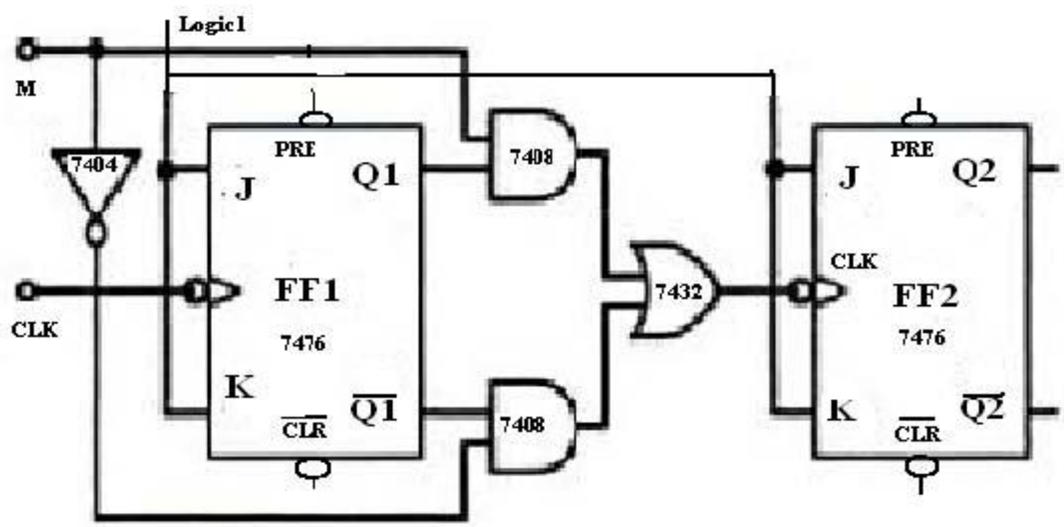
3-bit Asynchronous down counter:



TRUTH TABLE

3-bit Asynchronous down counter			
Clock	QC	QB	QA
0	1	1	1
1	1	1	0
2	1	0	1
3	1	0	0
4	0	1	1
5	0	1	0
6	0	0	1
7	0	0	0
8	1	1	1
9	1	1	0

Two Bit up/Down Counter using negative edge-triggered flip-



WHEN M=1

CLK	Q2	Q1
0	0	0
1	0	1
2	1	0
3	1	1

WHEN M=0

CLK	Q2	Q1
0	1	1
1	1	0
2	0	1
3	0	0

Procedure:

1 Connections are made as per the circuit diagram
2 Switch on the power supply.
3 Apply clock pulses and note the outputs after each clock pulse and note done the out puts.

Result: 3-bit Asynchronous up and down counters,2-bit up/down counter are designed and truth tables are verified.

Precautions:

1 All the connections should be made properly.
2 IC should not be reversed.

Experiment No:10

AIM:- Realize Basic gates (AND,OR,NOT) From Universal Gates(NAND & NOR).

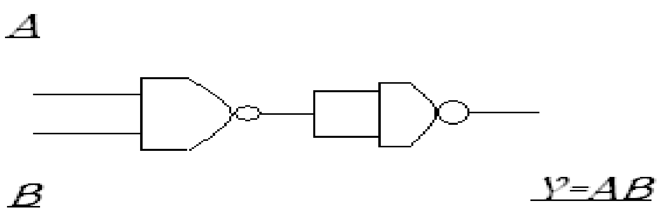
APPARATUS:- L.E.D., Bread-Board, I.C.'s, Wires, "5.0" V d.c. supply, etc.

THEORY:-

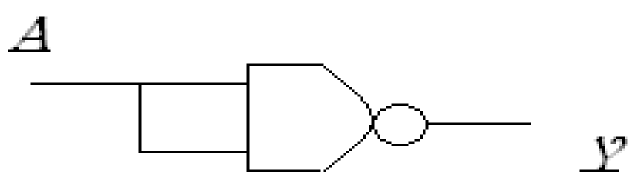
NAND Gates to AND, OR, NOT Gates:-

NAND gates is Universal gate. The Basic gates AND, OR, NOT can be realized from it. The Boolean equations and logic diagrams are as follows :

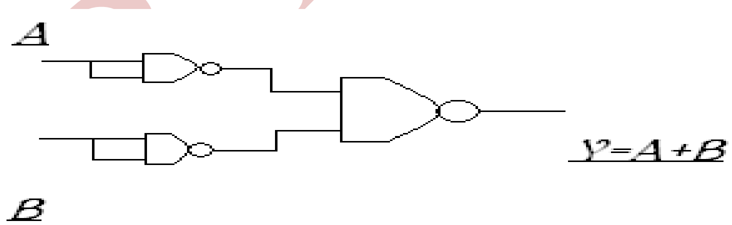
NAND TO AND :



NAND TO NOT :



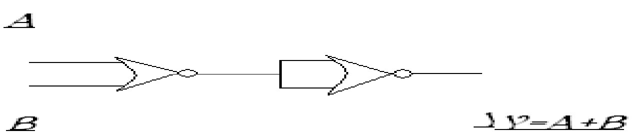
NAND TO OR :



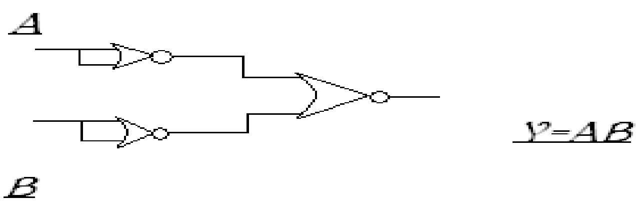
NOR Gate to AND, OR, NOT Gates :

NOR gate is also an Universal gate. The Basic gates AND, OR, NOT can be realized from it. The Boolean equations and logical diagrams are as follows :

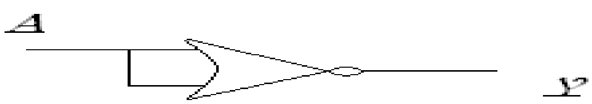
NOR to OR Gate :



NOR to AND Gate



NOR to NOT Gate



Truth tables :

NAND to AND Gate

Inputs		**Output**
A	**B**	**Y**
0	0	0
0	1	0
1	0	0
1	1	1

NAND to OR Gate

Inputs		**Output**
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	1

NAND to NOT Gate

input	output
A	Y
0	1
1	0

NOR to AND Gate

Inputs		Output
A	**B**	**Y**
0	0	0
0	1	0
1	0	0
1	1	1

NOR to OR Gate

Inputs		Output
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	1

NOR to NOT Gate

input	output
A	Y
0	1
1	0

RESULT:
The realization of basic gates(AND ,OR ,NOT) from universal gates(NAND &NOR) is successful.& The corresponding truth-tables are also verified.

PRECAUTIONS:-

1) Supply should not exceed 5v.
2) Connections should be tight and easy to inspect.
3) Use L.E.D. with proper sign convention and check it before conneting in circuit.

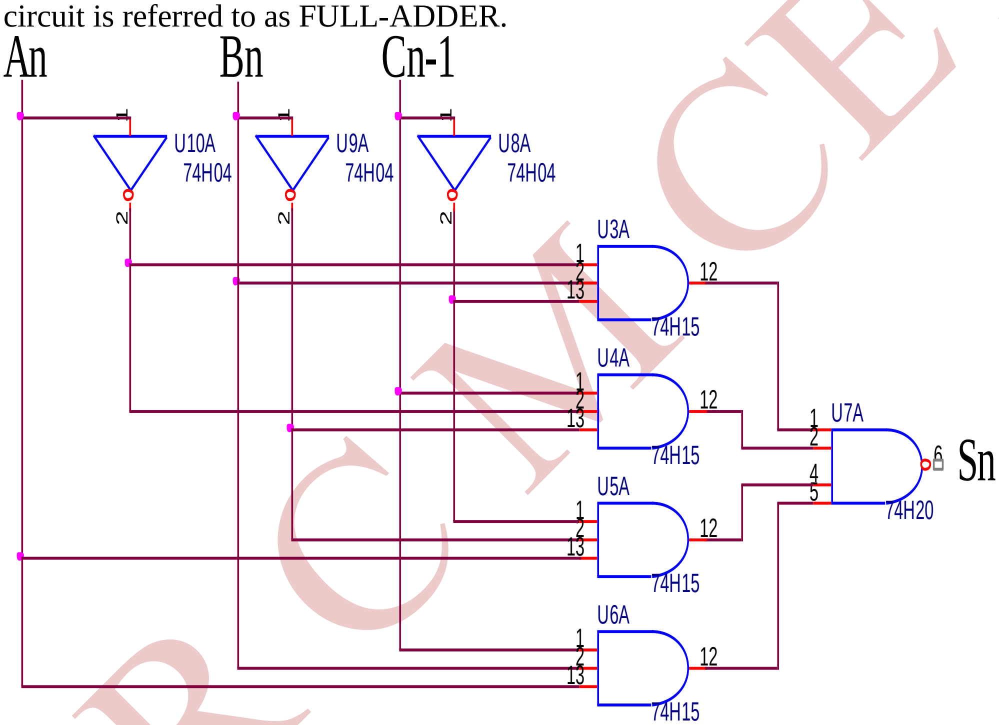
Experiment No:11

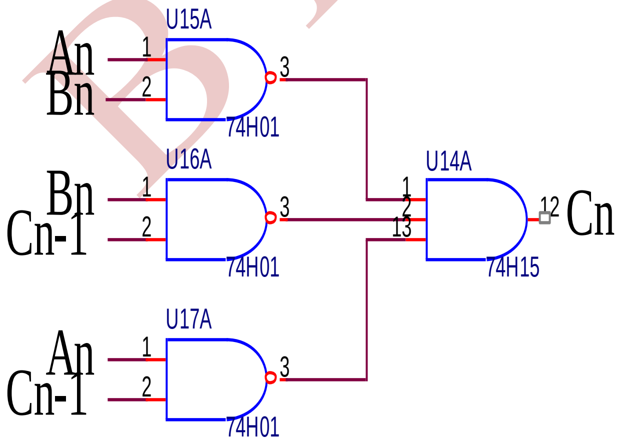
AIM:-To study about full adder & verify its truth table.

APPARATUS:-IC-(7486,7408,7432),Connecting wires, LED, Bread board,Cutter,5v supply.

THEORY:-

An half adder has only two inputs and there is no provision to add a carry coming from the lower order bits when multibit addition is performed. For this purpose, a third input terminal is added and this circuit is used to add An, Bn and Cn-1 where An and Bn are the nth order bits of the numbers A and B respectively and Cn-1 is the carry generated from the addition of (n-1)th order bits. This circuit is referred to as FULL-ADDER.





TRUTH TABLE:-

INPUTS			*OUTPUTS*	
An	*Bn*	*Cn-1*	*SUM*	*CARRY*
0	*0*	*0*	*0*	*0*
0	*0*	*1*	*1*	*0*
0	*1*	*0*	*1*	*0*
0	*1*	*1*	*0*	*1*
1	*0*	*0*	*1*	*0*
1	*0*	*1*	*0*	*1*
1	*1*	*0*	*0*	*1*
1	*1*	*1*	*1*	*1*

PROCEDURE:-

1. Write the truth table for variables An,Bn and Cn-1.
2. Truth table was solved with the help of K-map.
3. Circuit was connected and the outputs of sum and carry was got separately.
4. Connect the pin no.14 to 5v supply of all IC's used in circuit.
5.Pin no. 7 will be grounded of all IC's.

RESULT:- The truth table of full adder is verified.

PRECAUTIONS:-

1. Supply should not exceed 5v.
2. Connections should be tight and easy to inspect.
3. Use L.E.D. with proper sign convention and check it before conneting in circuit.