Distributed Modulation and Control of Modular Multilevel Converter for HVDC Application

2013

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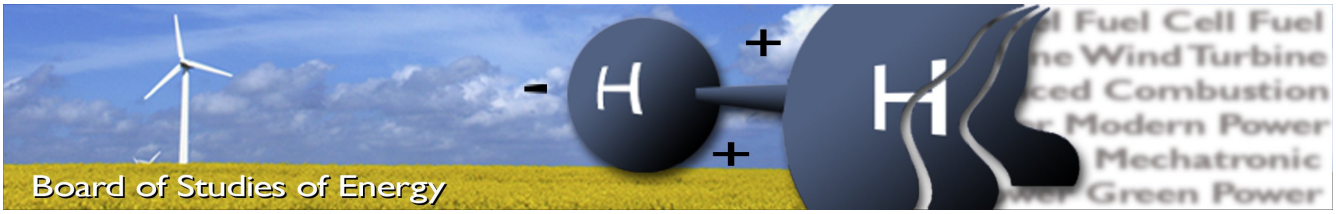

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SYNOPSIS:
The main task of this project is to examine the aspects of modulation and control of MMC (Modular Multilevel Converter); in particular, the focus is on distributed modulation and control.

Two real-time communication technologies, namely EtherCAT and SPI, are investigated with respect to the communication speed, connection capability, synchronization, cost, etc.

As a multilevel modulation technology, resampled uniform PS-PWM is studied through simulations and experiments. A new method to implement the resampling technique is proposed.

The whole distributed control system is described and analyzed. The plant and the controllers are modeled in frequency domain. Controller design through analytical methods and Matlab tools is presented. The sensitiveness of the distributed control system to communication delay, individual carrier frequency is studied through simulations.

Finally the design and tests of the prototype are documented.

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Pages, total: [87]
Appendix: [2]
Supplements: [1 CD]

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Preface

This 9th and 10th semester project is conducted at the department of Energy Technology, Aalborg University during the period from 1st of September 2012 to 30st of May 2013.

This project has been followed by two supervisors: Professor Remus Teodorescu, and Assistant Professor Laszlo Mathe, both from the department of Energy Technology, Aalborg University. I would like to thank both of them for their support and supervision to my work during the entire project period.

I would also like to thank Artjoms Timofejevs, Emanuel-Petre Eni and Daniel Gamboa, the authors of the previous project with the title "Modular Multilevel Converter for Large Transformer-less Wind Turbines". With their help, I was able to understand their work in their previous project, which has been proven to be very useful in this project.

2013-5-27

Shaojun Huang

Abstract

Modular Multilevel Converter (MMC) has gained a lot of interest in industry in the recent years due to its modular design and easy adaption for applications that require different power and voltage level, such as power transmission through HVDC. However, the control and operation of a real MMC consisting of large number of sub modules for high power high voltage application is a very challenge task. For the reason that distributed control architecture could maintain the modularity of the MMC, this control architecture will be investigate in this project.

The suitable communication technologies, which are essential to the distributed control, are discussed firstly. Two real-time communication protocols, namely EtherCAT and SPI, are analyzed with respect to the communication speed, connection topology, connection capability, synchronization accuracy and the cost. The prototype with the SPI solution has been made in the lab and has been successfully tested.

Secondly, the multilevel modulation technologies are examined. The focus is put on the phase shifted PWM (PS-PWM). Analysis of the performance of different PS-PWM, namely uniform PS-PWM and resampled uniform PS-PWM, is carried out in this project. A new method to implement the resampling technique, which is the key technique for the resampled uniform PS-PWM, is proposed and verified by the simulations and experiments.

Thirdly, the distributed control system is analyzed and modelled in frequency domain. Controller design is performed through analytical methods and Matlab tools. The sensitiveness of the distributed control system to modulation effect (phase-shifted PWM), communication delay, individual carrier frequency and sampling frequency is studied through simulations that are made in Matlab Simulink and PLECS.

Finally, the hardware design and software design of the prototype are presented. The experimental results are also documented in this report.

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Chapter 1 Introduction

The main work of this project is to examine the aspects of modulation and control of MMC (Modular Multilevel Converter); in particular, the focus is on distributed modulation and control. The background of the project is presented in section 1.1 of this chapter. Then the goal and limitation of this project will be described in section 1.2 and 1.3. Finally an outline of this thesis ends this chapter.

1.1 Background

HVDC (High Voltage Direct Current) technology can be used for connecting large offshore wind farms, powering islands, transmitting power over long distance, etc. The advantages of using HVDC transmission systems instead of the conventional AC transmission systems include:

- being able to use underground cables instead of overhead lines, thus avoid potential public oppositions when building new transmission lines
- the ability to connect two AC power systems of different frequency
- reducing the cost when transmitting power over very long distance (typically hundreds of kilometres)

HVDC technology evolved from current source converters to voltage source converters and largely reduced their size in the 1990s, as ABB introduced 'HVDC Light' to the market. Being a multilevel voltage source converter, MMC is a promising technology to reduce further the size of HVDC system due to the sine-like output voltage waveform, low harmonics as well as low size filter requirement. The commercial products with the brand name 'HVDC PLUS' (Siemens) [1], 'HVDC MaxSine' (Alstom) [2] and 'HVDC Light' (ABB)[3], as well as several successful HVDC projects (see Table 1-1) are all based on MMC concepts.

However, due to the large number of sub modules and floating capacitors, control and operation of such a complex plant is very challenging. For example, Siemens 'HVDC PLUS' uses 6×216 power modules for its 400 MW MMC [1]. As documented in [1], HVDC PLUS uses a centralized control structure. 'PLUSCONTROL' is the central control unit and has the following functions:

- Calculate reference voltage for each arm at the period of several microseconds
- Decide the switching status of the power switches on every power modules according to the capacitor voltages and arm current directions (sort and select)

The switching commands will be sent to each power module through two optical fibers and the capacitor voltage measured by each power module will be sent back through the same optical fibers. Though the centralized control structure has been successfully adopted by 'HVDC PLUS', several key issues regarding this control structure are not clearly explained in [1], such as:

- the communication bandwidth requirement is of interest since the switching status for hundreds of power modules needs to be sent at the period of several microseconds

- the computation burden and computation speed requirement for the central control unit is also concerned since the power module number is huge and the allowed computation time is limited (few microseconds)

Table 1-1: MMC for HVDC projects

project	installed year	manufacturer	DC link voltage	Power (MW)
Trans Bay	2010	Siemens	± 200 kV	400
BorWin2	2013	Siemens	300 kV	800
HelWin1	2013	Siemens	259 kV	576
DolWin1	2013	ABB	±320 kV	800
SylWin1	2014	Siemens	±320 kV	864
South-West Link	2014	Alstom	N/A	1440
HelWin2	2015	Siemens	±320 kV	690
Dolwin2	2015	ABB	±320 kV	900

The motivation for investigating the distributed control structure for MMC lies in the following potential benefits:

- reducing the computation burden of the central control unit by moving some control tasks to the slaves (located in the power modules)
- reducing the computation speed requirement and communication bandwidth requirement by increasing the period from several microseconds to hundreds of microseconds (or close to 1 millisecond)
- keeping the modularity feature of MMC by relieving the strong connections between the central control unit and the power modules which are seen in the centralized control

1.2 Goal of this project

The main aim of this project includes:

- to investigate the real-time communication technology, which is essential for the control (both centralized and distributed, though the focus will be put on the latter one) of MMC
- to investigate the suitable modulation methods for distributed control of MMC
- to analyze and design the distributed control of MMC
- to make a prototype and verify the above theory

1.3 Limitations

During the project development, some limitations are formed due to the lab conditions and the limited budget and time for the project:

- only one leg (single phase) of MMC is built. In addition, the DC link voltage is kept constant, i.e. this MMC is placed at one of the terminals of the HVDC system where the converter does not control the DC link voltage
- the prototype has only 6 power modules

Chapter 2 Basic Operation Principle of MMC

This chapter will introduce the basic operation principle of MMC and several other basic issues involved in the operation of MMC.

2.1 Description of the Power circuit

The block scheme of a three-phase MMC for HVDC application (at one terminal) is shown in Figure 2-1, whose DC side has a voltage level of V_{dc} and AC side is connected to an AC grid (50/60 Hz) through the filter inductors (L_f). With another MMC of the same structure, a full HVDC system with two terminals can be formed, which can connect two AC grids of different (or same) frequency and voltage level. In order to simplify the discussions of MMC control (to reduce the symbol and parameter number), only a single phase version of MMC is considered and will be analyzed for the rest of this report.

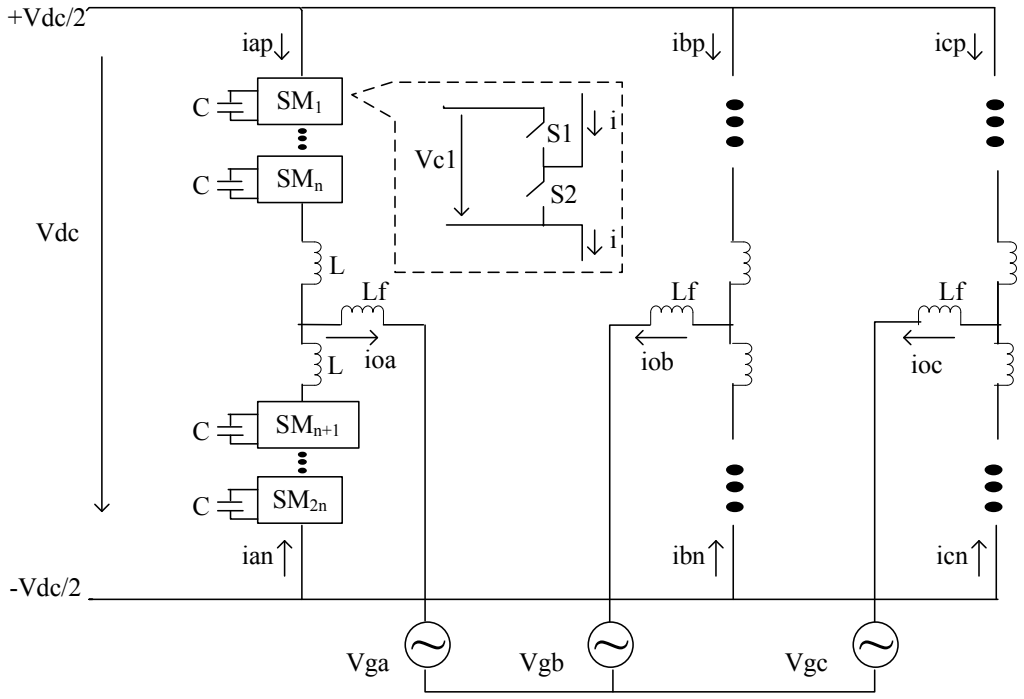


Figure 2-1: scheme of the three-phase MMC used for HVDC

The single phase version of MMC is shown in Figure 2-2, whose phase leg has 2N sub modules (the number of SMs per arm is denoted as N). The MMC is connected to a DC voltage source with the middle point grounded. The AC side of the MMC is connected to a grid through a filter inductor L_f. The energy can go in each direction of the MMC meanwhile the reactive power can be either inductive or capacitive.

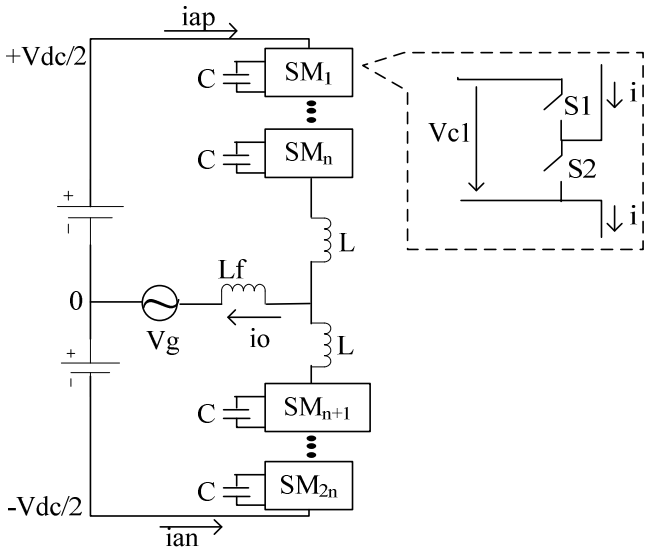


Figure 2-2: scheme of the single-phase MMC with grid connection

The sub module (denoted as SM, inside of the dotted lines in Figure 2-2) consists of one capacitor (C) and two power switches (S1/S2). Buffer inductors (L) are inserted into each arm to limit the rise rate of (fault) current.

2.2 Basic operation principle

In practice, an IGBT with a free-wheeling diode are normally used instead of the ideal switch (S1 or S2, see Figure 2-2). There are four possible combinations of the switches for each SM as shown in Table 2-1. During normal operation, the SM is either inserted or bypassed. Therefor through inserting or bypassing SMs, the SMs in one arm can form a controllable voltage source, which is shown in Figure 2-3 (denoted as V_{sp} for the upper arm and V_{sn} for the lower arm). By choosing an appropriate V_{sp} and V_{sn} at a certain sampling frequency, a sinusoidal AC output voltage (u_o) can be formed as shown in Figure 2-4[1].

Table 2-1: possible combinations of the switches in a sub module

combination	1	2	3	4
Switch status	S1=0 S2=0	S1=1 S2=0	S1=0 S2=1	S1=1 S2=1
comments	Current will flow through free-wheel diodes, SM is in energize mode	SM is inserted	SM is bypassed	This will make a short circuit in the SM, and therefore such a combination is forbidden

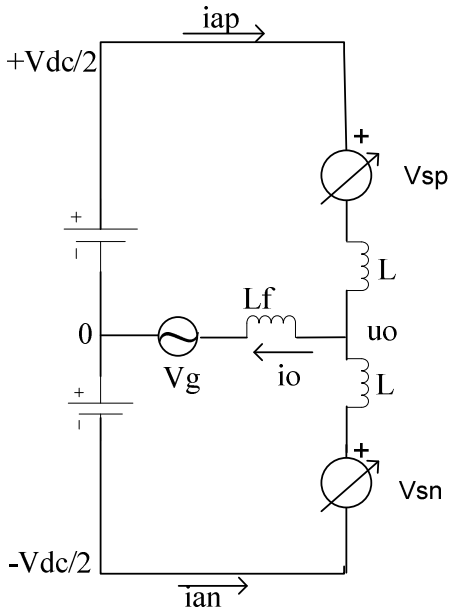


Figure 2-3: equivalent arm voltage source

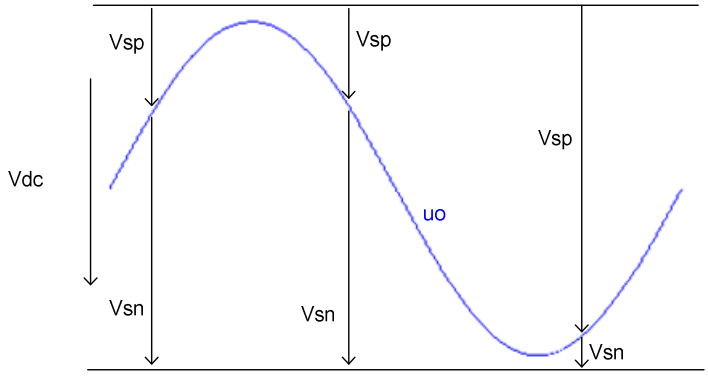


Figure 2-4: sinusoidal output voltage waveform

2.3 Difference current

Difference current (denoted as i_{diff}) is an important parameter of MMC, which is defined as the difference between the upper arm current (denoted as i_{ap}) and the lower arm current (denoted as i_{an}):

$$i_{diff} = i_{ap} - i_{an} \tag{1.1}$$

The difference current flows through the DC source to the phase leg in case of a single phase MMC (for three-phase MMC, the difference current will be more complicated as it can flow through different phase legs).

It is caused by the unbalance between the DC voltage source (V_{dc}) and the total voltage of the inserted SMs in the phase leg. The control of difference current will be further discussed in chapter 5.

2.4 Buffer inductors and fault management

As discussed in [4], the buffer inductors (L) are limiting the fast increase of the fault current during fault conditions, e.g. a short circuit between the DC terminals. At the very beginning of the fault (a short circuit between the DC terminals) appearance, the grid voltage is isolated by the filter inductor, so only the inserted SMs will contribute to the fault current, which can cause a big fault difference current (i_{diff}). Because the inserted SMs have a voltage level close to V_{dc} (see Figure 2-4, $V_{sp}+V_{sn}\approx V_{dc}$), the rise rate of the fault current (α) can be calculated according to Kirchhoff's law:

$$\alpha = \frac{V_{dc}}{2L} \tag{1.2}$$

The max value of α is determined by IGBT specifications, so the dimension of the buffer inductors has to be at least:

$$L \geq \frac{V_{dc}}{2\alpha_{\max}} \tag{1.3}$$

where $\alpha_{\max}$ is the maximum allowed value of α.

Because the fault current is limited by the buffer inductors, the IGBT is able to switch off at its normal current rating in a few micro-seconds, and the fault current will flow through the free-wheeling diodes. But the free-wheeling diodes are normally fast recovery diodes and do not have a high current withstand capacity either, so a thyristor having a high current withstand capacity should be used and take over the fault current until the AC breaker opens[1].

2.5 SM Capacitors

In steady state, if the difference current is controlled to be a constant value, and assume the voltage unbalance between the SMs in the same arm is neglectable, the waveform of the capacitor voltage is determined and only depends on the output power and power factor. This leads to the method of dimensioning the energy storage device (capacitor) [5]:

$$C_{SM} = \frac{P_s}{3 \cdot k \cdot N \cdot \omega_0 \cdot \varepsilon \cdot V_c^2} \left[1 - (\frac{k \cdot \cos\varphi}{2})^2 \right]^{\frac{3}{2}} \quad (1.4)$$

where

C_{SM} is the capacitance of individual SM,

P_s is the three-phase apparent power of the converter,

k is the voltage modulation index,

N is the number of SMs per arm,

ω_0 is the fundamental frequency,

ε is the voltage ripper of the capacitor in SM,

V_c is the mean value of the capacitor voltage,

$\cos\varphi$ is the power factor.

For a single phase MMC as in this project, P_s will be referring to single phase apparent power and the factor '3' in the denominator should be removed.

In the study of this project, parameter V_{dc}, rather than V_c ($= \frac{V_{dc}}{N}$) is kept constant, so a small rearrangement of the above equation is appropriate:

$$\frac{C_{SM}}{N} = \frac{P_s}{k \bullet \omega_0 \bullet V_{dc}^{\ 2} \bullet \varepsilon} \left[1 - (\frac{k \bullet \cos\varphi}{2})^2 \right]^{3/2} \quad (1.5)$$

where P_s is the single phase apparent power. It can be observed that when the parameters in the right side are given, the equivalent arm capacitance (denoted as C_{arm} and $C_{arm} = C_{SM} / N$) is also determined.

2.6 Discussions about choosing the number of sub modules

In practice, when SMs are made by the manufacturers, the capacitance (C_{SM}) is normally a fixed value (or has a fixed number of choices), then the number of SMs should be used for a specific HVDC application (i.e.

application parameters V_{dc} and P_s are given) is not arbitrary. After rearranging equation(1.5), the first constraint for choosing the number of SMs (N) is formed as:

$$N \le \frac{C_{SM} \bullet \varepsilon}{\frac{P_s}{k \bullet \omega_0 \bullet Vdc^2}\left[1-(\frac{k \bullet \cos\varphi}{2})^2\right]^{3/2}} \tag{1.6}$$

On the other hand, due to the limited voltage withstand capacity of individual SM, N must be large enough to share the entire DC link voltage. So the second constraint for choosing N is:

$$N \ge \frac{V_{dc}}{V_{c\max}} \tag{1.7}$$

where $V_{c\max}$ is the voltage withstand capacity of individual SM.

If there is a common interval of the above two ranges for N resulted from the two constraints, then the candidate N could be found. But if there is no such common interval, then the SM capacitance must be changed (assuming there are several number of values for choosing after the SM was made) otherwise the application parameters should be adjusted until there is a feasible N existed.

But for convenience, in order to investigate how the different value of N (e.g. 8~200) affects the control performance of the distributed control in this project, the capacitance of SM is considered to be able to change to any wanted value. Also there is no consideration of the voltage withstand capacity of SM. Therefore there is no constraint for choosing N in this study as it normally should be in practice.

2.7 Summary

This chapter introduces the basic operation principle of MMC for HVDC and clarifies some important concepts regarding MMC, such as difference current (i_{diff}), voltage ripple of SM (ε) and choosing N, thus a background for the following chapters are formed.

Chapter 3 Communication Technology for MMC

In this chapter, the promising communication technologies for the distributed control system are introduced and analyzed. At the beginning of this project, EtherCAT was selected as the communication technology for the prototype due to its high performance in terms of communication speed and connection capacity. But due to some unforeseen reasons, the hardware was not able to be ready in time for the test. So the plan B, where the SPI protocol via optic fibres was used instead, was brought to the table and succeeded in the prototype test. Therefore, both EtherCAT and SPI will be discussed with details in this chapter.

3.1 Introduction

The communication technology plays a very important role in the distributed control of MMC, because the control commands and some measurements are required to be exchanged among the different parts of the distributed control system. In fact, the communication technology is also essential for the centralized control, e.g. the master needs to collect each SM's voltage through communication for the purpose of the balance control [1], as it is almost impossible (or very costly) for the master to measure each SM's voltage directly, due to the big potential difference between each other. Of course, the bandwidth requirements for the centralized control and the distributed control are different.

For the normal operation of MMC, response time of the communication should be underlined in addition to the communication speed, as the parts under control (e.g. SMs, seen as slaves from the communication point of view) must response to the master in a given time period, otherwise the MMC might run out of control. In this sense, the non-real-time communication technologies such as Ethernet are out of consideration.

There are many available real-time communication protocols, such as Ethernet-based protocols (EtherCAT or PROFINET IRT), serial communication protocols (CAN, RS485, RS232 or SPI), which are widely used as field buses for industrial automation.

Among these protocols, EtherCAT is of more interest for the distributed control of MMC due to its high speed communication and the ability to connect a large number of slaves. EtherCAT is now widely used in the industry as many big companies, such as ABB, OMRON and Bechhoff Automation, are using or manufacturing EtherCAT products. Figure 3-1 is a picture of the EtherCAT piggyback controller boards made by Bechhoff Automation, which can be used to develop custom slaves of EtherCAT.

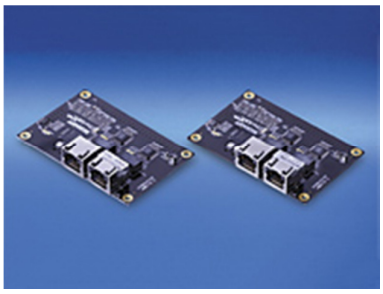


Figure 3-1 EtherCAT piggyback controller boards from Bechhoff Automation

(http://ethercat.org/en/products/9C0DDFE169894CD699496203B3D7DF63.htm)

In addition to EtherCAT, SPI and RS232 are also very interesting because they are integrated in many MCUs (e.g. F28335 or F28069 from TI [6]) and users can easily customize them to achieve a high speed, e.g. 10 Mbps or even higher. Different than EtherCAT, SPI or RS232 is normally used for on-board communications, e.g. between CPU and other on-board components due to the limited communication distance offered by SPI or RS232. However, through optic fibers, SPI or RS232 can be extended for long distance, and therefore is suitable for the distributed control system. Another advantage of communication through optical fibres is the good galvanic isolation. Figure 3-2 is a picture of optic transceivers made by Avago Technology, which can be used to transmit and receive signals via optic fibers.

Figure 3-2: optic transceivers from Avago Technology (white - transmitters; black - receivers)

The prototype made for this project is using SPI via optic fibers, because it is a cheap solution and more important is that it can be easily made in the university lab. EtherCAT and SPI will be further discussed with details in the following sections of this chapter.

3.2 EtherCAT

3.2.1 Basic operation principle

EtherCAT technology is supported by ETG (EtherCAT Technology Group), which consists of key user companies and leading suppliers of EtherCAT from the industry. The basic operation principle is illustrated by Figure 3-3.

One EtherCAT master and many slaves are connected in one line. EtherCAT datagram is encapsulated in a standard Ethernet frame. The Ethernet frame is sent from the master and passes through each slave like a flying train, and the slaves exchange their data with the master when it is passing through. Each slave only reads the data addressed to it and inserts the data for the master; it does not copy the whole Ethernet frame and relay the frame to next slave, thus a high communication speed is achieved. Meanwhile, only the master can launch the Ethernet frame, thus the frame collision which is seen in conventional Ethernet communication is avoided. This also accounts for the real-time feature of EtherCAT.

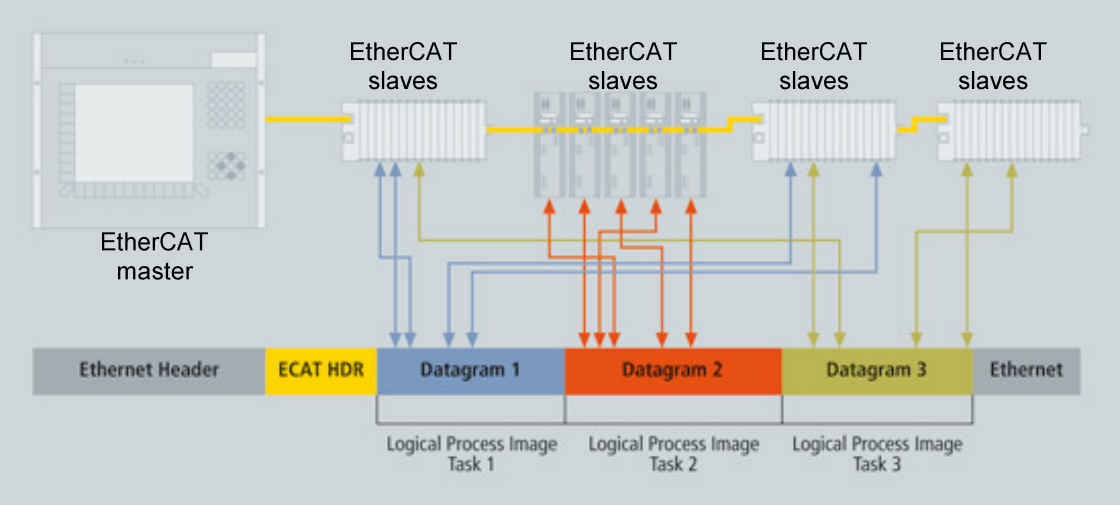


Figure 3-3: EtherCAT principle [7]

The length of the exchange data between the master and each slave (also known as 'process data') is very flexible, as it can vary between 1 bit and 60k bytes. This feature makes EtherCAT suitable for many applications with different purpose. Even other protocols can run over EtherCAT, e.g. CAN over EtherCAT. This feature also makes EtherCAT very efficient in terms of using the communication bandwidth because many one-bit data can be collected in one datagram and the Ethernet frame can be highly utilized.

The word 'master' used in this section (3.2) is different than the conception of the 'master' for the distributed control of MMC. In fact, the former one which is referring to 'EtherCAT master' is just a software package. The latter one is usually a host PC or an embedded system, which can be equipped with many EtherCAT masters. Meanwhile each EtherCAT master possesses one Ethernet port (or two ports if redundancy is considered) and can be connected to many EtherCAT slaves.

3.2.2 Communication speed

Table 3-1 has listed and compared the performance of the two key real-time Ethernet protocols: PROFINET IRT and EtherCAT, with the same line topology, 100 Mbps bandwidth and 100 slave devices [8]. As it can be seen, EtherCAT is faster than PROFINET IRT, especially when the payload is small. For example when the payload is 16 bytes, the minimum cycle time to communicate with all the slave devices for EtherCAT is only 250

micro-seconds, comparing to 650 micro-seconds for PROFINET IRT. This is because EtherCAT can use the bandwidth very efficiently as discussed in the above sub section (3.2.1).

Table 3-1

payload per device(bytes)	16	36	100
minimum cycle time for PROFINET IRT (μs)	~650	~650	~1250
minimum cycle time for EtherCAT (μs)	~250	~400	~850

It should be noticed that the above test for PROFINET and EtherCAT is based on a series connection topology (e.g. the case shown in Figure 3-5). If smaller cycle time is required, there are two ways to fulfil the requirement. One way is to use 1Gbps bandwidth version of these protocols instead of the 100Mbps version. The other way is to use a mixed topology, i.e. parallel + series. For instance, EtherCAT can equip the master (not EtherCAT master) with multiple communication ports (one port is one EtherCAT master), and each port can connect to as many as 65536 slaves. In this way, the master can double or triple its slaves without increasing the cycle time (maybe a little overhead time is needed to handle the multiple communication ports).

3.2.2.1 Communication Payload of each SM

The communication payload (only the cyclic payload is considered, as the bandwidth requirement will not depend on the non-cyclic data) of each SM is designed for the distributed control system as follows. The input for the high level control is all measured by the master, thus no needs for communication (only referring to the real-time Ethernet communication). The converter level control and fault management [9], needs the voltage of each SM's capacitor and the status of each SM. For the SM's control unit, the PWM and balance control only needs the voltage reference, resulted from the high level control and converter level control realized in the master control unit. This reference will be the same for all SMs located in the same arm. So for a three phase MMC, there will be only 6 different references. The resulted payload for each SM is shown in Figure 3-4. Only 8 bytes (64bit, including the reserved bits) are needed. The cycle time of EtherCAT for 400 SMs (N=200, the maximum number studied in this project) will be less than 1000 μs according to Table 3-1.

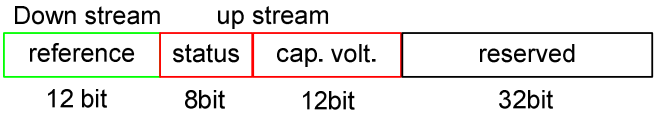


Figure 3-4: payload for each SM

3.2.3 Connection topology

EtherCAT has a very flexible connection topology for connecting slaves: line, tree, star or mixed (see Figure 3-5). Though the physical connection topology is a mixed structure, the Ethernet frame (the flying train) goes through each slave in a series manner, which means the frame goes to slave 1, then slave 2 till the last slave. This also implies that only one frame is existed in the communication system at any time. In order to have a parallel manner which means several frames may be existed in the system at one time, multiple EtherCAT masters must be equipped as discussed in the above sub section (3.2.2).

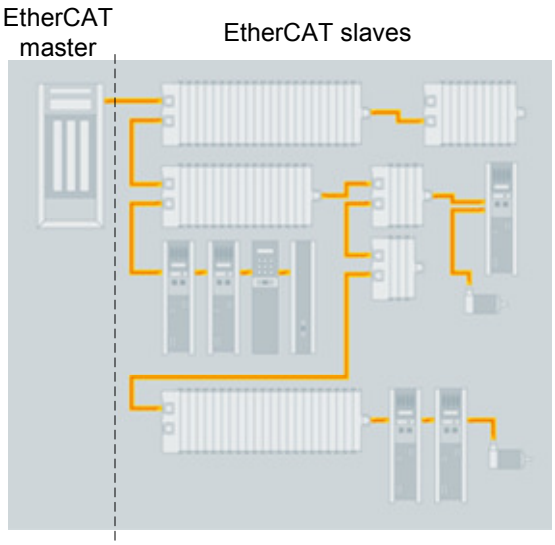


Figure 3-5: EtherCAT connection topology [7]

Another useful topology for EtherCAT is to connect the slaves in ring (Figure 3-6). In this topology, the EtherCAT master must run in the redundancy mode. In this mode, one EtherCAT master manages two ports (A and B). Normally the EtherCAT master sends the Ethernet frame from one port, but when there is a broken path in the forward direction it will send the Ethernet frame from both ports and the communication can be recovered. In this way, a redundancy of the communication can be achieved.

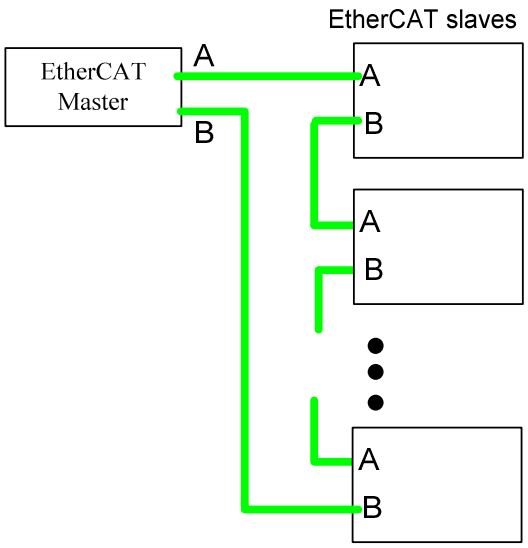


Figure 3-6: ring topology for communication redundancy

3.2.4 Synchronization and distributed clock

Synchronization is critical for the distributed modulation of MMC (see discussions in chapter 4). Thanks to the distributed clock function of EtherCAT, the accuracy of the synchronization can be as high as less than 1 micro-second. The distributed clocks are located at EtherCAT master and slaves and aligned through accurate calculation and compensation of the communication delay between EtherCAT master and slaves.

3.2.5 Galvanic isolation

Another important issue is the galvanic isolation for the communication. Considering the structure of MMC (see Figure 2-2), one SM could 'see' the whole DC link voltage if all the other SMs are bypassed (e.g. under a fault condition). Normally this DC link voltage could be as high as tens or hundreds of kilovolts (for HVDC applications) and the SM seeing this high voltage can pass it to all the other SMs as well as the master through communication cable if the isolation is not good enough. In this circumstance, using optic fibers instead of wires for communication connection is a good choice.

3.2.6 Integration for MMC

To integrate EtherCAT into MMC is also convenient as the EtherCAT master and slaves are commercially available and the users only need to build interfaces for the MMC. A conceptional diagram of integrating EtherCAT for MMC is shown in Figure 3-7. The master tasks can trigger the EtherCAT master function through callback routines while the MCU on SM can exchange data with the EtherCAT slave controller through SPI communication. A SM equipped with an EtherCAT slave controller (piggyback, see Figure 3-1) is shown in Figure 3-8.Unfortunately, this setup was not ready for the full test before the submission of this report.

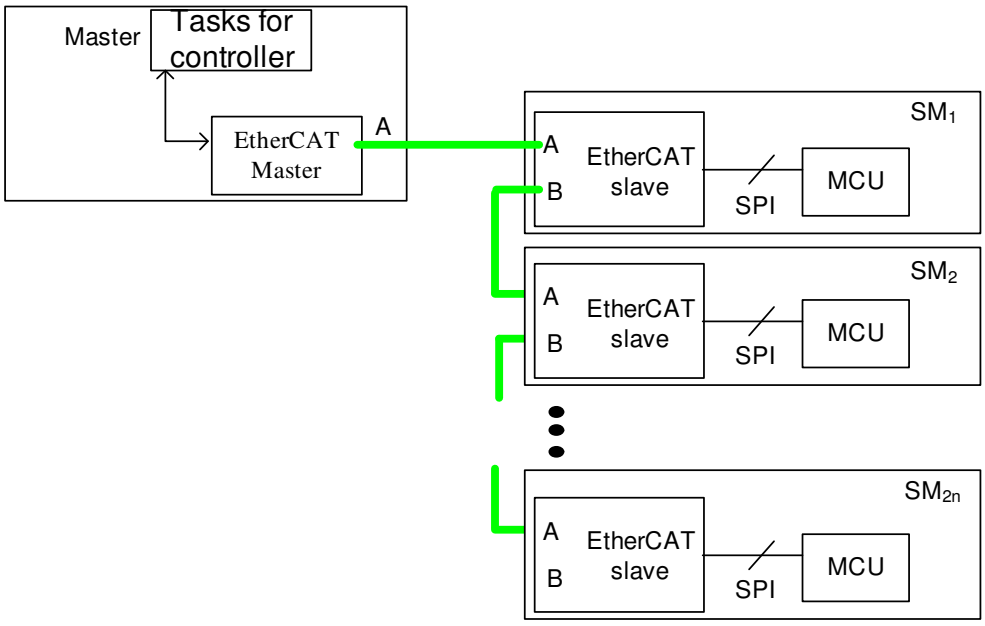


Figure 3-7: integration of EtherCAT into MMC with distributed control

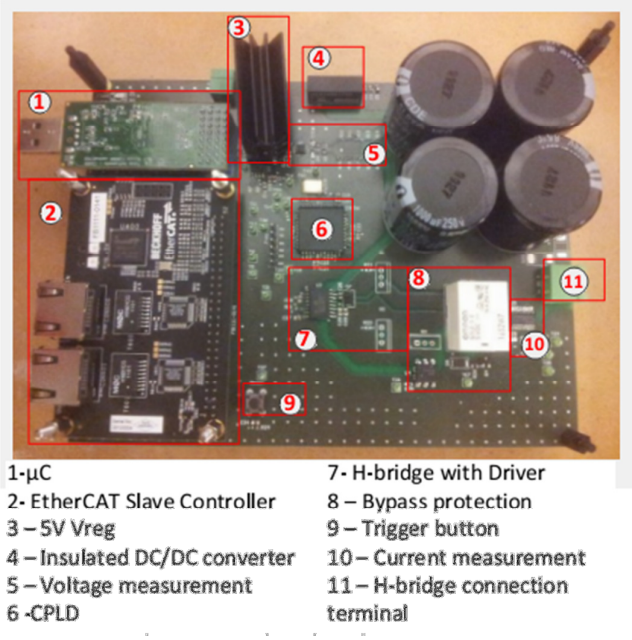


Figure 3-8: individual SM equipped with an EtherCAT slave controller (piggyback) [9]

3.3 SPI

3.3.1 Basic operation principle

As mentioned in section 3.1, SPI can be used for the communication between the master and SMs through optic fibers. SPI has two modes: 4-wire mode (see Figure 3-9) which contains 4 signals and 3-wire mode which

does not have 'SPISTE' signal. 'SPISTE' signal is used as chip select when the master is communicating with multiple slaves. This is inconvenient when using optic fibers as it needs extra optic fiber, especially when the number of SMs is large. Therefore in this project, 3-wire mode is chosen, and the chip selecting function is realized by addressing (software method) [10].

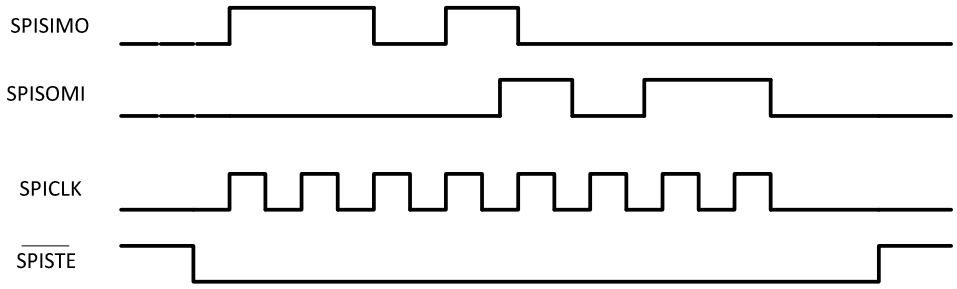


Figure 3-9: 4-wire mode of SPI

Data signal 'SPISIMO' (Tx) or 'SPISOMI' (Rx) is sent and read by the SPI modules at the rising and falling edge of the 'SPICLK' signal respectively. Another option that can be chosen by the users is an opposite way, i.e. the data signal could be sent and read at falling and rising edge of the 'SPICLK' signal respectively. These two options could lead to a different performance of SPI in terms of communication speed, especially when the propagation delay is asymmetrical, i.e. different propagation delay for a rising edge signal and for a falling edge signal. They will be discussed with details in section 3.3.4.

3.3.2 Connection topology

The master and slaves can be connected in a daisy chain as shown in Figure 3-10. The master provide one SPI port (consisting of 3 signals) while the SMs provide 2 SPI ports per SM. If the SMs are not able to be connected in one daisy chain due to the limitation of the communication speed, the master has to provide more SPI ports, working as a SPI hub. As a result, the topology becomes a mixed structure, which has many paralleled daisy chains. It is also possible to connect the master and the SMs with a pure parallel topology (or a star topology). For example, when the daisy chain length is reduced to the minimum, i.e. one SM per daisy chain, the above mixed topology becomes a pure parallel topology.

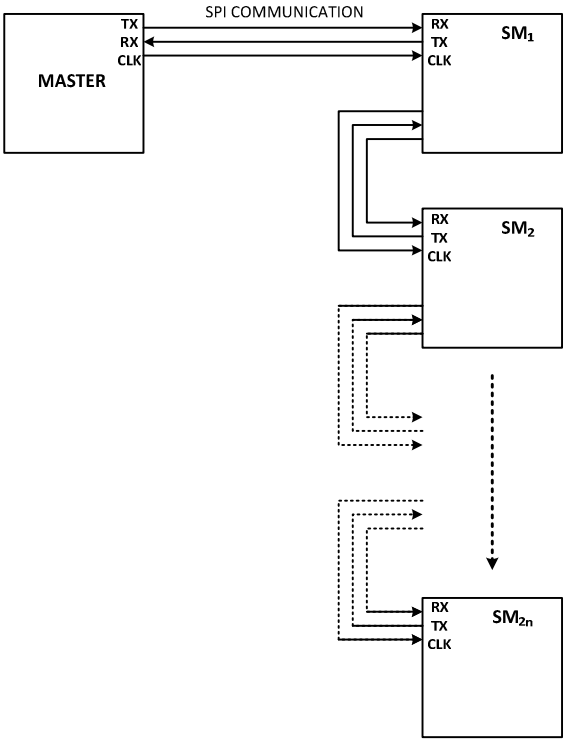


Figure 3-10: SPI daisy chain

3.3.3 Application level protocol

SPI protocol is so simple that it cannot handle the complicated communication needs of the distributed control system, such as setting SM position, synchronization, sending reference, inquiring measurements and status from SMs. Fortunately, the users are free to design their own application level protocols based on the basic SPI protocol. The application level protocol designed for the prototype will be presented in this sub section.

Char is the basic unit that can be handled by SPI module. Bit length of a char is between 1 and 16, according to the SPI module of the MCU used in the prototype. A 10-bit char is chosen as the basic unit to form a data frame. The bit definition of the char is shown in Figure 3-11.b. Bit9 defines the type of this char. When bit9 is '1', the char is a normal 'data'; when bit9 is '0', the char is a 'command or address'. Bit8~bit1 are actual payload, which could be a normal 'data' or a 'command or address', depending on the type of the char. The last bit is used for Cyclic Redundancy Check (CRC).

The data frames exchanged between the master and SMs are illustrated in Figure 3-11.a. The data frame sent from the master to SM comprises one 'command or address' char and maximum 4 'data' chars. The length of the 'data' part of the frame is variable from 0 to 4, depending on the specific 'command or address' part. After receiving one char from the master, the SM decides whether it should reply to the master or not. If it should, the response frame consists of one 'address' char and maximum 3 'data' chars.

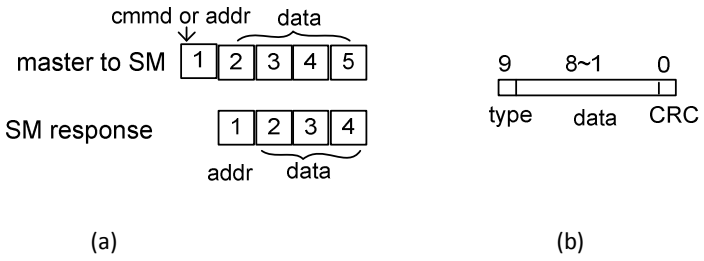


Figure 3-11: (a) data frame (b) bit definition of one char

From the above analysis, the maximum bit length (Λ) of the data frame is 50 bits. The key commands used for the application level protocol is listed in Table 3-2. Among these commands, only the commands '0x80+addr' (addr=1~100) are cycling commands, which are used to broadcast the reference calculated by the master controller and acquire measurements and status from each SM (see Table 3-2). The limitation of this protocol is that the SPI address is only from 1 to 100, i.e. the maximum number of the addressable SMs is 100. Hence, if the MMC has more than 100 SMs, this protocol has to be revised.

Table 3-2: key commands of the application level protocol

'cmmd or addr'	'data' part	response frame	comments
addr (1~100)	0~4 chars	4 chars	the 'data' part is extended to handle more commands, e.g. set SM position; meanwhile inquiring measurements and status from the addressed SM
0x80+addr (1~100)	4 chars	4 chars	broadcast reference; meanwhile inquiring measurements and status from the addressed SM
0x80+101	none	none	synchronization
0x80+107	2 chars	none	broadcast new capacitor voltage reference
0x80+108	none	none	broadcast; enable individual balance control
0x80+109	none	none	broadcast; disable individual balance control

3.3.4 SPI communication speed

The speed of SPI is decided by the 'SPICLK' signal, which is sent from the master. But the final communication speed depends on many factors, such as the speed of the optic transceivers (main factor) and the speed of the signal relaying between SMs. Since the communication speed is highly dependent on the specific design, the following discussions are based on the prototype made for this project. In addition, some suggestions about how to improve the communication speed are also made in this sub section.

The types of the optic transmitter and receiver chosen for the prototype are SFH757V [11] and SFH551V [12] from Avago Technology respectively (see the schematic in Appendix A). The main signal propagation delay lies in the delay from optic signal to electrical signal, which can be denoted as t_{pHL} for a falling edge signal and t_{pLH} for a rising edge signal respectively. From the datasheet [11, 12], there is $t_{pHL} < t_{pLH}$. This asymmetry feature of the propagation delay leads to a duty distortion of the transmitted signal.

SPI module of the MCU can choose sending Tx signal and reading Rx signal at different edge type of the Clk signal. For example in the case shown in Figure 3-12, SPI module will send Tx signal at the falling edge of the Clk signal and read Rx signal at the rising edge of the Clk signal. Considering a daisy chain of N SMs, the last SM will receive the Clk signal after $N \cdot t_{pHL}$ time and then starts to send its Tx signal to the master (SM's Tx signal is the Rx signal of the master). In the worst case (e.g. the data signal is a rising edge), the master receives this Rx signal after $N \cdot t_{pLH}$ time. In order that the Rx signal can be read by the master correctly, it must arrive at the master before the next rising edge of the master Clk. Hence, equation:

$$N \cdot (t_{pHL} + t_{pLH}) < \frac{T_{clk}}{2} \tag{2.1}$$

must be hold. Rearranging this equation, the maximum frequency of the Clk signal can be determined, i.e. the maximum communication speed of SPI:

$$\frac{1}{T_{clk}} \leq \frac{1}{2N(t_{pHL} + t_{pLH} + t_{other})} \tag{2.2}$$

It can be seen from equation (2.2) that the communication speed is reversely proportional to N (the number of SMs in the daisy chain) and the total propagation delay. Hence, the way to increase the communication speed is to reduce N and/or to reduce the total propagation delay. Of course, another limitation of the communication speed is the SPI module itself, i.e. the maximum clock frequency supported by the host MCU. But this limitation is usually not a problem since the users are free to choose the MCUs that support a high speed SPI, e.g. around 40Mbps can be achieved by the MCU F28335 from TI.

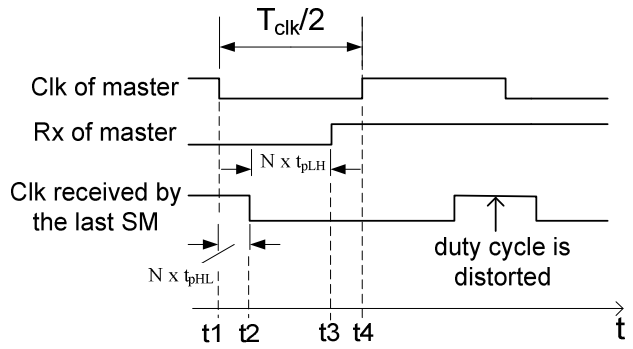


Figure 3-12 : propagation delay of the SPI communication (t1, falling edge of the master Clk; t2, the last SM receives this falling edge and starts to send its Tx signal; t3, the Rx signal arrives at the master; t4, the master reads the Rx signal)

On the other hand, if SPI module of the MCU chooses an opposite way to send and read its data signals, i.e. send Tx at the rising edge of CLK and read Rx at the falling edge of Clk, the last SM will receive Clk signal after $N \cdot t_{pLH}$ time. Because $t_{pHL} < t_{pLH}$, the master receives the Rx signal later than the case shown in Figure 3-12. Therefore, this method of sending and reading data signals leads to a smaller maximum communication speed of SPI and should be disregarded.

If the Clk frequency ($1/T_{clk}$) fulfils equation (2.1), it can be assured that the last SM can read the data signal from the master correctly.

In case of the prototype, there is N=3. Parameters t_{pHL} and t_{pLH} can be found in the datasheets: $t_{pHL} \approx 60ns$ and $t_{pLH} \approx 150ns$ at environment temperature 25 $°C$. The total propagation delay (include electric to optic, optic to electric and electric to electric signal delays) was measured for N=3, and the results are shown in Figure 3-13. It can be seen from Figure 3-13 that the total delay is 800ns. Therefore, the max SPI speed for N=3 can be estimated as:

$$\frac{1}{T_{clk}} \le \frac{1}{2N(t_{pHL} + t_{pLH} + t_{other})} = \frac{1}{2 \cdot 800ns} = 0.625MHz \qquad (2.3)$$

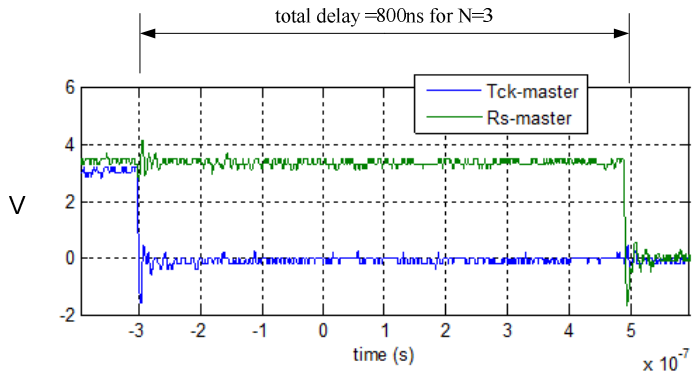


Figure 3-13: total propagation delay for N=3

Though this speed is not very fast, it is good enough for the prototype of a small number of total SMs (the reason will be discussed with details in section 3.3.4.1). In case for a real MMC of a large number of total SMs, the speed has to be increased. In order to do so, the total propagation delay and/or the daisy chain length must be reduced. The minimum daisy chain length is 1, i.e. the master SPI works as a hub and connects to each SM directly. Meanwhile, fast optic transceivers, such as AFBR-1624Z/1629Z and AFBR-2624Z/2529Z [13]made by Avago Technology, could be used to replace the above slow optic transceivers. According to the datasheets of the fast optic transceivers [13], the total propagation delay can be reduced to 60ns. Therefore the maximum speed could be achieved by the improved solution is approximately:

$$\frac{1}{T_{clk}} \leq \frac{1}{2 \cdot 1 \cdot 60ns} = 8.33MHz \tag{2.4}$$

From the above analysis, it can be concluded that the clock signal of the SPI, which determines the communication speed, is largely affected by the propagation delay. Therefore, a sophisticated clock scheme, which can compensate the propagation delay, could be another path leading to even higher communication speed. Based on the same reason, the serial communication protocols without clock signal, e.g. RS232, might be very promising in terms of increasing further the communication speed.

3.3.4.1 Discussions about the SPI communication speed required by the distributed control system

In the distributed control system, there are two types of data needed to be exchanged between the master and the SMs: the master needs to broadcast the references at the sampling frequency (f_{smp}) while the SMs need to send back their measurements and status.

For the first type of data (broadcast), the minimum communication speed has to be:

$$\frac{1}{T_{clk}} \geq f_{smp} \cdot \Lambda \tag{2.5}$$

where Λ is the bit length of the payload.

For the second type of data, the minimum communication speed has to be:

$$\frac{1}{T_{clk}} \geq \frac{\Lambda \cdot 2N}{\tau_v} \tag{2.6}$$

where Λ is the bit length of the payload,

N is the number of SMs per arm, 2N is the total SMs,

τ_v is the allowed delay for voltage measurements, which could be bigger than the sampling period.

Considering the case of the prototype, where $\Lambda = 50$, $N \leq 4$, $f_{smp} \leq 4000$ (Hz) and $\tau_v \approx 0.002$ (s), the minimum communication speed is 0.2 Mbps. Therefore, the designed SPI speed given by equation (2.3) is fast enough for the prototype.

Considering a real case of MMC, where N=200, equation (2.6) becomes significant and the minimum communication speed is estimated as:

$$\frac{1}{T_{clk}} \geq \frac{50 \cdot 2 \cdot 200}{0.002} = 10MHz \tag{2.7}$$

3.3.5 Synchronization

Synchronization is not a built-in feature of SPI, though SPI itself is a synchronous communication. Users must realize the synchronization by themselves. In the prototype for this project, the synchronization is realized through a software method, which uses a special command to inform all SMs to synchronize upon receiving this command. Because the software part that handles the synchronization is identical for all SMs, the delay caused by the software part should be the same for all SMs. Therefore the accuracy of the synchronization only depends on the propagation delay between the SMs.

From the analysis in the above sub section (3.3.4), the maximum propagation delay (σ_{sync}) between the first SM and the last SM in the daisy chain is:

$$\sigma_{sync} = (N-1) \cdot (t_{pHL} + t_{pLH} + t_{other}) \tag{2.8}$$

where N is the daisy chain length.

Without any compensation measure, this propagation delay is exactly the accuracy of the synchronization. It can be seen from equation (2.8) that the accuracy becomes poor when N is increasing. Therefore, when N is very large, the propagation delay has to be compensated by either software or hardware methods.

Considering the case of the prototype, the accuracy of the synchronization could be estimated as:

$$\sigma_{sync} = (4-1)\cdot(60+150+40) = 750ns \tag{2.9}$$

Comparing to the sampling frequency of the prototype, which is no bigger than 4kHz, this synchronization accuracy is acceptable. Therefore, for such a short daisy chain, there is no need to compensate the propagation delay.

3.3.6 Cost comparison of the EtherCAT and SPI solutions

The cost of the two communication solutions for the distributed control system is listed in Table 3-3. It can be seen from Table 3-3 that the SPI solution is much cheaper than EtherCAT solution. The price listed for the EtherCAT solution is based on the electric wire version (RJ5 connector).

Table 3-3: cost comparison of the EtherCAT and SPI solutions

item		EtherCAT solution*	SPI solution
master	hardware	Industrial PC + Windows OS ~16000DKK	F28335 control card ~600DKK
	software	TC3 Runtime license ~9000DKK	none
slave interface	hardware	piggyback board (RJ45 connector) ~540DKK	3 optic transceivers (SFH551V+SFH757V) ~450DKK
development tools	software	TC3 engineering licence ~19200 DKK	CCS free
total (N is the number of slaves)		$44200+540\cdot N$ DKK	$600+450\cdot N$ DKK

* price before discount

3.4 Summary

In this chapter, two real-time communication protocols: EtherCAT and SPI were discussed. EtherCAT can achieve high communication speed and high efficiency in terms of bandwidth utilization. It also possesses many useful features, such as high accuracy distributed clock and redundancy. It can be easily integrated into

the distributed control system for MMC as well. The disadvantage of the EtherCAT solution is its high price. In addition, it is not as easy to be customized as the SPI protocol is.

The SPI solution is cheap and user-friendly in terms of customization.

Chapter 4 Resampled Uniform PS-PWM for Distributed Control of MMC

The tasks of this chapter are to find a suitable modulation method for distributed control and to discuss the implementation methods. The outline of this chapter is as follows. Section 4.1 introduces a background for the resampling technology (sampling frequency is greater than the carrier frequency) and the resampled uniform PS-PWM. Section 4.2 discusses different implementations of PS-PWM with details, including the resampled uniform PS-PWM, which is based on the resampling technique. To overcome some of the disadvantages of the conventional methods to implement the resampling technique, a new implementation method, which uses high frequency saw-tooth carriers, is proposed in section 4.2. Section 4.3 discusses several practical issues and their solutions regarding the new method. Simulations and experiments are done in order to validate the new method in section 4.4, and finally the conclusions are presented in section 4.5.

4.1 Introduction

The family of multilevel modulation technology, evolved together with the multilevel converter technology, has a lot of modulation strategies [14], such as level-shifted PWM (LS-PWM) [15], phase-shifted PWM (PS-PWM) [16] and space vector modulation (SVM). This chapter pays its attention to PS-PWM for the following two reasons. The first reason is that it can naturally balance the power (charging or discharging) of different sub modules (SMs) in one leg (a certain level of unbalance is still existing, thus a balance control method is still a must). The second reason relies on the factor that it is suitable for the distributed control, as each SM can take care of exact one of the phase-shifted carriers.

There are two existing sampling techniques used in digitally-implemented PS-PWM, leading to the uniform PS-PWM and the resampled uniform PS-PWM respectively [17]. In the uniform PS-PWM, the reference is hold constant for a half switching period of each carrier (from trough to peak or from peak to trough, it is known as asymmetry uniform) or a whole switching period (from peak to peak or from trough to trough, it is known as symmetry uniform). The advantage of the uniform PS-PWM is its easy implementation, but the drawbacks are as follows: 1) the relatively lower controller bandwidth, as it is limited by the switching frequency of each SM; 2) the distortion of the output voltage summation of SMs per arm compared to the original voltage reference, due to the phase differences among the carriers. The resampled uniform PS-PWM can overcome these drawbacks by using resampling technique. The resampling technique is introduced by the author of [17], and further developed and applied in [18-20]. But to implement resampling technique is not a trivial job. The author of [17] has proposed two solutions to this technique: the software (DSP or MCU) solution and the hardware (FPGA) solution. The first solution is flexible, but it needs much computational overhead and can have a certain level of inaccuracy for the switching instance. The second solution is accurate, but inflexible and costly for the distributed control system if each SM has to be equipped with an FPGA.

An important objective of this chapter is to propose a new solution to implement the resampling technique which overcomes the abovementioned problems. The proposed solution is implemented by software (DSP or MCU) in order to be flexible, but it has a high accuracy in terms of switching edge. This solution is well suited for the resampled uniform PS-PWM in the distributed control system. The detailed implementation method as well as some practical issues will be discussed in the rest of this chapter.

4.2 PS-PWM in distributed control systems

4.2.1 Uniform PS-PWM

As a multicarrier PWM, the final output voltage is the summation of each SM's PWM output signal. Each PWM reference signal of the uniform PS-PWM will be hold for either a half or a whole carrier period. Due to the phase shift, each carrier reaches its maximum and/or minimum (depending on single or double update technique is applied) at different time instant, thus each SM loads the new reference to its PWM module at different time instant. For example in Figure 4-1 is illustrated this process when the update of the reference signal is done at the bottom of each carrier. The master sends the new reference values for the SMs, and SM1 loads the new reference at the time instance of its carrier's next minimum, while the other SMs are loading the new reference values at the time instances of their own carriers' next minimum. This leads to the distortion of the averaged output voltage of one arm, because each SM is holding the previous reference value until loading the new one. Reference [21]has also confirmed this statement and proposed a solution to solve this issue.

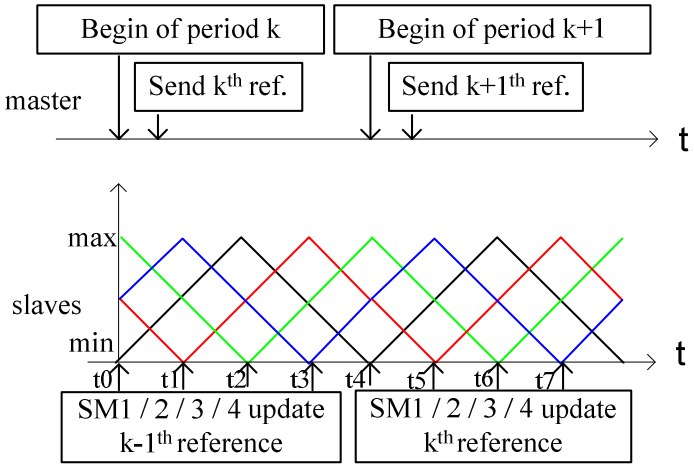


Figure 4-1: Timing and Carrier waveform of the uniform PS-PWM

Another problem is the time delay (duration between the begin of the sampling period and the reference being loaded, e.g. in Figure 4-1 from t0 to t4 is the time delay for SM1, while from t1 to t5 is the time delay for SM2 etc.), which limits the bandwidth of the controllers. Reference [22, 23]has proposed that the sampling should take place at different time instances for different SM (e.g. for SM1, the sampling instant is when the carrier of SM4 reaches its minimum), thus the sampling delay will be decreased. But the new reference is still loaded at the minimum (or maximum) and hold for either a half or a whole carrier period. This modulation is

still a uniform PS-PWM, but is referred as phase-shifted sampling. Thus the distortion of the averaged output voltage still exists. Meanwhile, the effective sampling frequency for each SM is still the same as the carrier frequency, no matter it is a phase-shifted sampling, or it is an in-phase sampling (the one showed in Figure 4-1).

4.2.2 Resampled Uniform PS-PWM

The resampled uniform PS-PWM is illustrated in Figure 4-2. The sampling occurs at the minimum or maximum of each carrier wave (e.g. t0 and t2) or whenever there is a carrier wave cross (e.g. t1 and t3). This leads to a resampling frequency of $f_s = 2N \bullet f_c$, where f_c is the carrier frequency of each SM and N is the number of SMs. So the resampling ratio (RSR, defined as the resampling frequency divided by the twice of the carrier frequency [17]) is also equal to N.

The difference between the uniform PS-PWM and the resampled uniform PS-PWM is that, for the latter, the reference is loaded at the same time for each SM. Figure 4-2 shows the carrier waveform of each SM; the new reference value is loaded to its PWM module at the next sampling instant. There is no distortion of the output voltage, because the reference for all the SMs is the same at any time.

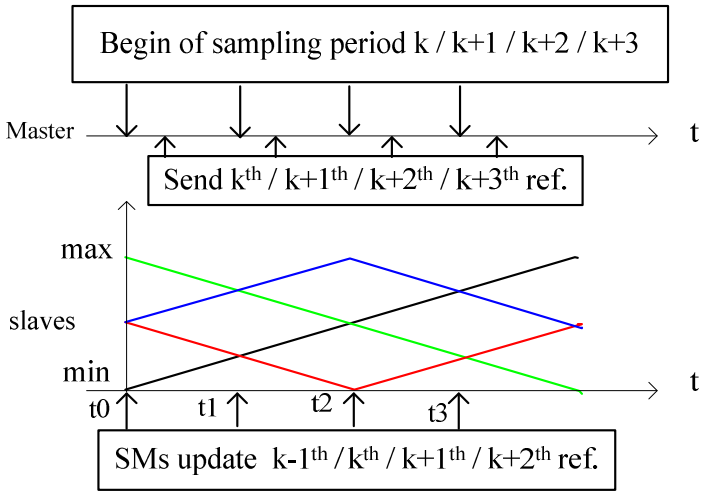


Figure 4-2: Timing and Carrier waveform of the resampled uniform PS-PWM

It should be noted that, lower sampling frequency is also acceptable (i.e. RSR<N), as long as the RSR is an integer number. This will affect the delay of PWM, but has no adverse effect on the output voltage (i.e. no distortion).

The key of the resampled uniform PS-PWM is the resampling technique, as illustrated in Figure 4-3.b. Without losing generality, only one carrier period of the SM (e.g. SM1) is shown in the figure. It can be seen from the figure that, by using this resampling technique, some reference commands have no chance to cross the carrier before the new reference is coming. It can be shown that, the resampled uniform PWM is closer to the naturally sampled PWM than the uniform PWM [17].

Reference [17] has proposed two solutions to implement the resampled uniform PWM: by software (DSP or MCU) and by hardware (FPGA). The difficulty of the implementation by software is how to reload the reference at a precise instant. This problem is illustrated in Figure 4-4. Taking the example when the reference value should be loaded at the time instant t_1, and the expected switching edge should be at t_{sw}. Due to latency of the digital controller it is loaded at the time instant of t2, leading to the actual switching edge is executed at t_2. It should be noticed that for this case the PWM module from the controller should be equipped with a 'greater than' comparator between the PWM counter and the value placed in the compare register. In most of the PWM modules from controllers only the event when the compare value is equal with the counter value is treated, which would lead to miss one switching edge (for the case when the newly loaded compare value is lower than the actual counter value). Though the hardware solution, like FPGAs, has no such a problem, as it was mentioned before, the drawback is its inflexibility and cost.

4.2.3 The Proposed Resampling Solution

As illustrated in Figure 4-3.c, the proposed solution uses a high frequency (equal with the resampling frequency) saw-tooth carrier wave, and uses two compare registers (ex. CMPA and CMPB) to decide the edge of the output PWM wave independently (ex. When CMPA matches the PWM counter, set the output=1; when CMPB matches, set the output=0). This is applicable to MCUs, e.g. from Texas Instrument (TMS320x2833x [6]) or from Freescale Semiconductor (MC56F847xx [24]). Moreover, very often the PWM unit from microcontrollers used to control power switches are equipped with two compare registers, to be able to generate the dead time. They can be configured and used for the above presented application. For the rest of this paper, the language (e.g. register names, hardware mechanism) is according to the MCU from Texas Instrument, in order to avoid confusion. Thanks to the shadow mechanism of the PWM module of the microcontroller, the compare value can be loaded to CMPA and CMPB exactly at the beginning of each modulation period, i.e. when the counter equals zero. Thus the latency of reloading the reference by the conventional software method is not a problem.

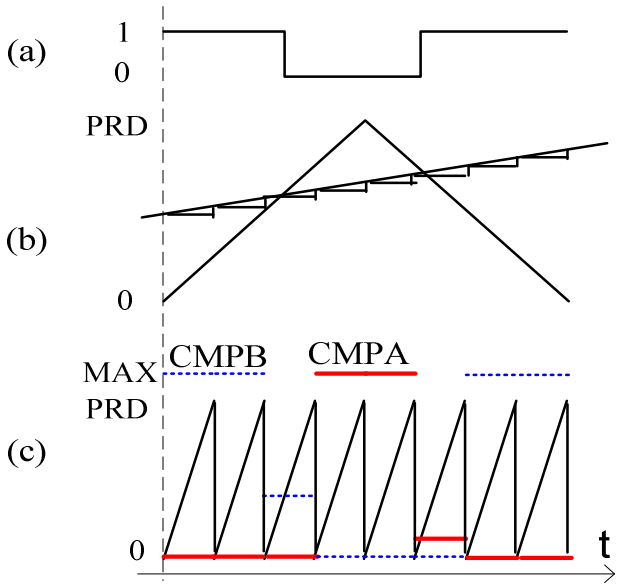


Figure 4-3: Resampling technique (a) the resulted switching signal (b) conventional solution for resampling technique (RSR=4) (c) the proposed solution to implement the resampled PWM, leading to the same final switching edge (PRD- period of the PWM counter)

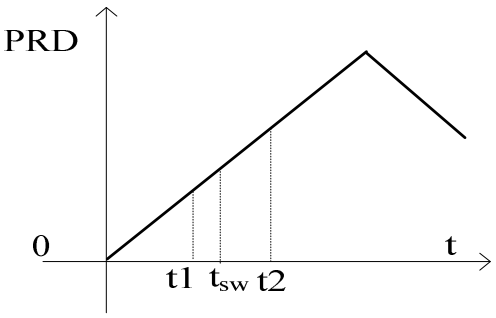


Figure 4-4: a latency of reloading the reference

To calculate the compare values for CMPA and CMPB is straightforward. The compare values are calculated in this way:

- For the case when the output is maintained for the upcoming period the same (i.e. no switching edge), a MAX value is loaded in one of the compare register and zero in the other compare register. For example to maintain the output of the SM in 1 it should be loaded CMPA=0 and CMPB=MAX; to maintain the output to 0 the compare registers should be: CMPA=MAX, CMPB=0.
- If there is a switching edge in the upcoming period (reference value has an intersection with carrier Figure 4-3.b), to create a falling edge CMPA should be set to 0 and CMPB the reference value, and when a rising edge has to be created CMPB will be set to 0 and in CMPA will be loaded the reference value.

In this solution, the PWM module is set to use saw-tooth carrier for each SM, while the triangle carrier is only a 'virtual' one. The 'virtual' triangle carrier serves as a means to calculate the compare values of CMPA and CMPB.

Other practical issues for the proposed solution, most of which are common issues for resampling technique and for distributed PS-PWM will be further discussed in section 4.3.

4.3 Practical issues regarding the implementation of the proposed solution

4.3.1 The Position of Each SM

The position of each SM (e.g. which SM is SM1, it could be different with the physical position), determines the initial phase shift of the carrier for each SM. This initial phase is regarding the 'virtual' triangle carrier (Figure 4-3.b), which is important for the calculation of the compare values, and not regarding the actual saw-tooth carrier, since the latter is always in phase with each other.

A possible method to decide the position of the SM may be done by hardware configuration, by allocating a position number to each SM. A drawback of this method is the inflexibility; it wouldn't be easy to re-enumerate the SMs when one of the SM has to be disabled due to a failure.

An alternative way to enumerate the SMs can be done by communication. The master manages all SMs and repositions all SMs whenever needs to do so [9].

4.3.2 Synchronization

A synchronization (SYNC) signal is needed in order to synchronize the tasks running in the master and all SMs. The SYNC signal may be an interrupt signal originated from a communication protocol, such as Controller Area Network (CAN) [14-16] or SPI as it was done in the prototype. Alternatively, a distributed clock, supported by EtherCAT (see chapter 3) can provide a more precise SYNC signal [25].

Upon receiving the SYNC signal, the PWM should reset its counter to an initial value. In this case, the initial value is zero, since the saw-tooth carrier is always in phase of each SM. But, if the duty (the non-zero one of CMPA/CMPB) is near zero, it's possible to have a duplicate switching edge, leading to extra losses (Figure 4-5).

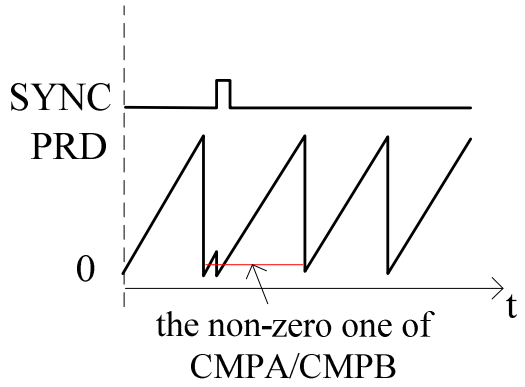


Figure 4-5: synchronization of the saw-tooth carrier

A possible solution to this issue is to track the duty ratio. If the duty ratio is near zero, the synchronization is temporarily disabled by the software, until the duty ratio is increased.

Temporarily disabling the synchronization is not a problem for the PWM, as the counter can keep running based on the local clock of the DSP (MCU) of each SM. For the same reason, the whole distributed system can keep running if the SYNC signal is missing for a short time.

4.3.3 Multi-time Switching

The multi-time switching is in terms of the 'virtual' triangle carrier period, as for the saw-tooth carrier period, only one-time switching is possible. However, the multi-time switching during a modulation period is a common issue for resampled uniform PWM. This is due to the resampling technique as illustrated by Figure 4-6, or it is caused by the fact that the reference has a very fast transition [17].

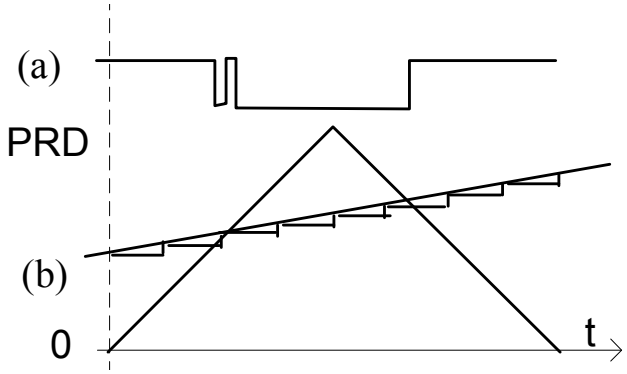


Figure 4-6: multi-time switching (a) the final switching waveform (b) the resampled reference and the 'virtual' triangle carrier

Whether it is an issue or not, depends on the consideration of the design regarding the switching losses and the heat dissipation. If it is considered as a problem, it can be avoided by a software 'flag' [17]. Consequently, when calculating the compare values of CMPA and CMPB, this flag should be considered. In the simulations and experiments of this paper, multi-time switching is allowed.

4.4 Simulation and Experiment

4.4.1 Simulation of different PS-PWM methods

In order to analyse the performance of uniform PS-PWM with in-phase sampling, with phase-shifted sampling and resampled uniform PS-PWM, simulations are carried out in Matlab/Simulink environment. The parameters for the simulations are presented in Table 4-1. Since the focus is put on the modulation method, the voltage control is made in open loop and the output is not connected to any load.

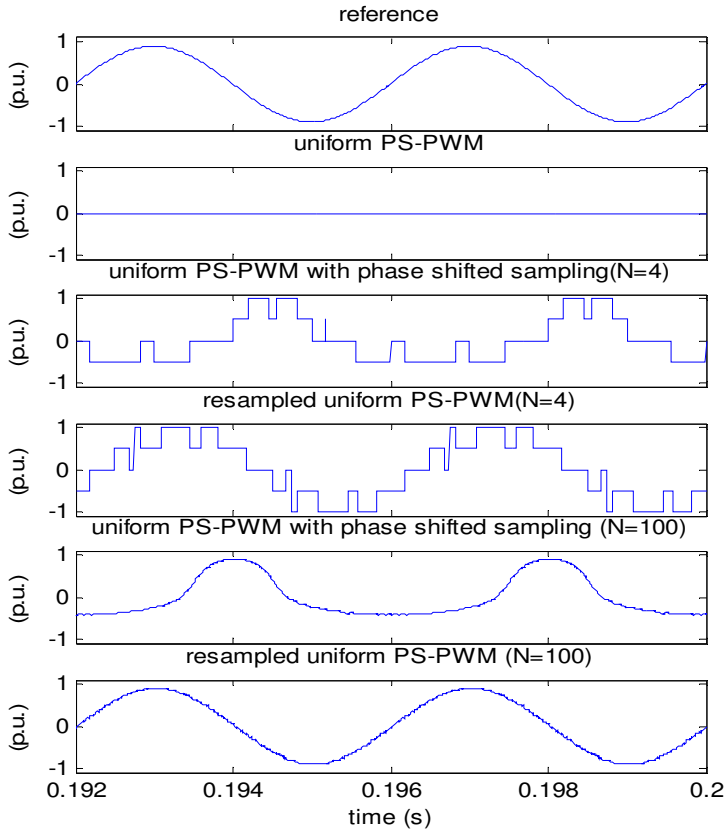
It can be seen from Figure 4-7 that with a reference signal frequency close to the Nyquist frequency, i.e. 250Hz (half of the sampling frequency 500Hz), the uniform PS-PWM cannot work at all. Though the uniform PS-PWM with phase-shifted sampling can partly track the reference, it is very questionable due to the very low AC gain (only 66% of the reference, Figure 4-7.b). Meanwhile, the resampled uniform PS-PWM has an AC gain 100%, indicating a perfect tracking of the reference signal. This is due to the frequency of the reference signal is far below the resampling frequency (= $f_c \bullet RSR \bullet 2$ where RSR is equal to the sub module number N). It can be noticed that even with a large N, uniform PS-PWM with phase shifted sampling always has a distorted waveform due to the reason given in section 4.2.1.

4.4.2 Experimental validation of the proposed solution to resampled uniform PS-PWM

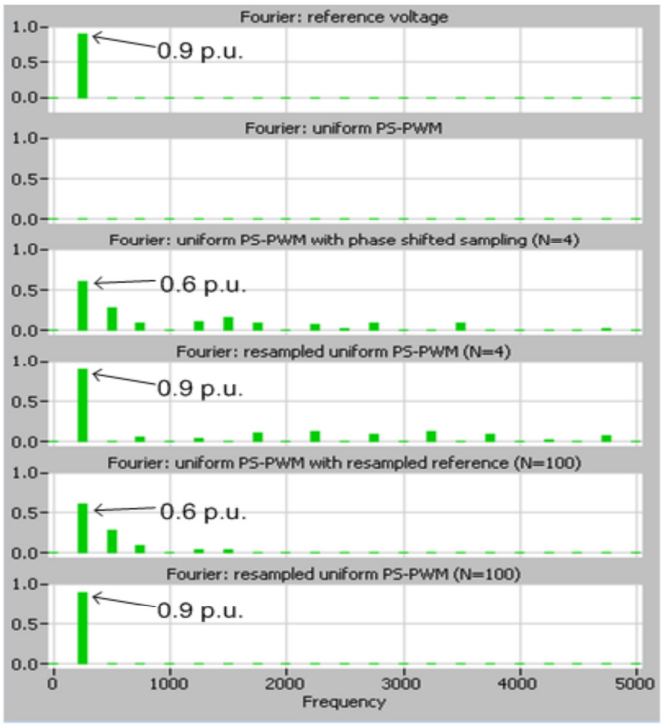
The experimental setup used to test the proposed solution is shown in Figure 4-8. The master is equipped with a TI MCU (320F28335), two current sensors to measure positive and negative arm current, and SPI communication through optic fibres. Each SM is equipped with a MCU (F28069, and its PWM module is the same as the one of F28335 [6]) to make the PWM modulation by the proposed method in the previous sections.

The experiment is divided into two steps. The first step is to demonstrate the ability of the DSP to produce the rising edge and falling edge at any instant during the PWM period by the independent comparators CMPA and CMPB, as this is the key of the proposed solution to implement resampled uniform PS-PWM. This is validated by the results shown in Figure 4-9: PWM1 signal can start with a rising edge (CMPA=0, duty is determined by the CMPB value), while PWM2 signal can start with a falling edge (CMPB=0, duty is determined by the CMPA value). The toggle signal is toggled when PWM counter equals zero to identify the PWM period.

The second step is to demonstrate the resampled uniform PS-PWM implemented by the proposed solution. It can be seen from Figure 4-10 that the output waveform of the PS-PWM is similar to the waveform resulted from the simulation. The output voltage has a DC component because it is measured to '-Vdc/2' (not to 'ground', see Figure 2-2).



(a)



(b)

Figure 4-7: Simulated output voltage of MMC using PS-PWM modulation (a) time domain (b) Fourier analysis

Table 4-1: parameters for simulation

parameter	abbv.	value
DC link voltage	Vdc	+/-1 [p.u.]
Output reference voltage	Vref	$0.9\sin(2\pi ft)$ [p.u.]
reference frequency	f	250 [Hz]
individual carrier frequency	f_c	500 [Hz]

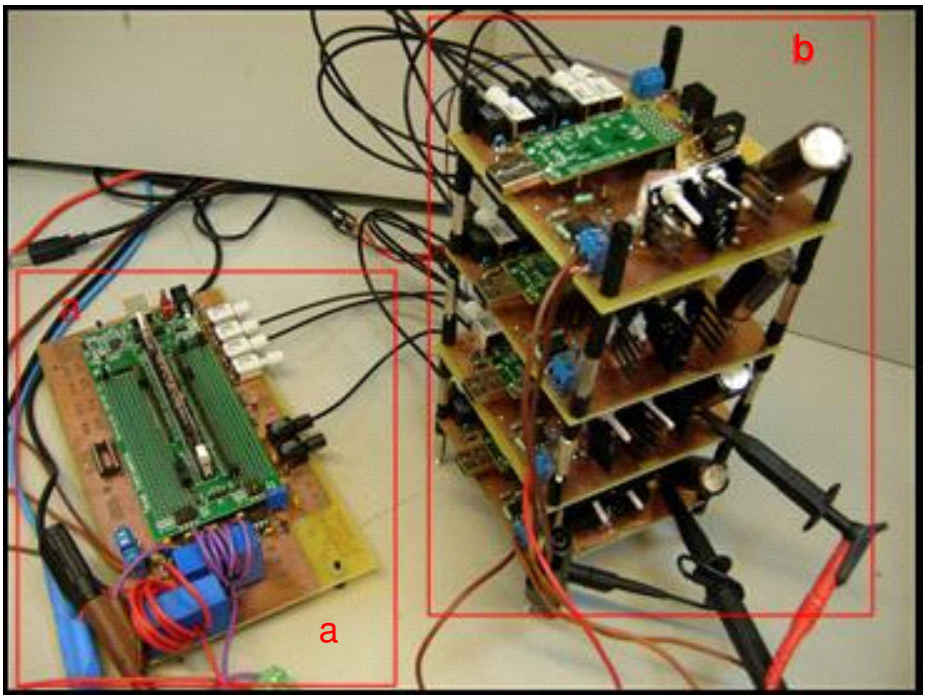


Figure 4-8: experiment setup (a) master (b) 4 SMs

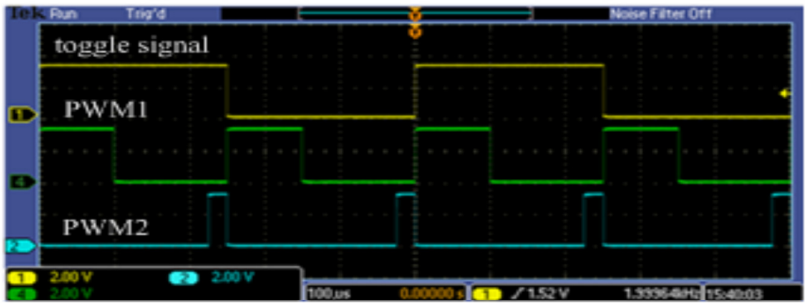


Figure 4-9: Measured PWM signals produced by MCU

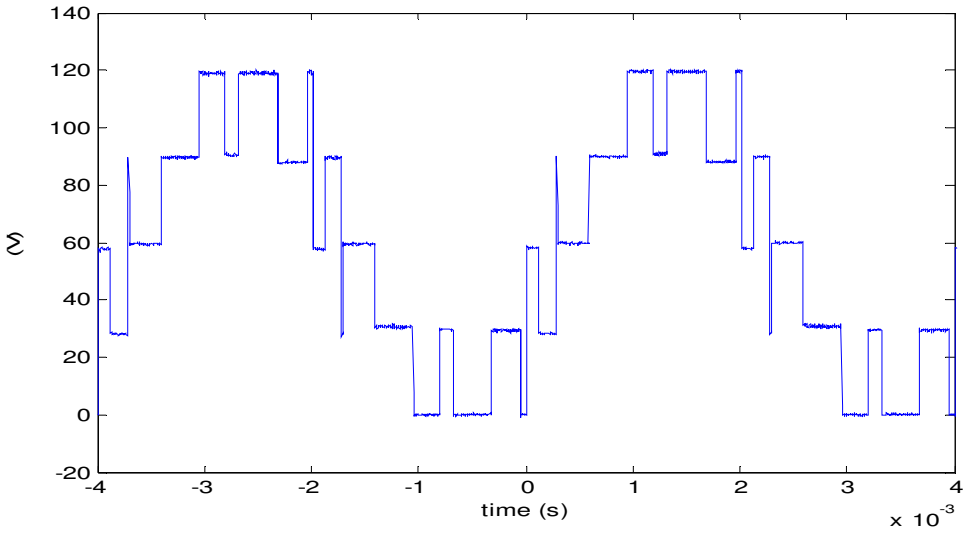


Figure 4-10: Measured output waveform of the resampled PS-PWM with a 250Hz sinusoidal reference.

4.5 Summary

A new technique to implement the resampled uniform PS-PWM method in microcontroller have been proposed and analyzed in this chapter. From the simulations and experimental results it can be concluded that the resampled uniform PS-PWM has a higher performance than the uniform PS-PWM with in-phase sampling or phase-shifted sampling, due to its high effective sampling frequency. The drawbacks of the previously proposed software implementation were overcome without causing a big overhead for the microcontroller. However, the microcontroller has to be equipped with a PWM unit which has two compare registers. The experimental results have demonstrated the suitability of the proposed solution for implementing resampled uniform PS-PWM.

Chapter 5 Distributed control of MMC for HVDC

The outline of this chapter is as follows. In section 5.1, the centralized and the distributed control structure are compared. Section 5.2 presents the distributed control architecture based on communication. Then section 5.3 compares the different modulation and control methods for MMC as well as the selection of the modulation and control methods suitable for the distributed control. Frequency domain analysis and controller design are carried out in section 5.4. In section 5.5, the simulation results are presented and discussed. The conclusions are made in section 5.6.

5.1 Control structure: centralized vs distributed

No matter what control structure is chosen, the following factors must be considered:

- a large number of SMs, it's a challenge to measure all capacitors' voltage and transmit to the control center
- SMs have different potential to ground, thus isolation must be considered when communication cables are chosen

To choose a control structure is the first crossroad in the way to the final successful control of MMC as subsequently, some multilevel converter control methods are limited to a certain control structure. There are two control structures: centralized control structure and distributed control structure. Both of them will be discussed in this section.

5.1.1 Centralized control

Having a simple structure, the centralized control for MMC has gained a lot of interest from lab researches as well as commercial practices, as it is adopted in the product 'HVDC PLUS' by Siemens [1]. As shown in Figure 5-1.a, for centralized control all the control tasks are implemented in the central control unit and then the switching commands are sent to each SM. The SM has no control task at all and it just follows the switching commands ('on' or 'off') from the central control unit. Of course, the SM has to measure the capacitor voltage and the current and send back the control unit.

The advantages of this control structure are:

- simple structure, as it has only one control unit which takes over all the control tasks
- can apply almost all the control methods published in the literatures regarding MMC, because all the information needed for the control will be gathered in the central unit

But, due to the fact that the central control unit runs the whole control algorithm and consequently a high bandwidth is required for communication and also high CPU computation ability, this control structure makes MMC costly.

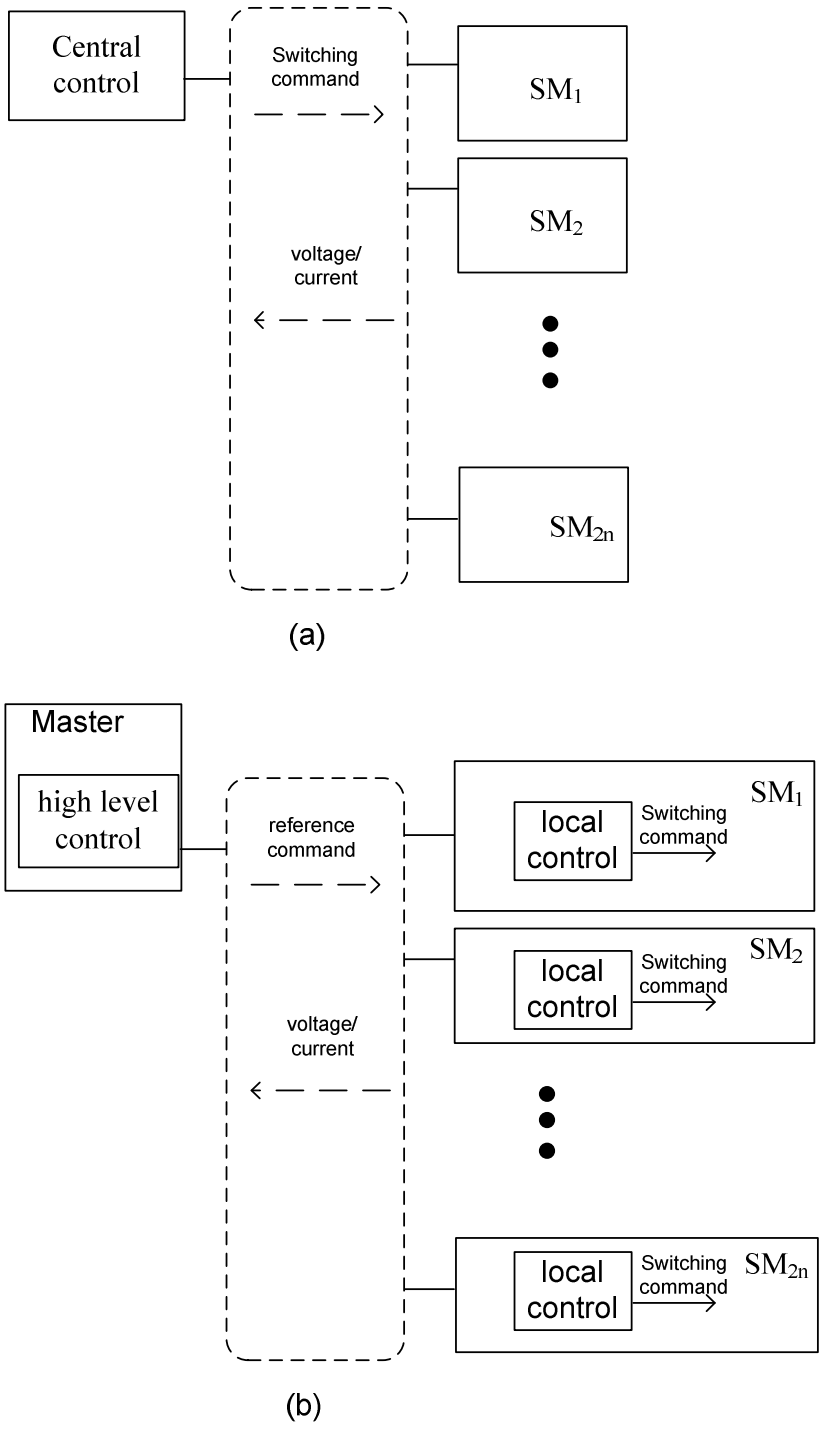


Figure 5-1: (a) centralized control structure (b) distributed control structure

5.1.2 Distributed control

In order not to lose the modularity feature, as it is the biggest advantage of MMC, distributed control is very promising. Distributed control systems find their many applications for Cascaded H-Bridge Multilevel (CHBM) converters [21, 26, 27] due to the feature of having many sub modules, thus they are also instructive

references for the study of MMC with distributed control disregarding the different converter topology. The peer-to-peer configuration [27] and the master-slave configuration [21, 26]are two possible distributed control structures. For both cases, the distributed parts (peers or slaves) should do as much as possible logic work. As an example, the master-slave configuration is shown in Figure 5-1.b. The master will do a part of the control tasks: high level control while the slaves (located in each SM) will do the rest part: local control. The key difference of this structure comparing to the centralized control is that the switching command is made in each individual SM and not in the central control unit.

Advantages of the distributed control are:

- Computation burden could be shared among master controller and slave controllers
- Benefit the modularized design of MMC (easy maintenance, and manufacturing)

Disadvantages may be:

- Cooperation between master controller and slave controllers is a challenge
- Controller design is more challenging compare to the centralized control
- Some multilevel converter control methods are not suitable for distributed control

5.2 Architecture of the distributed control

In this section, architecture of the distributed control system for the single phase MMC will be introduced (Figure 5-2), which consists of one master and 2N slave devices. The master will deal with the high level controls, such as power control (active and reactive), and the converter level controls, such as average voltage and difference current control. The slave will only deal with the sub module level control (capacitor voltage balance control) and the generation of the PWM signals.

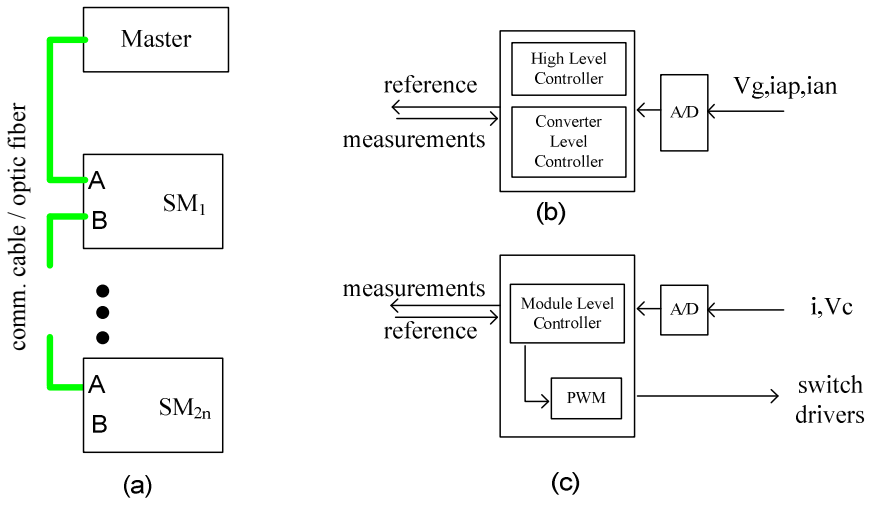


Figure 5-2: the distributed control system architecture (a) connection of the master and sub module slaves (b) function blocks of the master (c) function blocks of one slave

Time parameters of the control system are defined in Table 5-1. Assuming that the master will communicate firstly with SM1, then with SM2, at last with SM2n, i.e. in a polling manner, there is a relation $t_1 < t_2 < \bullet\bullet\bullet < t_{2n}$. The master and slaves can achieve very accurate synchronization ($\leq 1\mu s$) by the real-time communication protocol, e.g. EtherCAT or SPI as discussed in chapter 3. The time sequence diagram of the master and slaves is shown in Figure 5-3. The slaves are in event-driven mode, i.e. the slave tasks will start immediately after receiving the reference from the master. Thus the sampling period for module level controller (for example: T_{Modu1}) is changeable due to varying communication delay which depends on the network conditions.

Table 5-1: time parameters for the distributed control system

$t_1,\ t_2,\ldots,\ t_{2n}$	communication delay from master to SM1, ..., SM2n
T_{high}	sampling period for high level controller
T_{conv}	sampling period for converter level controller
$T_{Modu1},\ldots,T_{Modu2n}$	sampling period for module level controller
Δt	execution time of the master task

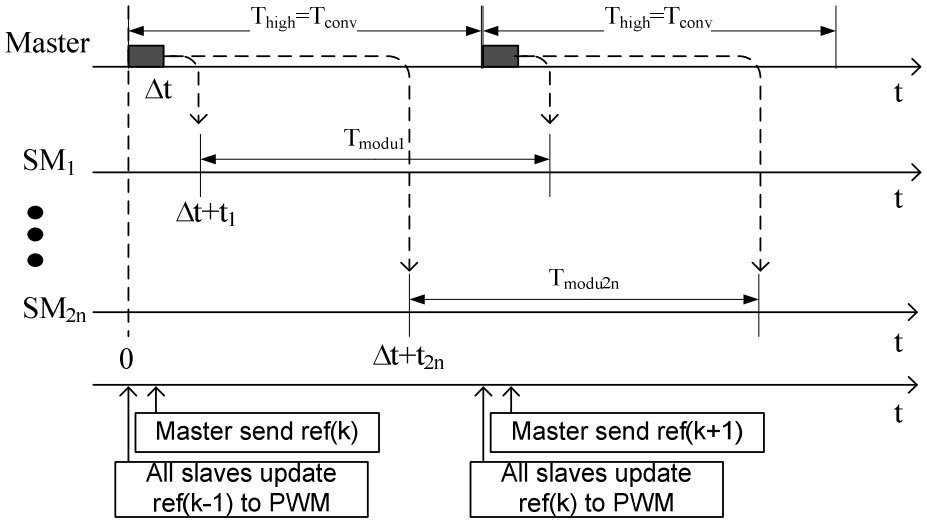


Figure 5-3: time sequence diagram

5.3 Modulation and Control methods

5.3.1 PWM modulation and individual balance control

PWM Modulation methods for multilevel converters, such as PD (Phase Disposition), POD (Phase Opposition Disposition), APOD (Alternative Phase Opposition Disposition), PSC (Phase Shifted Carrier), are analyzed in

paper [15]. Among others, PD and PSC are two basic modulation methods, which will be further analyzed regarding suitableness for distributed control.

Among other variations, 'close-loop proportion' control [22] (see Figure 5-4.b) and 'sort plus select' [28] are two basic voltage balance control methods. From the implementation point of view, the former method is suitable for PSC modulation while the latter one is suitable for PD modulation. As combinations (modulation + balance control), they are compared and the results are tabulated in Table 5-2. According to the advantages and the suitableness listed in Table 5-2, PSC/ close-loop proportion control are selected as the modulation and balance control methods for the distributed control system in the following study.

The PSC PWM modulation (shorted as PS-PWM) for the distributed control system could be categorized into two types: the uniform PS-PWM and the resampled uniform PS-PWM (see chapter 4). According to the conclusions made in chapter 4, the resampled uniform PS-PWM is superior to the uniform PS-PWM because it can offer higher controller bandwidth and less voltage distortion and therefore is chosen as the modulation method for the distributed control system. According to the time instant of updating the reference to the PWM module, the resampled uniform PS-PWM could have two sub-types. In one sub-type, which has already been discussed in chapter 4, the reference is updated to the PWM module on each SM at a synchronized instant (e.g. the beginning of the coming sampling period of the master, see Figure 5-3), i.e. in a synchronous manner. The advantage of this sub-type is that the output voltage has almost no distortion but the disadvantage is that the SMs have to wait until the next synchronized instant to update the reference.

In the second sub-type (which has not been covered in chapter 4), the reference is updated to the PWM immediately after the slave receiving the reference from the master and superposing a small additional reference resulted from the individual balance control. The advantage of this sub-type is that the delay is reduced to as small as possible. But due to the time of receiving reference from the master is different for each slave (see Figure 5-3), if updating the reference for PWM according to this sub-type, the references for each SM will be different at most of the time (e.g. it's possible that at one moment, some SMs are using the 'old' reference while other SMs are using the updated 'new' reference), resulting a distorted output voltage. This phenomenon is similar to the voltage distortion caused by the uniform PS-PWM, which has been discussed in chapter 4. This sub-type could be referred as updating reference in an asynchronous manner in contrast to the first sub-type.

The above two methods of updating reference (in synchronous manner and in asynchronous manner) will be further discussed through simulations in section 5.5.

Table 5-2: comparison of the modulation and balance control methods

modulation / balance control	Advantage	Disadvantage	suitability for distributed control
PD/ sort plus select	always stable due to no close loop control	1)indeterminate switching frequency 2)heavy computation load due to sorting if sub module number is high	not suitable due to the need for capacitor voltages from all sub modules
PSC/ close-loop proportion control	1)reduced harmonics due to high equivalent switching frequency 2)low switching frequency	1)stability problem due to close loop control 2)arm inductors suffering high voltage pulses due to non-simultaneous switching	suitable, the voltage balance control can be done locally in individual sub module

5.3.2 Average voltage control and difference current control

According to the distributed control architecture, the average voltage control and difference current control (belong to the converter level control) are implemented by the master. Two PI controls (structured as two nested control loops with current control inside and voltage control outside) will be used to control the voltage and the current respectively, as proposed by the authors of [22] (see Figure 5-4.a). The average voltage control is a powerful means for overall balance control and it works as a complement to the individual balance control (see Figure 5-4.b). It has a faster response than the individual balance control because it can 'manipulate' the current through its current minor control loop while the individual balance control method cannot.

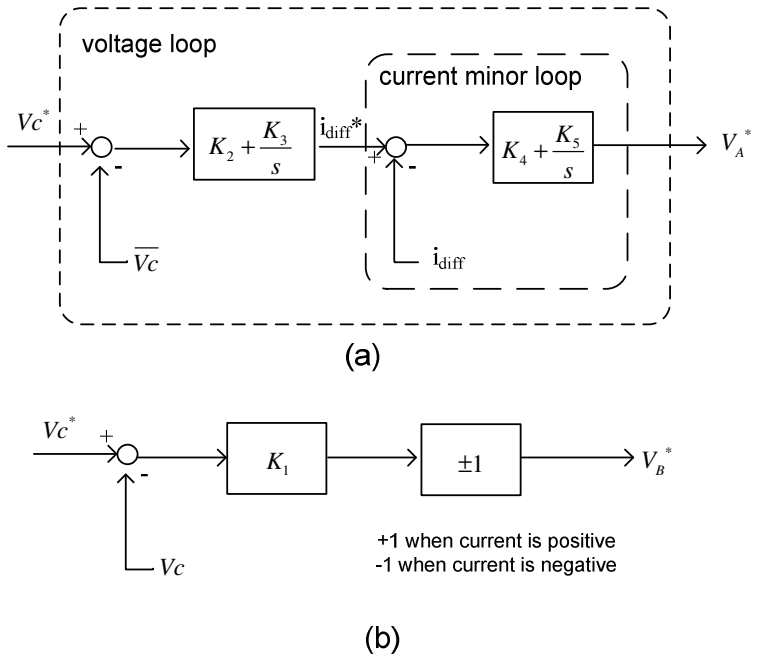


Figure 5-4: balance control methods (a) average voltage control (b) individual balance control

5.4 Frequency domain modelling and controller design

5.4.1 Module level control-capacitor voltage balance

5.4.1.1 Plant model

In paper [29], a time domain model of the SM is revealed. In case the discharging resistance (which is in parallel to the capacitor of the SM, representing a leakage) is neglected and considering only one SM, the differential equation of the plant (mainly only the capacitor) becomes:

$$C_{SM} \bullet \frac{dV_c}{dt} = S_{sw} \bullet i_x \tag{5.1}$$

where C_{SM} is the capacitance, V_c is capacitor voltage, i_x (x =ap for the upper arm SM; x=an for the lower arm SM) is the current flowing through the SM, and S_{sw} is the switching state of the SM. When S_{sw} =1/0, the SM is inserted/by-passed.

But this plant model is not yet able to be used for the controller design because the output of the individual balance control (an additional voltage reference V_B^*, see Figure 5-4.b) is not part of the plant model. Some modifications are necessary.

In normal operation condition, the frequency of i_x is close to 50 Hz. When the carrier frequency is high enough (5~10 times of the frequency of i_x), the current i_x can be deemed as constant at each carrier period. So in one period of the carrier (T_{crr}), the right side of equation could be approximated as:

$$\int_{T_{crr}} S_{SW} \cdot i_x \approx \int_{T_{crr}} d \cdot i_x \tag{5.2}$$

where d is the duty cycle, resulted from the high level control output (denoted as V_{out}^*), the average voltage control output V_A^* (see Figure 5-4.a) and the individual balance control output V_B^* (Figure 5-4.b).

Further considering that the individual balance control only output V_B^* while V_{out}^* and V_A^* could be looked as disturbances, the plant model is formed as:

$$C_{SM} \frac{dV_c}{dt} = d_B \cdot i_x \tag{5.3}$$

where d_B is the duty from individual balance control output V_B^*,

V_c is the capacitor voltage (more accurately speaking, is the average voltage in T_{crr}).

And in s-domain, the plant model can be written as:

$$\frac{V_c(s)}{d_B(s)} = \frac{i_x(s)}{sC_{SM}} \tag{5.4}$$

which is now able to be used for the individual balance control design since d_B is proportional to V_B^*, the output of the individual balance control.

5.4.1.2 Discussions about the plant model

The plant model is an approximated model and the higher the carrier frequency is, the more accurate the model is. Also because the s-domain function of i_x is complicated, it is better to consider i_x as a constant value (e.g. use the average value instead of the instantaneous value of i_x) and the plant model is piece-wise valid and can be simplified.

5.4.1.3 The whole control loop

Using a first order filter with a time constant $\tau_1 = \frac{1}{2f_{crr}}$, where f_{crr} is the individual carrier frequency, to emulate the delay caused by PWM, the block diagram of the control loop 1 can be formed as shown in Figure 5-5. A limiter is added due to the limited allowed duty cycle.

It should be noticed that the equivalent arm capacitance C_{arm} is used instead of the individual capacitance C_{SM} of SM (where $C_{arm} = \frac{C_{SM}}{N}$), because C_{arm} will be kept constant when N is varying between 8 and 200 (see Table 5-5). In this way, the designed control loop 1 (K_1) can be reused for different N. Accordingly, the input reference is also amplified by N (Figure 5-5).

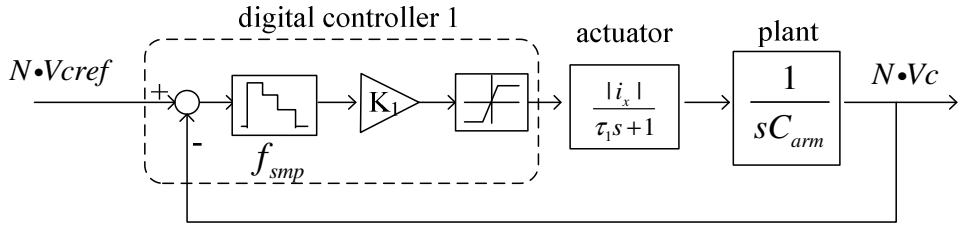


Figure 5-5: control loop 1-the individual balance control

Sampling effect could be neglected when analyze the individual balance control since f_{smp} is much larger than f_{crr} (see Table 5-5).The open loop transfer function could be derived as:

$$G_{o1} = \frac{K_1 \bullet |i_x|}{sC_{arm}(\tau_1 s + 1)} \tag{5.5}$$

5.4.1.4 Optimum K1

Assume that the variation of the capacitor voltage is ε and the limitation of the limiter is γ, the range of K_1 which could lead to a linear operation of the controller is:

$$K_1 \le \frac{\gamma}{\varepsilon \bullet N \bullet V_{ref}} = \frac{\gamma}{\varepsilon \bullet V_{dc}} \tag{5.6}$$

Considering the example case (γ=2%, ε=10%, Vdc=360kV) for this project, there is $K_1 \le 0.00056$ [1/kV]. Root locus is plotted in Figure 5-6 with the parameters listed in Table 5-5($|i_x|$ is simplified as the average current, which is around 6kA). The red thick lines stand for $0 \le K_1 \le 0.001$. It could be seen that K_1

=0.00056 is the optimum, because when K_1 is increasing (along the red line), the dominant root is moving toward left (meaning faster response) without creating overshoot and the maximum value allowed by the limiter is 0.00056.

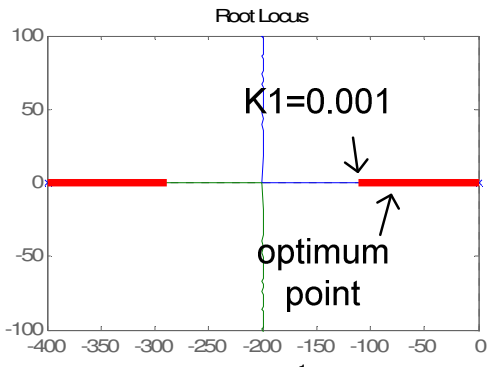


Figure 5-6: root locus of the loop 1 (open loop)

5.4.2 Converter level control-average voltage and difference current control

5.4.2.1 Plant models

As discussed in section 5.3, the converter level control is structured as two nested control loops: loop 2 and loop 3 (Figure 5-7). Loop 2 is for difference current control while loop 3 is for average voltage control. A first order delay is used to represent the PWM delay and the time constant τ_2 is depending on the effective switching frequency, namely

$$\tau_2 = \frac{1}{2N \bullet f_{crr}} \tag{5.7}$$

Plant 2 is an L-R circuit while plant 3 consists of N capacitors with an equivalent capacitance C_{arm} because under normal operation condition, there are always approximately N sub modules are inserted in the phase leg. Since the plant models are not changing when N is varying, the designed controllers can be reused for different N.

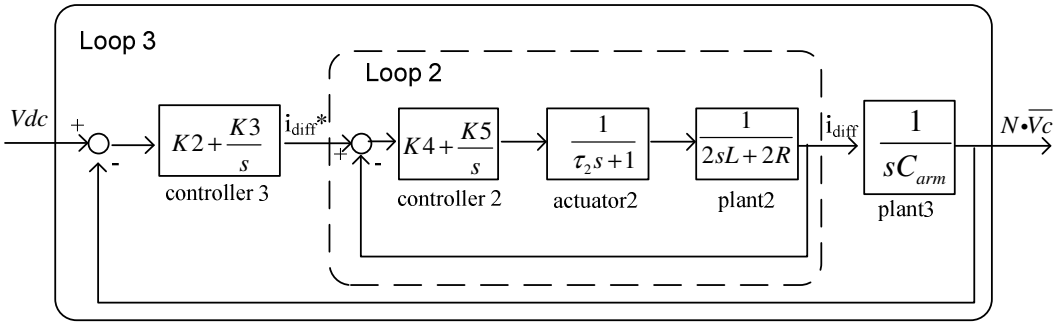


Figure 5-7: control loop 2 (difference current control) and control loop 3 (average voltage control) in s-domain

5.4.2.2 Controller 2 design

In this sub section, the controller design was firstly made in s-domain in order to use analytical methods. Then the best candidate design was selected through simulations in z-domain, because the model in z-domain was more close to the real system. Though design in z-domain directly might be able to have a more accurate result because the sampling period (T_{smp}, around 1ms) is not neglectable in compare to the designed bandwidth, it is left to the future work due to the limited time of this project.

The open loop transfer function is:

$$G_{o2} = (K_4 + \frac{K_5}{s}) \cdot \frac{1}{\tau_2 s+1} \cdot \frac{1}{2sL+2R} \tag{5.8}$$

It can be rewritten as:

$$G_{o2} = \frac{K_4(sT_{ic}+1)}{sT_{ic}} \cdot \frac{1}{\tau_2 s+1} \cdot \frac{\frac{1}{2R}}{sT_a+1} \tag{5.9}$$

where time constant $T_{ic} = K_4 / K_5$ and $T_a = L / R$.

If the modulus optimum method [30] is used to find the optimum design of the controller according to the form of equation (5.9), the resulted bandwidth would be too high for the sampling frequency (around 1kHz). Therefore the following design process did not consider the modulus optimum method.

Choosing $T_{ic} \approx T_a + \tau_2$, equation (5.9) could be further simplified as:

$$G_{o2} \approx \frac{1}{s\frac{T_{ic} \cdot 2R}{K_4}} \tag{5.10}$$

(Considering the parameters in Table 5-5, T_a was found to be around 2ms while τ_2 <0.2ms when N>12 according to equation(5.7) , hence $\tau_2 << T_a$)

If the final close loop system is expected to have a first order form $\frac{1}{1+sT_{ref}}$, there is:

$$T_{ref} = \frac{T_{ic} \cdot 2R}{K_4} \tag{5.11}$$

Based on this equation and the assumption $T_{ic} \approx T_a + \tau_2$, K_4 and K_5 could be found as:

$$K_4 = \frac{2R(T_a + \tau_2)}{T_{ref}} \tag{5.12}$$

$$K_5 = \frac{2R}{T_{ref}} \tag{5.13}$$

In s-domain, the above designed controller should have no overshoot in step response, but it is not the case in z-domain as well as in the real system. Therefore the next step is to choose several candidate values for T_{ref} and verify them in z-domain by simulations. The block diagram of the z-domain model is shown in Figure 5-8. A unit delay is inserted in loop 2 because the first sub-type of resampled uniform PS-PWM is applied, i.e. updating the reference in a synchronous manner (see section 5.3).

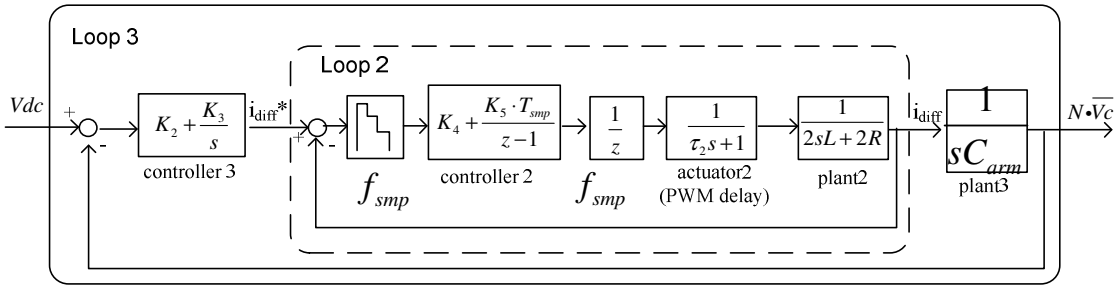


Figure 5-8: control loop 2 and control loop 3 in z-domain

Considering the lowest sampling frequency is 1 kHz, the candidate values for T_{ref} are chosen as listed in Table 5-3.

Table 5-3: candidates for the reference system

candidate	1	2	3	4	5
Reference freq. (Hz)	600	800	900	1000	1500
T_{ref} (s)	1/600	1/800	1/900	1/1000	1/1500

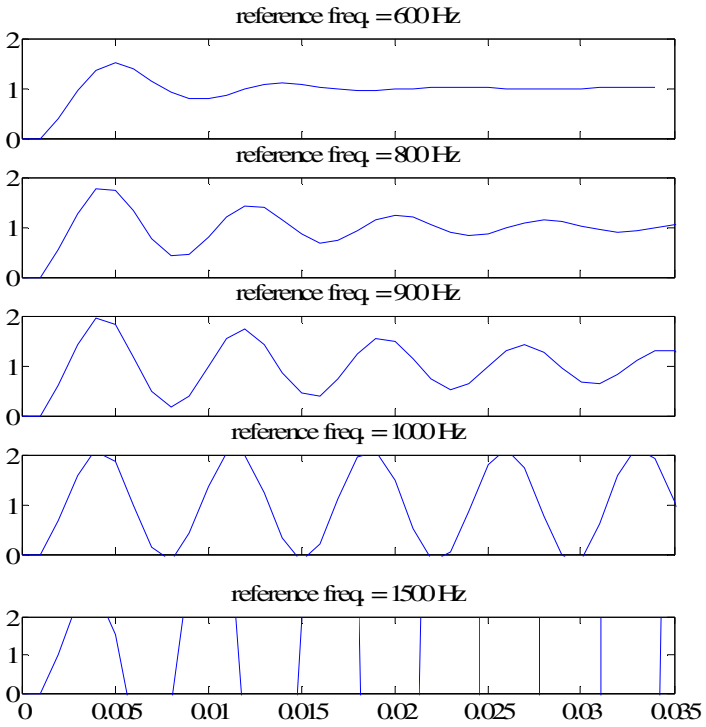


Figure 5-9: step responses of the close loop transfer function in z-domain

From the simulation results in Figure 5-9(parameters are chosen from the example case, see Table 5-5), the first candidate is the best due to its small oscillation. The results are understandable as the reference frequency approaching to and going over the sampling frequency, the oscillation are becoming bigger until unstable at last. Though the first candidate has an overshoot in step response, further reducing the reference

frequency (i.e. < 600Hz) to reduce the overshoot was not considered here due to the compromised effectiveness of disturbance rejection.

5.4.2.3 Controller 3 design

Since the bandwidth of the control loop 3 (the outer loop) should be 10 times slower than the current inner loop, the sampling effect is neglectable (the sampling frequency should be faster than the current inner loop). Considering the current inner loop as an ideal control, i.e. the transfer function for the inner loop is 1, the open loop transfer function of the loop 3 is:

$$G_{o3} = (K_2 + \frac{K_3}{s}) \cdot \frac{1}{sC_{arm}} \tag{5.14}$$

Firstly, due to the bandwidth of the designed inner loop is around 800 rad/s, the outer loop bandwidth is expected to be around 80 rad/s or even lower.

The bandwidth of the outer loop is roughly estimated by (let K_3=0):

$$BW_3 \approx \frac{K_2}{C_{arm}} \tag{5.15}$$

So,

$$K_2 \approx BW_3 \cdot C_{arm} \tag{5.16}$$

Secondly, the close loop transfer function of loop 3 could be formed as:

$$G_{c3} = \frac{\frac{1}{C_{arm}}(K_2 \cdot s + K_3)}{S^2 + \frac{K_2}{C_{arm}} s + \frac{K_3}{C_{arm}}} \tag{5.17}$$

Therefore K_3 could be estimated by:

$$K_3 = \frac{{K_2}^2}{4\xi^2 \cdot C_{arm}} \tag{5.18}$$

where ξ is the damping ratio.

In order to have no overshoot, the damping ratio is chosen to be 1. As a summary of section 5.4, all the designed controllers are listed in Table 5-4.

Table 5-4: summary of the designed control gains

items	formula	comments	Value (use Table 5-5)
K_1	$\frac{\gamma}{\varepsilon \bullet V_{dc}}$	$\gamma = 0.02$ $\varepsilon = 0.10$	0.00056[1/kV]
K_2	$BW_3 \cdot C_{arm}$	$BW_3 = 80$ rad/s	0.02[A/V]
K_3	$\frac{K_2{}^2}{4\xi^2 \cdot C_{arm}}$	$\xi = 1$	0.4[A/V˙s]
K_4	$\frac{2R(T_a + \tau_2)}{T_{ref}}$	$T_{ref} = \frac{1}{600}$ s $T_a = \frac{L}{R}$	1.387[V/A]
K_5	$\frac{2R}{T_{ref}}$	$T_{ref} = \frac{1}{600}$ s	600[V/A˙s]

5.5 Simulation results and discussions

The simulation was implemented in Matlab Simulink + PLECS with the parameters given in Table 5-5 and the controller gains in Table 5-4. The DC link voltage and AC power are chosen to be comparable with the recent HVDC projects (see Table 1-1).

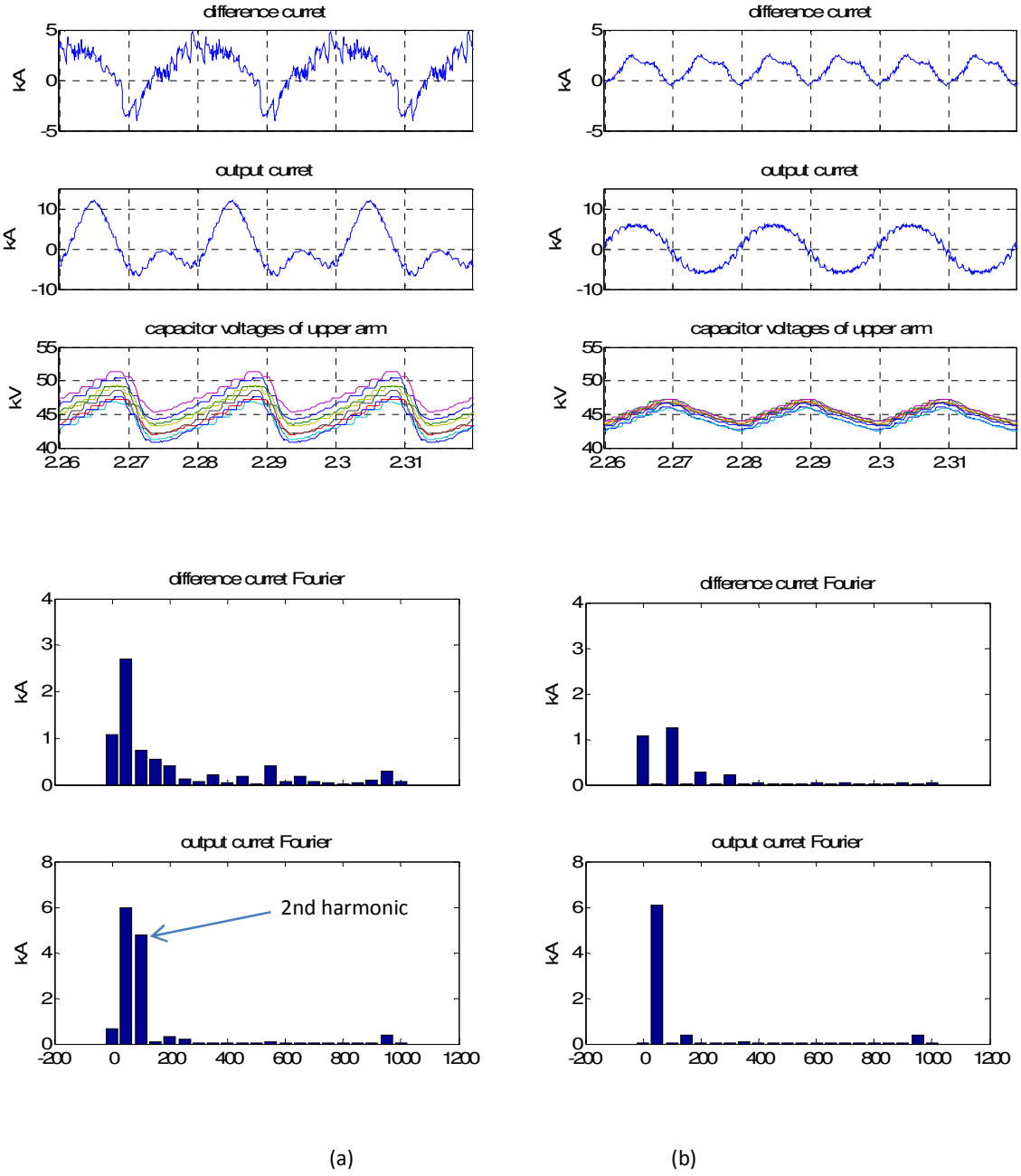
Table 5-5: parameters for simulation (an example case)

items	value	comments
DC link voltage (Vdc)	360 kV	
number of SMs per arm (N)	8~200	
Equivalent arm capacitance (Carm)	0.25 mF	
AC power (P)	378 MW	1 p.u.
AC voltage (Vg), single phase, rms	89 kV	1 p.u.

arm inductance (L)	1 mH	0.015 p.u.
Arm resistance, equivalent on-resistance of switches (R)	~0.5 ohm	0.024 p.u.
Filter inductance (Lf)	2.5 mH	0.037 p.u.
Grid frequency (F)	50 Hz	
Individual carrier frequency f_{crr}	$\geq$ 200 Hz	
Sampling frequency f_{smp}	$\geq$ 1kHz	

5.5.1 Two methods for updating the reference of the PWM

The first study is to find out which one is better of the two methods for updating the reference to PWM module. As discussed in section 5.3, the second method (updating the reference in an asynchronous manner) will lead to a distorted output voltage while the first method (updating the reference in a synchronous manner) will have more accuracy in terms of following the reference. This argument is validated by the simulation (Figure 5-10). It can be seen that more and bigger current harmonics (in both difference current and output current) appeared for method 2 (Figure 5-10.a) comparing to method 1 (Figure 5-10.b). A dc component appeared for method 2 because of the distorted output voltage. Though the voltage variation for method 2 is a little bigger than the one for method 1 due to the bigger difference current, the variation is still in the allowed limit ($\leq 10\%$). This proves the effectiveness of the balance control.



(a) (b)

Figure 5-10: comparison between the two methods by simulation (N=8, f_{crr} =500Hz, f_{smp} =1 kHz) (a) method 2, updating the reference in an asynchronous manner (time shift between each SM is 10 μs) (b) method 1, updating the reference in a synchronous manner

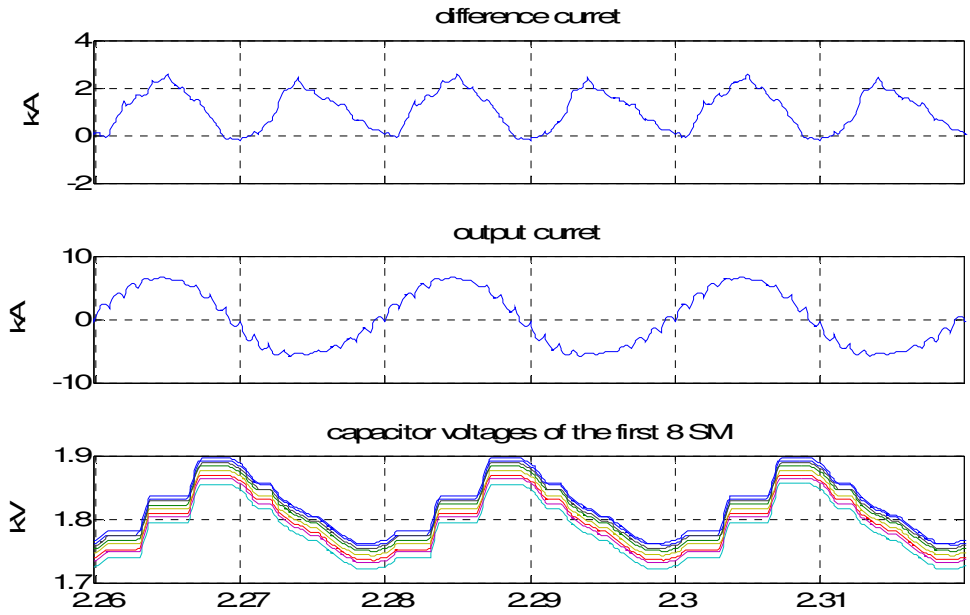
5.5.2 Lower boundary of carrier and sampling frequency

The second study is to find the lower boundary of the carrier frequency f_{crr} and the sampling frequency f_{smp} .

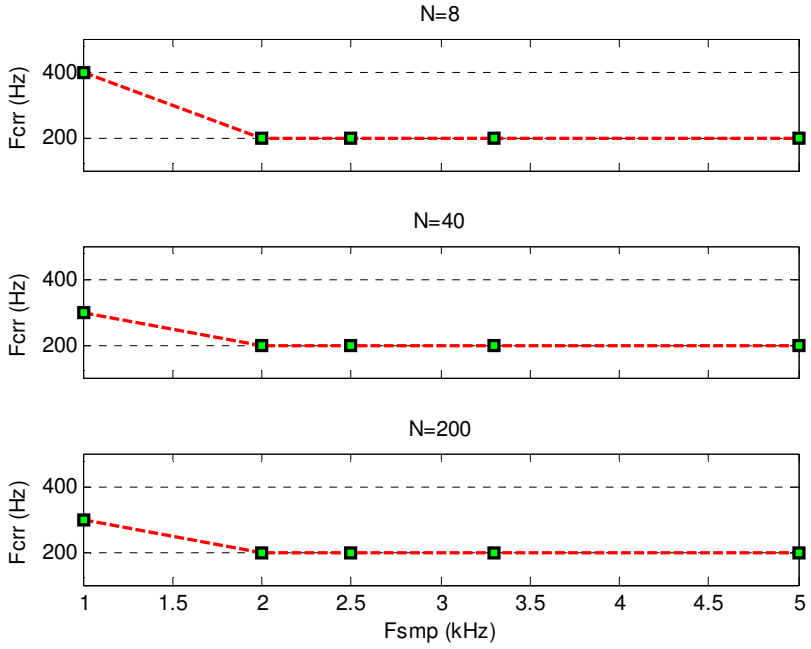
Since updating reference in a synchronous manner is found better in the first study, this method will be used

in the rest study. The sampling frequency is investigated from 1 kHz, as lower frequency may not be good for the high level controls. The carrier frequency is investigated from 100Hz to 1 kHz by a step of 100Hz. The criterion for the investigation is that the deviation of the capacitor voltage is less than 10% under steady state. The results of this investigation are shown in Figure 5-11. Figure 5-11.a shows the simulation results for one example case of the lower boundary found for N=200 and f_{smp} =1 kHz. Figure 5-11.b gives all lower boundaries found for N=8, 40 and 200.

It can be seen that when f_{smp} is no less than 2 kHz, the lowest f_{crr} is always 200 Hz, because the individual balance control is dependent on the individual carrier frequency rather than the sampling frequency (see the frequency domain model in section 5.4). It can be observed from Figure 5-11.b that When the max f_{smp} is 1 kHz, f_{crr} must be no less than 300 Hz. If higher f_{smp} is required by the high level control, the communication bandwidth must be increased by the methods discussed in chapter 3.



(a)



(b)

Figure 5-11: simulation results (a) one example case (N=200, f_{crr} =300Hz, f_{smp} =1 kHz) (b) lower boundaries of f_{crr} for different N and f_{smp}

5.6 Summary

Architecture of a distributed control system for MMC was introduced and analyzed in this chapter. Suitable modulation and control methods for distributed control were selected. The whole distributed control of the MMC was modelled in frequency domain through three different control loops. The control loops were then analyzed and the controllers were designed by analytical methods based on the frequency domain models. Due to a small adaption of the plant models, the designed controllers can be reused for any number of sub modules.

Resampled uniform PS-PWM was concluded to be the best type of PS-PWM for the distributed control of MMC in chapter 4. This chapter further analyzed the resampled uniform PS-PWM by discussing the different methods of updating the reference to the PWM of each SM. Simulation results of the MMC with grid connection have shown that updating the reference for resampled uniform PS-PWM in a synchronous manner is better than in an asynchronous manner.

Finally, lower boundaries of the individual carrier frequency were found for N in the range of 8 to 200 and the sampling frequency in the range of 1 kHz to 5 kHz. The results could help the designers to choose an appropriate switching frequency as it is important for calculating the losses of the converter.

Chapter 6 The prototype and experiments

This chapter begins with an introduction to the prototype (hardware). Then the key issues regarding the software design are presented. Next, the experiments are performed and the measurements are presented. Finally a summary is made.

6.1 Hardware design

In order to verify the distributed modulation and control methods, a down-scaled prototype was made for this project. An old prototype (has 1 master + 4 SMs equipped with SPI via optic fibers) was designed and made by the authors of the previous project [10], but it had not been fully tested. In this project which was a continuous work to the above mentioned project, the old prototype was improved and fully tested. Also, additional SMs have been made to be able to increase the voltage levels.

As it can be seen in Figure 6-1, the full MMC comprises one master control unit and 6 SMs, arranged in two arms of a single phase leg. PCB layout of the new master and the new SM can be seen in Figure 6-2 and Figure 6-3. They are the improved version of the old ones made in the previous project [10]. The improvement lies in:

- the master is equipped with 4 SPIs, working as a hub. In this way, the connection ability is improved (one SPI cannot connect all the SMs due to the limited communication speed)
- the master has 4 measuring channels to measure grid voltage, arm currents and DC link voltage. In this way the performance of the high level control and the converter level control could be improved by reducing the delay of measurement
- an Op-Amp is inserted as a buffer between the voltage sensor and the ADC in SM, in order to improve the accuracy of ADC

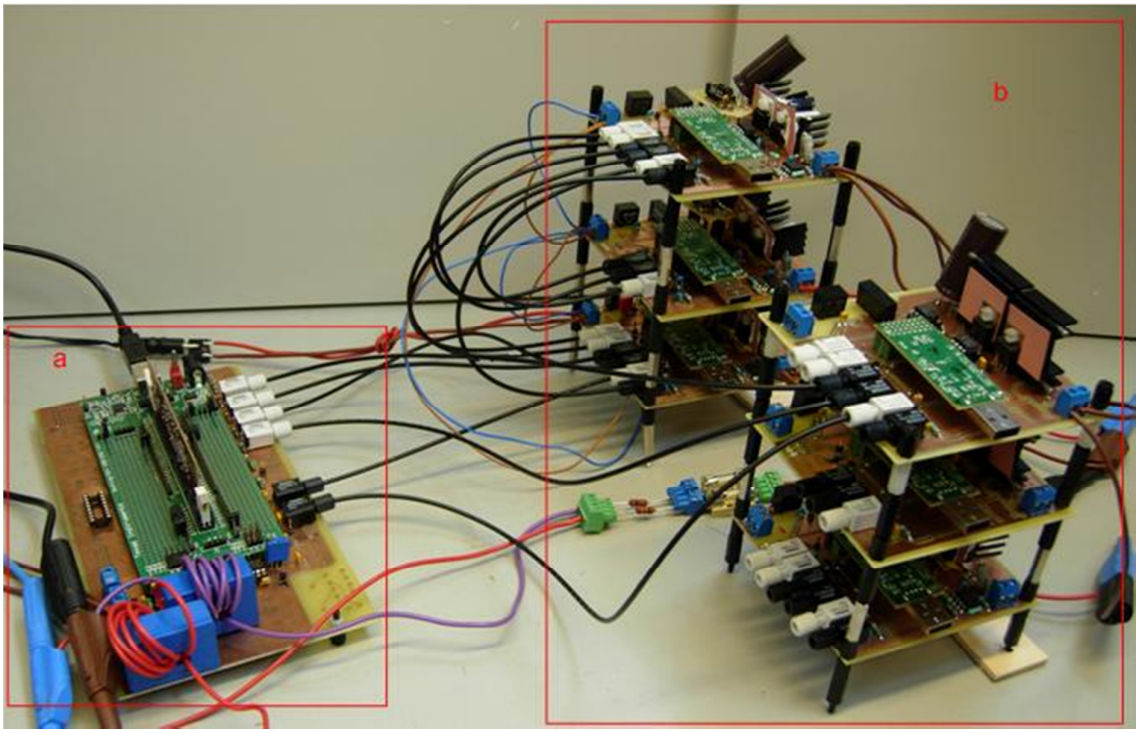


Figure 6-1: full view of the prototype (a) the master (b) 2x3 sub modules

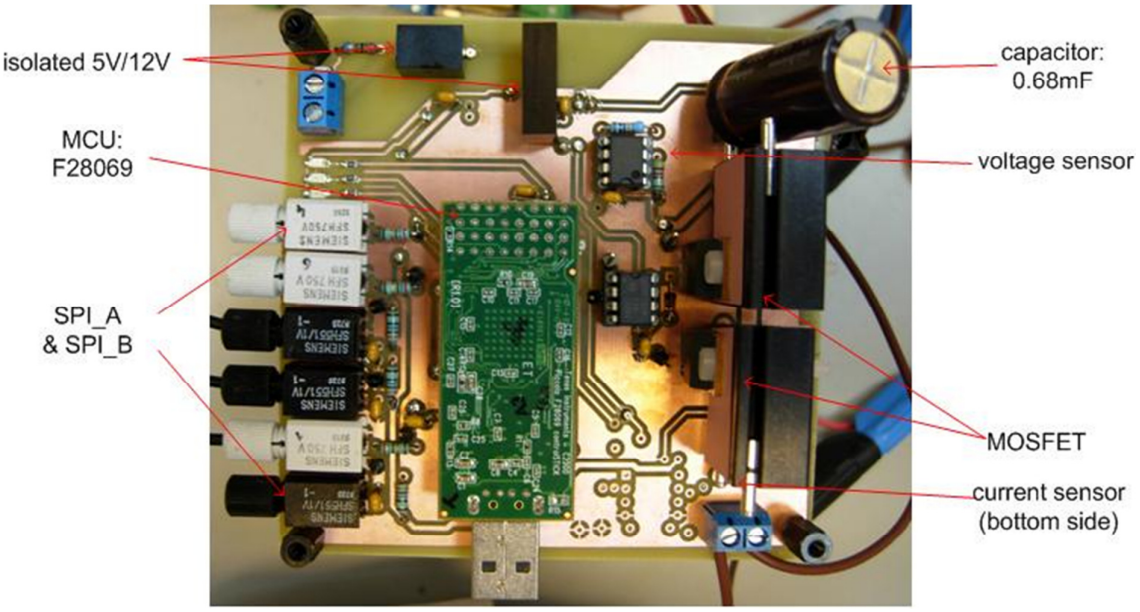


Figure 6-2: PCB layout of the new sub module

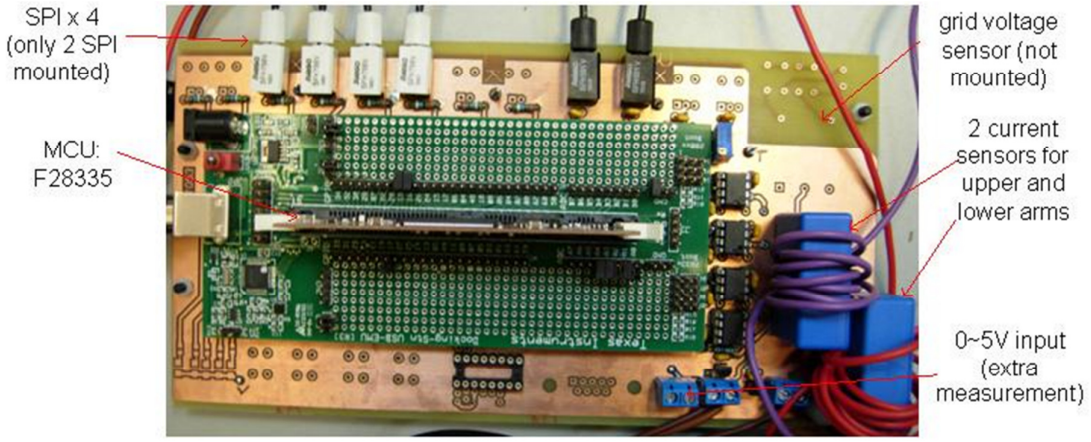


Figure 6-3: PCB layout of the new master

The complete schematic as well as the material lists of the master and the SM could be found in Appendix A.

6.2 Software design

6.2.1 Software for the slave MUC

6.2.1.1 SPI communication protocol

In order to explain the complicated process of the SPI protocol (application level), a flow chart is shown in Figure 6-4. The process consists of two routines: the SPI RX (receive) interrupt routine, which is triggered when the slave MCU (F28069) receives a whole Char (1~16 bit, predefined by the SPI module) from the master SPI, and the protocol processing routine, which can identify a data frame and process the specific commands (see Table 3-2).

In the 'SPI RX interrupt' routine, the time-critical command will be handled first. For example, the synchronization command (SYNC) must be handled as soon as possible in order to improve the synchronization accuracy (to make sure that every SM has the same response time). All other commands will be saved to a buffer called 'Rx buffer' if the SPI address is matched, otherwise the commands will be disregarded.

In the 'protocol processing' routine, a valid SPI frame whose length depends on the specific commands will be first identified. Subsequently, the valid SPI frame will be processed according to the specific commands.

6.2.1.2 Overvoltage protection and balance control

If the capacitor is over charged due to some reasons, e.g. the master gives a fault command or all other SMs are bypassed, all the surrounding components (gate driver, bootstrap diode, bootstrap capacitor, MOSFET and the capacitor itself) of the power circuit will be put in a dangerous condition. Unfortunately, the hardware does not have such protection to avoid this situation. To reduce this risk to a reasonable level, the protection is implemented in software. The protection will detect the capacitor voltage at a period of hundreds of

microseconds based on the following two considerations. On the one hand, the rise-rate of the voltage is very slow comparing to the detecting period (the sampling period) since the current is limited by the current rating of the MOSFET. On the other hand the additional computation burden for software protection could be limited to a tolerable range at the chosen detection period. Whenever the protection detects an overvoltage the SM will be forced to be bypassed (until manually reset), thus the capacitor can be stopped from further charging.

Current protection is not considered in the software design, since the response speed of the software protection is not good enough for current protection. Fortunately, the DC source used for the following experiments has a good current protection, which serves as an external current protection for the prototype since the fault current that goes through the prototype will also go through the DC source. Therefore the current protection is also assured. Of course, the fault current inside a SM, e.g. a shoot through due to a bad dead-time, cannot be protected by the external protection. Due to the limitation of the budget for the prototype, this risk has to be taken. Therefore, the turn-on, turn-off time and the dead-time must be carefully tested before any power experiments. Since the dead-time is assured by hardware (the PWM module of the MCU), the probability of an internal fault current is quite lower than the one of an external fault current, which happens very often during the software debugging stage.

The individual balance control is just a 'c' language implementation of the control algorithm which has been realized in the simulation model in Matlab Simulink and has been explained in chapter 5.

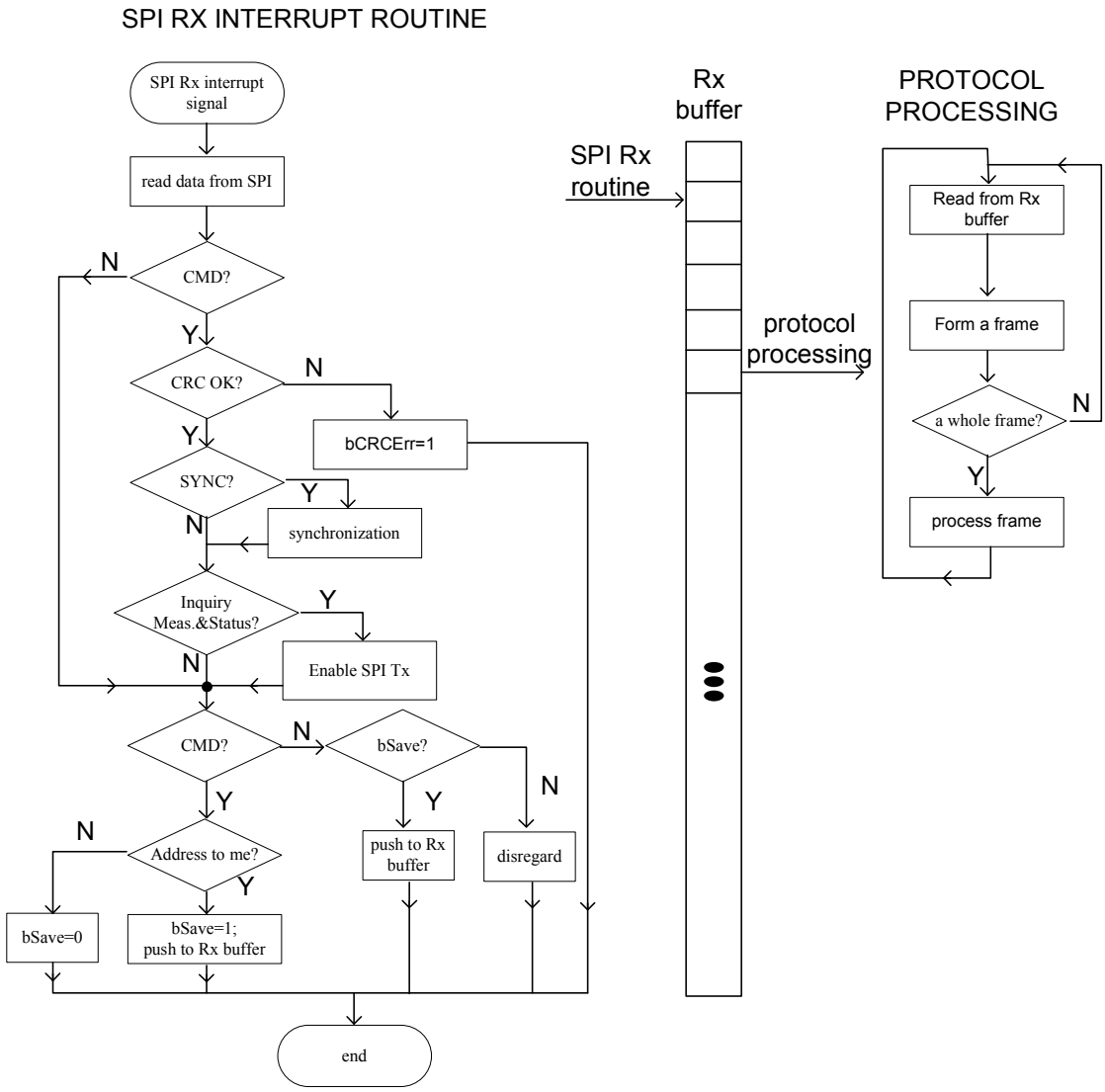


Figure 6-4: flow chart of the SPI communication protocol

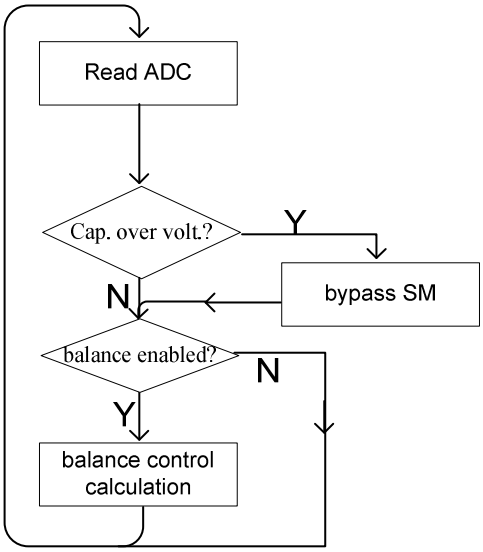


Figure 6-5: flow chart of the overvoltage protection and balance control

The flow chart of the overvoltage protection and the balance control is shown in Figure 6-5. The task will read the ADC results first. Then the overvoltage fault will be detected. At last, the balance control will be performed.

6.2.2 Software for the master MCU

6.2.2.1 SPI communication protocol

The SPI communication process for the master is simpler than the slave side, as it needs not to handle the time-critical commands or address detection (the master doesn't have SPI address as the slaves do). The flow chart is shown in Figure 6-6. The 'SPI RX INTERRUPT' routine saves all data to the 'Rx buffer'. Then the protocol processing routine will process the valid frames received from the slaves.

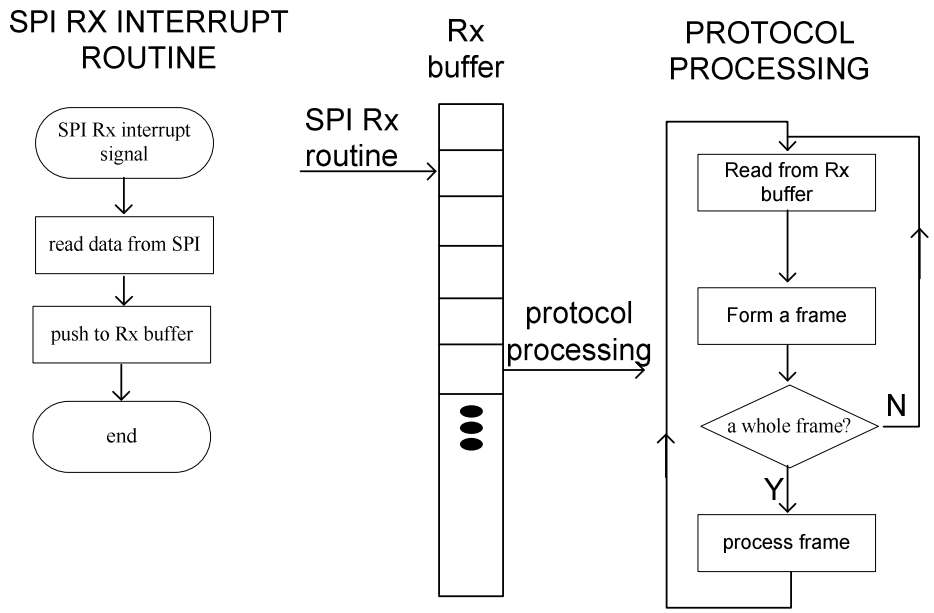


Figure 6-6: SPI communication in Master

6.2.2.2 Software startup and high level/converter level controls

The main job of the master is to manage all SMs and to perform high level/converter level controls (see Figure 6-7).

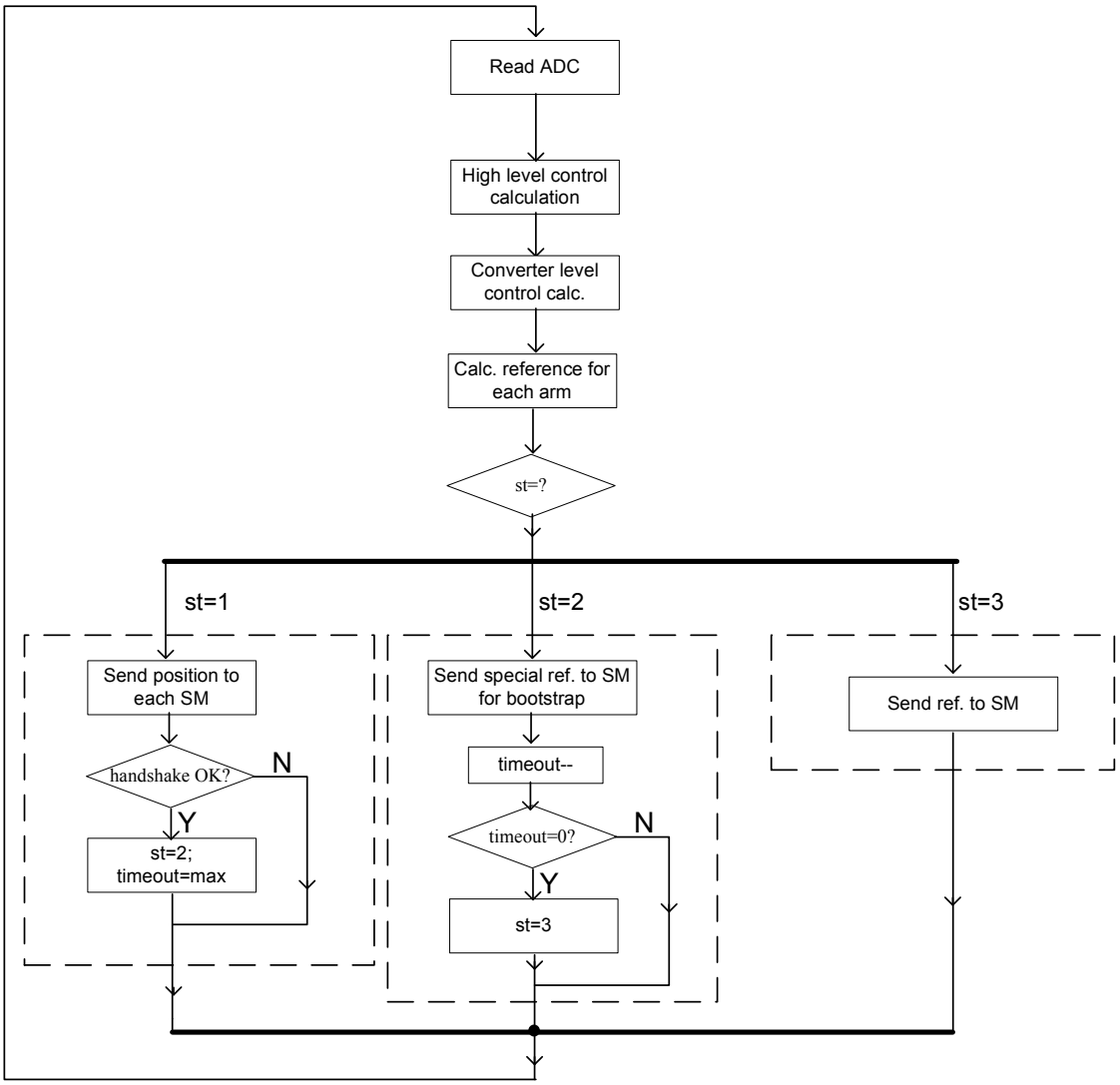


Figure 6-7: flow chart of software start-up, High level control and converter level control (cycling at sampling frequency)

The software startup is as the following (Figure 6-7):

- after CPU reset or power-up, the state machine (ST) is initialized to state '1'. In this state, the master will send assigned SM position to each SM, meanwhile the SMs will send their status back to the master. After the master has detected that all SMs are in the correct status, i.e. the handshake between the master and SMs is finished, the state machine will be changed to state '2'
- In state 2, the master will send a special command to all SMs to charge the bootstrap capacitors for the gate driver. This is a special step designed for the hardware, as the gate driver cannot work properly before the bootstrap capacitor is charged. After a predefined period, the state machine will step into state '3' automatically
- In state 3, the reference command will be sent to SMs periodically. State 3 is the final state and the state machine will keep running in this state until next CPU reset or power-up

The control algorithm for the converter level control has been explained in chapter 5. The high level control is an open loop control with a sinusoidal output to drive a RL load.

6.3 Experiments

6.3.1.1 Dead-time test

Before actually charge the capacitor, the dead-time of the PWM signals must be assured. The gate signals for the upper switch and the lower switch are measured as shown in Figure 6-8. As it can be seen from Figure 6-8, the dead-time is approximately 1 microsecond.

6.3.1.2 Balance control test with N=1

The simplest MMC with N=1 is tested to verify the power circuit and the distributed control methods.

As shown in Figure 6-9, at the beginning (t<0) the capacitors' voltages (vc1 and vc2) are around 34V, which is the same as the DC link voltage, but they are not balanced as vc2 is slightly higher than vc1. Then at t=0s, the balance control is enabled and the capacitors' voltages start to decrease to their reference voltage (30 V). The voltage balance between the SMs is also achieved because the mean values of vc1 and vc2 become almost the same in steady state. This proves that the voltage balance control with a distributed control structure is able to regulate and balance the SM's voltage effectively.

Because the high level control (power control) is an open loop control, it cannot eliminate the steady state error. Therefore, the magnitude of the output current is also decreased when the SM's voltage is decreased due to the balance control (see Figure 6-9).

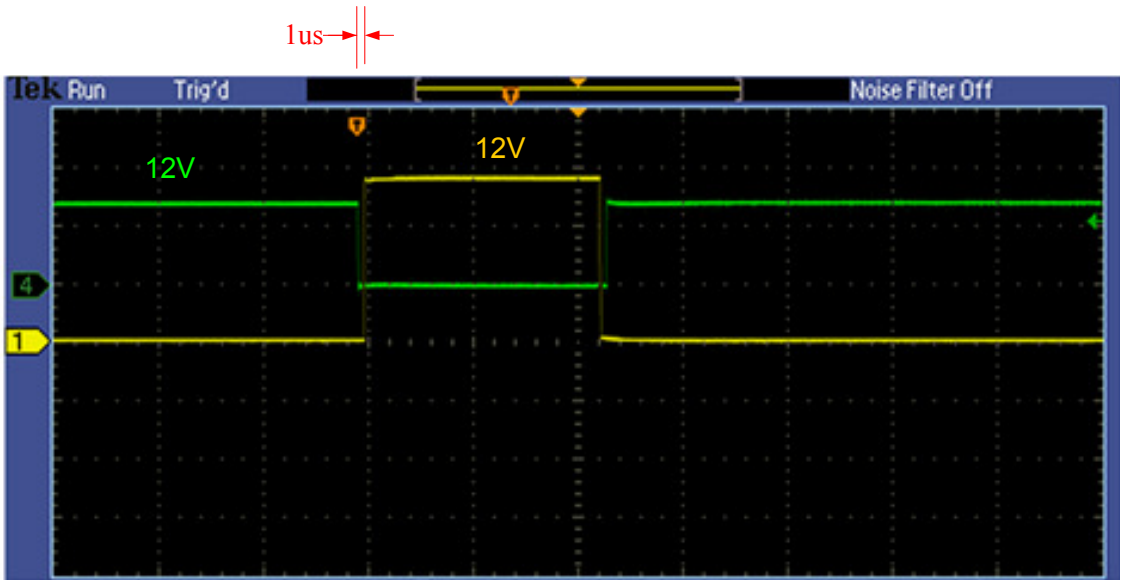


Figure 6-8: measured dead-time (green signal, gate signal of the upper switch; yellow signal, gate signal of the lower switch)

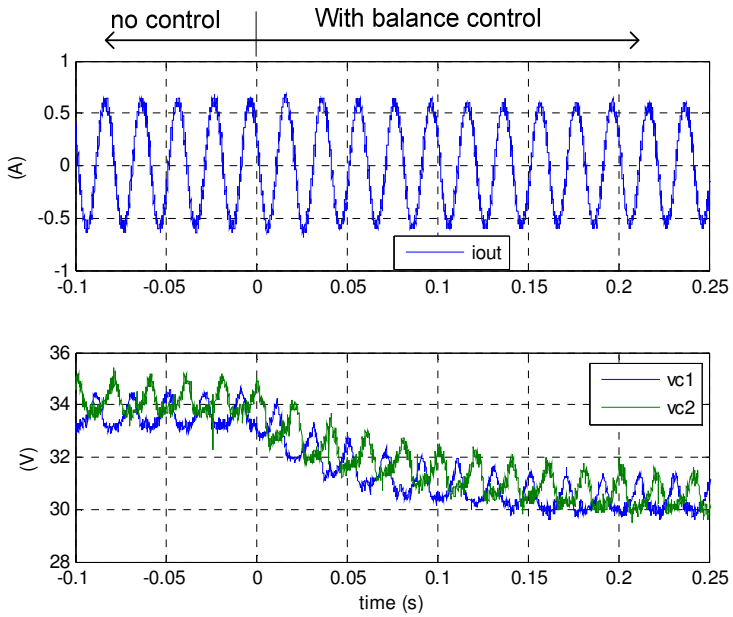


Figure 6-9: balance control test (N=1, f_{smp} =4kHz, buffer L=1.5mH per arm, DC link=±17V, load $R_L / L_L \approx$ 15ohm/9ohm, PF≈0.85 lagging)

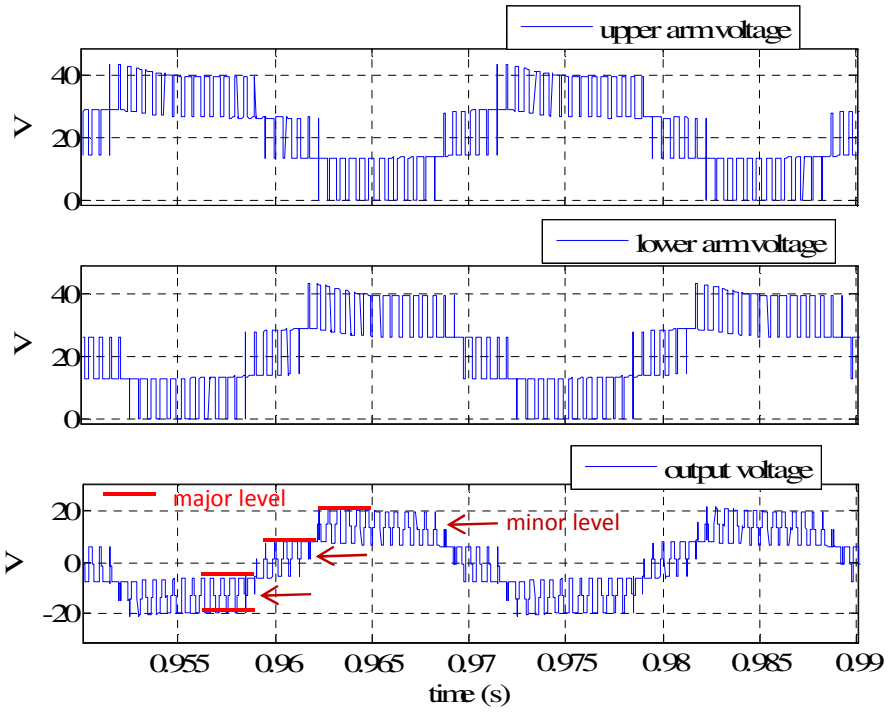
6.3.1.3 Full test with N=3

In order to mutually verify the simulation model (made in Matlab/Simulink+PLECS, see chapter 5) and the prototype (including the hardware and software), an additional simulation model was made for this chapter, which has the same converter level control (average voltage and difference current control) and the SM level control (individual balance control) with the model made in chapter 5, but has different high level control because of different load type (it has just a RL load while the simulation model made in chapter 5 was grid connected). The simulation and experimental results are shown in Figure 6-11 and Figure 6-10.

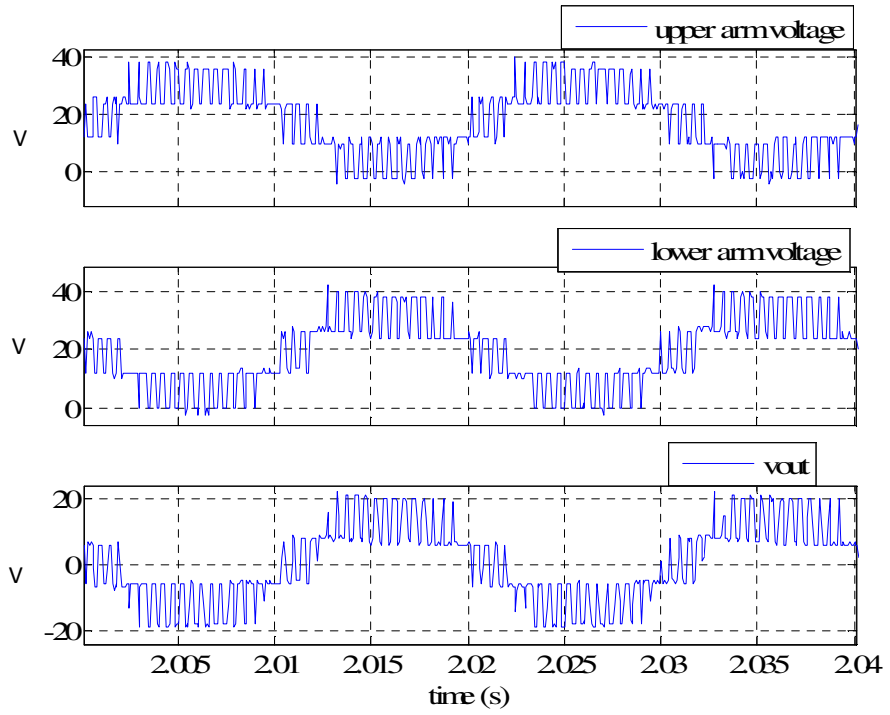
When N>1, it would be interesting to see the multilevel output voltage generated by the MMC. As shown in Figure 6-10, 4 voltage levels (major level) appear in the output voltage as expected (both the simulation and experiment results) because the number of the voltage level should be equal to N+1, where N is 3, the number of SMs per arm. It can be observed that, 3 minor levels also appear between the major levels due to the disturbance of the balance control. Actually, this phenomenon can be used to generate more voltage levels, i.e. 2N+1 levels, as documented in [31]. But the arm voltage sources (both the upper and lower arm, denoted as Vsp and Vsn, see Figure 2-3) always possess only the major voltage level as shown in Figure 6-10, i.e. they are not disturbed by the balance control. In order to test the effect of the designed voltage control, the DC

voltage reference is set to 40V (±20V) while the DC source voltage is kept to be 44V (±22V). As expected, the maximum/minimum output voltage level was regulated to be ±20V (Figure 6-10).

It can be seen from Figure 6-11 that the output current is a nice sinusoidal waveform due to the increased voltage level even though the power factor is increased to 0.92 from 0.85 of the above experiment (see Figure 6-9). It can be observed that the difference current has big ripples. A reason accounts for this might be that the difference current control is disturbed by the voltage balance control. Without balance control, the inserted SMs in the upper arm should be always the same as the bypassed SMs in the lower arm, thus the total inserted SMs in one leg is always equal to N. Hence, the voltage appears on the buffer inductors is almost constant and near zero, leading to very small ripples in the difference current. However, when the balance control is enabled, the total inserted SMs in one leg is no long always equal to N, leading to a big voltage impact on the buffer inductors and subsequently big current ripples in difference current. The simulation results and the experimental results are well matched except that the measured capacitor voltage (Vc1 and Vc4) was not ideally balanced as it was in the simulation due to the accuracy of the voltage sensors of the prototype (SM1 is the old version SM while SM4 is the new version SM which has a better accuracy than the old one).

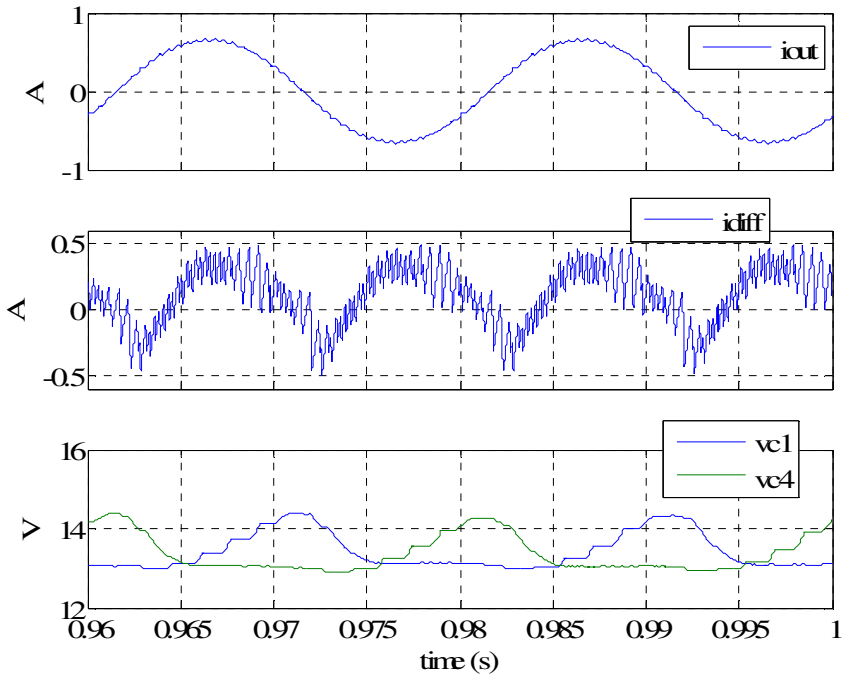


(a)

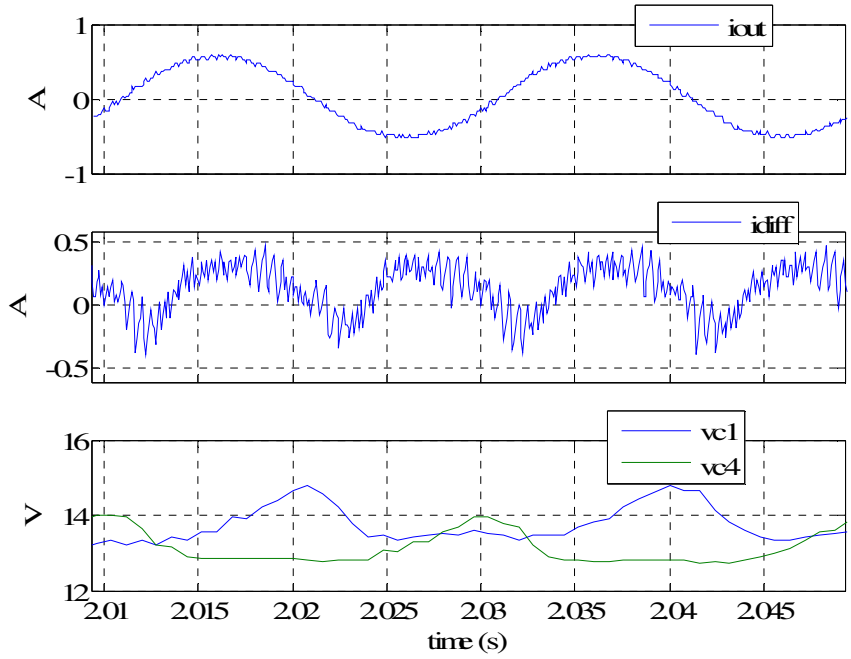


(b)

Figure 6-10: 4-level voltage (a)simulated results (b)experimental results(N=3, f_{smp} =4kHz, L=1.5mH, DC link=±22V, load $R_L / L_L \approx$ 21ohm/9ohm, PF ≈ 0.92 lagging)



(a)



(b)

Figure 6-11: current and capacitor voltage (a)simulated results (b)experimental results(N=3, f_{smp} =4kHz, L=1.5mH, DC link=$\pm$ 22V, load $R_L / L_L \approx$ 21ohm/9ohm, PF $\approx$ 0.92 lagging)

6.4 Summary

In this chapter, the hardware design (the improved version) and the software design for the prototype have been introduced. The prototype was fully tested and the results were described and analysed. By comparing the experimental results and the simulation results from the simulation model, which has the same parameters of the prototype, the prototype and the simulation model made in Matlab + PLECS were mutually verified.

Chapter 7 Conclusion and the future work

7.1 Conclusions

The work of this thesis is mainly focused on the following three aspects of the distributed control of MMC.

The first aspect is the communication technology for the distributed control. EtherCAT is found suitable for the distributed control of MMC due to its real-time communication ability, fast speed, high efficiency, redundancy and accurate distributed clock. SPI via optical fibers is found cheap and can fulfil partly the requirements of the distributed control. It has been used in the prototype and proved suitable for the distributed control when sub module number is not large and redundancy is not a requirement.

The second aspect is the modulation technology. PS-PWM is found suitable for the distributed control as this modulation method makes it possible that the individual balance control can be implemented on each SM. Resampled uniform PS-PWM is found having better performance than the other PS-PWM methods. In addition, updating the reference for all SMs in a synchronous manner is better than in an asynchronous manner. This also implies that synchronization is essential for the distributed modulation. The key technology for implementing resampled uniform PS-PWM is the resampling technology. In the thesis, a new method to realize the resampling technology is proposed, which is found having good performance and easy to realize with commercial available MCUs. Experiments have proved the feasibility of the proposed method to realize the resampling technique.

The last aspect is the distributed control methods. Architecture of a suitable distributed control system is described and its timing feature regarding communication delay is discussed. Design through analytical methods for the controllers of the distributed control is presented after deriving the corresponding plant models in frequency domain. The design has been generalized for MMC with almost arbitrary number of SMs. The design methods are also suitable for different applications of MMC since they are analytical methods. Simulations of MMC with almost arbitrary number (8~200) of SMs and experiments of MMC with small number of SMs have proved the concept of the distributed control of MMC for HVDC.

In addition, the hardware design and the software design of the downscaled prototype were presented with details.

7.2 Main contributions

- A new method to implement the resampled uniform PS-PWM method in microcontroller has been proposed, which uses high frequency saw-tooth carrier and two independent comparators, usually available in microcontrollers, to create the proper switching instances needed for the resampling modulation technique

- Analysis, frequency domain modelling and design of the distributed control of the MMC has been carried out
- Designed, built and tested the new master for the prototype; improved/fixed the old SMs and built two new SMs; designed, programmed and tested the software for the master and the SMs' MCUs

7.3 The future work

Due to the limited time for this project, some work, which is not covered in this thesis but might be interesting for the future project, will be discussed here.

For example, the communication protocol RS232, which has no clock signal as the SPI does, is very promising to increase further the communication speed. Of course, the EtherCAT protocol could be tested when the setup is ready, and the comparison between these communication protocols in terms of the communication performance should be of interest for the designer of the distributed control of MMC.

The analysis of the distributed control of MMC carried on in this thesis did not consider the dependency of the different control loops (the average control, the individual balance control and the high level control) in order to have simplified models of the plant and the controllers. Therefore a better insight into the control of MMC could be offered if the dependency is included in the analysis in the future work.

The prototype could be further improved with respect to the accuracy of the sensors. The current rating of the prototype is around 1A but the current sensors used for the prototype have the measuring range of 50 A (they were taken from some old setups to save money), leading to a poor accuracy in the range of the prototype rating. Therefore a better control performance might be able to be achieved if the accuracy of the current sensors is improved in the future work.

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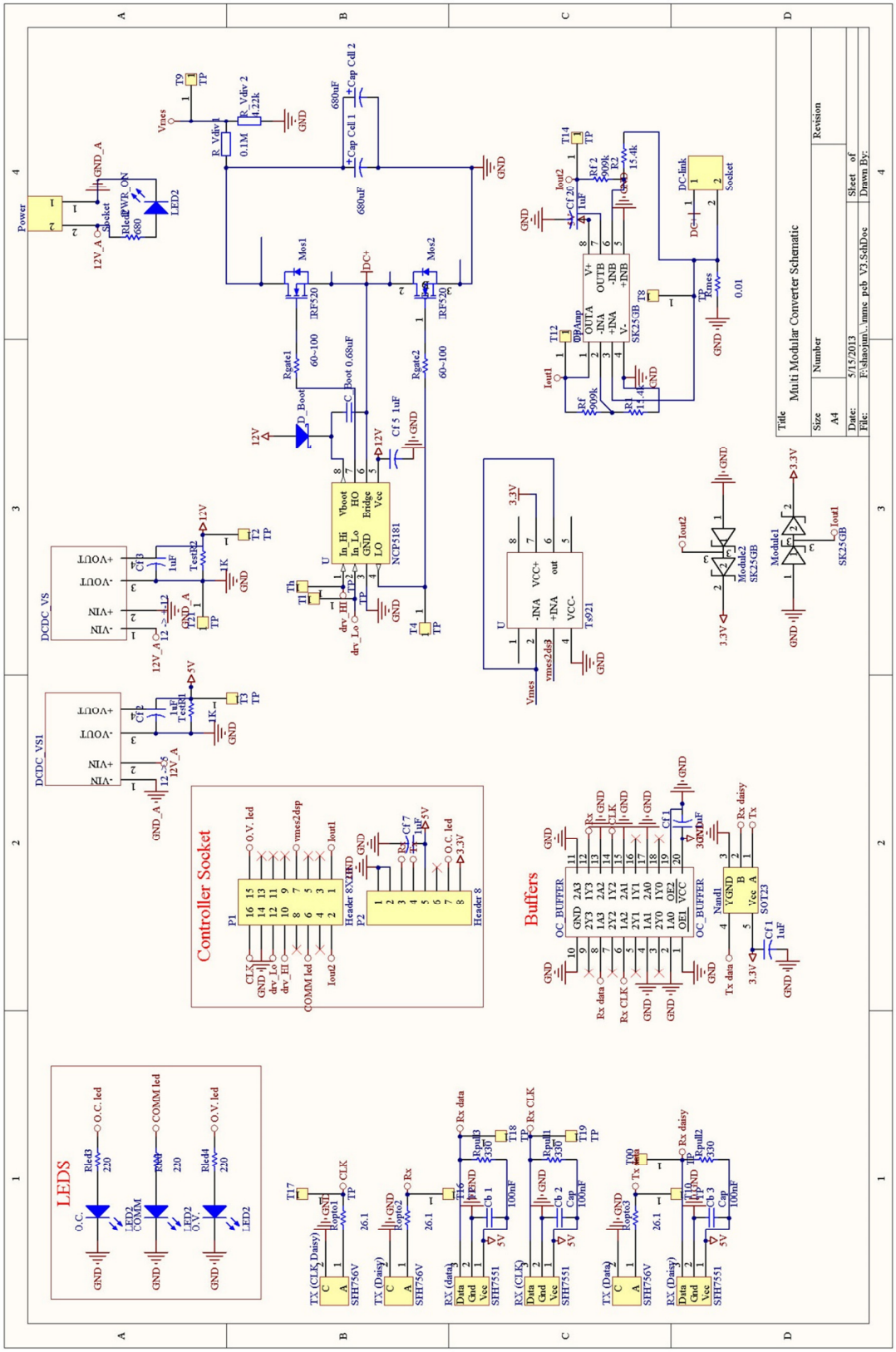
Appendix A: Schematic

A.1 Sub module

Bill of Material

Comment	Description	Designator	Quantity	Value
Res1	Resistor, current sensor	Rmes	1	0.01
Res2	Resistor, voltage divider	R_Vdiv 1	1	0.1M
Cap680	Capacitor	C_Boot	1	0.68uF
Res1	Resistor	TestR1, TestR2	2	1K
Cap2, Cap100	Capacitor	Cf 1, Cf 2, Cf 3, Cf 5, Cf 7, Cf 20	7	1uF
Res2	Resistor	R_Vdiv 2	1	4.22k
4R9	Resistor	Rgate1, Rgate2	2	60~100
Res1	Resistor	R1, R2	2	15.4k
Res1	Resistor	Ropto1, Ropto2, Ropto3	3	26.1
Cap	Capacitor	Cb 1, Cb 2, Cb 3	3	100nF
Res1	Resistor	Rled, Rled3, Rled4	3	220
Res1	Resistor	Rpull1, Rpull2, Rpull3	3	330
Res1	Resistor	Rled2	1	680
EKC00JU422F00	100V	Cap Cell 1, Cap Cell 2	2	680uF
Res1	Resistor	Rf, Rf 2	2	909k
12 -> +12	Halfbridge IGBT module	DCDC_VS	1	
12 -> 5	Halfbridge IGBT	DCDC_VS1	1	

	module			
D Schottky	Schottky Diode ,100V	D_Boot	1	
Header 8		P2	1	
Header 8X2H		P1	1	
IRF520,N-Channel 100V (D-S), 175'C	MOSFET	Mos1, Mos2	2	
LED2	Typical RED, GREEN	COMM, O.C., O.V., PWR_ON	4	
NCP5181	Half-Bridge Driver	DRV	1	
OC_BUFFER	SPI buffer	OC_BUFFER	1	
SFH551	Optic Receiver	RX (CLK), RX (Daisy), RX (data)	3	
SFH756V	Optic Transmitter Diode	TX (CLK Daisy), TX (Daisy), TX (Data)	3	
BAT54S ,DIODE, SCHOTTKY, 0.2A	voltage limiter	Module1, Module2	2	
LM358AN	buffer for current ADC	OpAmp	1	
Socket		DC-link, Power	2	
NC7SZ00P5XX	Nand Gate	Nand1	1	
TP	test point	T00, T2, T3, T4, T8, T9, T10, T12, T14, T16, T17, T18, T19, T21, Th, Tl	16	
Ts921	buffer for voltage ADC	U	1	


LEDS
Controller Socket
Buffers
Multi Modular Converter Schematic
Size
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Number
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NCP5181
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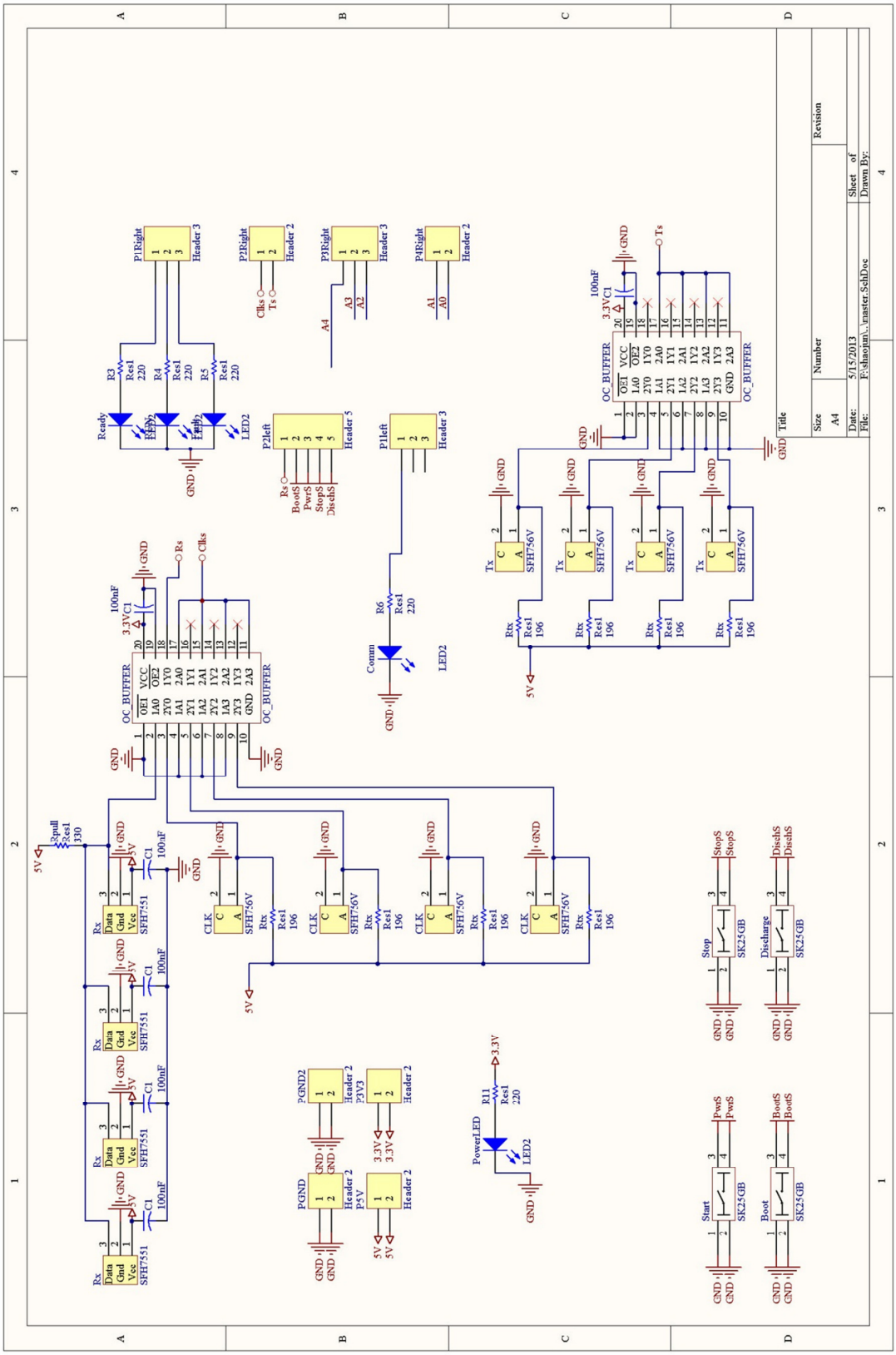
SFH756V
SFH7551

A.2 Master

Bill of Material

Comment	Description	Designator	Quantity	Value
Cap2	Capacitor	C1	10	100nF
Cap2	Capacitor	C1	5	33pF
Res1	Resistor	R3, R4, R5, R6, R11	5	220
Res1	Resistor	R5	4	1K
Res1	Resistor	R5	4	1K96
Res1	Resistor	R5	5	31.6
Res1	Resistor	R5	3	50
Res1	Resistor	R5	1	150
Res1	Resistor	R5	1	350
Res1	Resistor	Rpull	1	330
Res1	Resistor	Rtx	8	196
Header 2	Header, 2-Pin	DC Link meas input, input meas, P2Right, P3V3, P4Right, P5V, PGND, PGND2	8	
Header 3	Header, 3-Pin	+-15v, P1left, P1Right, P3Right	4	
Header 5	Header, 5-Pin	P2left	1	
IA55	IA55	I sensor 1, I sensor 2	2	
LED2	RED, GREEN	Comm, Fault, PowerLED, Ready, RUN	5	
LM7812	Vol. regulator	U1	1	
LM7912	Vol. regulator	U2	1	
OC_BUFFER	SPI buffers	OC_BUFFER, OC_BUFFER1	2	
SFH7551	Opto Receiver	Rx	4	

SFH756V	Opto Transmitter	CLK, Tx	8	
	buttons	Boot, Discharge, Start, Stop,	4	
LM25	voltage sensor	V Sensor 1	1	
Ts921	ADC buffers	U3, U4, U5, U6	4	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Number
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5/15/2013
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SFH7551
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SK25GB
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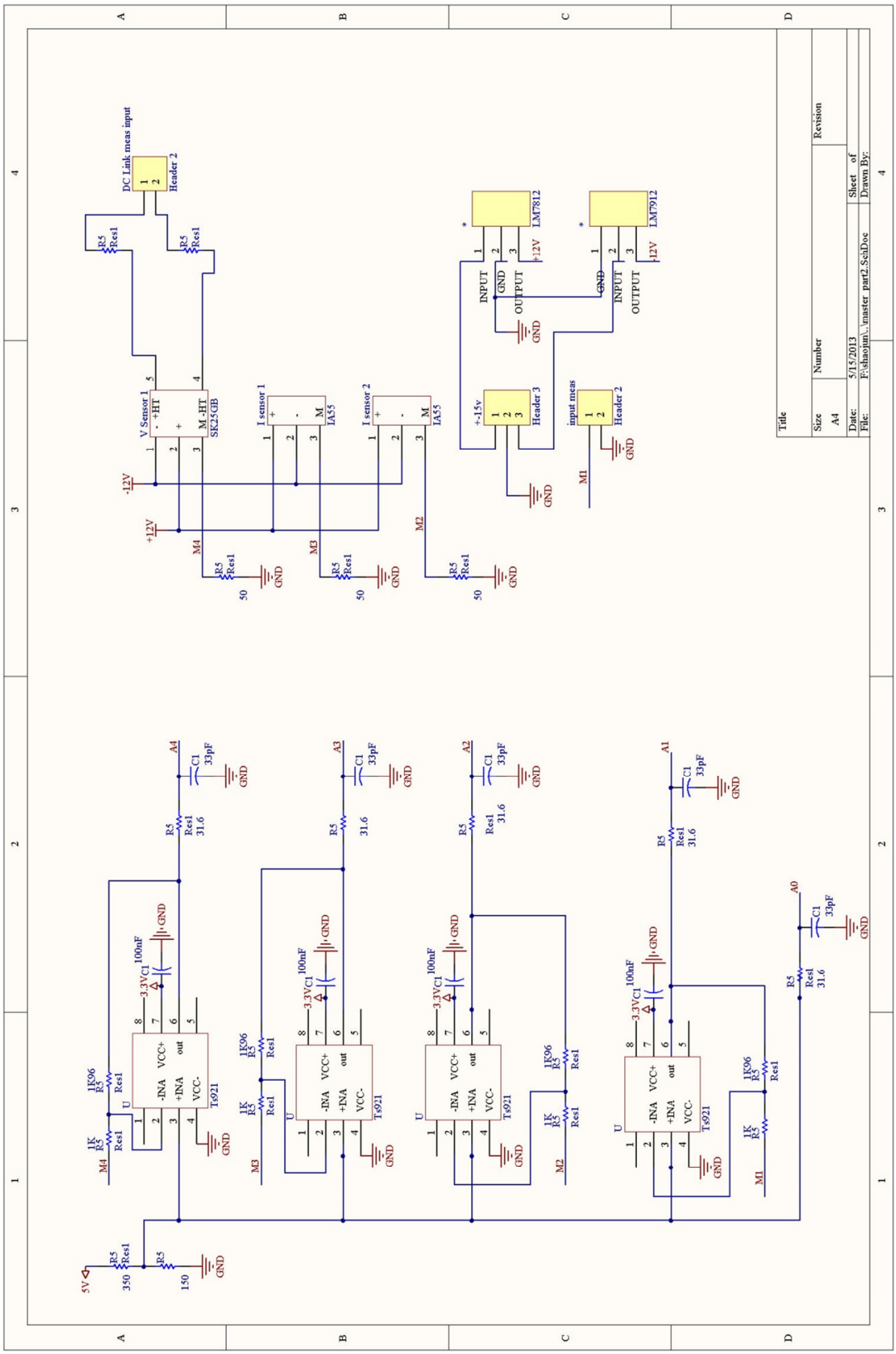
Header 3
Header 5
LED2
Res1
100nF
3.3V
5V
GND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Header 2
V Sensor 1
SK25GB
I sensor 1
I sensor 2
LA55
LM7812
LM7912
+-15v
Header 3
input meas
Header 2
-12V
+12V
5V
GND
R5
Res1
1K
1E96
100nF
33pF
3.3VC1
U
Ts921
-INA
+INA
VCC+
VCC-
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Appendix B: Published papers

Two papers that are based on the work documented in this thesis are listed as:

[1] Shaojun Huang, Remus Teodorescu and Laszlo Mathe, "Analysis of Communication Based Distributed Modulation and Control of MMC for HVDC", EPE, 2013 IEEE. Accepted.

[2] Shaojun Huang, Laszlo Mathe and Remus Teodorescu, "A New Method to Implement Resampled Uniform PWM Suitable for Distributed Control of Modular Multilevel Converter". IECON 2013, Submitted.