Bruce Jacob David Wang

University of Maryland

DRAM: Architectures, Interfaces, and Systems

A Tutorial

Bruce Jacob and David Wang

Electrical & Computer Engineering Dept. University of Maryland at College Park

http://www.ece.umd.edu/~blj/DRAM/



ISCA 2002

Bruce Jacob David Wang

University of Maryland

Outline

- Basics
- DRAM Evolution: Structural Path
- Advanced Basics
- DRAM Evolution: Interface Path
- Future Interface Trends & Research Areas
- Performance Modeling: Architectures, Systems, Embedded

Break at 10 a.m. — Stop us or starve

DRAM TUTORIAL	
ISCA 2002	Basics
Bruce Jacob David Wang	
University of Maryland	DRAM ORGANIZATION
	DRAM
	Storage element Column Decoder
	Word Line (capacitor) Data In/Out Sense Amps
	Bit Line Bit Lines
	Switching
	element

DRAM TUTORIAL			
ISCA 2002	Basics		
Bruce Jacob David Wang			
University of Maryland	BO2 I KAN2MI22ION		
			DRAM
			Column Decoder
	Dete		Sense Amno
		Buffers	Bit Lines
		Row Decoder	Memory Array

Bruce Jacob David Wang

University of Maryland

Basics

[PRECHARGE and] ROW ACCESS





	DRAM TUTORIAL
Basics	ISCA 2002
	Bruce Jacob David Wang
DAIAIRANSFER	University of Maryland



note: page mode enables overlap with CAS

Bruce Jacob David Wang

University of Maryland

Basics

BUSTRANSMISSION



ISCA 2002

Bruce Jacob David Wang

University of Maryland

Basics



A: Transaction request may be delayed in Queue B: Transaction request sent to Memory Controller C: Transaction converted to Command Sequences (may be queued)

D: Command/s Sent to DRAM

 E_1 : Requires only a **CAS** or

- E₂: Requires **RAS + CAS** or
- E_{3:} Requires **PRE + RAS + CAS**

F: Transaction sent back to CPU

"DRAM Latency" = A + B + C + D + E + F

DRAM TUTORIAL					
ISCA 2002	Basics				
Bruce Jacob David Wang					
University of Maryland	PHISICAL UKGANIZATION				
	x2 DRAM Column Decoder Data Sense Amps Buffers Bit Lines Bit Lines				

This is per bank ... Typical DRAMs have 2+ banks

Row Deco

÷

Memory

Array

x4 DRAM

Row Deco

÷

Memory

Array

x8 DRAM

Row Deco

:

Memory

Array

x2 DRAM

DRAM TUTORIAL ISCA 2002	Basics
Bruce Jacob David Wang	
University of Maryland	Read Timing for Conventional DRAM
	RAS Row Access CAS Data Transfer Address Column Address Address Q Valid Dataout Valid













Bruce Jacob David Wang

University of Maryland

DRAM Evolution





 $(\overline{RAS} + \overline{CAS} + \overline{OE} \dots == Command Bus)$

ISCA 2002

Bruce Jacob David Wang

University of Maryland

DRAM Evolution



Inter-Row Read Timing for ESDRAM

Regular CAS-2 SDRAM, R/R to same bank



ESDRAM, R/R to same bank



ISCA 2002

Bruce Jacob David Wang

University of Maryland

DRAM Evolution



Write-Around in ESDRAM

Regular CAS-2 SDRAM, R/W/R to same bank, rows 0/1/0



ESDRAM, R/W/R to same bank, rows 0/1/0



(can second READ be this aggressive?)





Bruce Jacob David Wang

University of Maryland

DRAM Evolution

Internal Structure of MoSys 1T-SRAM



ISCA 2002

Bruce Jacob David Wang

University of Maryland

DRAM Evolution

Comparison of Low-Latency DRAM Cores

DRAM Type	Data Bus Speed	Bus Width (per chip)	Peak BW (per Chip)	RAS–CAS (t _{RCD})	RAS–DQ (t _{RAC})
PC133 SDRAM	133	16	266 MB/s	15 ns	30 ns
VCDRAM	133	16	266 MB/s	30 ns	45 ns
FCRAM	200 * 2	16	800 MB/s	5 ns	22 ns
1T-SRAM	200	32	800 MB/s	—	10 ns
DDR 266	133 * 2	16	532 MB/s	20 ns	45 ns
DRDRAM	400 * 2	16	1.6 GB/s	22.5 ns	60 ns
RLDRAM	300 * 2	32	2.4 GB/s	???	25 ns

ISCA 2002

Bruce Jacob David Wang

University of Maryland

Outline

- Basics
- DRAM Evolution: Structural Path
- Advanced Basics
- Memory System Details (Lots)
- DRAM Evolution: Interface Path
- Future Interface Trends & Research Areas
- Performance Modeling:
 Architectures, Systems, Embedded

What Does This All Mean?



ISCA 2002

DRAM TUTORIAL

Bruce Jacob David Wang

University of Maryland



DRAM TUTORIAL Memory System Design ISCA 2002 Bruce Jacob David Wang Clock Network I/O Technology University of Maryland Chip Packaging Topology DRAM **DRAM** Chip Memory **Pin Count Architecture System** Address Mapping) **Access Protocol Row Buffer** Management

DRAM	TUTORIA	۱L
------	---------	----

Bruce Jacob David Wang

University of Maryland

DRAM Interfaces

The Digital Fantasy



Pretend that the world looks like this





Signal Propagation



Ideal Transmission Line

~ 0.66c = 20 cm/ns

PC Board + Module Connectors + Varying Electrical Loads

= Rather non-Ideal Transmission Line

DRAM TUTORIAL

ISCA 2002

Bruce Jacob David Wang

University of Maryland





ISCA 2002

Bruce Jacob David Wang

University of Maryland

Path Length Differential



High Frequency AND Wide Parallel Busses are Difficult to Implement

ISCA 2002

Bruce Jacob David Wang

University of Maryland

Subdividing Wide Busses



ISCA 2002

Bruce Jacob David Wang

University of Maryland

Why Subdivision Helps



Worst Case Skew must be Considered in System Timing






SDRAM Topology Example



DRAM TUTORIAL

ISCA 2002

Bruce Jacob David Wang

ISCA 2002

Bruce Jacob David Wang

University of Maryland

RDRAM Topology Example









ISCA 2002

Bruce Jacob David Wang

University of Maryland

I/O - Multi Level Logic



ISCA 2002

Bruce Jacob David Wang

University of Maryland

Packaging

DIP "good old da ys"



SOJ Small Outline J-lead



Features	Target Specification		
Package	FBGA	LQFP	
Speed	800MBp	550Mbps	
Vdd/Vddq	2.5V/2.5V (1.8V)		
Interface	SSTL_2		
Row Cycle Time t _{RC}	35ns		

TSOP Thin Small Outline Package

LQFP Low Profile Quad Flat Package







Memory Roadmap for Hynix NetDDR II

DRAM	TUTORIAL
------	----------

ISCA 2002

Bruce Jacob David Wang

University of Maryland

Access Protocol



ISCA 2002

Bruce Jacob David Wang

University of Maryland

Access Protocol (r/r)





ISCA 2002

Bruce Jacob David Wang

University of Maryland

Access Protocol (pipelines)



"Same" Latency, 2X pin frequency, Deeper Pipeline

When pin frequency increases, chips must either reduce "real latency",or support longer bursts, or

pipeline more commands.

ISCA 2002

Bruce Jacob David Wang

University of Maryland

Outline

- Basics
- DRAM Evolution: Structural Path
- Advanced Basics
- DRAM Evolution: Interface Path
- SDRAM, DDR SDRAM, RDRAM Memory System Comparisons
- Processor-Memory System Trends
- RLDRAM, FCRAM, DDR II Memory Systems Summary
- Future Interface Trends & Research Areas
- Performance Modeling: Architectures, Systems, Embedded

SDRAM System In Detail



ISCA 2002

DRAM TUTORIAL

Bruce Jacob David Wang

ISCA 2002

Bruce Jacob David Wang

University of Maryland

SDRAM Chip

133 MHz (7.5ns cycle time) Multiplexed Command/Address Bus Programmable Burst Length, 1,2,4 or 8 Quad Banks Internally Supply Voltage of 3.3V Low Latency, CAS = 2 , 3 LVTTL Signaling (0.8V to 2.0V)

(0 to 3.3V rail to rail.)

 	-
\cup	
256 MDit	F
	F
	F
51 nin	
J4 PIII	
•	
TEOD	
1306	
	F
	F
	F
	F
	F
	F

14 Pwr/Gnd 16 Data 15 Addr 7 Cmd 1 Clk 1 NC

Condition Specification	Cur.	Pwr
Operating (Active) Burst = Continous	300mA	1W
Operating (Active) Burst = 2	170mA	560mW
Standby (Active) All banks active	60mA	200mW
Standby (powerdown) All banks inactive	2mA	6.6mW

SDRAM Access Protocol (r/r)



Back-to-back Memory Read Accesses to Different Chips in SDRAM

Clock Cycles are still long enough to allow for pipelined back-to-back Reads

DRAM TUTORIAL

ISCA 2002

Bruce Jacob David Wang

SDRAM Access Protocol (w/r)



ISCA 2002

DRAM TUTORIAL

Bruce Jacob David Wang

ISCA 2002

Bruce Jacob David Wang

University of Maryland

SDRAM Access Protocol (w/r)



Read Following a Write Command to Same SDRAM Device

DDR SDRAM System



DRAM TUTORIAL

ISCA 2002

Bruce Jacob David Wang

ISCA 2002

Bruce Jacob David Wang

University of Maryland

DDR SDRAM Chip

133 MHz (7.5ns cycle time) Multiplexed Command/Address Bus Programmable Burst Lengths, 2, 4 or 8* Quad Banks Internally Supply Voltage of 2.5V*

Low Latency, CAS = 2 , 2.5, 3 *

SSTL-2 Signaling (Vref +/- 0.15V) (0 to 2.5V rail to rail)





ISCA 2002

Bruce Jacob David Wang

University of Maryland

DDR SDRAM Protocol (r/r)



Back-to-back Memory Read Accesses to Different Chips in DDR SDRAM

ISCA 2002

Bruce Jacob David Wang

University of Maryland

RDRAM System



ISCA 2002

Bruce Jacob David Wang

University of Maryland

Direct RDRAM Chip

400 MHz (2.5ns cycle time)	256 MBit
Separate Row-Col Command Busses	86 pin
Burst Length = 8*	FBGA
4/16/32 Banks Internally*	49 Pwr/Gnd*
Supply Voltage of 2.5V*	16 Data 8 Addr/Cmd
Low Latency, CAS = 4 to 6 full cycles*	4 Clk*
RSL Signaling (Vref +/- 0 2V)	6 CTL * 2 NC
(800 mV rail to rail)	1 Vref *



All packets are 8 (half) cycles in length, the protocol allows near 100% bandwidth utilization on all channels. (Addr/Cmd/Data)

DRAM TUTORIAL RDRAM Drawbacks ISCA 2002 Bruce Jacob David Wang High Frequency University of I/O Test and **RSL: Separate** Maryland Package Cost Power Plane 30% die cost for logic @ 64 Mbit node **Control Logic -**Active Decode **Row buffers** Single Chip Logic + Open Provides All Row Buffer. Data Bits for (High power Each Packet for "quiet" state) (Power)

Significant Cost Delta for First Generation

ISCA 2002

Bruce Jacob David Wang

University of Maryland

System Comparison

	SDRAM	DDR	RDRAM
Frequency (MHz)	133	133*2	400*2
Pin Count (Data Bus)	64	64	16
Pin Count (Controller)	102	101	33
Theoretical Bandwidth (MB/s)	1064	2128	1600
Theoretical Efficiency (data bits/cycle/pin)	0.63	0.63	0.48
Sustained BW (MB/s)*	655	986	1072
Sustained Efficiency* (data bits/cycle/pin)	0.39	0.29	0.32
RAS + CAS (t _{RAC}) (ns)	45 ~ 50	45 ~ 50	57 ~ 67
CAS Latency (ns)**	22 ~ 30	22 ~ 30	40 ~ 50

133 MHz P6 Chipset + SDRAM CAS Latency ~ 80 ns

*StreamAdd

**Load to use latency

DRAM TUTORIAL Differences of Philosophy ISCA 2002 Bruce Jacob David Wang SDRAM - Variants University of Maryland DRAM Controller Chips Complex Inexpensive Simple Interconnect Interface Logic **RDRAM - Variants** DRAM Controller Chips Simplified expensive Complex Interconnect Interface Logic **Complexity Moved to DRAM**

ISCA 2002

Bruce Jacob David Wang

University of Maryland

Technology Roadmap (ITRS)

	2004	2007	2010	2013	2016
Semi Generation (nm)	90	65	45	32	22
CPU MHz	3990	6740	12000	19000	29000
MLogicTransistors/ cm^2	77.2	154.3	309	617	1235
High Perf chip pin count	2263	3012	4009	5335	7100
High Performance chip cost (cents/pin)	1.88	1.61	1.68	1.44	1.22
Memory pin cost	0.34 -	0.27 -	0.22 -	0.19 -	0.19 -
(cents/pin)	1.39	0.84	0.34	0.39	0.33
Memory pin count	48-160	48-160	62-208	81-270	105-351

Trend:

Free Transistors & Costly Interconnects

ISCA 2002

Bruce Jacob David Wang

University of Maryland

Choices for Future



ISCA 2002

Bruce Jacob David Wang

University of Maryland

EV7 + RDRAM (Compaq/HP)

- RDRAM Memory (2 Controllers)
- Direct Connection to processor
- 75ns Load to use latency
- 12.8 GB/s Peak bandwidth
- 6 GB/s read or write bandwidth
- 2048 open pages (2 * 32 * 32)



ISCA 2002

Bruce Jacob David Wang

University of Maryland

What if EV7 Used DDR?

- Peak Bandwidth 12.8 GB/s
- 6 Channels of 133*2 MHz DDR SDRAM ==
- 6 Controllers of 6 64 bit wide channels, or
- 3 Controllers of 3 128 bit wide channels

System	EV7 + RDRAM	EV7 + 6 controller DDR SDRAM	EV7 + 3 controller DDR SDRAM
Latency	75 ns	~ 50 ns*	~ 50 ns*
Pin count	~265** + Pwr/Gnd	~ 600** + Pwr/Gnd	~ 600** + Pwr/Gnd
Controller Count	2	6***	3***
Open pages	2048	144	72

* page hit CAS + memory controller latency.

** including all signals, address, command, data, clock, not including ECC or parity *** 3 controller design is less bandwidth efficient.

ISCA 2002

Bruce Jacob David Wang

University of Maryland

What's Next?

- DDR II
- FCRAM
- RLDRAM
- RDRAM (Yellowstone etc)
- Kentron QBM

DDR II - DDR Next Gen



ISCA 2002

DRAM TUTORIAL

Bruce Jacob David Wang

ISCA 2002

Bruce Jacob David Wang

University of Maryland

DDR II - Continued

Posted Commands



ISCA 2002

Bruce Jacob David Wang

University of Maryland

FCRAM

Fast Cycle RAM (aka Network-DRAM)

Features	DDR SDRAM	FCRAM/Network-DRAM
Vdd, Vddq	2.5 +/- 0.2V	2.5 +/- 0.15
Electrical Interface	SSTL-2	SSTL-2
Clock Frequency	100~167 MHz	154~200 MHz
t _{RAC}	~40ns	22~26ns
t _{RC}	~60ns	25~30ns
# Banks	4	4
Burst Length	2,4,8	2,4
Write Latency	1 Clock	CASL -1

FCRAM/Network-DRAM looks like DDR+

ISCA 2002

Bruce Jacob David Wang

University of Maryland

FCRAM Continued



Faster t_{RC} allows Samsung to claim higher bus efficiency * Samsung Electronics, Denali MemCon 2002
ISCA 2002

Bruce Jacob David Wang

University of Maryland

RLDRAM

DRAM Type	Frequency	Bus Width (per chip)	Peak Bandwidth (per Chip)	Random Access Time (t _{RAC})	Row Cycle Time (t _{RC})
PC133 SDRAM	133	16	200 MB/s	45 ns	60 ns
DDR 266	133 * 2	16	532 MB/s	45 ns	60 ns
PC800 RDRAM	400 * 2	16	1.6 GB/s	60 ns	70 ns
FCRAM	200 * 2	16	0.8 GB/s	25 ns	25 ns
RLDRAM	300 * 2	32	2.4 GB/s	25 ns	25 ns

Comparable to FCRAM in latency Higher Frequency (No Connectors) non-Multiplexed Address (SRAM like)

DRAM TUTORIAL RLDRAM Continued **ISCA 2002 Bruce Jacob** High-end PC and Server **David Wang** University of Maryland Northbridge Processor Memory Controller 2.4GB/s X32 2.4GB/s X32 ??? RLDRAM is a great replacement to SRAM in L3 cache applications because of its high density, low power and low cost * Infineon Presentation, Denali MemCon 2002

ISCA 2002

Bruce Jacob David Wang

University of Maryland

RAMBUS Yellowstone

- Bi-Directional Differential Signals
- Ultra low 200mV p-p signal swings
- 8 data bits transferred per clock
- 400 MHz system clock
- 3.2 GHz effective data frequency
- Cheap 4 layer PCB
- Commodity packaging



DRAM TUTORIAL Kentron QBMTM **ISCA 2002 Bruce Jacob David Wang** DDR A DDR B DDR A DDR B DDR B DDR A DDR B DDR A University of Maryland SWITCH open open open Clock Controller DDR A d٩ DDR B Output $d_0 \times d_1 \times d_0 \times d_1 \times d_0 \times d_1 \times d_0 \times d_1$ "Wrapper Electr onics around DDR memory" Generates 4 data bits per cycle instead of 2. **Quad Band Memory**

ISCA 2002

Bruce Jacob David Wang

University of Maryland

A Different Perspective

Everything is bandwidth

- Row Cmd/Addr Bandwidth
- Col. Cmd/Addr Bandwidth
 - Write Data Bandwidth
 - Read Data Bandwidth

Latency and Bandwidth

Pin-bandwidth and

Pin-transition *Efficiency (bits/cycle/sec)

ISCA 2002

Bruce Jacob David Wang

University of Maryland

Research Areas: Topology



Unidirectional Topology:

- Write Packets sent on Command Bus
- Pins used for Command/Address/Data
- Further Increase of Logic on DRAM chips





Access Distribution for Temp Control Avoid Bank Conflicts Access Reordering for performance

Example: Bank Conflicts



More Banks per Chip == Performance == Logic Overhead

DRAM TUTORIAL

ISCA 2002

Bruce Jacob David Wang

ISCA 2002

Bruce Jacob David Wang

University of Maryland

Example: Access Reordering



Prec = Precharge (close page/evict data in row buffer/sense amp)

ISCA 2002

Bruce Jacob David Wang

University of Maryland

Outline

- Basics
- DRAM Evolution: Structural Path
- Advanced Basics
- DRAM Evolution: Interface Path
- Future Interface Trends & Research Areas
- Performance Modeling:
 Architectures, Systems, Embedded

ISCA 2002

Bruce Jacob David Wang

University of Maryland

Simulator Overview

CPU: SimpleScalar v3.0a

- 8-way out-of-order
- L1 cache: split 64K/64K, lockup free x32
- L2 cache: unified 1MB, lockup free x1
- L2 blocksize: 128 bytes

Main Memory: 8 64Mb DRAMs

- 100MHz/128-bit memory bus
- Optimistic open-page policy

Benchmarks: SPEC '95



Note: TRANSFER WIDTH of Direct Rambus Channel

- equals that of ganged FPM, EDO, etc.
- is 2x that of Rambus & SLDRAM

DRAM	TU	TOR	AL
------	----	-----	----

ISCA 2002

Bruce Jacob David Wang

University of Maryland

DRAM Configurations

Rambus & SLDRAM dual-channel:



ISCA 2002

Bruce Jacob David Wang

University of Maryland

First ... Refresh Matters



Assumes refresh of each bank every 64ms

ISCA 2002

Bruce Jacob David Wang

University of Maryland

Overhead: Memory vs. CPU

Total Execution Time in CPI — SDRAM



ISCA 2002

Bruce Jacob David Wang

University of Maryland

Definitions (var. on Burger, et al)

- t_{PROC} processor with perfect memory
- t_{REAL} realistic configuration
- t_{BW} CPU with wide memory paths
- t_{DRAM} time seen by DRAM system



ISCA 2002

Bruce Jacob David Wang

University of Maryland

Memory & CPU — PERL

Bandwidth-Enhancing Techniques I:



ISCA 2002

Bruce Jacob David Wang

University of Maryland

Memory & CPU — PERL

Bandwidth-Enhancing Techniques II:



Average Latency of DRAMs



ISCA 2002

DRAM TUTORIAL

Bruce Jacob David Wang

Average Latency of DRAMs



ISCA 2002

Bruce Jacob David Wang

DRAM TUTORIAL

DDR2 Study Results



DRAM TUTORIAL

ISCA 2002

Bruce Jacob David Wang

ISCA 2002

Bruce Jacob David Wang

University of Maryland

DDR2 Study Results

Perl Runtime



ISCA 2002

Bruce Jacob David Wang

University of Maryland

Row-Buffer Hit Rates



ISCA 2002

Bruce Jacob David Wang

University of Maryland

Row-Buffer Hit Rates

Hits vs. Depth in Victim-Row FIFO Buffer



ISCA 2002

Bruce Jacob David Wang

University of Maryland

Row Buffers as L2 Cache





DRAM	TUTORIA	۱L
------	---------	----

ISCA 2002

Bruce Jacob David Wang

University of Maryland

Cost-Performance

FPM, EDO, SDRAM, ESDRAM:

- Lower Latency => Wide/Fast Bus
- Increase Capacity => Decrease Latency
- Low System Cost

Rambus, Direct Rambus, SLDRAM:

- Lower Latency => Multiple Channels
- Increase Capacity => Increase Capacity
- High System Cost

However, 1 DRDRAM = Multiple SDRAM

ISCA 2002

Bruce Jacob David Wang

University of Maryland

Conclusions

100MHz/128-bit Bus is Current Bottleneck

 Solution: Fast Bus/es & MC on CPU (e.g. Alpha 21364, Emotion Engine, ...)

Current DRAMs Solving Bandwidth Problem (but not Latency Problem)

- Solution: New cores with on-chip SRAM (e.g. ESDRAM, VCDRAM, ...)
- Solution: New cores with smaller banks (e.g. MoSys "SRAM", FCRAM, ...)

Direct Rambus seems to scale best for future high-speed CPUs

ISCA 2002

Bruce Jacob David Wang

University of Maryland

Outline

- Basics
- DRAM Evolution: Structural Path
- Advanced Basics
- DRAM Evolution: Interface Path
- Future Interface Trends & Research Areas
- Performance Modeling:
 Architectures, Systems, Embedded

ISCA 2002

Bruce Jacob David Wang

University of Maryland

Motivation

Even when we restrict our focus ...

SYSTEM-LEVEL PARAMETERS

- Number of channels
- Channel latency
- Banks per channel
- Request-queue size
- Row-access
- DRAM precharge
- DRAM buffering
- Number of MSHRs

Width of channels Channel bandwidth Turnaround time Request reordering Column-access CAS-to-CAS latency L2 cache blocksize Bus protocol

Fully | **partially** | **not** independent (this study)

ISCA 2002

Bruce Jacob David Wang

University of Maryland

Motivation

... the design space is highly non-linear ...



ISCA 2002

Bruce Jacob David Wang

University of Maryland

Motivation

... and the cost of poor judgment is high.



ISCA 2002

Bruce Jacob David Wang

University of Maryland

System-Level Model

SDRAM Timing



ISCA 2002

Bruce Jacob David Wang

University of Maryland

System-Level Model

Timing diagrams are at the DRAM level ... not the system level



ISCA 2002

Bruce Jacob David Wang

University of Maryland

System-Level Model

Timing diagrams are at the DRAM level ... not the system level


ISCA 2002

Bruce Jacob David Wang

University of Maryland

Request Timing



Read/Write Request Shapes



ISCA 2002

DRAM TUTORIAL

Bruce Jacob David Wang





ISCA 2002

Bruce Jacob David Wang

University of Maryland

Burst Scheduling (Back-to-Back Read Requests)

128-Byte Bursts:

64-Byte Bursts:

32-Byte Bursts:

- Critical-burst-first
- Non-critical bursts are promoted
- Writes have lowest priority (tend back up in request queue ...)
- Tension between large & small bursts: amortization vs. faster time to data

New Bar-Chart Definition



- t_{PROC} CPU with 1-cycle L2 miss
- t_{REAL} realistic CPU/DRAM config
- t_{SYS} CPU with 1-cycle DRAM latency
- t_{DRAM} time seen by DRAM system

ISCA 2002

DRAM TUTORIAL

Bruce Jacob David Wang

ISCA 2002

Bruce Jacob David Wang

University of Maryland

System Overhead



ISCA 2002

Bruce Jacob David Wang

University of Maryland

System Overhead







DRAM TUTORIAL

ISCA 2002

Bruce Jacob David Wang



DRAM TUTORIAL

ISCA 2002

Bruce Jacob David Wang



DRAM TUTORIAL

ISCA 2002

Bruce Jacob David Wang



DRAM TUTORIAL

ISCA 2002

Bruce Jacob David Wang



ISCA 2002

DRAM TUTORIAL





DRAM TUTORIAL

ISCA 2002

Bruce Jacob David Wang

Burst Width Scales with Bus

Range of Burst-Widths Modeled



ISCA 2002

DRAM TUTORIAL

Bruce Jacob David Wang

Burst Width Scales with Bus

Range of Burst-Widths Modeled



Bruce Jacob

ISCA 2002

DRAM TUTORIAL

David Wang

Focus on 3.2 GB/s — MCF



DRAM TUTORIAL

ISCA 2002

Bruce Jacob David Wang









Focus on 3.2 GB/s — BZIP



ISCA 2002

DRAM TUTORIAL

Bruce Jacob David Wang



Queue Size & Reordering

BZIP: 1.6 GB/s (1 channel)



ISCA 2002

Bruce Jacob David Wang

DRAM TUTORIAL

DRAM	TUTORIA	۱L
------	---------	----

ISCA 2002

Bruce Jacob David Wang

University of Maryland

Conclusions

DESIGN SPACE is NON-LINEAR, COST of MISJUDGING is HIGH

CAREFUL TUNING YIELDS 30-40% GAIN

MORE CONCURRENCY == BETTER (but not at expense of LATENCY)

- Via Channels \rightarrow NOT w/ LARGE BURSTS
- Via Banks \rightarrow ALWAYS SAFE
- **Via Bursts** \rightarrow **DOESN'T PAY OFF**
- Via MSHRs \rightarrow NECESSARY

BURSTS AMORTIZE COST OF PRECHARGE

• Typical Systems: 32 bytes (even DDR2) \rightarrow THIS IS NOT ENOUGH

ISCA 2002

Bruce Jacob David Wang

University of Maryland

Outline

- Basics
- DRAM Evolution: Structural Path
- Advanced Basics
- DRAM Evolution: Interface Path
- Future Interface Trends & Research Areas
- Performance Modeling:
 Architectures, Systems, Embedded

ISCA 2002

Bruce Jacob David Wang

University of Maryland

Embedded DRAM Primer





ISCA 2002

Bruce Jacob David Wang

University of Maryland

Whither Embedded DRAM?

Microprocessor Report, August 1996: "[Five] Architects Look to Processors of Future"

- Two predict imminent merger of CPU and DRAM
- Another states we cannot keep cramming more data over the pins at faster rates (implication: embedded DRAM)
- A fourth wants gigantic on-chip L3 cache (perhaps DRAM L3 implementation?)

SO WHAT HAPPENED?

Embedded DRAM for DSPs

TRADITIONAL CACHE

MOTIVATION

TAGLESS SRAM



Bruce Jacob David Wang

ISCA 2002

University of Maryland

DRAM TUTORIAL

ISCA 2002

Bruce Jacob David Wang

University of Maryland

DSP Buffer Organization Used for Study



Bandwidth vs. Die-Area Trade-Off for DSP Performance

ISCA 2002

Bruce Jacob David Wang

University of Maryland

E-DRAM Performance

Embedded Networking Benchmark - Patricia 200MHz C6000 DSP : 50, 100, 200 MHz Memory



ISCA 2002

Bruce Jacob David Wang

University of Maryland

E-DRAM Performance

Embedded Networking Benchmark - Patricia 200MHz C6000 DSP : 50MHz Memory



E-DRAM Performance

Embedded Networking Benchmark - Patricia 200MHz C6000 DSP : 100MHz Memory



ISCA 2002

DRAM TUTORIAL

Bruce Jacob David Wang

E-DRAM Performance

Embedded Networking Benchmark - Patricia 200MHz C6000 DSP: 200MHz Memory



ISCA 2002

DRAM TUTORIAL

Bruce Jacob David Wang

ISCA 2002

Bruce Jacob David Wang

University of Maryland

Performance-Data Sources

"A Performance Study of Contemporary DRAM Architectures," *Proc. ISCA* '99. V. Cuppu, B. Jacob, B. Davis, and T. Mudge.

"Organizational Design Trade-Offs at the DRAM, Memory Bus, and Memory Controller Level: Initial Results," University of Maryland Technical Report UMD-SCA-TR-1999-2. V. Cuppu and B. Jacob.

"DDR2 and Low Latency Variants," *Memory Wall Workshop 2000*, in conjunction w/ ISCA '00. B. Davis, T. Mudge, V. Cuppu, and B. Jacob.

"Concurrency, Latency, or System Overhead: Which Has the Largest Impact on DRAM-System Performance?" *Proc. ISCA '01*. V. Cuppu and B. Jacob.

"Transparent Data-Memory Organizations for Digital Signal Processors," *Proc. CASES '01.* S. Srinivasan, V. Cuppu, and B. Jacob.

"High Performance DRAMs in Workstation Environments," *IEEE Transactions on Computers*, November 2001. V. Cuppu, B. Jacob, B. Davis, and T. Mudge.

Recent experiments by Sadagopan Srinivasan, Ph.D. student at University of Maryland.
ISCA 2002

Bruce Jacob David Wang

University of Maryland

Acknowledgments

The preceding work was supported in part by the following sources:

- NSF CAREER Award CCR-9983618
- NSF grant EIA-9806645
- NSF grant EIA-0000439
- DOD award AFOSR-F496200110374
- ... and by Compaq and IBM.

DRAM TUTORIAL

ISCA 2002

Bruce Jacob David Wang

University of Maryland

CONTACT INFO

Bruce Jacob

Electrical & Computer Engineering University of Maryland, College Park http://www.ece.umd.edu/~blj/ blj@eng.umd.edu

Dave Wang

Electrical & Computer Engineering University of Maryland, College Park http://www.wam.umd.edu/~davewang/ davewang@wam.umd.edu

