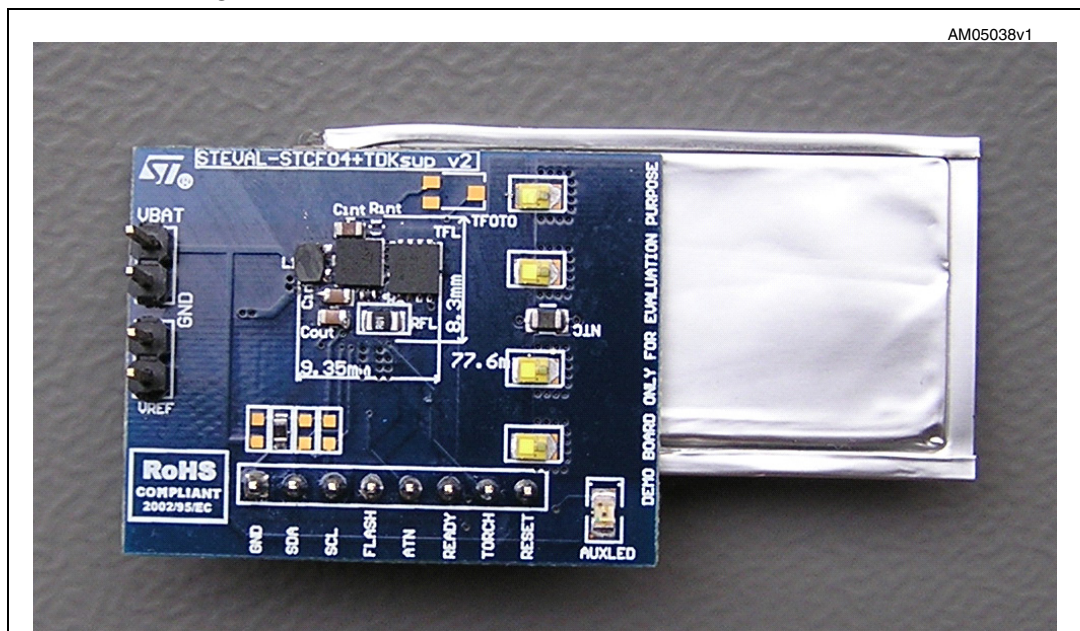


### Driver for double flash LED with I<sup>2</sup>C interface

#### Introduction

This application note is dedicated to the design of a flash LED driver using the STCF04 device, which is a buck-boost converter with an I<sup>2</sup>C interface dedicated to charging a super-capacitor. The schematic, functional description, recommendations for PCB layout, and external component selection are also covered. This device is designed for driving four LEDs. A detailed functional description can be found in [Figure 1](#) below.

**Figure 1. Picture of the demonstration board and the external transistor with TDK EDLC**



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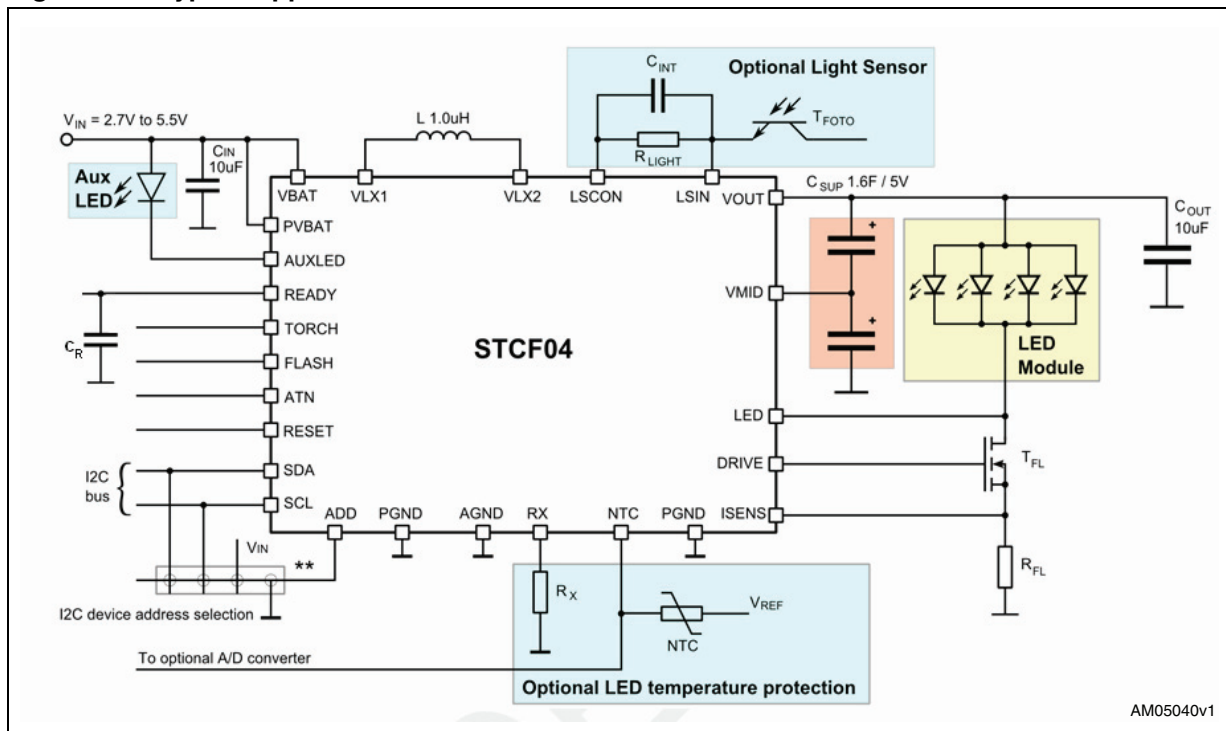
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# 1 Schematic description

The Flash LED driver STCF04 has a high operational frequency (1.8 MHz) which allows the use of small-sized external components.

## 1.1 Application schematic with external transistor

Figure 2. Typical application schematic



\*\* : Connect to  $V_I$ , GND, SDA, or SCL to choose one of the four different I<sup>2</sup>C slave addresses.

Blue rectangle: optional components to support auxiliary functions.

## 2 Selection of external components

### 2.1 Input and output capacitor selection

It is recommended to use ceramic capacitors with low ESR as input and output capacitors. It is recommended to use 10  $\mu\text{F}$  / 6.3 V as a minimum value for the input capacitor, and 10  $\mu\text{F}$  / 6.3 V as the optimal value for the output capacitor to achieve a good stability of the device, for a supply range varying from low input voltage (2.5 V) to the maximum ratings of output power.

*Note:* See recommended components in [Table 1](#).

### 2.2 Inductor selection

The STCF04 device works with the switching algorithm ILIM-ZCOM. It charges the inductor until the current crosses the threshold for the ILIM function and then it discharges the energy in the inductor to the output until it reaches the zero current value. Therefore, it is recommended to use a 1  $\mu\text{H}$  inductor as the minimum value, which guarantees a proper function with the used algorithm and speed of used components in the silicon design.

*Note:* See recommended components in [Table 1](#).

### 2.3 LED selection

All LEDs with a forward voltage range from 2.5 V to 4.5 V are compatible with the STCF04. The forward voltage spread of any selected LED must, however, lay within this range (2.5 V to 4.5 V). It is possible to set the level of the LED current in Flash mode and Torch mode by setting the dimming registers. The maximum level of the LED current in Flash mode can be set by changing the external Flash resistor.

*Note:* See recommended components in [Table 1](#).

### 2.4 NTC and RX resistor selection

The STCF04 requires a negative thermistor (NTC) for sensing the LED temperature, as well as an  $R_X$  resistor and an external voltage reference in order to use the NTC feature. Please refer to the typical application schematic in [Figure 2](#) for more details.

Once the NTC feature is activated, the internal switch connects the  $R_X$  resistor to the NTC, and this creates a voltage divider supplied by the external reference voltage connected to the NTC.

If the temperature of the NTC-thermistor rises due to the heat dissipated by the LED, the voltage on the NTC pin increases. When this voltage exceeds 0.56 V, the NTC\_W bit in the STATUS register is set to high, and the ATN pin is set to low to inform the microcontroller that the LED is becoming hot. The NTC\_W bit is cleared by reading the STATUS register.

If the voltage on the NTC pin rises further and exceeds 1.2 V, the NTC\_H bit in the STATUS register is set to high, and the ATN pin is set to low to inform the microcontroller that the LED is too hot and the device automatically goes to Ready mode to avoid damaging the LED.

This status is latched, until the microcontroller reads the STATUS register. Reading the STATUS register clears the NTC\_H bit.

The selection of the NTC and RX resistor values strongly depends on the power dissipated by the LED and all components surrounding the NTC-thermistor and on the cooling capabilities of each specific application. The RX and the NTC values in [Table 1](#) below work well in the demonstration board presented in this application note. A real application may require a different type of NTC-thermistor to achieve optimal thermal protection.

The procedure to activate the NTC-feature is described in [Section 5.2: Monitoring mode](#).

**Table 1. Recommended components**

Component	Manufacturer	Part number	Value	Size
L	Murata	LQM2HPN1R0MJC	1 $\mu$ H / 1.5 A	2.5 x 2.0 x 1.1 mm
	TDK	VLS252012T-1R0N1R7	1 $\mu$ H / 1.7 A	2.5 x 2.0 x 1.2 mm
CIN,COU	TDK	C1608X5R0J106MT	10 $\mu$ F / 6.3 V	0603
Rx	Rohm	MCR01MZPJ15K	15 k $\Omega$	0402
NTC	Murata	NCP21WF104J03RA	100 k $\Omega$	0805
CSUP	Murata	DME2W5R5K404M	400 mF / 5.5 V	20.5 x 18.5 x 3 mm
	TDK	EDLC152344	550 mF / 5.5 V	44 x 23 x 1.5 mm
		EDLC272020	500 mF / 5.5 V	20 x 20 x 2.7 mm
	CAP-xx	GS 2 19F	1.6 F / 5 V	40 x 17 mm
LED MODUL	Luxeon	4x LXCL-PWF4	White LED	0805
T <sub>FL</sub>	STMicroelectronics	STL8NH3LL	8 A / 12 m $\Omega$	3.3 x 3.3 x 0.9 mm
R <sub>FL</sub>	Tyco	TL2BR01FTE	0R01	1206
C <sub>INT</sub> <sup>(1)</sup>	TDK		10 $\mu$ F / 6.3 V	0402
R <sub>LIGHT</sub> <sup>(1)</sup>	Tyco			0402
T <sub>FOTO</sub> <sup>(1)</sup>	Vishay	TEMT6000		4 x 2 x 1 mm
AUXLED			Red LED	0603
C <sub>R</sub>			100 nF	0402

1. Optional components for the auxiliary light sensor feature.

## 3 PCB design

### 3.1 PCB design rules

The STCF04 is a powerful switching device working from low input voltages and high duty cycle, where the PCB must be designed in line with switched supplies design rules. The power tracks (or wires on the demonstration board) must be as short as possible and wide enough, because of the large currents involved. It is recommended to use a 3 to 4-layer PCB to obtain the best performance. All external components must be placed as close as possible to the STCF04. All high-energy switched loops should be as small as possible to reduce EMI. Most of the LEDs need efficient cooling, which may be done by using a dedicated copper area on the PCB. Please report to the selected LED's reference guide to design the heatsink. If a modification to any PCB layer is required, it is highly recommended to use an adequate number of vias. Place the NTC resistor as close as possible to the LED for good temperature sensing. Direct connection between GND and PGND is necessary in order to achieve correct output current value. No LED current should flow through this track! Vias connecting the STCF04 pins to the copper tracks (if used) must be 0.1 mm in diameter for the BGA version.

It is recommended to connect the LEDs close to the  $V_{OUT}$  and ILED pins for a stable operation margin. The impedance of this connection should be lower than  $0.4 \Omega$ .

### 3.2 PCB layout

#### 3.2.1 An example of the 3-layer PCB with the external transistor STL8NH3LL

Figure 3. Top layer

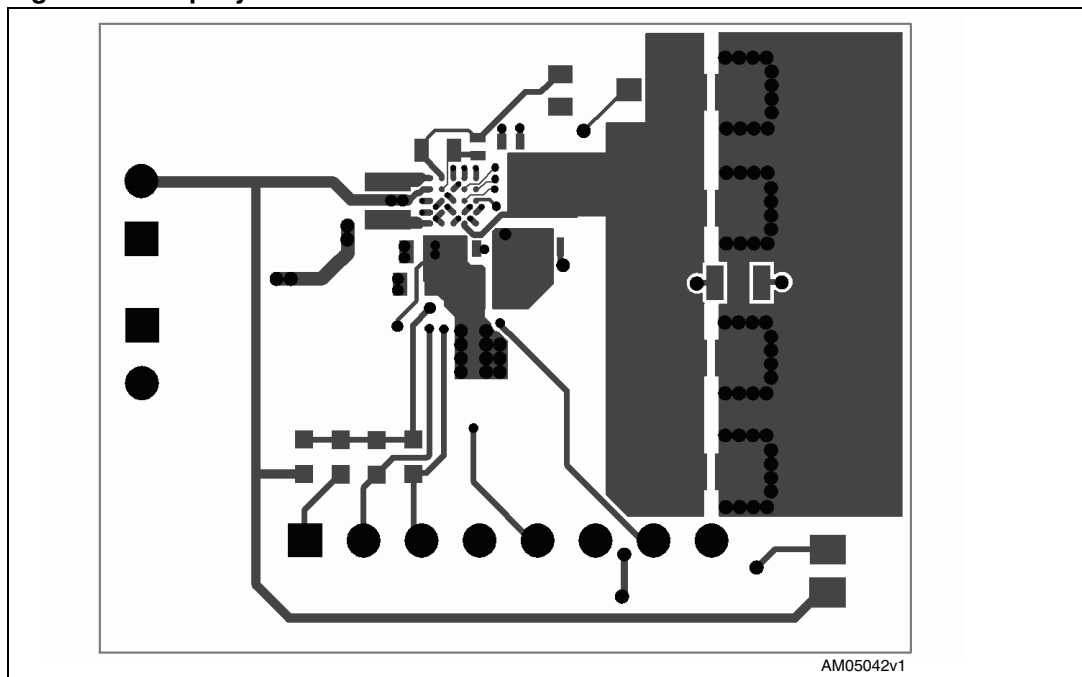


Figure 4. Middle layer 1

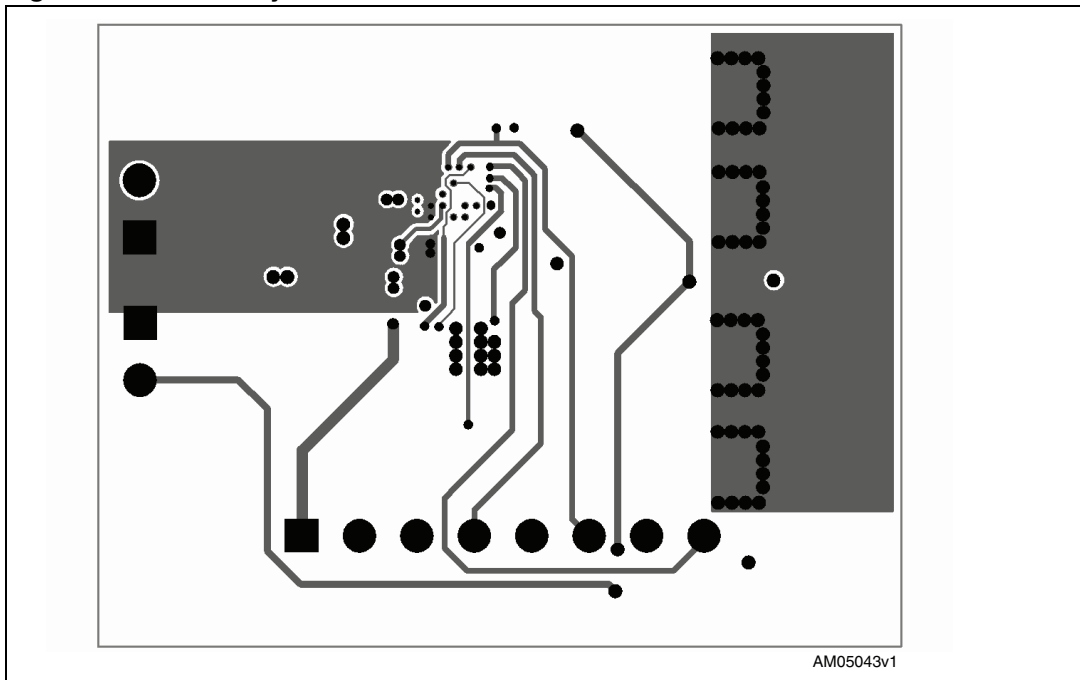


Figure 5. Bottom layer

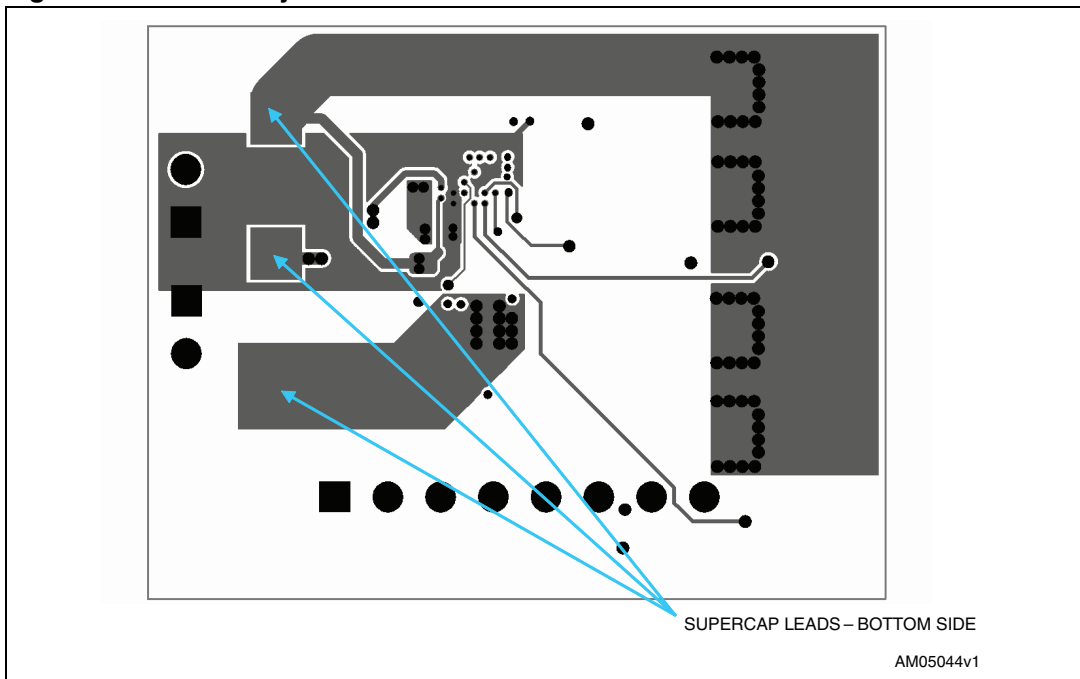
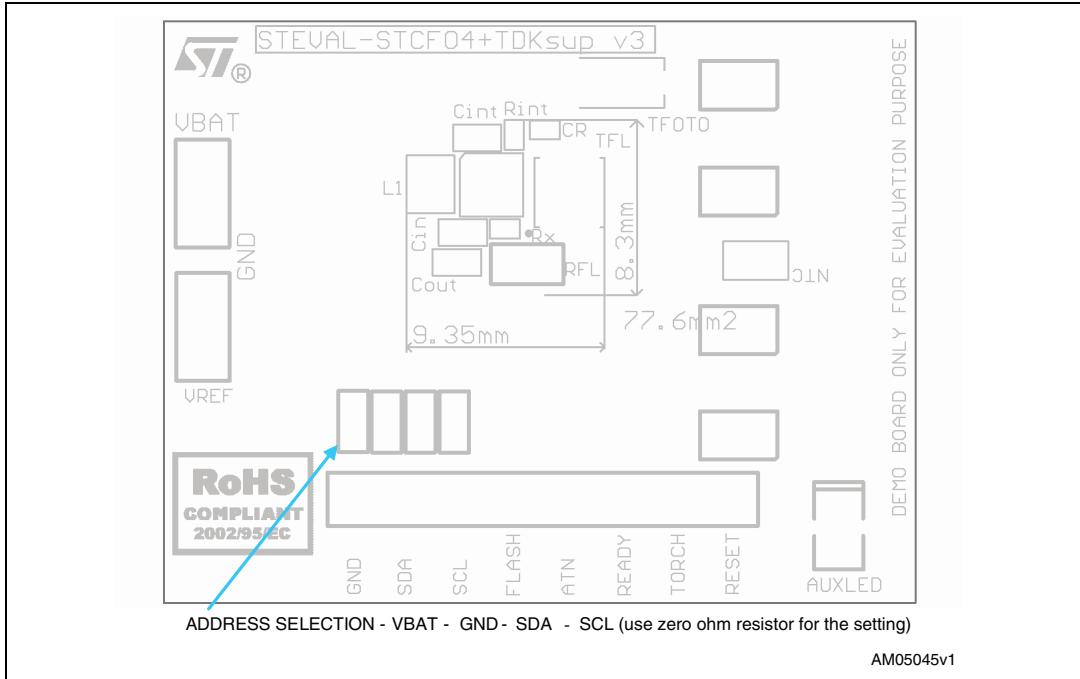




Figure 6. Top overlay



## 4 Internal registers

### 4.1 Accessing the internal registers

There are six internal registers in the STCF04 (which are the COMMAND, FLASH, AUX\_LED, STATUS, FEATURE, and TORCH registers). The STATUS register is read-only.

The COMMAND and FEATURE registers can be accessed in any operation mode. All the other registers can be accessed in any mode, except in Shutdown, Shutdown + NTC, and Monitoring mode. When the device enters Shutdown mode, the FLASH, AUX\_LED, STATUS, and TORCH registers are cleared. The COMMAND and FEATURE register values remain untouched when entering Shutdown mode, however reading their value gives 0 when the bit PWR\_ON = 0. [Table 2](#) shows the accessibility of each register in all operation modes.

In other words, whenever the PWR\_ON bit in the COMMAND register is set to zero, then only the COMMAND and FEATURE registers can be accessed. It is necessary to set the PWR\_ON bit to 1 to access all the registers.

**Table 2. Accessibility of internal registers**

Register	Address	Mode		Shutdown value	Power-ON reset value
		Shutdown and Monitoring	Idle, Charging, Flash, Torch and AUX LED		
COMMAND	00	Read / Write	Read / Write	Untouched	Cleared
FLASH	01	Inaccessible	Read / Write	Cleared	Cleared
AUX_LED	02	Inaccessible	Read / Write	Cleared	Cleared
STATUS	03	Inaccessible	Read only	Cleared	Cleared
FEATURE	04	Read / Write	Read / Write	Untouched	Cleared
TORCH	05	Inaccessible	Read / Write	Cleared	Cleared

## 5 Operation modes

### 5.1 Shutdown mode

Shutdown mode is entered after the Power-ON reset. This mode is mainly used to decrease the power consumption of the device. In this mode, only the I<sup>2</sup>C interface is live. The only action which can be performed in Shutdown mode is to access the COMMAND and FEATURE registers. Entering Shutdown mode by writing to the COMMAND register aborts any running operation and clears the values of the FLASH, AUX\_LED, STATUS, and TORCH registers. The COMMAND and FEATURE register values are not affected by entering Shutdown mode, but an attempt to read their value always gives 0 when the bit PWR\_ON = 0.

The following data must be written to the COMMAND register to enter Shutdown mode.

**Table 3. COMMAND register data for entering Shutdown mode**

CMD_REG	PWR_ON	FLASH_ON	TCH_ON	NTC_ON	TCHV_H	CHRG	MONTR	N/A
	0	x	x	x	x	x	0	0
	MSB							LSB

### 5.2 Monitoring mode

The super-capacitor voltage is monitored by a comparator in this mode. The comparator is the only analog circuit which is enabled and that is why the consumption of the STCF04 is minimized in this mode. Information about the super-capacitor voltage is given by the logic level on the READY pin. If the voltage is higher than  $V_{DCTHRESHOLD}$ , the READY pin is low. When the voltage falls by 200 mV below the  $V_{DCTHRESHOLD}$ , the READY pin goes high. The level of the  $V_{DCTHRESHOLD}$  can be set by the VDC\_0 and VDC\_1 bits in the FEATURE register.

**Table 4.  $V_{DCTHRESHOLD}$  voltage setup**

VDC_1	VDC_0	$V_{DCTHRESHOLD}$
0	0	4.5 V
0	1	5.0 V
1	0	5.5 V

Monitoring mode can be entered from Shutdown mode by setting the MONTR bit in the COMMAND register to 1.

**Table 5. COMMAND register data for entering Monitoring mode**

CMD_REG	PWR_ON	FLASH_ON	TCH_ON	NTC_ON	TCHV_H	CHRG	MONTR	N/A
	0	x	x	x	x	x	1	0
	MSB							LSB

Note: Monitoring mode can be also entered from Idle mode, but the device has a greater power consumption in this case.

### 5.3 Idle mode

Idle mode allows accessing of all the internal registers. The NTC feature can be activated in this mode and the temperature of the LED can be sensed by the A/D converter of the microcontroller. The following data must be written to the COMMAND register to enter Idle mode.

Table 6. COMMAND register data for entering Idle mode

CMD_REG	PWR_ON	FLASH_ON	TCH_ON	NTC_ON	TCHV_H	CHRG	MONTR	N/A
	1	0	0	x	x	0	0	0
	MSB							LSB

### 5.4 NTC feature

The NTC feature can be used in all modes. The NTC is activated automatically in the Flash and Torch mode regardless of the value of the NTC\_ON bit. NTC must be activated manually in all the other modes.

The NTC feature is activated by setting the NTC\_ON bit in the COMMAND register to 1.

Table 7. COMMAND register data for activation of the NTC feature

CMD_REG	PWR_ON	FLASH_ON	TCH_ON	NTC_ON	TCHV_H	CHRG	MONTR	N/A
	x	x	x	1	x	x	x	0
	MSB							LSB

As soon as the NTC feature is activated, the internal switch connects the NTC resistor to the R<sub>X</sub> resistor, thereby creating a voltage divider. The voltage on this divider can be, if desired, monitored by the A/D converter of the microcontroller. An external voltage reference must be connected to the NTC to use this feature. The bits NTC\_W and NTC\_H of the STATUS register are not properly set if there is no external reference voltage connected to the NTC.

If the NTC feature is not going to be used, neither the negative thermistor nor the external reference needs to be connected. In this case, it is recommended to ground the RX pin. As the NTC feature is automatically activated during Flash and Torch mode, leaving the RX pin floating could lead to unwanted interruptions of the light due to non-defined voltage on the RX pin.

If the NTC feature is activated and the PWR\_ON bit in the COMMAND register is zero, the bits NTC\_W and NTC\_H in the STATUS register are not set properly, because the comparators which determine their values are not enabled in this case. But it is still possible to measure the voltage on the NTC pin through the A/D converter.

Table 8 summarizes the NTC feature possibilities.

**Table 8. NTC feature possibilities**

Operation mode	Way of activation	Voltage on the Rx-NTC divider	NTC_W, NTC_H bits
Shutdown	Manual	Available	Not set
Monitoring	Manual	Available	Not set
Idle	Manual	Available	Set
Charging	Manual	Available	Set
Flash	Automatic	Available	Set
Torch	Automatic	Available	Set
Aux LED	Manual	Available	Set

### 5.5 Torch mode

This mode is intended to be used for low light intensities. The LED current in Torch mode can be adjusted in a range from 15 mA up to 320 mA.

Torch mode is activated by writing the following data to the COMMAND register.

**Table 9. COMMAND register data for entering Torch mode**

CMD_REG	PWR_ON	FLASH_ON	TCH_ON	NTC_ON	TCHV_H	CHRG	MONTR	N/A
	1	0	1	x	x	x	x	0
	MSB							LSB

The TORCH DIMMING register value (TDIM) must also be set, unless it has already been set during a previous operation. If the TDIM register is not set, then the default output current value is at the minimum.

It is also possible to set the safety timeout for Torch mode through the TTRCH1 and TTRCH0 bits.

If Torch mode was terminated by entering Ready or Flash mode, it can be restarted again by writing the corresponding data to the COMMAND register only, because entering any of the Ready and Flash modes does not influence the TDIM value. If the Torch mode was terminated by entering Shutdown mode, then the TDIM value must be set again during restart of Torch mode, because entering Shutdown mode clears the TDIM and TTRCH values.

As soon as Torch mode is activated, the NTC feature is automatically activated too in order to protect the LED against overheating. The NTC feature is activated even if the NTC\_ON bit in the COMMAND register is set to zero.

### 5.6 Flash mode

This mode is intended to be used for high light intensities. The LED current in Flash mode can be adjusted up to 12 A with the input voltage ranging from 2.7 V up to 5.5 V with recommended external components.

**Table 10. COMMAND register data for entering Flash mode**

CMD_REG	PWR_ON	FLASH_ON	TCH_ON	NTC_ON	TCHV_H	CHRG	MONTR	N/A
	1	1	0	x	x	x	x	0
	MSB							LSB

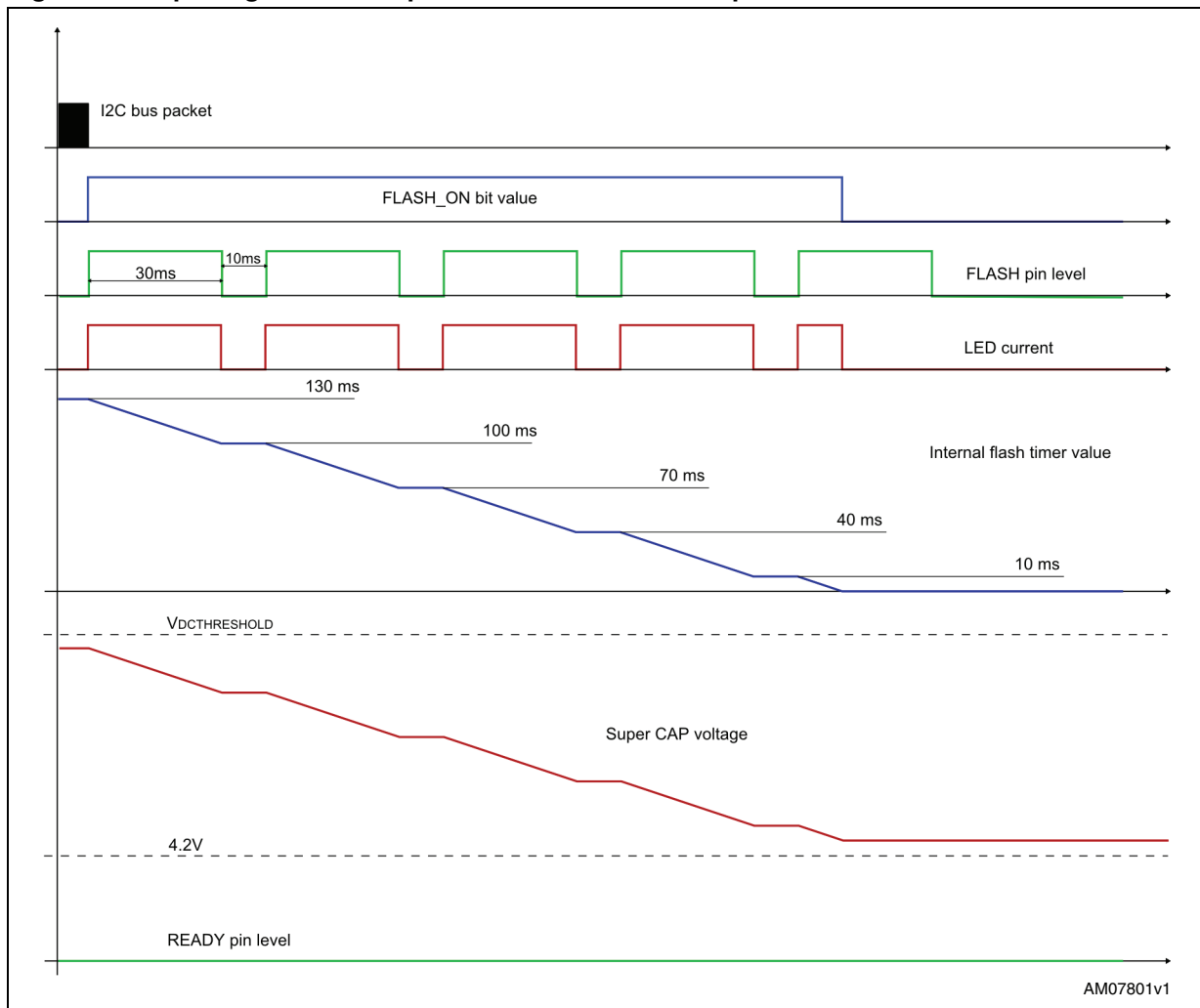
The FLASH register value must also be set.

The activation of Flash mode requires the FLASH pin to be high. Flash mode is active only when the FLASH\_ON bit in the COMMAND register is set to 1 and the FLASH pin is high. This gives the user the possibility to choose between a soft and a hard triggering of the Flash mode.

Soft triggering is done by writing data to the internal registers only, while the FLASH pin is permanently kept high, e.g. by connecting it to V<sub>BAT</sub>. This saves one pin of the microcontroller, which can be used for a different purpose, but this way of triggering is less accurate than the hard one. The second disadvantage of this solution is that the FLASH duration can only be set in discrete steps of the internal timer.

Hard triggering of the Flash mode requires the microcontroller to manage the FLASH pin. The COMMAND and the FLASH registers are loaded with data before the FLASH pin is set to high. This allows the user to avoid the I<sup>2</sup>C bus latency. Flash mode then starts as soon as the FLASH pin is set to high. It takes typically about 0.3 ms to ramp up the LED current to the adjusted value. When the FLASH pin is kept high long enough, the internal timer reaches zero and the Flash mode is over. As soon as the FLASH is timed out, the ATN pin is pulled down for 11 μs to inform the microcontroller that the STATUS register was updated and that the FLASH is over. If the FLASH pin is set to low before the internal timer reaches zero, Flash mode is interrupted and can be restarted by setting the FLASH pin to high again. The internal timer is stopped while the FLASH pin is low. This means that the user can split the FLASH into several pulses of a total length equal to the FTIM value. *Figure 7* shows the case for FTIM = 17 (130 ms FLASH time). The cumulative time when the FLASH pin is high is 150 ms (5 pulses 30 ms long), but the last FLASH pulse is only 10 ms long. The reason is that the internal FLASH timer reaches zero and the FLASH\_ON bit is set to 0.

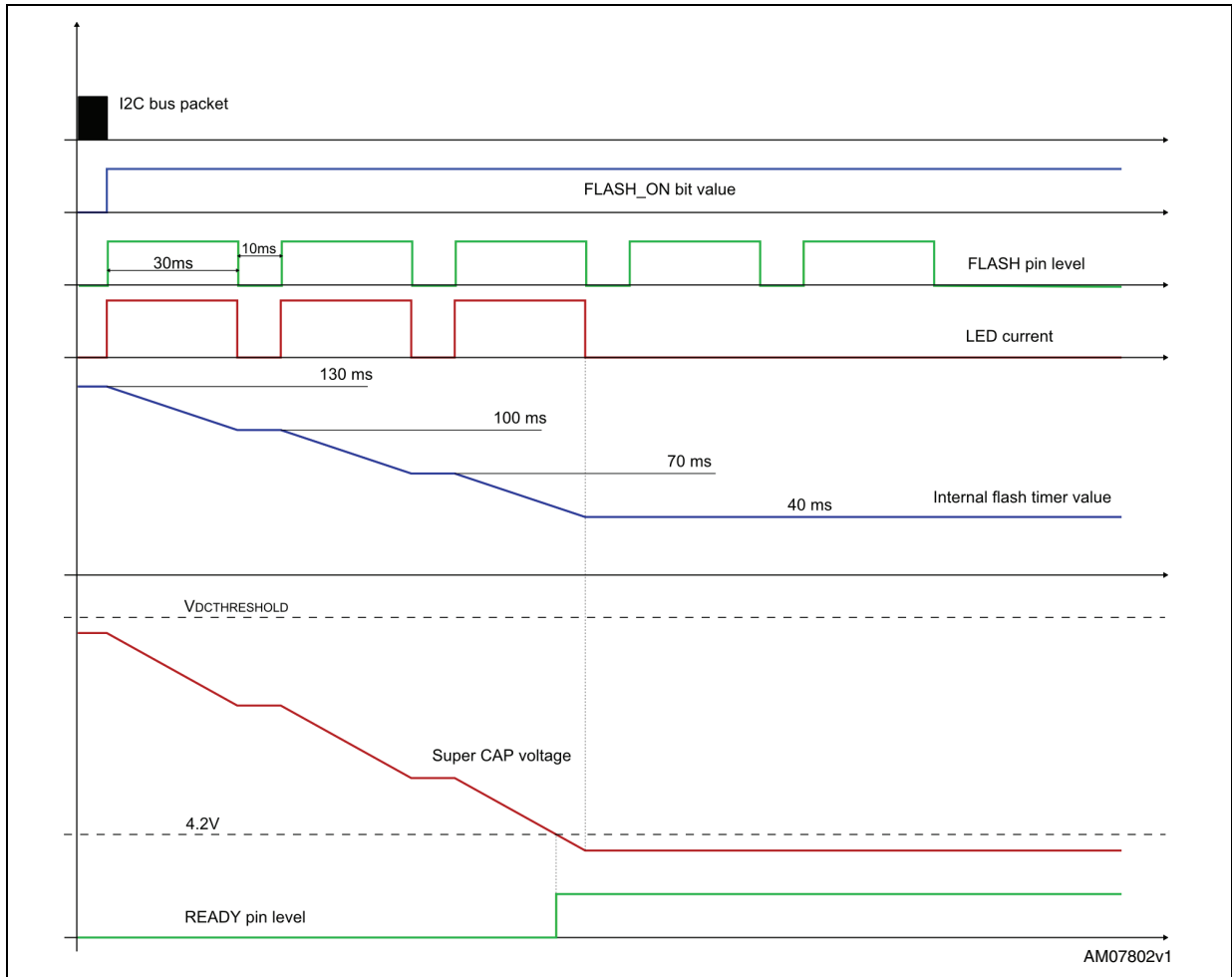
Figure 7. Splitting the FLASH pulse into several shorter pulses



Hard triggering therefore allows a smooth setting of the FLASH duration. The resolution is about 8.8  $\mu$ s. The minimum FLASH duration is limited by the ramp-up time of the LED current and the maximum is limited by the FTIM value.

*Note:* When performing multiple flashes, it is necessary to make sure that the super-capacitor contains enough energy to cover all the required flashes in the burst. If the super-capacitor voltage falls below 4.2 V during the burst, the internal FLASH timer is stopped and the device waits until the super-capacitor is recharged to the  $V_{DCTHRESHOLD}$  value. Then the burst can continue. See [Figure 8](#) for more details.

Figure 8. Burst of flashes with insufficient energy in the super-capacitor





## 6 The STATUS register and the ATN pin

**Table 11. STATUS register bits**

Bit name	N/A	F_RUN	FL_R	NTC_W	NTC_H	OT_F	FL_OVR	LTH
	MSB							LSB

A detailed description of each bit is given in the STCF04 datasheet.

**Table 12. Effect of the STATUS register bits on the operation of the device**

Bit name	F_RUN STAT_REG	FL_R STAT_REG	NTC_W STAT_REG	NTC_H STAT_REG	OT_F STAT_REG	FL_OVR STAT_REG	LTH STAT_REG
Default value	0	0	0	0	0	0	0
Latched <sup>(1)</sup>	NO	NO	YES	YES	YES	NO	NO
Forces Ready mode when set	NO	NO	NO	YES	YES	NO	NO
Sets ATN LOW when set	NO	YES	YES	YES	YES	YES	NO

1. YES means that the bit is set by internal signals and is reset to its default value by an I<sup>2</sup>C read operation of STAT\_REG.  
NO means that the bit is set and reset by internal signals in real-time.

When the STATUS register is latched, reading and writing to the registers is still possible, but the bits FLASH\_ON and TCH\_ON in the COMMAND register and AUXL register cannot be changed until the device is unlatched. It is necessary to read the STATUS register to unlatch the device.

The ATN pin is also pulled down when the internal timer reaches zero in Flash mode. In this case the ATN pin is pulled down for 11  $\mu$ s only. It is recommended to connect the ATN pin to the interrupt input of the microcontroller. If it is not connected to the interrupt input, the ATN pin should be polled fast enough so as not to miss the 11  $\mu$ s pulse; e.g., by a programming loop which is entered after starting Flash mode. This loop runs until the ATN pin gets low. It is recommended to make a timeout of such a loop.

The ATN pin is an open drain output and an external pull-up resistor should be connected to it. The ATN pin is capable of sinking a maximum 3 mA current. This is why the minimum value of the pull-up resistor connected to it should not be lower than 1.8 k $\Omega$ .

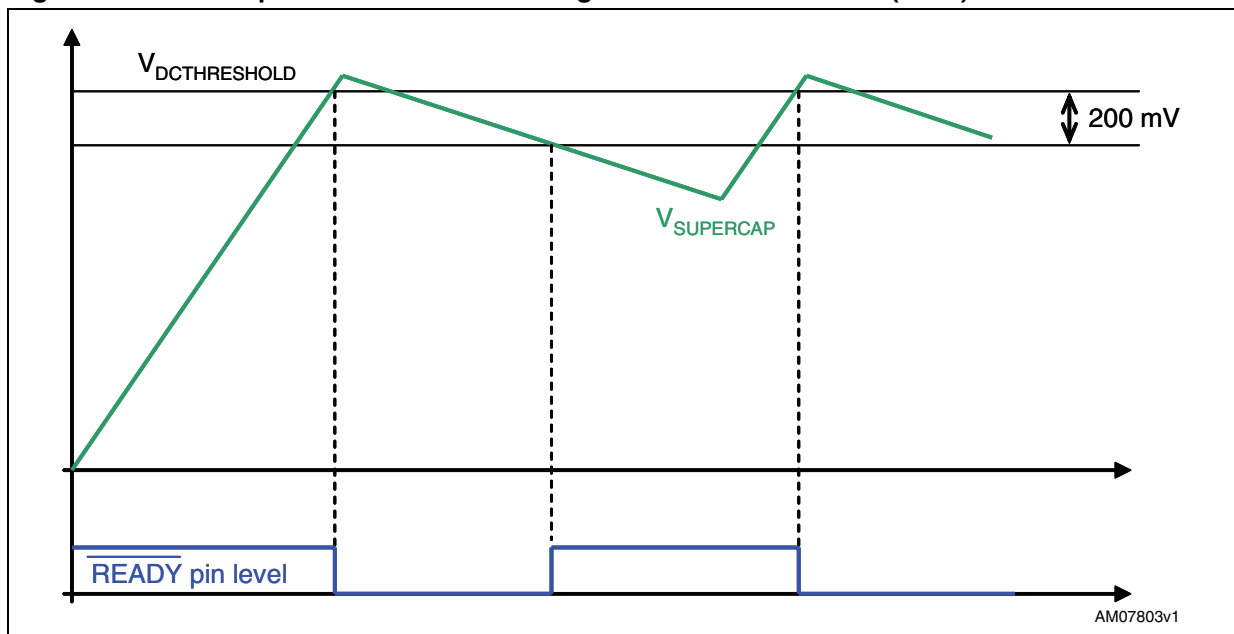
## 7 READY pin

It is an open drain output, which provides information about the voltage on the super-capacitor. The signal is active low. The behavior of this pin depends on the mode of operation.

### 7.1 Function of the READY pin in Monitoring mode and Torch mode (fixed)

The threshold for the transition from high to low level is defined by the  $V_{DCTHRESHOLD}$  voltage in this case. This voltage is set by the VDC\_0 and VDC\_1 bits in the FEATURE register. The comparator works with a fixed hysteresis of 200 mV in this case, so the transition from low to high level occurs when the voltage of the super-capacitor falls to  $V_{DCTHRESHOLD} - 0.2$  V.

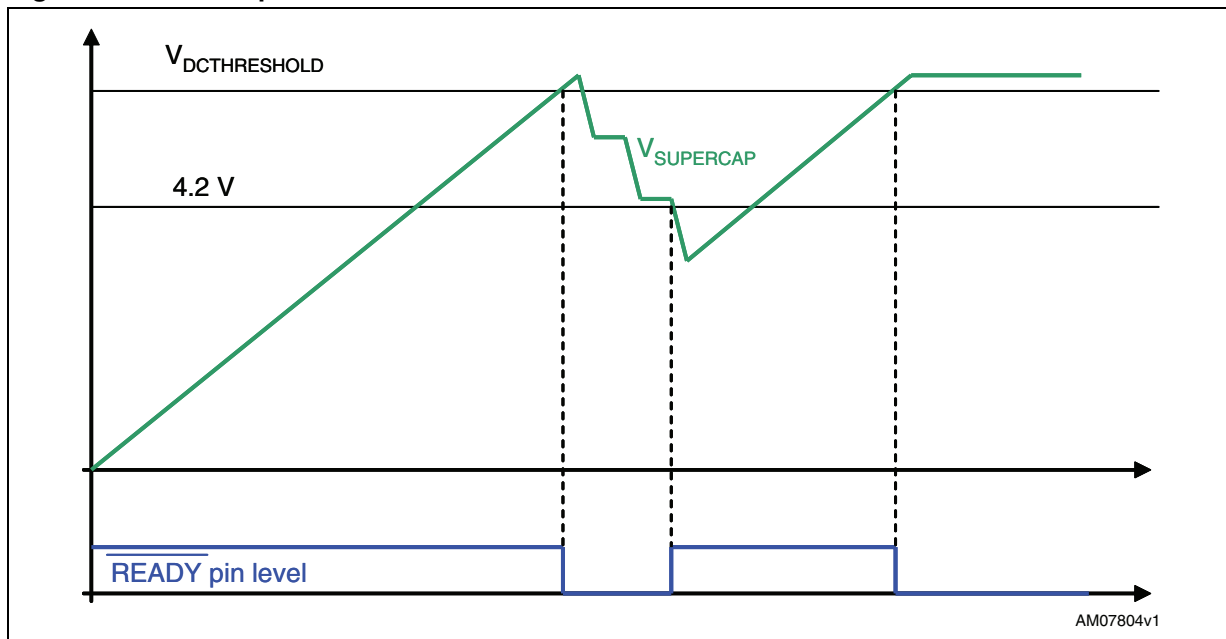
Figure 9. READY pin behavior in Monitoring mode and Torch mode (fixed)



### 7.2 Function of the READY pin in Flash mode

The threshold for the transition from high to low level is defined by the  $V_{DCTHRESHOLD}$  voltage again. Unlike Monitoring mode, the transition from low to high occurs when the super-capacitor voltage falls to 4.2 V. This threshold is fixed and cannot be changed by any settings of the registers.

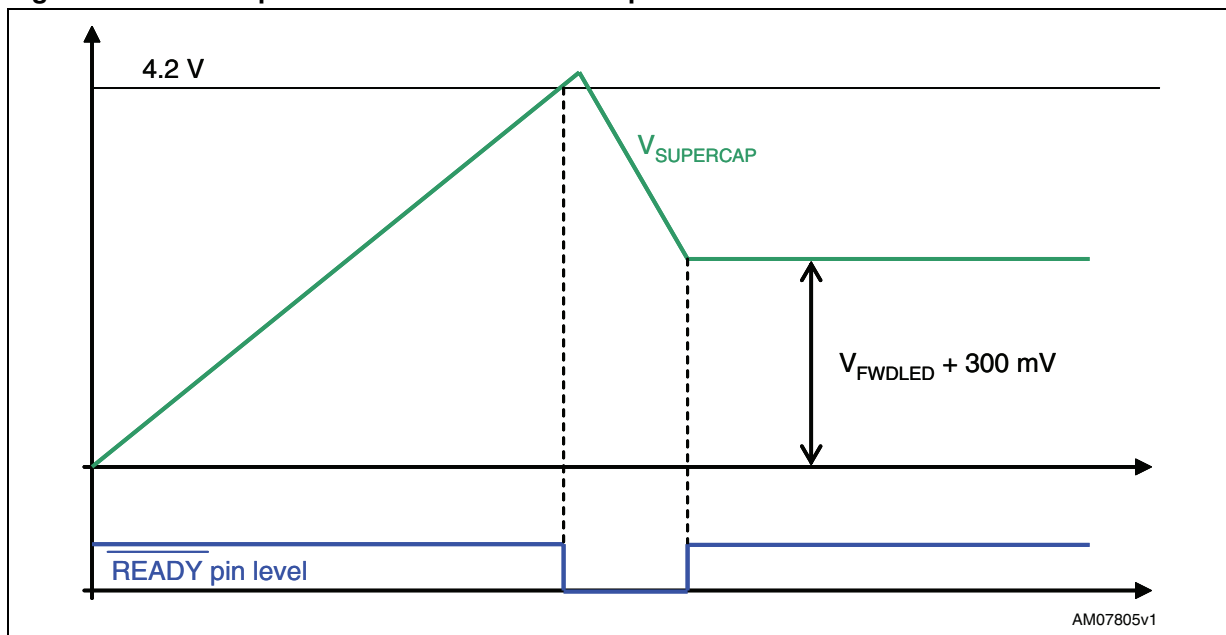
Figure 10. READY pin behavior in Flash mode



### 7.3 Function of the READY pin in Torch mode (optimized)

The threshold for the transition from high to low level is 4.2 V in this case. It is a fixed threshold, which cannot be changed by any settings of the registers. The transition from low to high occurs when the voltage on the LEDIN pin falls to 300 mV, which is the optimum value from an efficiency point of view.

Figure 11. READY pin behavior in Torch mode optimized

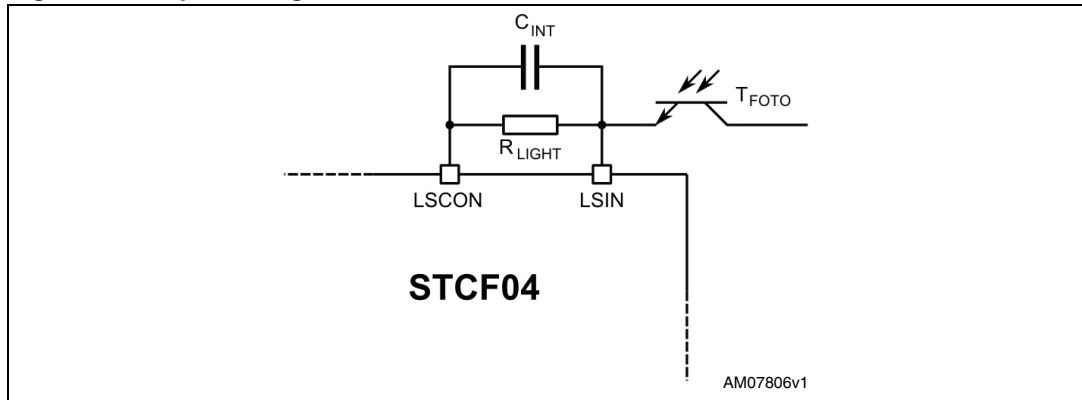


The READY pin is an open drain output, which is capable of sinking a maximum 3 mA current. That is why the minimum value of the pull-up resistor connected to it should not be lower than 1.8 k $\Omega$ .

## 8 The light sensor

The light sensor is an optional feature which optimizes the FLASH duration according to the light conditions in the flashed scene. This feature requires three external components to be connected to the STCF04 according to [Figure 12](#). It is recommended to connect the collector of the phototransistor to  $V_{REF} = 1.8$  V. The integrating capacitor  $C_{INT}$  is discharged before every FLASH pulse. This reset takes approximately 200  $\mu$ s. During the FLASH the voltage on this capacitor increases according to the amount of light in the scene and  $T_{FOTO}$ ,  $R_{LIGHT}$ , and  $C_{INT}$  parameters. The values of these components must be selected according to the final application purpose.

**Figure 12. Optional light sensor feature**

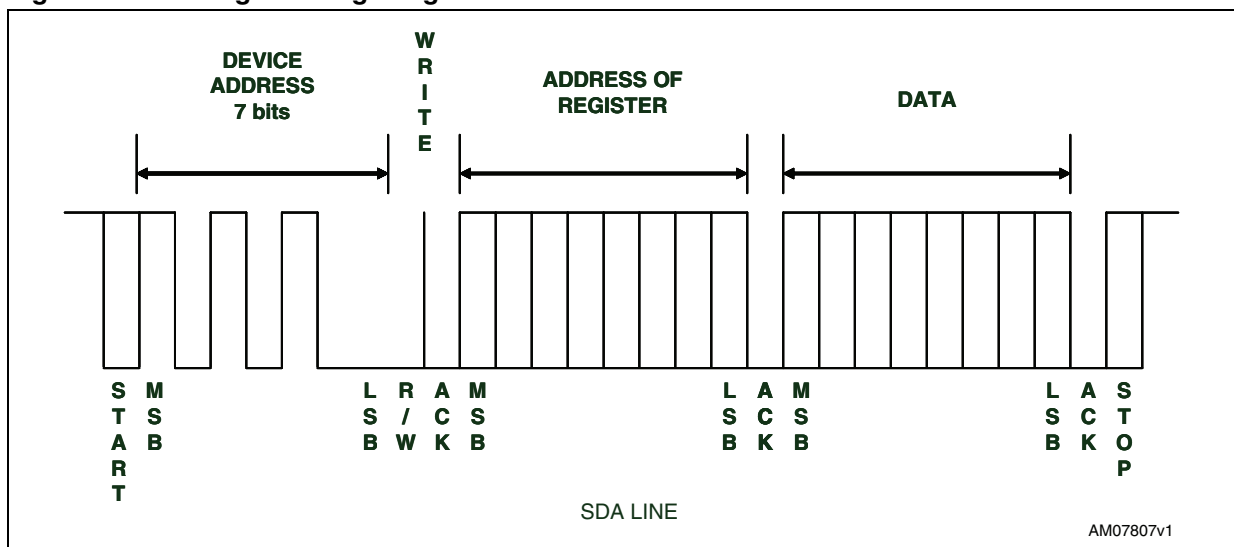


## 9 Reading and writing to the STCF04 registers through the I<sup>2</sup>C bus

### 9.1 Writing to a single register

Writing to a single register starts with a START bit followed by the 7-bit device address of the STCF04. The 8<sup>th</sup> bit is the R/W bit, which is 0 in this case. R/W = 1 means a reading operation. Then the master awaits an acknowledgement from the STCF04. The 8-bit address of the desired register is sent afterwards to the STCF04. It is also followed by an acknowledge pulse. The last transmitted byte is the data which is going to be written into the register. It is followed again by an acknowledge pulse from STCF04. Then the master generates a STOP bit and the communication is over. See [Figure 13](#) below.

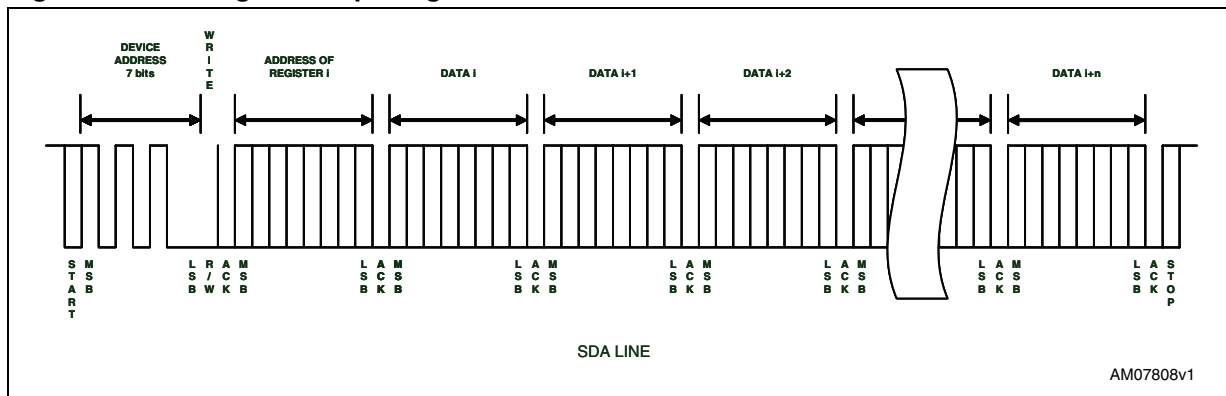
Figure 13. Writing to a single register



### 9.2 Writing to multiple registers with incremental addressing

It would not be practical to send the device address and the address of the register when writing to multiple registers several times. The STCF04 supports writing to multiple registers with incremental addressing. When data is written to a register, the register address is automatically incremented (by one), and therefore the next data can be sent without sending again the device address and the register address. See [Figure 14](#) below.

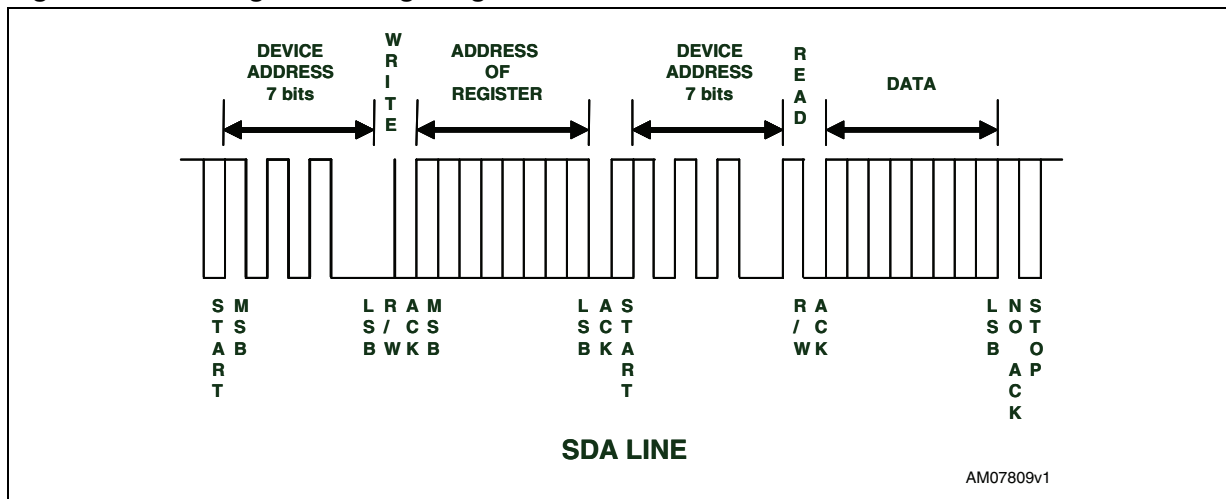
Figure 14. Writing to multiple register



### 9.3 Reading from a single register

The reading operation starts with a START followed by the 7-bit device address of the STCF04. The 8<sup>th</sup> bit is the R/W-bit, which is 0 in this case. STCF04 confirms receipt of the address + R/W bit by an acknowledge pulse. The address of the register which should be read is sent and confirmed by an acknowledge pulse from the STCF04 again. Then the master generates a START bit again and sends the device address followed by the R/W bit, which is now 1. The STCF04 confirms receipt of the address + R/W bit by an acknowledge pulse, and starts to send data to the master. No acknowledge pulse from the master is required after receiving the data. Then, the master generates a STOP bit to terminate the communication. See [Figure 15](#) below.

Figure 15. Reading from a single register

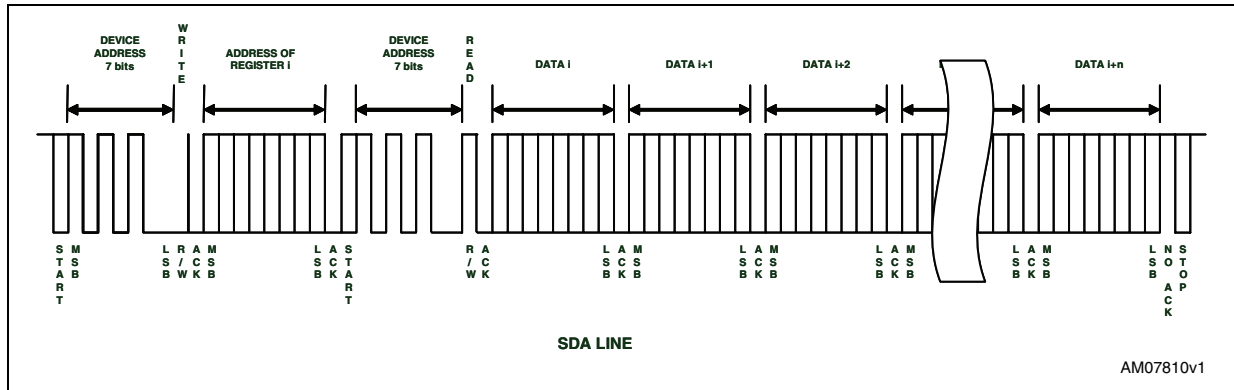


### 9.4 Reading from multiple registers with incremental addressing

Reading from multiple registers starts in the same way as reading from a single register. As soon as the first register is read, the register address is automatically incremented. If the master generates an acknowledge pulse after receiving the data from the first register, then

reading from the next register can start immediately without having to once again send the device and the register addresses. The last acknowledge pulse before the STOP-bit is not required. See *Figure 16* below.

**Figure 16. Reading from multiple registers**





## 10 Examples of register setup for each mode

### 10.1 Example 1: 10 A FLASH with 30 ms duration

The value of FDIM (3 bits) must be set to 0x7. The value of FTIM (5 bits) must be set to 0x6.

Bit PWR\_ON must be set to 1.

Bit FLASH\_ON must be set to 1.

Bit TCH\_ON must be set to 0.

Bit NTC\_ON can be set to any value, because NTC is automatically ON when Flash mode is active. Setting this bit to 0 does not switch off the NTC.

**Table 13. COMMAND register data for entering Flash mode**

CMD_REG	PWR_ON	FLASH_ON	TCH_ON	NTC_ON	TCHV_H	CHRG	MONTR	N/A
	1	1	0	0	0	0	0	0
	MSB							LSB

**Table 14. FLASH register data**

FL_REG	FTIM_4	FTIM_3	FTIM_2	FTIM_1	FTIM_0	FDIM_2	FDIM_1	FDIM_0
	0	0	1	1	0	1	1	1
	MSB							LSB

It is necessary to write 4 bytes to the STCF04 to make a FLASH.

**Table 15. I<sup>2</sup>C data packet for activation of Flash mode**

Byte	Hex	Binary								Comment
1	62	0	1	1	0	0	0	0	0	Device address + R/W bit
2	00	0	0	0	0	0	0	0	0	COMMAND register address
3	C1	1	1	0	0	0	0	0	0	Data of the COMMAND register
4	37	0	0	1	1	0	1	1	1	Data of the FLASH register

### 10.2 Example 2: 60 mA Torch with 10 s duration

The value of TDIM (4 bits) must be set to 0x4 to setup the current source to 60 mA.

Bit PWR\_ON must be set to 1.

Bit FLASH\_ON must be set to 0.

Bit TCH\_ON must be set to 1.

Bit NTC\_ON can be set to any value, because NTC is automatically ON, when Torch mode is active. Setting this bit to 0 does not switch off the NTC.

**Table 16. COMMAND register data for entering Torch mode**

CMD_REG	PWR_ON	FLASH_ON	TCH_ON	NTC_ON	TCHV_H	CHRG	MONTR	N/A
	1	0	1	0	0	0	0	0
	MSB							LSB

**Table 17. TORCH register data**

DIM_REG	TTRCH1	TTRCH0	TDIM_3	TDIM_2	TDIM_1	TDIM_0	N/A	N/A
	1	0	0	1	0	0	0	0
	MSB							LSB

The following packet sets the TORCH register.

**Table 18. I<sup>2</sup>C data packet for setting the TORCH register**

Byte	Hex	Binary								Comment
1	60	0	1	1	0	0	0	0	0	Device address + R/W bit
2	05	0	0	0	0	0	1	0	1	TORCH register address
3	90	1	0	0	1	0	0	0	0	Data of the TORCH register

The following packet sets the COMMAND register.

**Table 19. I<sup>2</sup>C data packet for setting the COMMAND register**

Byte	Hex	Binary								Comment
1	60	0	1	1	0	0	0	0	0	Device address + R/W-bit
2	00	0	0	0	0	0	0	0	0	COMMAND register address
3	A0	1	0	1	0	0	0	0	0	Data of the COMMAND register

The TORCH pin must be high to enter Torch mode.

### 10.3 Example 3: An Auxiliary LED running at 10 mA for 500 ms

The auxiliary LED can be activated from Idle mode only.

A 10 mA output current is reached when AUX1 is set to 0x2.

AUXT must be set to 0x5 to have 500 ms duration of the auxiliary LED lighting.

**Table 20. COMMAND register data for the AUX\_LED**

CMD_REG	PWR_ON	FLASH_ON	TCH_ON	NTC_ON	TCHV_H	CHRG	MONTR	N/A
	1	0	0	0	0	0	0	0
	MSB							LSB

**Table 21. AUX\_LED register data**

AUX_LED	AUXI_3	AUXI_2	AUXI_1	AUXI_0	AUXT_3	AUXT_2	AUXT_1	AUXT_0
	0	0	1	0	0	1	0	1
	MSB							LSB

Writing the 3 bytes in [Table 22](#) to STCF04 puts it into Idle mode. This can be skipped if it is already in Idle mode.

**Table 22. I<sup>2</sup>C data packet for activating Idle mode**

Byte	Hex	Binary								Comment
1	60	0	1	1	0	0	0	0	0	Device address + R/W bit
2	00	0	0	0	0	0	0	0	0	COMMAND register address
3	80	1	0	0	0	0	0	0	0	Data of the COMMAND register

Writing the following 3 bytes to the STCF04 activates the auxiliary LED for the desired time.

**Table 23. I<sup>2</sup>C data packet for activating the AUX\_LED**

Byte	Hex	Binary								Comment
1	60	0	1	1	0	0	0	0	0	Device address + R/W bit
2	02	0	0	0	0	0	0	1	0	Auxiliary LED register address
3	25	0	0	1	0	0	1	0	1	Data of the Auxiliary LED register

## 11 Revision history

**Table 24. Document revision history**

Date	Revision	Changes
27-Aug-2010	1	Initial release.
13-Feb-2012	2	Modified title in cover page. Removed references to part number STCS44.

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