XPS Multi-CHannel External Memory Controller (XPS MCH EMC) (v2.00a)

DS575 July 21, 2008 **Product Specification**

Introduction

The Xilinx Multi-channel External Memory Controller (XPS MCH EMC) provides the control interface for external synchronous, asynchronous SRAM and Flash memory devices through the MCH or PLB interfaces. It is assumed that the reader is familiar with the PLB and MCH protocol.

Features

The XPS MCH EMC is a soft IP core designed for Xilinx FPGAs and contains the following features:

- Connects as a 32-bit slave on PLB v4.6 bus of 32, 64 or 128 bits
- Parameterizable number (0 to 4) of channel interfaces that can be configured with a Xilinx CacheLink (XCL) protocol (see "Reference Documents")
- Can be used with PLB interface only or MCH interface only or in combination of both PLB and MCH interfaces
- Supports multiple (up to 4) external memory banks
- Supports single-beat and burst transactions
- Supports target-word first PLB Cacheline read and line-word first PLB Cacheline write transactions of 4, 8 and 16 words
- Supports target word of 1, 4, 8 and 16 words for first XCL cache line transactions
- Supports low latency PLB Point-to-Point topology
- Supports Synchronous / Asynchronous SRAMs and Flash memory devices
- Supports memory data widths of 32-bit, 16-bit and 8-bit
- Supports data width matching (memory data width must be less than or equal to the PLB or the MCH data width)
- Supports configurable cycle time for read and write operations

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	Spartan®-3E, Automotive Spartan-3E, Spartan-3, Automotive Spartan-3, Spartan-3A, Automotive Spartan-3A, Spartan-3AN, Spartan-3A DSP, Automotive Spartan-3A DSP, Virtex®-4, QPro Virtex-4 Hi Rel, QPro Virtex-4 Rad Tolerant, Virtex-5, Virtex-II Pro	
Version of Core	xps_mch_emc	v2.00a
Resources Used		
	Min	Max
Slices	Refer to Table 13, Table 14 and Table 15	
LUTs		
FFs		
Block RAMs	N/A	
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs & Application Notes	N/A	
Design Tool Requirements		
Xilinx Implementation Tools	ISE® 10.1i or later	
Verification	ModelSim SE/EE 6.0c or later	
Simulation	ModelSim SE/EE 6.0c or later	
Synthesis	XST 10.1i or later	
Support		
Support provided by Xilinx, Inc.		

Functional Description

The XPS MCH EMC consists of the MCH PLB Interface Module, Select Parameters module, Mem State Machine module, Mem Steer module, Address Counter Mux module, Counters module, I/O Registers module and IPIC Interface module.

Figure 1 illustrates the top level block diagram of XPS MCH EMC.

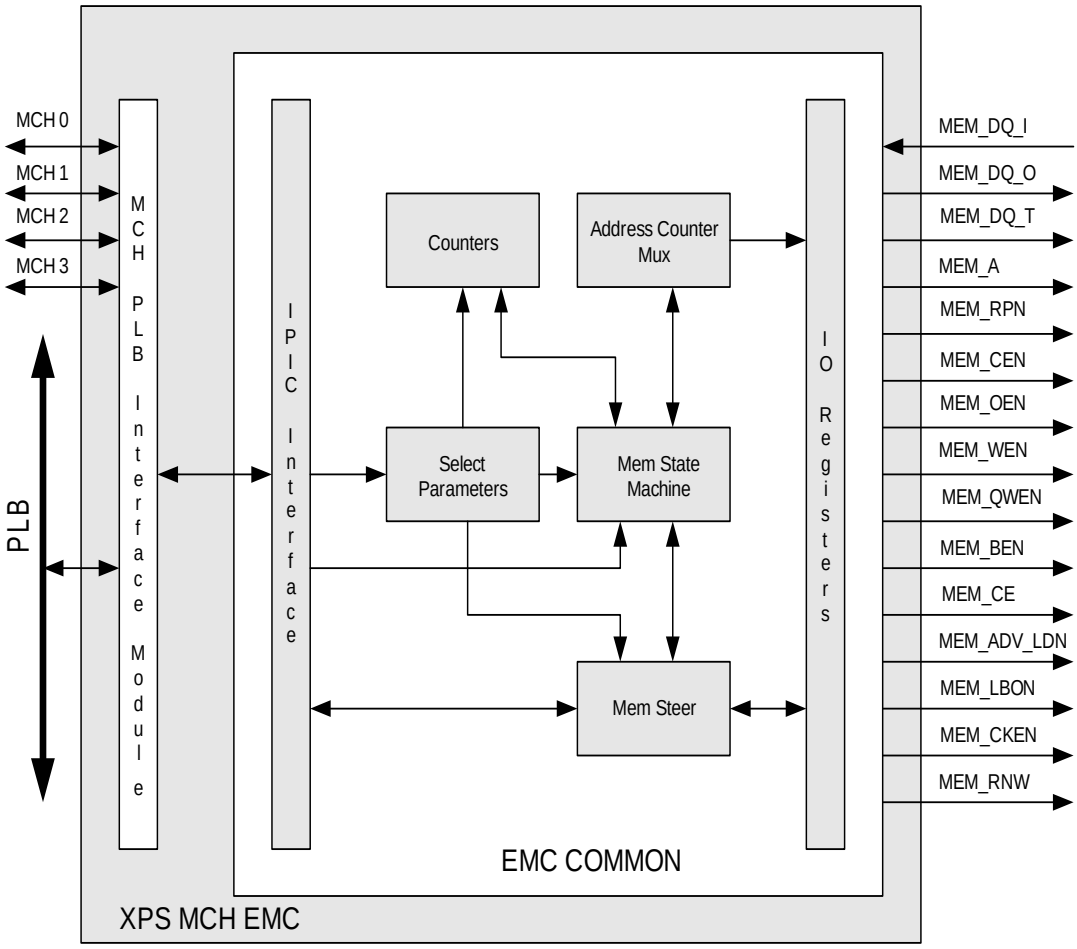


Figure 1: **XPS MCH EMC Top Level Block Diagram**

MCH PLB Interface Module

The MCH PLB Interface Module provides an optional interface to the MCH interface and PLB. The MCH PLB Interface Module consists of an optional PLB slave interface, a parameterizable number of channel interfaces and arbitration logic to select between the MCH interfaces and the PLB interface. The appropriate multiplexors/de-multiplexors connect the selected channel or PLB transaction to the EMC core. This module does the necessary protocol and timing translation between MCH interface and IPIC interface or between PLB interface and IPIC interface.

Select Parameters

The Select Parameters module provides necessary pipeline delays or timing delays based on the type of memory. It also indicates the type of memory connected to the core.

Mem State Machine

The state diagram of Mem State Machine is shown in Figure 2.

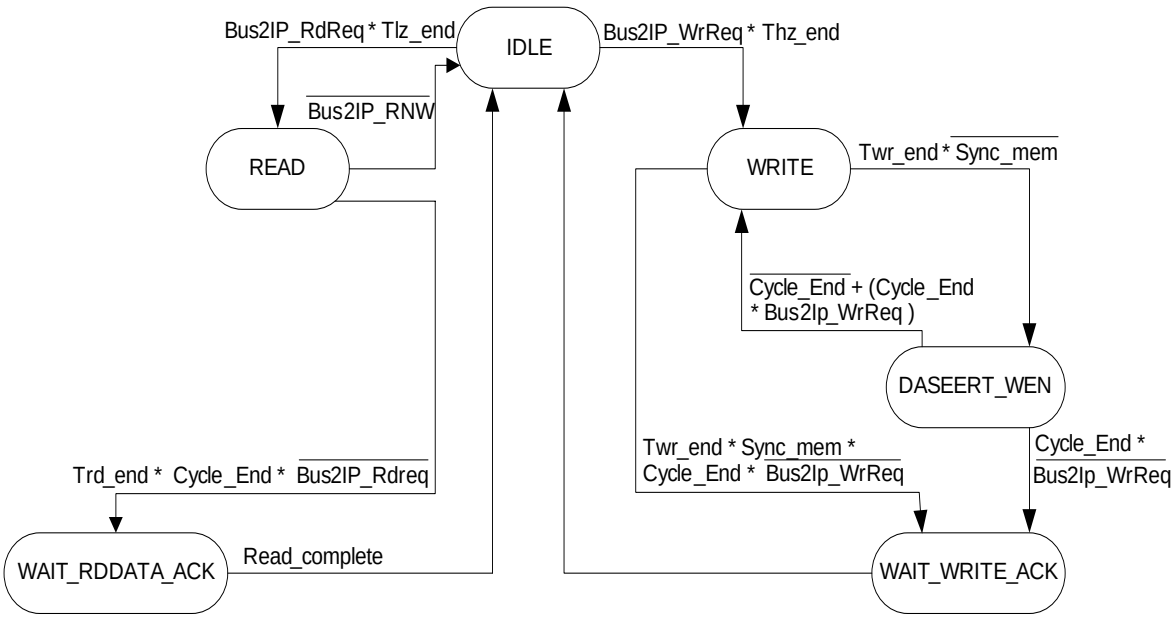


Figure 2: **XPS MCH EMC Mem State Machine**

The Mem State Machine controls read and write transactions for the memory. It handles both single and burst conditions and provides necessary control signals to the Counters, Mem Steer and Address Counter Mux modules.

Mem Steer

The Mem Steer module contains the logic to provide the steering of read data, write data and memory control signals. It generates the acknowledge signals for the MCH PLB Interface Module. This module contains data width matching logic when the data bus width of the memory is less than the MCH/PLB data bus width.

Address Counter Mux

The Address Counter Mux module provides the address count to the Mem Steer module and provides the address suffix to generate the memory address. It also handles the cycle end logic which is directed to the Mem State Machine.

Counters

This module contains the counters for counting the read cycle time and write cycle time.

I/O Registers

Registers are used on all signals to and from the memory bank to provide consistent timing on the memory interface. The I/O Registers module present in the design depends upon the setting of the C_INCLUDE_NEGEDGE_IOREGS. All signals output to the memory bank are registered on the rising edge of the system clock. If C_INCLUDE_NEGEDGE_IOREGS = 1, the signals are registered again on the falling edge

of the system clock, as shown in Figure 3, and can be used at lower clock frequency to provide adequate setup and hold times to synchronous memories.

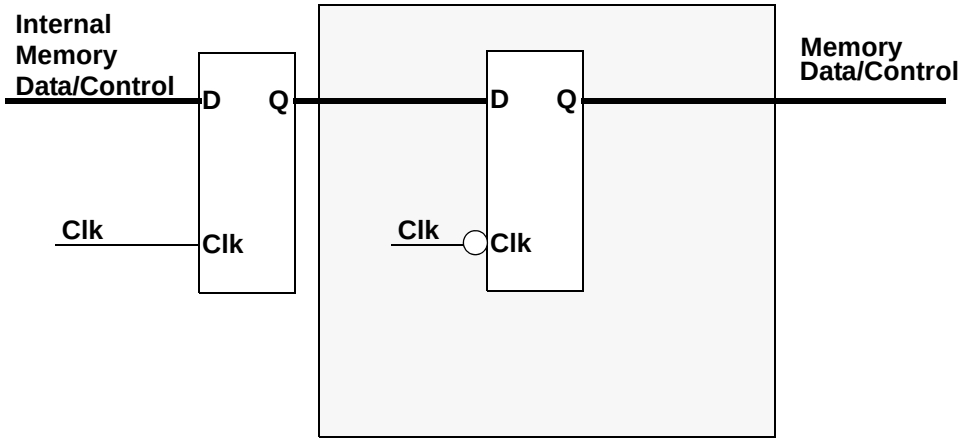


Figure 3: **XPS MCH EMC Output Registers When C_INCLUDE_NEGEDGE_IOREGS = 1**

IPIC Interface

The IPIC Interface module connects the EMC core to the MCH PLB Interface Module.

XPS MCH EMC I/O Signals

The XPS MCH EMC I/O signals are listed and described in Table 1.

Table 1: **XPS MCH EMC I/O Signals**

Port	Signal Name	Interface	I/O	Default Value	Description
System Signals					
P1	MCH_PLB_CLK[1]	System	I	-	MCH/PLB clock
P2	RdClk[2]	System	I	-	Read clock to capture the data from Memory
P3	MCH_PLB_Rst[1]	System	I	-	MCH/PLB reset
PLB Interface Signals[3]					
P4	PLB_ABus[0 : 31]	PLB	I	-	PLB address bus
P5	PLB_PAValid	PLB	I	-	PLB primary address valid indicator
P6	PLB_masterID[0:C_SPLB_MID_WIDTH - 1]	PLB	I	-	PLB current master identifier
P7	PLB_RNW	PLB	I	-	PLB read not write
P8	PLB_BE[0:(C_SPLB_WIDTH/8) - 1]	PLB	I	-	PLB byte enables
P9	PLB_wrBurst	PLB	I	-	PLB burst write transfer indicator
P10	PLB_rdBurst	PLB	I	-	PLB burst read transfer indicator
P11	PLB_size[0 : 3]	PLB	I	-	PLB transfer size

Table 1: **XPS MCH EMC I/O Signals <Italic>(Continued)**

Port	Signal Name	Interface	I/O	Default Value	Description
P12	PLB_type[0 : 2]	PLB	I	-	PLB transfer type
P13	PLB_wrDBus[0:C_SPLB_ DWIDTH - 1]	PLB	I	-	PLB write data bus
P14	PLB_MSize[0 : 1]	PLB	I	-	PLB master data bus size
Unused PLB Interface Signals					
P15	PLB_UABus[0 : 31]	PLB	I	-	PLB upper address bus
P16	PLB_SAValid	PLB	I	-	PLB secondary address valid indicator
P17	PLB_rdPrim	PLB	I	-	PLB secondary to primary read request indicator
P18	PLB_wrPrim	PLB	I	-	PLB secondary to primary write request indicator
P19	PLB_abort	PLB	I	-	PLB abort bus indicator
P20	PLB_busLock	PLB	I	-	PLB bus lock
P21	PLB_TAttribute[0 : 15]	PLB	I	-	PLB transfer attribute bus
P22	PLB_lockerr	PLB	I	-	PLB lock error indicator
P23	PLB_wrPendReq	PLB	I	-	PLB pending write bus request indicator
P24	PLB_rdPendReq	PLB	I	-	PLB pending read bus request indicator
P25	PLB_rdPendPri[0 : 1]	PLB	I	-	PLB pending write request priority
P26	PLB_wrPendPri[0 : 1]	PLB	I	-	PLB pending write request priority
P27	PLB_reqPri[0 : 1]	PLB	I	-	PLB current request priority
PLB Slave Interface Signals[3]					
P28	Sl_addrAck	PLB	O	0	Slave address acknowledge
P29	Sl_SSize[0 : 1]	PLB	O	0	Slave data bus size
P30	Sl_wait	PLB	O	0	Slave wait indicator
P31	Sl_rearbitrate	PLB	O	0	Slave rearbitrate bus indicator
P32	Sl_wrDack	PLB	O	0	Slave write data acknowledge
P33	Sl_wrComp	PLB	O	0	Slave write transfer complete indicator
P34	Sl_wrBTerm	PLB	O	0	Slave terminate write burst transfer
P35	Sl_rdBus[0:C_SPLB_ DWIDTH - 1]	PLB	O	0	Slave read data bus
P36	Sl_rdDAck	PLB	O	0	Slave read data acknowledge
P37	Sl_rdComp	PLB	O	0	Slave read transfer complete indicator

Table 1: **XPS MCH EMC I/O Signals <Italic>(Continued)**

Port	Signal Name	Interface	I/O	Default Value	Description
P38	Sl_rdBTerm	PLB	O	0	Slave terminate read burst transfer
P39	Sl_rdWdAddr[0 : 3]	PLB	O	0	Slave read word address
P40	Sl_MBusy[0:C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave busy indicator
P41	Sl_MWrErr[0:C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave write error indicator
P42	Sl_MRdErr[0:C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave read error indicator
MCH Interface Signals[4]					
P43	MCHx_Access_Control[5]	MCH	I	-	Control signal to the access buffer of the MCH interface. This signal indicates the type of access to be performed (read or write) and the size of the access (byte, halfword or word)
P44	MCHx_Access_Data[0:C_MCH_NATIVE_DWIDTH - 1][5]	MCH	I	-	Write data to the access buffer of the MCH interface
P45	MCHx_Access_Write[5]	MCH	I	-	Write signal to access buffer of the MCH interface
P46	MCHx_Access_Full[5]	MCH	O	0	Indicates that the access buffer of the MCH interface is full
P47	MCHx_ReadData_Control[5]	MCH	O	1	Control signal for the read data buffer of the MCH interface. These signals indicates if the data from the read data buffer is valid
P48	MCHx_ReadData_Data[0:C_MCH_NATIVE_DWIDTH - 1][5]	MCH	O	0	Read data from the read data buffer of the MCH interface
P49	MCHx_ReadData_Read[5]	MCH	I	-	Read signal to the read data buffer of the MCH interface
P50	MCHx_ReadData_Exists[5]	MCH	O	0	Indicates that the read data buffer of the MCH interface is not empty
External Memory Signals					
P51	MEM_DQ_I[0:C_MAX_MEM_WIDTH - 1]	External memory	I	-	Memory input data bus
P52	MEM_DQ_O[0:C_MAX_MEM_WIDTH - 1]	External memory	O	0	Memory output data bus
P53	MEM_DQ_T[0:C_MAX_MEM_WIDTH - 1]	External memory	O	0	Memory output 3-state signal
P54	MEM_A[0:C_MCH_SPLB_AWIDTH - 1]	External memory	O	0	Memory address bus
P55	MEM_RPN	External memory	O	1	Memory reset/power down

Table 1: **XPS MCH EMC I/O Signals <Italic>(Continued)**

Port	Signal Name	Interface	I/O	Default Value	Description
P56	MEM_CEN[0:C_NUM_BANKS_MEM - 1]	External memory	O	1	Memory chip enables[6] (active low)
P57	MEM_OEN[0:C_NUM_BANKS_MEM - 1]	External memory	O	1	Memory output enable
P58	MEM_WEN	External memory	O	1	Memory write enable
P59	MEM_QWEN[0:(C_MAX_MEM_WIDTH/8) - 1]	External memory	O	1	Memory qualified write enables
P60	MEM_BEN[0:(C_MAX_MEM_WIDTH/8) - 1]	External memory	O	0	Memory byte enables
P61	MEM_CE[0:C_NUM_BANKS_MEM - 1]	External memory	O	0	Memory chip enables[6] (active high)
P62	MEM_ADV_LDN	External memory	O	1	Memory advance burst address/load new address
P63	MEM_LBON	External memory	O	1	Memory linear/interleaved burst order
P64	MEM_CKEN	External memory	O	0	Memory clock enable
P65	MEM_RNW	External memory	O	1	Memory read not write

Notes:

1. User must connect this port manually when C_INCLUDE_PLB_IPIF=0
2. This clock is used to capture the data from memory. Connection to this port is must otherwise design will fail. Generally this should be connected to system/bus clock. User can connected this to other clock nets e.g. phase shift clock or feedback clock.
3. The signals in this section are unused if C_INCLUDE_PLB_IPIF = 0. The inputs are ignored and the outputs are driven to zero.
4. MCH signals are unused when C_NUM_CHANNELS = 0.
5. x = values for XCL channels 0 to 3.
6. Most asynchronous memory devices will only use MEM_CEN. Most synchronous memory devices will use both MEM_CEN and MEM_CE. Refer to the device data sheet for correct connection of these signals.

XPS MCH EMC Design Parameters

To allow the user to create a XPS MCH EMC that is uniquely tailored for the user's system, certain features are parameterizable in the XPS MCH EMC design. This allows the user to have a design that utilizes only the resources required by the system and runs at the best possible performance. The features that are parameterizable in the XPS MCH EMC are as shown in Table 2.

Table 2: **XPS MCH EMC Design Parameters**

Generic	Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
XPS MCH EMC Parameters					
G1	Target FPGA family	C_FAMILY	spartan3e, aspartan3e, spartan3, aspartan3, spartan3a, aspartan3a, spartan3an, virtex4, qvirtex4, qrvirtex4, virtex5, virtex2p	virtex5	string
G2	Number of memory banks	C_NUM_BANKS_MEM	1 - 4	1	integer
G3	Arbitration mode between MCH and PLB	C_PRIORITY_MODE	0 = Fixed priority mode	0	integer
G4	Include PLB slave interface	C_INCLUDE_PLB_IPIF[1]	0 = Don't include PLB interface 1 = Include PLB interface	1	integer
G5	Includes support for write buffer	C_INCLUDE_WRBUF	0 = Don't include the write buffer 1 = Include the write buffer	1	integer
G6	PLB master ID bus width	C_SPLB_MID_WIDTH	$\log_2$(C_SPLB_NUM_MASTERS) with a minimum value of 1	1	integer
G7	Number of PLB masters	C_SPLB_NUM_MASTERS	1 - 16	1	integer
G8	Selects point-to-point or shared bus topology	C_SPLB_P2P	0 = Shared bus topology 1 = Point-to-Point bus topology	0	integer
G9	Data bus width for MCH and PLB	C_SPLB_DWIDTH	32, 64, 128	32	integer
G10	Address bus width for MCH and PLB	C_MCH_SPLB_AWIDTH	32	32	integer
G11	Data bus width of the smallest master	C_SPLB_SMALLEST_MASTER	32, 64, 128	32	integer

Table 2: **XPS MCH EMC Design Parameters <Italic>(Continued)**

Generic	Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
G12	Slave data bus width	C_MCH_NATIVE_ DWIDTH	32	32	integer
G13	Input/output data and control signals using the falling edge of the clock	C_INCLUDE_ NEGEDGE_IOREGS[2]	0 = Don't include negative edge IO registers (data and control signals are input/output on the rising edge of the clock) 1 = Include negative edge IO registers (data and control signals are input/output on the falling edge of the clock)	0	integer
G14	Width of memory bank x data bus	C_MEMx_WIDTH[3]	8, 16, 32	32	integer
G15	Execute multiple memory access cycles to match memory bank x data width to MCH and PLB data width	C_INCLUDE_DATAWIDTH _MATCHING_x[3,4]	0 = Don't include data width matching 1 = Include data width matching	0	integer
G16	Memory type of memory bank x	C_SYNCH_MEM_x[3]	0 = Memory type is asynchronous 1 = Memory type is synchronous	0	integer
G17	Pipeline delay (in clock cycles) of memory bank x	C_SYNCH_ PIPEDELAY_x[3]	1, 2	2	integer
Memory Bank Timing Parameters					
G18	Read cycle chip enable low to data valid duration of memory bank x	C_TCEDV_PS_ MEM_x[3,5,6]	Integer number of picoseconds	15000[7]	integer
G19	Read cycle address valid to data valid duration of memory bank x	C_TAVDV_PS_ MEM_x[3,5,8]	Integer number of picoseconds	15000[7]	integer
G20	Read cycle chip enable high to data bus high impedance duration of memory bank x	C_THZCE_PS_ MEM_x[3,9,10]	Integer number of picoseconds	7000[7]	integer
G21	Read cycle output enable high to data bus high impedance duration of memory bank x	C_THZOE_PS_ MEM_x[3,9,11]	Integer number of picoseconds	7000[7]	integer
G22	Write cycle time of memory bank x	C_TWC_PS_ MEM_x[3,12,13]	Integer number of picoseconds	15000[7]	integer

Table 2: **XPS MCH EMC Design Parameters <Italic>(Continued)**

Generic	Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
G23	Write enable minimum pulse width duration of memory bank x	C_TWP_PS_ MEM_x[3,12,14]	Integer number of picoseconds	12000[7]	integer
G24	Write cycle write enable high to data bus low impedance duration of memory bank x	C_TLZWE_PS_ MEM_x[3,15,16]	Integer number of picoseconds	0[7]	integer
Auto Calculated Parameter[17]					
G25	Maximum data width of the memory devices in all banks	C_MAX_MEM_WIDTH[3]	8, 16, 32	32	integer
Address Space Parameters					
G26	Base address of memory bank x	C_MEMx_BASEADDR[3]	Valid address range[18]	None[18]	std_ logic_ vector
G27	High address of memory bank x	C_MEMx_HIGHADDR[3]	Valid address range[18]	None[18]	std_ logic_ vector
Clock Period Parameter					
G28	MCH/PLB clock period	C_MCH_PLB_CLK_ PERIOD_PS[19]	Integer number of picoseconds	10000	integer
MCH Interface Parameters					
G29	Number of MCH channels	C_NUM_CHANNELS[20]	0 - 4	2	integer
G30	Interface protocol for channel x (x = 0 to 3)	C_MCHx_PROTOCOL[21]	0 = XCL protocol	0	integer
G31	Depth of the access buffer for channel x (x = 0 to 3)	C_MCHx_ACCESSBUF_ DEPTH	4, 8, 16	16	integer
G32	Depth of the read data buffer for channel x (x = 0 to 3)	C_MCHx_RDDATABUF_ DEPTH[22]	0, 4, 8, 16	16	integer

Table 2: **XPS MCH EMC Design Parameters <Italic>(Continued)**

Generic	Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
XCL Channel Parameters					
G33	Size of the cacheline in number of 32-bit words for each channel x configured as an XCL channel	C_XCLx_LINESIZE	1, 4, 8, 16	4	integer
G34	Type of write transactions for each channel x configured as an XCL channel	C_XCLx_ WRITEXFER[23]	0 = No write transfers 1 = Single transfers only 2 = Cacheline transfers only	1	integer

Notes:

1. When C_INCLUDE_PLB_IPIF = 0, the XPS MCH EMC will have only MCH interface, PLB transactions are not supported for this setting.
2. This parameter should only be set to 1 under the following conditions:
   - Tfpga_outdelay + Tsetup_memory + Tboard_route_delay < Clock_period/2
   - Tmemory_outdelay + Tfpga_setup + Tboard_route_delay < Clock_period/2
3. x = values for memory banks 0 to 3.
4. Always set this parameter to 1 when C_MEMx_WIDTH < C_MCH_NATIVE_DWIDTH
5. Read cycle time is the maximum of C_TCEDV_PS_MEM and C_TAVDV_PS_MEM.
6. Chip enable low to data valid, C_TCEDV_PS_MEM, is equivalent to t_{ACE} for asynchronous SRAM and t_{ELQV} for Flash in the respective memory device data sheets.
7. A value must be set for this parameter if the memory type in this bank is asynchronous. Refer to the memory device data sheet for the correct value
8. Address valid to data valid, C_TAVDV_PS_MEM, is equivalent to t_{AA} for asynchronous SRAM and t_{AVQV} for Flash in the respective memory device data sheets.
9. Read cycle recovery to write is the maximum of C_THZCE_PS_MEM and C_THZOE_PS_MEM.
10. Chip enable high to data bus high impedance, C_THZCE_PS_MEM, is equivalent to t_{HZCE} for asynchronous SRAM and t_{EHQZ} for Flash in the respective memory device data sheets.
11. Output enable high to data bus high impedance, C_THZOE_PS_MEM, is equivalent to t_{HZOE} for asynchronous SRAM and t_{GHQZ} for Flash in the respective memory device data sheets.
12. Write enable low time is the maximum of C_TWC_PS_MEM and C_TWP_PS_MEM.
13. Write cycle time, C_TWC_PS_MEM, is equivalent to t_{WC} for asynchronous SRAM and t_{CW} for Flash in the respective memory device data sheets.
14. Write cycle minimum pulse width, C_TWP_PS_MEM is equivalent to t_{WP} for asynchronous SRAM and t_{PWE} for Flash in the respective memory device data sheets.
15. Write enable high to data bus low impedance, C_TLZWE_PS_MEM, is equivalent to t_{LZWE} for asynchronous SRAM and t_{WHGL} for Flash in the respective memory device data sheets.
16. C_TLZWE_PS_MEM is the parameter set to meet write recovery to read time requirements.
17. This parameter is automatically calculated when using EDK, otherwise the user must set this parameter to the maximum value of the C_MEMx_WIDTH generics.
18. No default value will be specified for C_MEMx_BASEADDR and C_MEMx_HIGHADDR to insure that the actual value is set, i.e. if the value is not set, a compiler error will be generated. The range specified by C_MEMx_BASEADDR and C_MEMx_HIGHADDR must be a power of 2.
19. Proper value must be assigned to this parameter when C_INCLUDE_PLB_IPIF=0.
20. When C_NUM_CHANNELS = 0, the XPS MCH EMC will have only PLB interface, MCH transactions are not supported for this setting.
21. Each channel can be configured to support a transfer protocol. Only the Xilinx CacheLink (XCL) protocol is supported at this time.
22. If the channel is connected to a master which can consume data as soon as it is available (i.e., instruction side interfaces), set the depth of the read data buffer to zero for that channel to save resources and latency.
23. If an XCL channel is connected to a master that will only perform read transfers, then the entry in C_XCLx_WRITEXFER should be set to 0 indicating that no write transfers will be performed.

Allowable Parameter Combinations

Note that it is assumed all the external memory devices are accessible through MCH interface. They are also accessible through the PLB interface, if the design has been parameterized to include the PLB interface.

The PLB slave interface is only included in the design if C_INCLUDE_PLB_IPIF is set to 1. When C_INCLUDE_PLB_IPIF = 0, then the C_INCLUDE_WRBUF is unused.

If C_SYNCH_MEM_x = 1, then C_SYNCH_PIPEDELAY_x specifies the pipeline delay of that synchronous memory type. All other timing parameters for that memory bank can remain at the default value of 0. If C_SYNCH_MEM_x = 0, C_SYNCH_PIPEDELAY_x is unused. All other timing parameters for that memory bank must be set to the value specified in the memory device data sheet.

C_INCLUDE_NEGEDGE_IOREGS provides no benefit when interfacing to asynchronous memories. Therefore, if there are no synchronous memories in the system, this parameter should be set to 0.

Optimal MCH Parameter Settings

The only channel transfer protocol supported at this time is the Xilinx Cachelink (XCL) interface.

If an XCL channel is connected to a master that will only perform read transactions, then C_XCLx_WRITEXFER should be set to 0 indicating that no write transfers will be performed. This will reduce the channel logic to only contain logic for read transactions.

If an XCL channel is connected to a master that can consume data as soon as it is available, then C_MCHx_RDDATABUF_DEPTH for that channel can be set to 0. This will eliminate the read data buffer and eliminate the latency that would normally exist while reading data from this buffer. If the master cannot consume data as soon as it is available then, C_MCHx_RDDATABUF_DEPTH for that channel should be set to accommodate any latency the master has while reading data from the read data buffer.

Optimal performance will be achieved when the buffer depth of the access buffer is set greater than or equal to the line size of the channel (C_MCHx_ACCESSBUF_DEPTH ≥ C_XCLx_LINESIZE).

Parameter Port Dependencies

The dependencies between the XPS MCH EMC design parameters and I/O signals are described in Table 3. In addition, when certain features are parameterized out of the design, the related logic will no longer be part of the design. The unused input signals and related output signals are set to a specified value.

Table 3: **Parameter Port Dependencies**

Generic or Port	Parameter	Affects	Depends	Description
Design Parameters				
G2	C_NUM_BANKS_MEM	P56, P57, P61	-	Specifies the number of external memory (SRAMs, Flash) banks
G4	C_INCLUDE_PLB_IPIF	P4 - P42	-	PLB input signals are unused and output signals are tied to 0 when C_INCLUDE_PLB_IPIF = 0
G5	C_INCLUDE_WRBUF	-	G4	Unused when C_INCLUDE_PLB_IPIF = 0

Table 3: **Parameter Port Dependencies**

Generic or Port	Parameter	Affects	Depends	Description
G6	C_SPLB_MID_WIDTH	P6	G4, G7	Specifies width of master ID bus Unused when C_INCLUDE_PLB_IPIF = 0 Width is equal to log_2(C_SPLB_NUM_MASTERS)
G7	C_SPLB_NUM_MASTERS	P40 - P42	G4	Defines width of slave response signals Unused when C_INCLUDE_PLB_IPIF = 0
G8	C_SPLB_P2P	-	G4	Unused when C_INCLUDE_PLB_IPIF = 0
G9	C_SPLB_DWIDTH	P8, P13, P35	-	Data bus width of MCH/PLB interface
G10	C_MCH_SPLB_AWIDTH	P7	-	Address bus width of MCH/PLB interface
G11	C_SPLB_SMALLEST_MASTER	-	G4	Unused when C_INCLUDE_PLB_IPIF = 0
G12	C_MCH_NATIVE_DWIDTH	P44, P48	-	Defines data bus width of MCH interface signals
G25	C_MAX_MEM_WIDTH	P51, P52, P53, P59, P60	-	Maximum data bus width of the external memory (SRAMs, Flash) devices in all banks
G29	C_NUM_CHANNELS	P43 - P50	-	For all the channels numbered greater than the value of the parameter C_NUM_CHANNELS, the MCH interface input signals are unused and the output signals are tied to the default value
G30	C_MCHx_PROTOCOL	-	G29	Unused when x is greater than C_NUM_CHANNELS - 1
G31	C_MCHx_ACCESSBUF_DEPTH	-	G29	Unused when x is greater than C_NUM_CHANNELS - 1
G32	C_MCHx_RDDATABUF_DEPTH	-	G29	Unused when x is greater than C_NUM_CHANNELS - 1
G33	C_XCLx_LINESIZE	-	G29	Unused when x is greater than C_NUM_CHANNELS - 1
G34	C_XCLx_WRITEXFER	-	G29	Unused when x is greater than C_NUM_CHANNELS - 1
I/O Signals				
P51	MEM_DQ_I[0:C_MAX_MEM_WIDTH - 1]	-	G25	External memory (SRAMs, Flash) input data bus

Table 3: **Parameter Port Dependencies**

Generic or Port	Parameter	Affects	Depends	Description
P52	MEM_DQ_O[0:C_MAX_MEM_ WIDTH - 1]	-	G25	External memory (SRAMs, Flash) output data bus
P53	MEM_DQ_T[0:C_MAX_MEM_ WIDTH - 1]	-	G25	External memory (SRAMs, Flash) output 3-state signal
P54	MEM_A[0:C_MCH_SPLB_ AWIDTH - 1]	-	G10	External memory (SRAMs, Flash) address bus
P56	MEM_CEN[0:C_NUM_BANKS_ MEM - 1]	-	G2	External memory (SRAMs, Flash) active low chip enables
P57	MEM_OEN[0:C_NUM_BANKS_ MEM - 1]	-	G2	External memory (SRAMs, Flash) active low output enables
P59	MEM_QWEN[0:C_MAX_ MEM_WIDTH/8 - 1]	-	G20	External memory (SRAMs, Flash) qualified write enables
P60	MEM_BEN[0:C_MAX_ MEM_WIDTH/8 - 1]	-	G20	External memory (SRAMs, Flash) byte enables
P61	MEM_CE[0:C_NUM_BANKS_ MEM - 1]	-	G2	External memory (SRAMs, Flash) active high chip enables

XPS MCH EMC Address Map Description

As shown in the Table 4, the XPS MCH EMC currently supports up to four banks of external memory. The number of available banks actually used is determined by the value of C_NUM_BANKS_MEM parameter. This parameter may take values in between 1 and 4, inclusive. The banks that are used, if any, are banks 0 to C_NUM_BANKS_MEM - 1. Each bank of memory has it's own independent base address and high address range.The address range of a bank of memory is restricted to have a size, in bytes, that is in terms of power of 2 and to be address-aligned to the same power of 2. This means that for an address-range of size is 2^n, the *n* least significant bits of the base address will be 0 and *n* least significant bits of the high address will be 1. For example, a memory bank with an addressable range of 16M (2^{24}) bytes could have a base address of 0xFF000000 and a high address of 0xFFFFFFFF. A memory bank with an addressable range of 64K (2^{16}) bytes could have a base address of 0xABCD0000 and a high address of 0xABCDFFFF. The XPS MCH EMC core transactions must fall between the Bank x base address C_MEMx_BASEADDR and high address C_MEMx_HIGHADDR.

The addresses for memory bank is shown in Table 4.

Table 4: **XPS MCH EMC Memory Bank**

Memory	Base Address	High Address	Access
Bank 0	C_MEM0_BASEADDR	C_MEM0_HIGHADDR	Read/Write
Bank 1	C_MEM1_BASEADDR	C_MEM1_HIGHADDR	Read/Write
Bank 2	C_MEM2_BASEADDR	C_MEM2_HIGHADDR	Read/Write
Bank 3	C_MEM3_BASEADDR	C_MEM3_HIGHADDR	Read/Write

Memory Data Types and Organization

Memory can be accessed through the XPS MCH EMC as one of three types: byte (8-bit), halfword (16-bit) or word (32-bit). Data to and from the MCH and PLB is organized as big-endian. The bit and byte labeling for the big-endian data types is shown below in Figure 4.

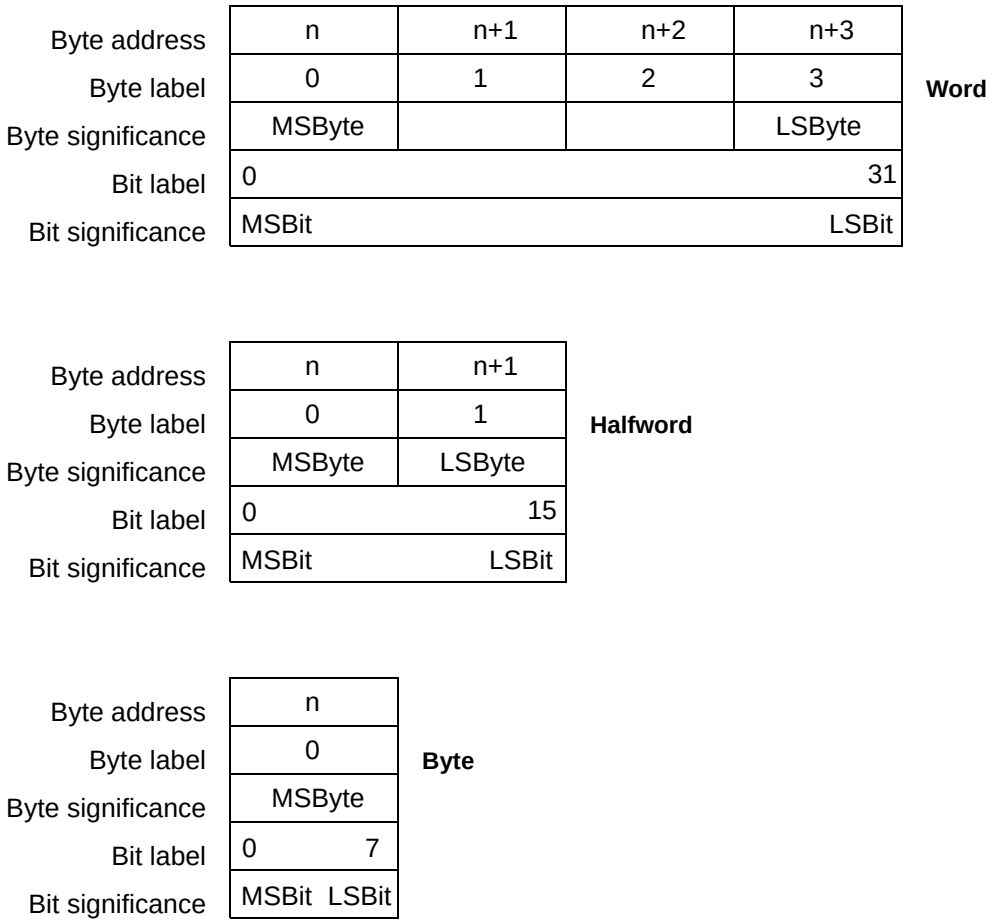


Figure 4: **Memory Data Types**

Connecting to Memory

Clocking Synchronous Memory

The XPS MCH EMC does not provide a clock output to any synchronous memory. The MCH/PLB clock should be routed through an output buffer to provide the clock to the synchronous memory.

To synchronize the synchronous memory clock to the internal FPGA clock, the FPGA system design should include a DCM external to the XPS MCH EMC core that uses the synchronous memory clock input as the

feedback clock as shown in Figure 5. This means that the synchronous clock output from the FPGA must be routed back to the FPGA on a clock pin with a connection to a DCM clock feedback input.

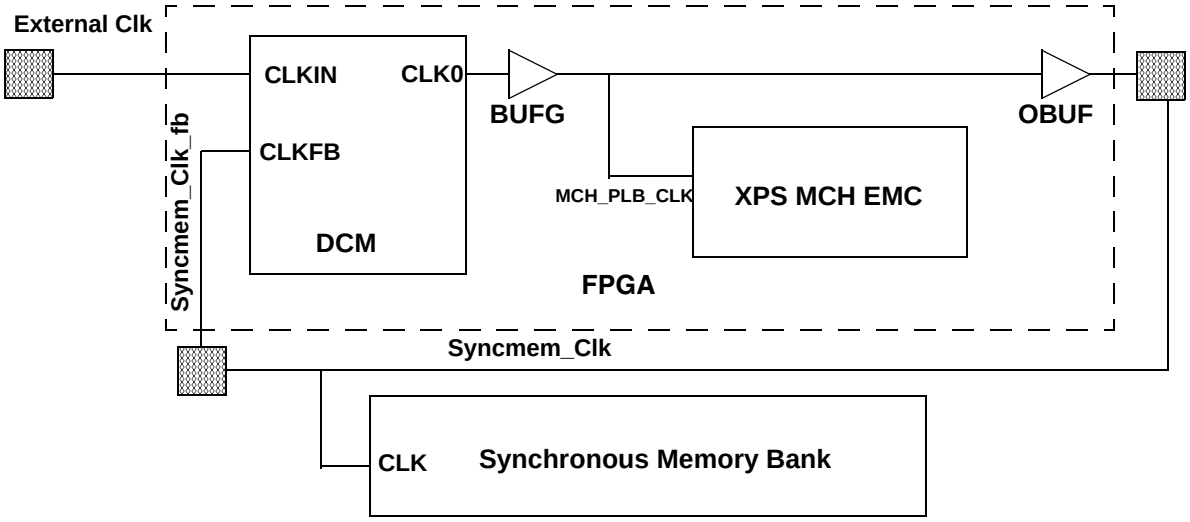


Figure 5: **Synchronous Memory Bank Clocked by FPGA Output With Feedback**

If the synchronous memory is clocked by the same external clock as the FPGA, or if the clock feedback is not available, the DCM shown in Figure 6 should be included in the FPGA external to the XPS MCH EMC core.

Note: If DLLs are used, the designer must reference XAPP132 v2.4, "Using the Virtex Delay-Locked Loop" for the correct DLL implementation.

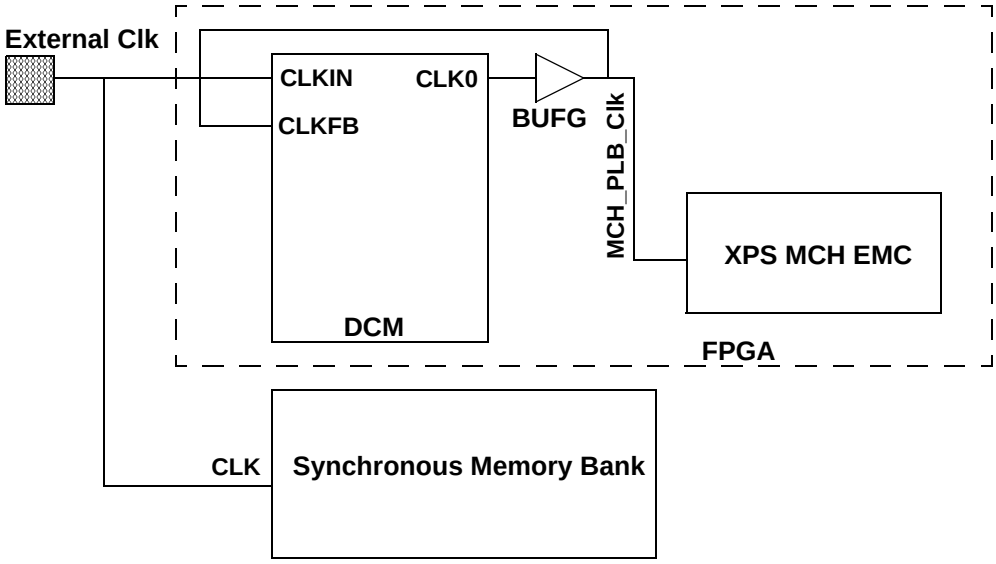


Figure 6: **Synchronous Memory Bank Clocked by External Clock**

Address Bus, Data Bus and Control Signal Connections

The three primary considerations for connecting the controller to memory devices are the width of the MCH/PLB data bus, the width of the memory subsystem and the number of memory devices used.

The width of the memory subsystem is simply the maximum width of data that can be read from or written to the memory subsystem. The memory width must be less than or equal to the MCH/PLB data bus width.

The data and address signals at the memory controller are labeled with big-endian bit labeling (for example: D(0 : 31), D(0) is the MSB), whereas most memory devices are either endian agnostic (they can be connected either way) or little-endian D(31 : 0) with D(31) as the MSB.

Care must be taken when connecting the chip enable signals. Most asynchronous memory devices will only use MEM_CEN, while most synchronous memory devices will use both MEM_CEN and MEM_CE. MEM_CEN is a function of the address decode while MEM_CE is a function of the state machine logic.

Caution must be exercised with the connections to the external memory devices to avoid incorrect data and address connections. The following tables show the correct mapping of memory controller pins to memory device pins.

Table 5 shows variables used in defining memory subsystem and Table 6 shows interconnection of XPS MCH EMC signals to memory interface signals.

Table 5: **Variables Used In Defining Memory Subsystem**

Variable	Allowed Range	Definition
BN	0 to 3	Memory bank number
DN	0 to 31	Memory device number within a bank. The memory device attached to the most significant bit in the memory subsystem is 0; device numbers increase toward the least significant bit.
MW	8 to 32	Width in bits of memory subsystem
DW	1 to 32	Width in bits of data bus for memory device
MAW	1 to 32	Width in bits of address bus for memory device
AU	1 to 32	Width in bits of smallest addressable data word on the memory device
AS	X[1]	Address shift for address bus = $\log_2((MW*AU/DW)/8)$
HAW	1 to 32	Width in bits of MCH/PLB address bus

Notes:
1. The value of X depends on variables MW, AU and DW.

Connecting to SRAM

Table 6: **XPS MCH EMC To Memory Interconnect**

Description	XPS MCH EMC Signals (MSB:LSB)	Memory Device Signals (MSB:LSB)
Data bus	MEM_DQ(DN*DW:((DN+1)*DW)-1)	D(DW-1 : 0)
Address bus	MEM_A(HAW-MAW-AS:HAW-AS-1)	A(MAW-1 : 0)
Chip enable (active low)	MEM_CEN(BN)	CEN
Output enable (active low)	MEM_OEN	OEN
Write enable (active low)	MEM_WEN	WEN (for devices that have byte enables)
Qualified write enable (active low)	MEM_QWEN(DN*DW/8)	WEN (for devices that do not have byte enables)
Byte enable (active low)	MEM_BEN((DN*DW/8) : (((DN+1)*DW/8)-1))	BEN(DW/8-1 : 0)

Example 1: Connection to 32-bit memory using two IDT71V416S SRAM parts.

Table 7 shows variables for simple SRAM example.

Table 7: **Variables For Simple SRAM Example**

Variable	Value	Definition
BN	0	Memory bank number
DN	0 to 1	Memory device number within a bank. The memory device attached to the most significant bit in the memory subsystem is 0; device numbers increase toward the least significant bit.
MW	32	Width in bits of memory subsystem
DW	16	Width in bits of data bus for memory device
MAW	18	Width in bits of address bus for memory device
AU	16	Width in bits of smallest addressable data word on the memory device
AS	2	Address shift for address bus = $\log_2((MW*AU/DW)/8)$
HAW	32	Width in bits of host address bus (e.g. MCH/PLB)

Table 8 shows connection to 32-bit memory using 2 IDT71V416S (256K X 16-Bit) parts.

Table 8: **Connection To 32-bit Memory Using two IDT71V416S Parts**

DN	Description	XPS MCH EMC Signals (MSB:LSB)	Memory Device Signals (MSB:LSB)
0	Data bus	MEM_DQ(0 : 15)	I/O(15 : 0)
	Address bus	MEM_A(12 : 29)	A(17 : 0)
	Chip enable (active low)	MEM_CEN(0)	CS
	Output enable (active low)	MEM_OEN	OE
	Write enable (active low)	MEM_WEN	WE
	Byte enable (active low)	MEM_BEN(0 : 1)	$\overline{BHE}$:$\overline{BLE}$

Table 8: **Connection To 32-bit Memory Using two IDT71V416S Parts <Italic>(Continued)**

DN	Description	XPS MCH EMC Signals (MSB:LSB)	Memory Device Signals (MSB:LSB)
1	Data bus	MEM_DQ(16 : 31)	I/O(15 : 0)
	Address bus	MEM_A(12 : 29)	A(17 : 0)
	Chip enable (active low)	MEM_CEN(0)	CS
	Output enable (active low)	MEM_OEN	OE
	Write enable (active low)	MEM_WEN	WE
	Byte enable (active low)	MEM_BEN(2 : 3)	$\overline{BHE}$:$\overline{BLE}$

Connecting to Intel StrataFlash

StrataFlash parts contain an identifier register, a status register and a command interface, so the bit label ordering for these parts is critical in order to function properly. Table 9 shows example of how to connect the big-endian XPS MCH EMC bus to the little-endian StrataFlash parts.

The proper connection ordering is also indicated in a more general form in Table 6. StrataFlash parts have a x8 mode and a x16 mode, selectable with the BYTE# input pin. To calculate the proper address shift, the minimum addressable word is 8 bits for both x8 and x16 mode, since A0 always selects a byte.

Example 2: Connection to 32-bit memory using two StrataFlash parts in x16 mode.

Supports byte read, but no byte write; smallest data type that can be written is 16-bit data.

Table 9 shows variables for StrataFlash (x16 mode) example.

Table 9: **Variables For StrataFlash (x16 mode) Example**

Variable	Value	Definition
BN	0	Memory bank number
DN	0 to 1	Memory device number within a bank. The memory device attached to the most significant bit in the memory subsystem is 0; device numbers increase toward the least significant bit.
MW	32	Width in bits of memory subsystem
DW	16	Width in bits of data bus for memory device
MAW	24	Width in bits of address bus for memory device
AU	8	Width in bits of smallest addressable data word on the memory device
AS	1	Address shift for address bus = $\log_2((MW*AU/DW)/8)$
HAW	32	Width in bits of host address bus (e.g. MCH/PLB)

Table 10 shows connection to 32-bit memory using two StrataFlash parts.

Table 10: **Connection To 32-bit Memory Using two StrataFlash Parts**

DN	Description	XPS MCH EMC Signals (MSB:LSB)	StrataFlash Signals (MSB:LSB)
0	Data bus	MEM_DQ(0 : 15)	DQ(15 : 0)
	Address bus	MEM_A(7 : 30)	A(23 : 0)
	Chip enable (active low)	GND,GND,MEM_CEN(0)	CE(2 : 0)
	Output enable (active low)	MEM_OEN	OE#
	Write enable (active low)	MEM_QWEN(0)	WE#
	Reset/Power down (active low)	MEM_RPN	RP#
	Byte mode select (active low)	N/A - tie to GND	BYTE#
	Program enable (active high)	N/A - tie to VCC	V_{PEN}
1	Data bus	MEM_DQ(16 : 31)	DQ(15 : 0)
	Address bus	MEM_A(7 : 30)	A(23 : 0)
	Chip enable (active low)	GND, GND, MEM_CEN(0)	CE(2 : 0)
	Output enable (active low)	MEM_OEN	OE#
	Write enable (active low)	MEM_QWEN(2)	WE#
	Reset/Power down (active low)	MEM_RPN	RP#
	Byte mode select (active low)	N/A - tie to GND	BYTE#
	Program enable (active high)	N/A - tie to VCC	V_{PEN}

Example 3: Connection to 32-bit memory using four StrataFlash parts in x8 mode.

Supports byte reads and writes.

Table 11 shows variables for StrataFlash (x8 mode) example.

Table 11: **Variables For StrataFlash (x8 mode) Example**

Variable	Value	Definition
BN	0	Memory bank number
DN	0 to 3	Memory device number within a bank. The memory device attached to the most significant bit in the memory subsystem is 0; device numbers increase toward the least significant bit.
MW	32	Width in bits of memory subsystem
DW	8	Width in bits of data bus for memory device
MAW	24	Width in bits of address bus for memory device
AU	8	Width in bits of smallest addressable data word on the memory device
AS	2	Address shift for address bus = $\log_2((MW*AU/DW)/8)$
HAW	32	Width in bits of host address bus (e.g. MCH/PLB)

Table 12 shows connection to 32-bit memory using four StrataFlash parts.

Table 12: **Connection To 32-bit Memory Using four StrataFlash Parts**

DN	Description	XPS MCH EMC Signals (MSB:LSB)	StrataFlash Signals (MSB:LSB)
0	Data bus	MEM_DQ(0 : 7)	DQ(7 : 0)[1]
	Address bus	MEM_A(8 : 29)	A(21 : 0)
	Chip enable (active low)	GND, GND, MEM_CEN(0)	CE(2 : 0)
	Output enable (active low)	MEM_OEN	OE#
	Write enable (active low)	MEM_QWEN(0)	WE#
	Reset/Power down (active low)	MEM_RPN	RP#
	Byte mode select (active low)	N/A - tie to GND	BYTE#
	Program enable (active high)	N/A - tie to VCC	V_{PEN}
1	Data bus	MEM_DQ(8 : 15)	DQ(7 : 0)[1]
	Address bus	MEM_A(8 : 29)	A(21 : 0)
	Chip enable (active low)	GND,GND, MEM_CEN(0)	CE(2 : 0)
	Output enable (active low)	MEM_OEN	OE#
	Write enable (active low)	MEM_QWEN(1)	WE#
	Reset/Power down (active low)	MEM_RPN	RP#
	Byte mode select (active low)	N/A - tie to GND	BYTE#
	Program enable (active high)	N/A - tie to VCC	V_{PEN}
2	Data bus	MEM_DQ(16 : 23)	DQ(7 : 0)[1]
	Address bus	MEM_A(8 : 29)	A(21 : 0)
	Chip enable (active low)	GND, GND, MEM_CEN(0)	CE(2 : 0)
	Output enable (active low)	MEM_OEN	OE#
	Write enable (active low)	MEM_QWEN(2)	WE#
	Reset/Power down (active low)	MEM_RPN	RP#
	Byte mode select (active low)	N/A - tie to GND	BYTE#
	Program enable (active high)	N/A - tie to VCC	V_{PEN}

Table 12: **Connection To 32-bit Memory Using four StrataFlash Parts <Italic>(Continued)**

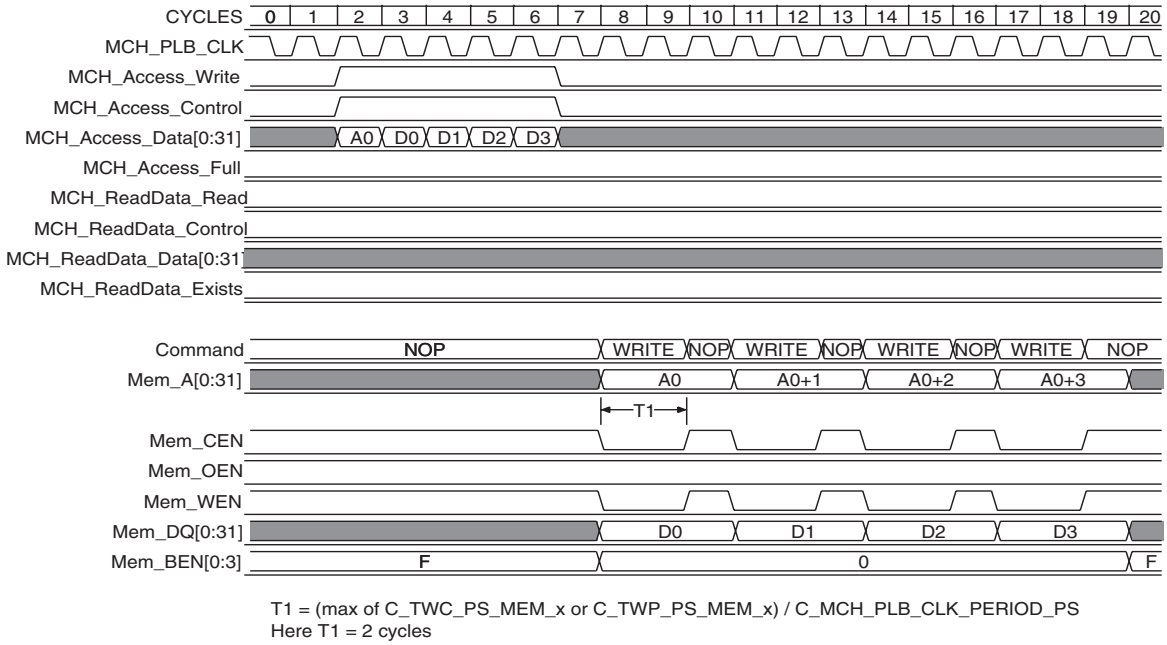
DN	Description	XPS MCH EMC Signals (MSB:LSB)	StrataFlash Signals (MSB:LSB)
3	Data bus	MEM_DQ(24 : 31)	DQ(7 : 0)[1]
	Address bus	MEM_A(8 : 29)	A(21 : 0)
	Chip enable (active low)	GND, GND, MEM_CEN(0)	CE(2 : 0)
	Output enable (active low)	MEM_OEN	OE#
	Write enable (active low)	MEM_QWEN(3)	WE#
	Reset/Power down (active low)	MEM_RPN	RP#
	Byte mode select (active low)	N/A - tie to GND	BYTE#
	Program enable (active high)	N/A - tie to VCC	V_{PEN}

Notes:
1. In x8 configuration, DQ(15:8) are not used and should be treated according to manufacturer's data sheet.

XPS MCH EMC Timing Diagrams

XCL Protocol Cacheline Write Timing Diagrams

Figure 7 shows an XCL channel performing a cacheline write on 32-bit Asynchronous SRAM.



T1 = (max of C_TWC_PS_MEM_x or C_TWP_PS_MEM_x) / C_MCH_PLB_CLK_PERIOD_PS
Here T1 = 2 cycles

Figure 7: **XCL Cacheline Write Operation With 32-Bit Asynchronous SRAM**

Figure 8 shows an XCL channel performing a cacheline write on 32-bit Synchronous SRAM.

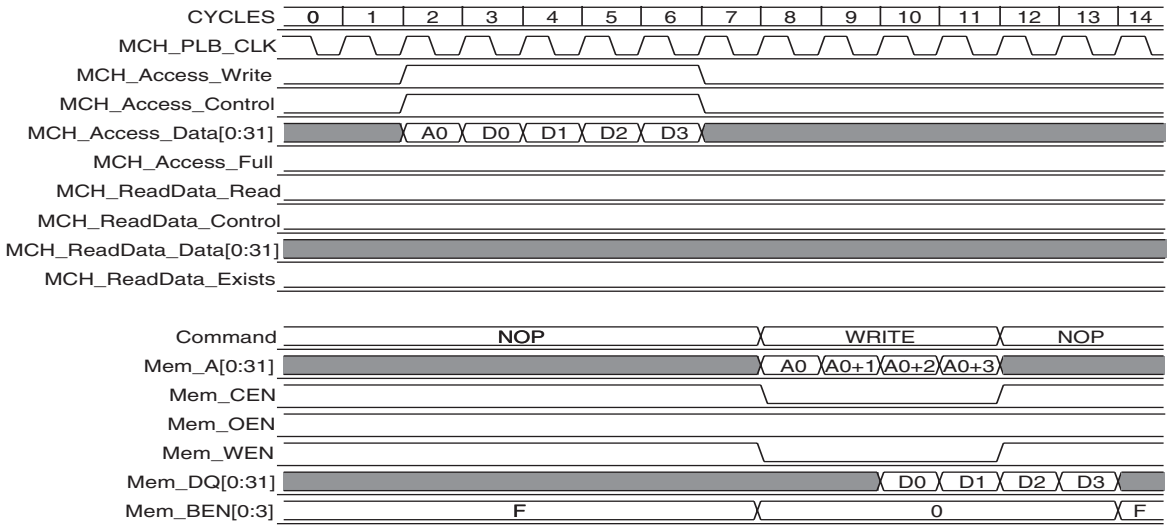
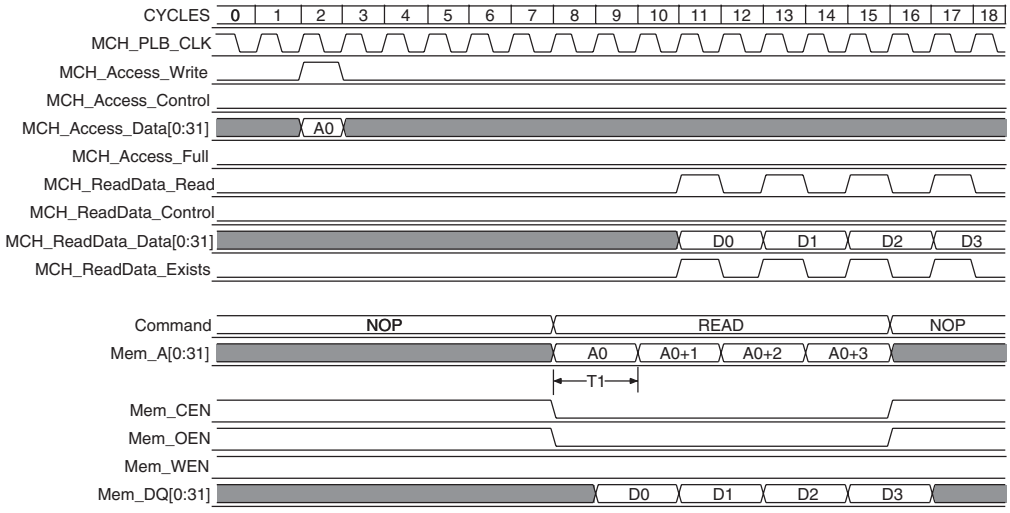


Figure 8: **XCL Cacheline Write Operation With 32-Bit Synchronous SRAM**

XCL Protocol Cacheline Read Timing Diagrams

Figure 9 shows an XCL channel performing a cacheline read on 32-bit Asynchronous SRAM.



T1 = [(Max of C_TAVDV_PS_MEM_x or C_TCEDV_PS_MEM_x) /
C_MCH_PLB_CLK_PERIOD_PS] + 1
Here T1 = 2 cycles

Figure 9: **XCL Cacheline Read Operation With 32-Bit Asynchronous SRAM**

Figure 10 shows an XCL channel performing a cacheline read on 32-bit Synchronous SRAM.

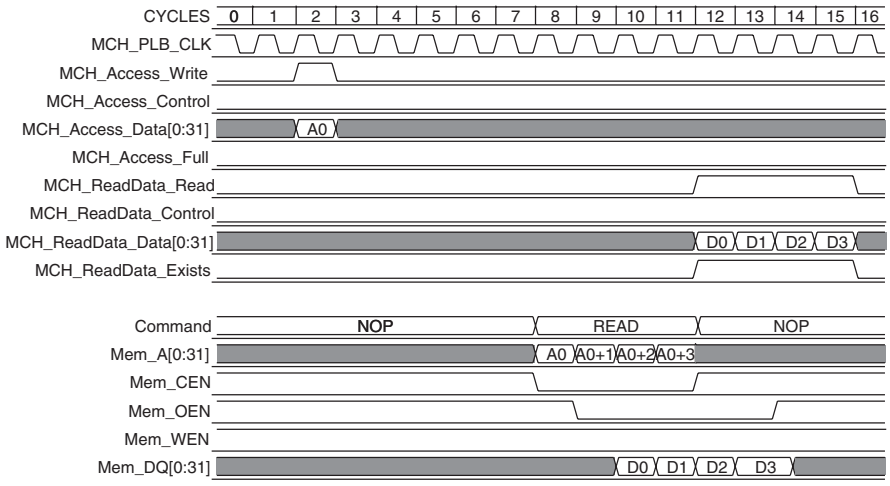


Figure 10: **XCL Cacheline Read Operation With 32-Bit Synchronous SRAM**

XCL Protocol Cacheline Write Read Timing Diagrams

Figure 11 shows an XCL channel performing a cacheline write followed by cacheline read operation on 32-bit Asynchronous SRAM.

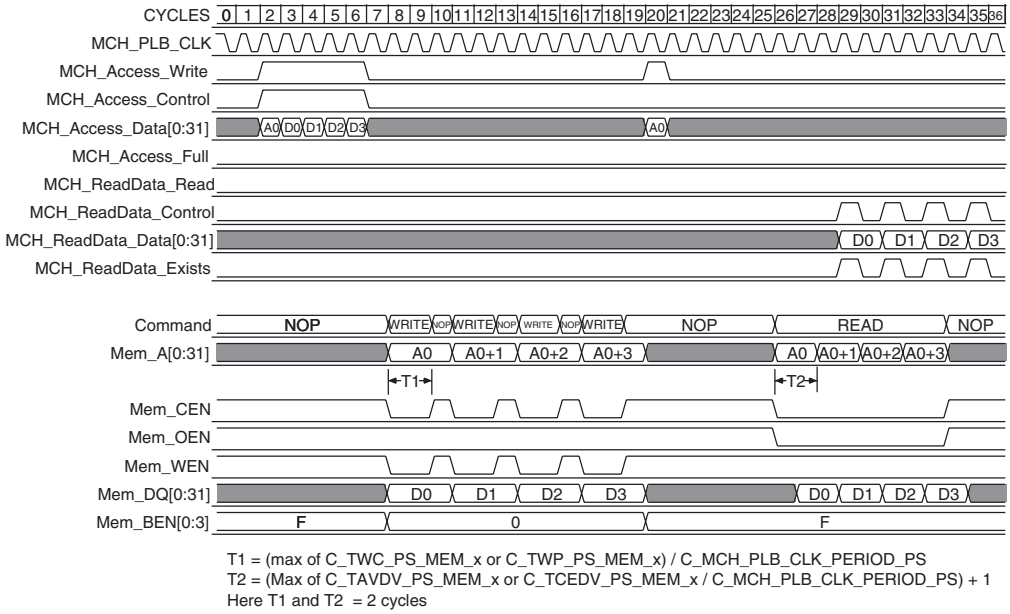


Figure 11: **XCL Cacheline Write Read Operation With 32-Bit Asynchronous SRAM**

Figure 12 shows an XCL channel performing a cacheline write followed by cacheline read operation on 32-bit Synchronous SRAM.

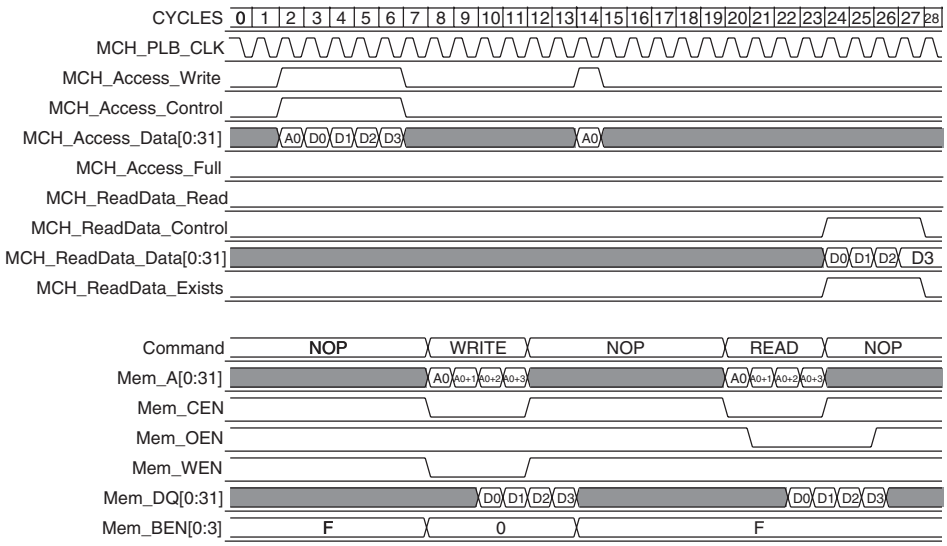
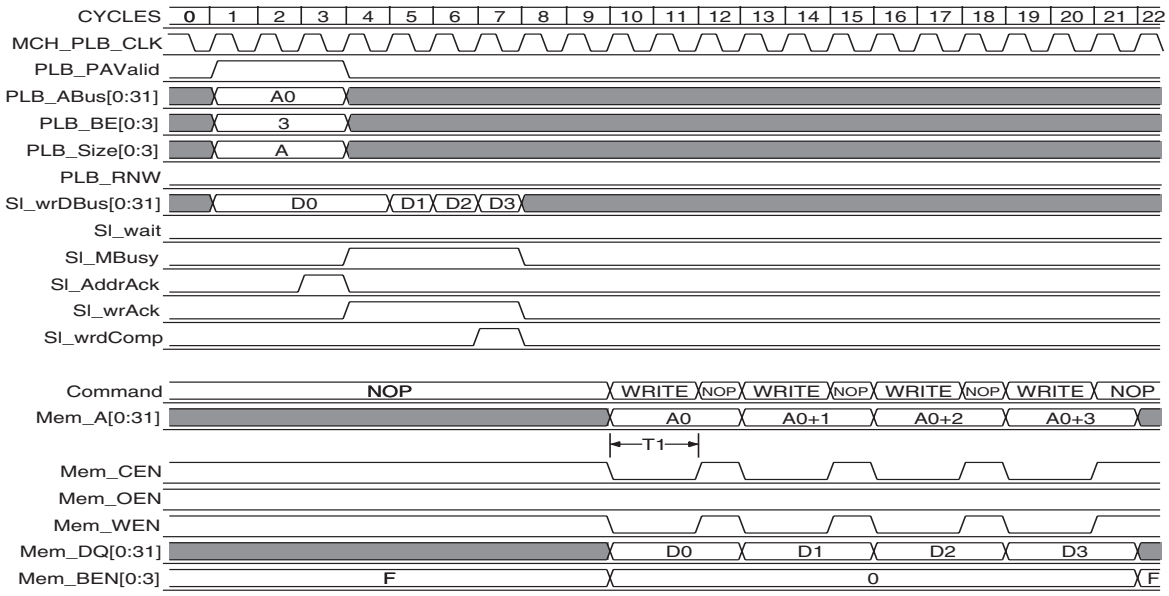


Figure 12: **XCL Cacheline Write Read Operation With 32-Bit Synchronous SRAM**

PLB Burst Write Timing Diagrams

Figure 13 shows PLB burst write operation on 32-bit Asynchronous SRAM.



T1 = (max of C_TWC_PS_MEM_x or C_TWP_PS_MEM_x) / C_MCH_PLB_CLK_PERIOD_PS
Here T1 = 2 cycles

Figure 13: **PLB Burst Write Operation With 32-Bit Asynchronous SRAM**

Figure 14 shows PLB burst write operation on 32-bit Synchronous SRAM.

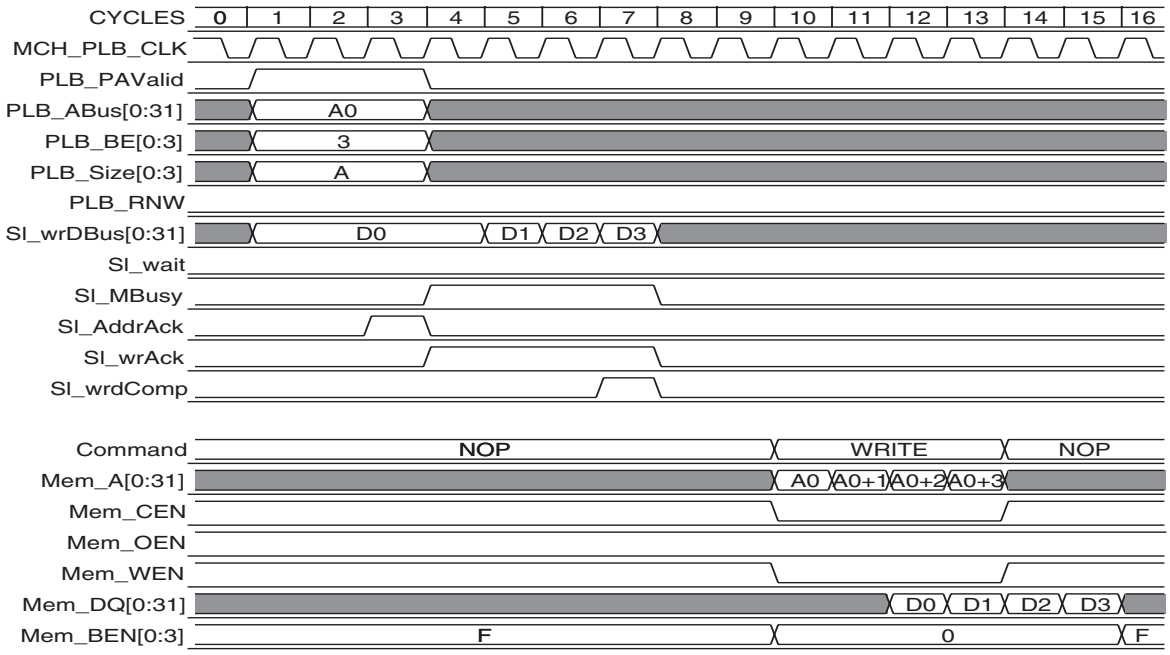
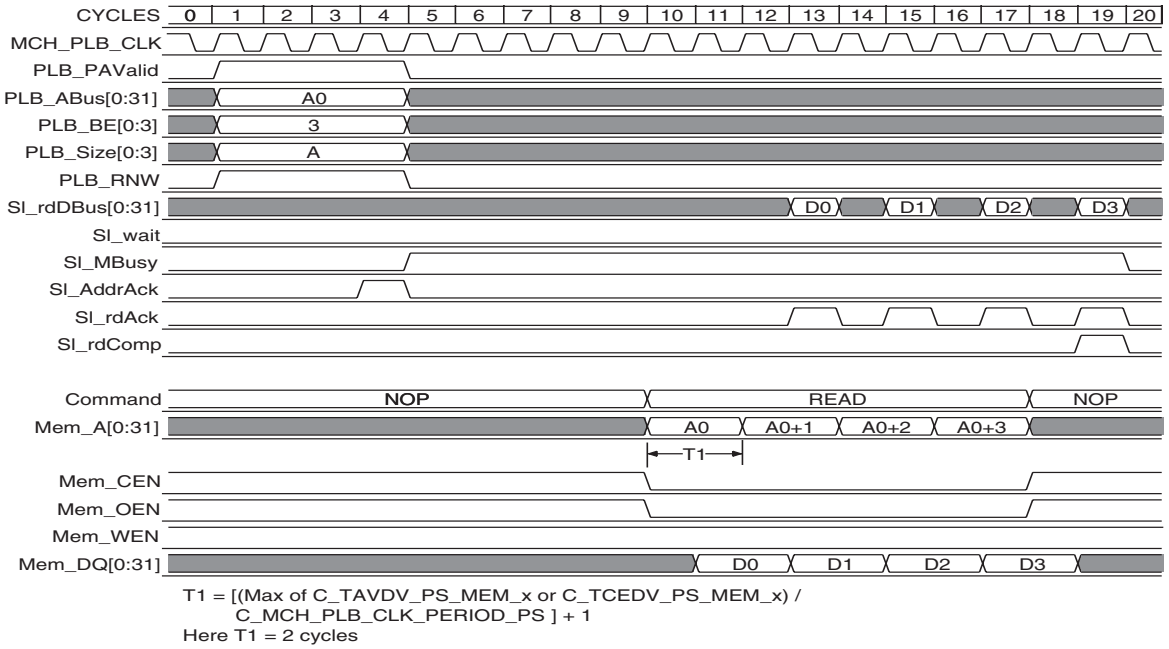


Figure 14: **PLB Burst Write Operation With 32-Bit Synchronous SRAM**

PLB Burst Read Timing Diagrams

Figure 15 shows PLB burst read operation on 32-bit Asynchronous SRAM.



T1 = [(Max of C_TAVDV_PS_MEM_x or C_TCEDV_PS_MEM_x) / C_MCH_PLB_CLK_PERIOD_PS] + 1
Here T1 = 2 cycles

Figure 15: **PLB Burst Read Operation With 32-Bit Asynchronous SRAM**

Figure 16 shows PLB burst read operation on 32-bit Synchronous SRAM.

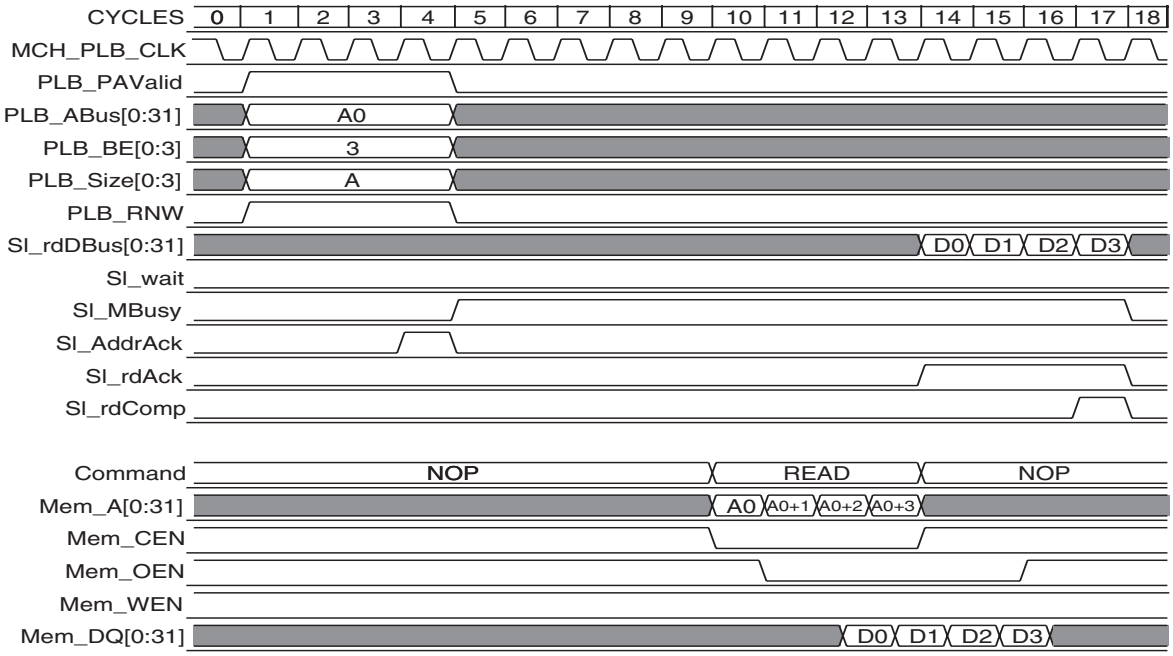


Figure 16: **PLB Burst Read Operation With 32-Bit Synchronous SRAM**

Design Constraints

Timing Constraints

A timing constraint should be placed on the system clock, setting the frequency to meet the bus timing requirements. An example is shown in Figure 17.

```
NET "MCH_PLB_CLK" TNM_NET = "MCH_PLB_CLK";
TIMESPEC "TS_MCH_PLB_Clk" = PERIOD "MCH_PLB_Clk" 10 ns HIGH 50%
```

Figure 17: **XPS MCH EMC Timing Constraints**

Pin Constraints

If external pullups/pulldowns are not available on the MEM_DQ signals, then these pins should be specified to use pullup or pulldown resistors. An example is shown in Figure 18.

```
NET "MEM_DQ<0>" PULLDOWN;
NET "MEM_DQ<1>" PULLDOWN;
NET "MEM_DQ<2>" PULLDOWN;
. . . .

NET "MEM_DQ<31>" PULLDOWN;
```

Figure 18: **XPS MCH EMC Pin Constraints**

Design Implementation

Target Technology

The intended target technology is Virtex and Spartan family FPGAs.

Device Utilization and Performance Benchmarks

Core Performance

Because the XPS MCH EMC core will be used with other design modules in the FPGA, the utilization and timing numbers reported in this section are estimates only. When the XPS MCH EMC core is combined with other designs in the system, the utilization of FPGA resources and timing of the XPS MCH EMC design will vary from the results reported here.

The XPS MCH EMC resource utilization for various parameter combinations measured with Virtex-4(xc4vlx25-11-ff676) as the target device is detailed in Table 13.

Table 13: **Performance and Resource Utilization Benchmarks for Virtex-4 (XC4VLX25-11-FF676)**

Parameter Values									Device Resources			
C_SPLB_DWIDTH	C_NUM_BANKS_MEM	C_NUM_CHANNELS	C_INCLUDE_PLB_IPIF	C_INCLUDE_WRITE_BUFFER	C_MAX_MEM_WIDTH	C_MEMx_WIDTH	C_SYNCH_MEM_x	C_SYNCH_PIPEDELAY_x	Slices	Slice Flip-Flops	LUTs	Fmax (MHz)
32	1	1	0	0	8	8	0	1	238	318	238	197
32	1	4	1	1	8	8	1	2	1088	907	1208	149
32	2	4	1	1	32	16,32	1,1	2,2	1205	1043	1316	127
32	3	3	1	0	32	32,8,16	0,1,1	1,2,2	1070	917	1148	141
32	3	4	1	1	32	8,16,32	1,0,0	2,1,1	1261	1076	1469	129
32	4	3	1	0	32	32,8,16,32	1,0,1,0	2,1,2,1	985	920	1171	143
32	4	4	1	1	32	8,16,8,32	0,0,0,0	1,1,1,1	1260	1052	1404	127
32	4	0	1	1	32	32,8,16,32	1,1,1,1	2,2,2,2	476	613	469	174
128	4	0	1	1	32	32,8,16,32	1,1,1,1	2,2,2,2	444	623	510	185
128	4	4	1	1	32	8,16,8,32	1,0,1,0	2,1,2,1	1414	1088	1556	135

Notes:

1. For all above cases, the parameter C_INCULDE_DATAWIDTH_MATCHING_x = 1
2. For all above cases, the rest of the parameters listed in Table 2 are assigned with the default values
3. All above cases for Virtex-4 are executed by providing MCH_PLB_Clk = 8 ns (125 MHz) period constraint in UCF

The XPS MCH EMC resource utilization for various parameter combinations measured with Virtex-5(xc5vlx30-2-ff676) as the target device is detailed in Table 14.

Table 14: **Performance and Resource Utilization Benchmarks for Virtex-5 (XC5VLX30-2-FF676)**

Parameter Values									Device Resources			
C_SPLB_DWIDTH	C_NUM_BANKS_MEM	C_NUM_CHANNELS	C_INCLUDE_PLB_IPIF	C_INCLUDE_WRITE_BUFFER	C_MAX_MEM_WIDTH	C_MEMx_WIDTH	C_SYNCH_MEM_x	C_SYNCH_PIPEDELAY_x	Slices	Slice Flip-Flops	LUTs	Fmax (MHz)
32	1	1	0	0	8	8	0	1	129	318	216	248
32	1	4	1	1	8	8	1	2	518	894	1065	160
32	2	4	1	1	32	16,32	1,1	2,2	629	1032	1176	156
32	3	3	1	0	32	32,8,16	0,1,1	1,2,2	567	926	1120	150
32	3	4	1	1	32	8,16,32	1,0,0	2,1,1	613	1067	1299	155
32	4	3	1	0	32	32,8,16,32	1,0,1,0	2,1,2,1	497	929	1156	151
32	4	4	1	1	32	8,16,8,32	0,0,0,0	1,1,1,1	572	1047	1248	162
32	4	0	1	1	32	32,8,16,32	1,1,1,1	2,2,2,2	290	615	394	166
128	4	0	1	1	32	32,8,16,32	1,1,1,1	2,2,2,2	266	625	403	163
128	4	4	1	1	32	8,16,8,32	1,0,1,0	2,1,2,1	627	1084	1350	151

Notes:

1. For all above cases, the parameter C_INCULDE_DATAWIDTH_MATCHING_x = 1
2. For all above cases, the rest of the parameters listed in Table 2 are assigned with the default values
3. All above cases for Virtex-5 are executed by providing MCH_PLB_Clk = 6.66 ns (150 MHz) period constraint in UCF

The XPS MCH EMC resource utilization for various parameter combinations measured with Spartan-3e (xc3s500e-5-fg320) as the target device is detailed in Table 15.

Table 15: **Performance and Resource Utilization Benchmarks for Spartan-3e (XC3S500E-5-FG320)**

Parameter Values									Device Resources			
C_SPLB_DWIDTH	C_NUM_BANKS_MEM	C_NUM_CHANNELS	C_INCLUDE_PLB_IPIF	C_INCLUDE_WRITE_BUFFER	C_MAX_MEM_WIDTH	C_MEMx_WIDTH	C_SYNCH_MEM_x	C_SYNCH_PIPEDELAY_x	Slices	Slice Flip-Flops	LUTs	Fmax (MHz)
32	1	1	0	0	8	8	0	1	261	318	238	126
32	1	4	1	1	8	8	1	2	824	905	1181	107
32	2	4	1	1	32	16,32	1,1	2,2	1045	1037	1278	102
32	3	3	1	0	32	32,8,16	0,1,1	1,2,2	851	917	1135	100
32	3	4	1	1	32	8,16,32	1,0,0	2,1,1	1025	1073	1432	102
32	4	3	1	0	32	32,8,16,32	1,0,1,0	2,1,2,1	819	915	1159	102
32	4	4	1	1	32	8,16,8,32	0,0,0,0	1,1,1,1	981	1055	1366	100
32	4	0	1	1	32	32,8,16,32	1,1,1,1	2,2,2,2	410	612	461	107
128	4	0	1	1	32	32,8,16,32	1,1,1,1	2,2,2,2	545	623	514	105
128	4	4	1	1	32	8,16,8,32	1,0,1,0	2,1,2,1	1045	1088	1520	101

Notes:

1. For all above cases, the parameter C_INCULDE_DATAWIDTH_MATCHING_x = 1
2. For all above cases, the rest of the parameters listed in Table 2 are assigned with the default values
3. All above cases for Spartan-3e are executed by providing MCH_PLB_Clk = 10 ns (100 MHz) period constraint in UCF

System Performance

To measure the system performance (Fmax) of this core, this core was added to a Virtex-4 system, a Virtex-5 system, and a Spartan-3A system as the Device Under Test (DUT) as shown in Figure 19, Figure 20, and Figure 21.

Because the XPS MCH EMC core will be used with other design modules in the FPGA, the utilization and timing numbers reported in this section are estimates only. When the XPS MCH EMC core is combined with other designs in the system, the utilization of FPGA resources and timing of the XPS MCH EMC design will vary from the results reported here.

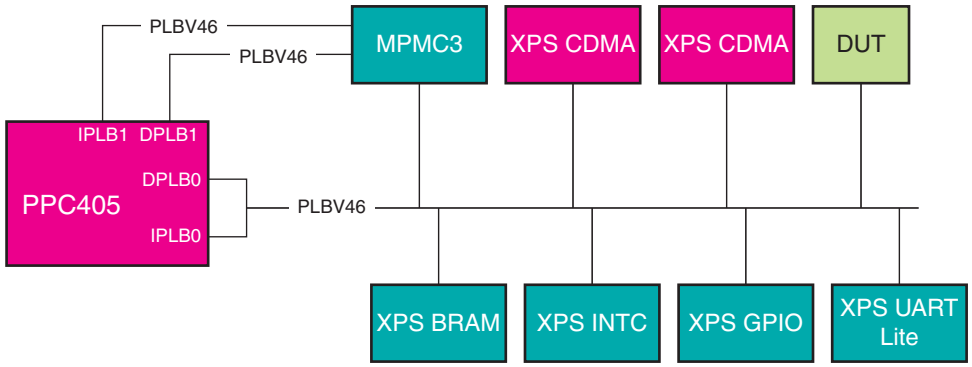


Figure 19: **Virtex-4 FX System**

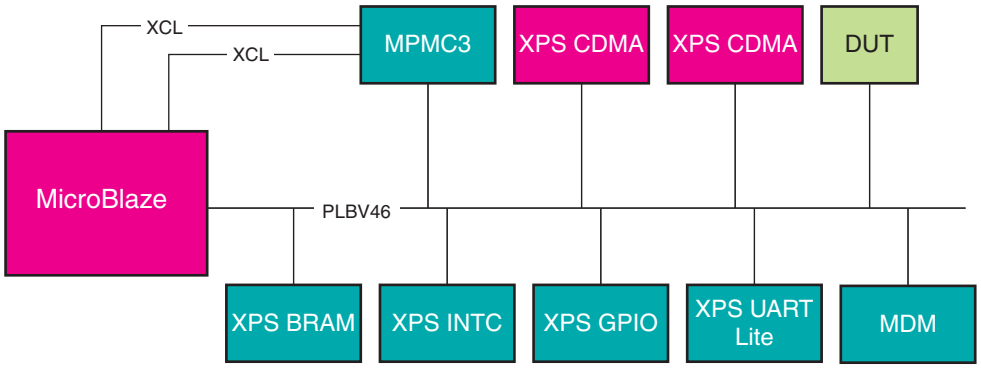


Figure 20: **Virtex-5 LX System**

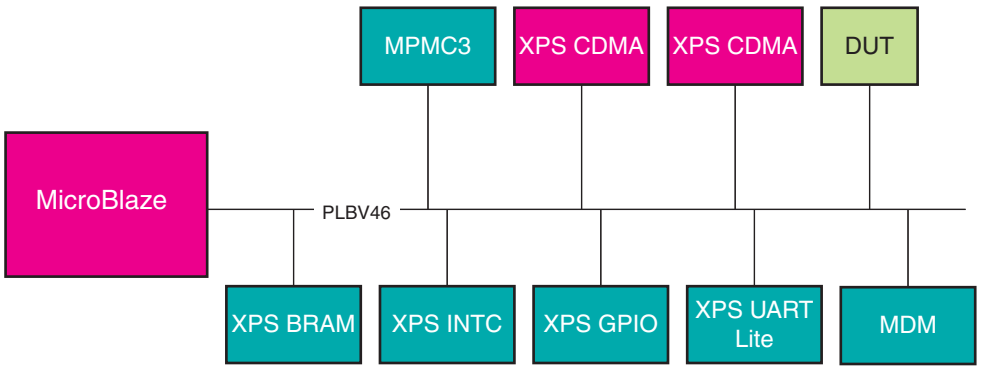


Figure 21: **Spartan-3A System**

The target FPGA was then filled with logic to drive the LUT and BRAM utilization to approximately 70% and the I/O utilization to approximately 80%. Using the default tool options and the slowest speed grade for the target FPGA, the resulting target FMax numbers are shown in Table 16.

Table 16: **XPS EMC System Performance**

Target FPGA	Target f_{MAX} (MHz)
S3A700 -4	90
V4FX60 -10	100
V5LXT50 -1	120

The target fMAX is influenced by the exact system and is provided for guidance. It is not a guaranteed value across all systems.

Specification Exceptions

N/A

Reference Documents

The following documents contain reference information important to understand the XPS MCH EMC design:

1. UG081 *MicroBlaze™ Processor Reference Guide*
2. DS626 *Multi-Channel (MCH) PLBV46 Slave Burst Data Sheet*
3. DS562 *PLBV46 SLAVE BURST Data Sheet*
4. IBM CoreConnect 128-Bit Processor Local Bus: Architecture Specification version 4.6

Notice of Disclaimer

Revision History

Date	Version	Revision
5/8/08	1.0	Initial Xilinx release.
6/24/08	1.1	Incorporated CR468304; updated links in Reference Documents section.
7/21/08	1.2	Added QPro Virtex-4 Hi-Rel and QPro Virtex-4 Rad Tolerant FPGA support.