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Dual range flyback topology for high efficiency at dual voltage mains

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Abstract: This study introduces a dual range flyback converter, which overcomes low efficiency of the conventional flyback converter for universal mains voltages, i.e. 220 and 110 V AC mains. The topology comprises of reconfigurable primary power loops enabled by additional state switches. This combination allows the converter to run in parallel or series modes, enhancing the performance at 220 V AC high line or 110 V AC low line mains. It reduces the voltage rating of devices, supports two working points that operate in boundary conduction mode under fixed frequency and improves the utilisation of the devices. A 100 kHz, 60 W, 110 V AC or 220 V AC to 13 V DC converter has been designed and tested. The experimental results of the proposed converter have been compared against a conventional flyback converter. The results show a small improvement of performance at low voltage (110 V AC) and considerable performance improvement at high voltage (230 V AC): 0.6 and 2.3% efficiency improvement at full load, respectively.

1 Introduction

The power supply unit (PSU) is largely used in electronic apparatus for converting the AC voltage from the mains to low DC voltages, normally 24, 12 or 5 V. The flyback topology is commonly used as the DC–DC converter for the PSU as shown in Fig. 1. This is due to its low material costs, isolation, flexibility and simplicity [1–4]. The efficiency of the flyback converter depends on the input DC voltage, which is rectified from the AC voltage of the mains by a passive rectifier [1, 2]. For low rating applications, a diode bridge-based passive rectifier is the standard solution [5] due to its simplicity and low cost. However, the rectified DC voltage cannot be controlled. Nowadays, two very different ranges of mains voltage exist in the world, the 110 Vac low line (LL) such as that used in the USA and Canada and the 220–230 Vac high line (HL) such as that used in Europe and China [5]. Commercial PSUs need to be compatible with different regions. Thus, a large supported range of mains voltages, from 90 to 264 Vac, is required. This compromises the efficiency [3, 6–8].

Both the efficiency and cost are dominantly related to the switching devices and passive components [3, 7, 9]. The universally compatible flyback converter needs devices and components to withstand both high-voltage stresses when using at HL and high-current stress when using at LL, which results in difficulties in choosing suitable devices and components without compromise of the efficiency and cost. Nowadays, the need for higher efficiency is increasing with efficiency regulation policies, such as energy star and consumer electronics control (CEC), requiring a minimum efficiency of 84–87% [10, 11]. Typical mass production flyback converters are usually about 85% efficiency, particularly at HL operation. Other than meeting the standard an increased efficiency results in a reduction of cooling assembly; thus, both the size and cost of a PSU can be reduced.

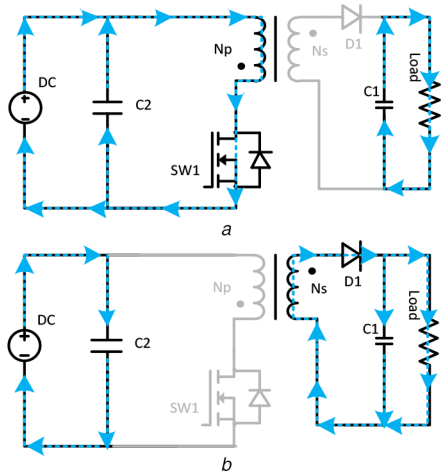

Fig. 1 *Conventional flyback converter current loops in* ***(a)*** ON interval, ***(b)*** OFF interval

There are a few methods to improve the flyback converter efficiency. The synchronous rectification can be adopted in cases of high-output currents to reduce voltage drop on the output rectifier [12–14]. The active clamp [6, 15] or inductor–capacitor snubber circuit design [16, 17] can be used to improve efficiency at cases of high primary spike losses. These occur at every switching event due to the leakage inductance.

Other parameters such as the duty cycle on time (D_{on}) and operation modes (continues conduction, boundary conduction and discontinues conduction) can also be optimised mainly using control and transformer design in order to increase efficiency [2, 7]. Usually, optimal efficiency is achieved at the boundary conduction mode (BCM). The duty cycle on time D_{on} is usually set between 30 and 50% to achieve higher efficiency [2, 3, 18, 19].

The BCM operation gives a good balance between discontinuous conduction mode (DCM) and continuous conduction mode (CCM). The deeper the degree of the CCM, the lower the root-mean-square (RMS) current. This results in lower conduction losses, but higher switching losses due to a larger transient voltage and current at switching events [20]. At the DCM, the secondary rectifier has no current flow at the end of each cycle; thus, lower switching losses are achieved with zero-current switching at the secondary-side rectifier [4]. Quasi-resonant (QR) control [21] can achieve the BCM for wider combinations of input voltages and output loads. Therefore, QR control provides higher efficiency compared with fixed frequency controls. However, the QR control has its own limitations and drawbacks, such as preventing CCM at high load [10], lower efficiency at light load [11] and a wide range of operating frequencies, especially at both 220 and 110 V inputs [8].

Table 1 Performance comparison between conventional flyback converter and DRF converter

Parameter	Conventional	DRF
conduction mode in fixed frequency	BCM at LL and DCM at HL or CCM at LL and BCM at HL	BCM at LL and HL
duty cycle	*D* at LL and *D*/2 at HL	*D* at LL and HL
devices voltage stress	low at LL and high at HL	low at LL and HL
devices current stress	high at LL and low at HL	low at LL and HL

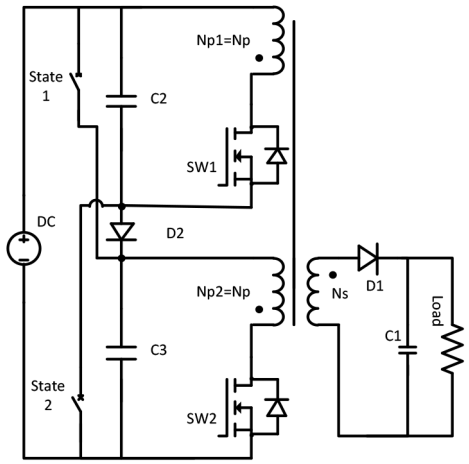

Fig. 2 *DRF converter topology*

The duty cycle D_{on} is set by the turns ratio of the primary and secondary windings (N_p and N_s for the primary and secondary number of turns, respectively) and the converter input and output voltages (V_{in} and V_o), as shown in (1). These parameters also affect the voltage stress [18] on the primary switch and the secondary rectifier, therefore, operating in low D_{on} (N_p/N_s is relatively small) would cause high-voltage stress on the rectifier and high-current stress on the primary switch due to a narrow current pulse [2]. On the other hand, operating in high D_{on} would create the opposite phenomena. Considering these reasons, D_{on} is optimal between 30 and 50%, depending on design constraints [19].

2 Limitation of operation in BCM

To achieve a BCM operation, the design needs to comply with both CCM and DCM limitations. The duty ratio under CCM condition [22] depends on the input voltage, output voltage and the turn ratio (V_{in}, V_o, N_s, N_p, respectively) as follows:

$$D_{on} = \frac{N_p V_o}{N_s V_{in} + N_p V_o} \tag{1}$$

Under DCM, the input power [23] depends on the primary inductance, peak current and the switching frequency (L_p, I_{pk}, F_{sw}, respectively) as follows:

$$P_{in} = \frac{1}{2} L_p I_{pk}^2 F_{sw} = \frac{1}{2} L_p \left(\frac{V_{in} D_{on}}{L_p F_{sw}} \right)^2 F_{sw} = \frac{V_{in}^2 D_{on}^2}{2 L_p F_{sw}} \tag{2}$$

Hence, by combining (1) and (2), setting CCM and DCM, we obtain the conditions for BCM in the form of

$$2 P_{in} L_p F_{sw} = \frac{V_{in}^2 V_o^2 N_p^2}{\left(V_{in} N_s + V_o N_p \right)^2} \tag{3}$$

The parameters L_p, N_p, N_s, V_o are constant and determined by the PSU specification and transformer design while P_{in} is determined by the load and the efficiency of the PSU. Therefore, the only way to ensure BCM, at a certain load, in more than one nominal input voltages is to change the frequency. Hence, for a given load and fixed frequency, there is only one voltage that gives BCM operation. Solving that problem by working in the QR control would cause a new set of problems as explained above. Other than avoiding drawbacks from using the QR control, the fixed frequency operation is attractive due to its simpler control using cheaper parts. The challenge in designing a fixed frequency PSU in universal mains is setting the BCM working point. Setting the BCM at LL would cause inefficient deep DCM operation at HL, contrariwise, setting BCM at HL, would cause lossy deep CCM at LL. Furthermore, setting aside the BCM design problem, increasing the input voltage reduces the on time, which prevents using an optimal D_{on} at both line levels.

In this paper, a new topology of the flyback converter, namely the dual range flyback (DRF) is proposed. This new topology aims to increase the efficiency by operating in BCM and optimal D_{on} in both HL and LL voltages to achieve high efficiency. Comparisons of summarised operation principle between the DRF and conventional flyback converter are shown in Table 1. The specific operation principle of the DRF is introduced in Section 3. Simulation and experimental results of the comparison are shown in Section 4. Conclusions are drawn in Section 5.

3 Proposed converter

3.1 Converter circuit

As shown in Fig. 2, the proposed new topology, the DRF, offers high efficiency at a large range of input voltages and currents by using the most efficient, cost-saving devices and components. It is also important to mention that this new DRF can operate with existing efficiency improvement solutions, such as QR, synchronous rectifier (SR), snubbers or active clamp to further increase the overall converter efficiency.

The DRF compromises two primary sides, which share one coupled three-winding transformer. The circuit of the secondary side of the DRF is identical to the conventional flyback converter, but the voltage rating is lower. Furthermore, using multiple outputs on the DRF secondary will operate in the same way as a conventional multiple-output flyback converter. The number of turns of the two primary sides, Np1 and Np2 are identical as indicated by N_p. The input DC voltage is equally split into two identical capacitors C2 and C3 that are connected in series via a diode D2. The two-state switches are employed for different operation modes: the HL mode (HLM) when high-voltage mains is connected (220–240 Vac) and the LL mode (LLM) when the low-voltage mains is connected (100–120 Vac). The LLM/HLM mode can be detected automatically by a simple comparator or other voltage sense such as in [24]. At the LLM, the two-state switches, State1 and State2, are switched ON, setting the two primary sides effectively in parallel. At the HLM, the state switches are turned OFF, setting the two primary sides in series. Note that the state switches are switched only once at start-up according to the mains voltage, therefore, their switching losses are negligible. Simple metal–oxide–semiconductor field-effect transistors (MOSFETs) with low conduction resistance $[R_{ds(on)}]$ should be selected even if the device switching energy is high due to large output capacitance. These switches could also be replaced by mechanical relays or contactors depending on cost, efficiency, footprint or any other constraints. Although mechanical relay shows better conduction, they have limited life cycle and the hold-up power reduces overall efficiency. These two-state switches can be low-voltage rating because each device needs to withstand half of the DC input voltage rectified from the mains, only at the HLM, assuming balanced voltage sharing. The diode D2 only conducts current when operating at the HLM and no reverse recovery loss occurs because of its non-switch operation in this topology. The voltage rating of the diode is relatively low as it only blocks voltage at the LLM and not the full HL voltage. Therefore, at least the additional components can be low costs with simple cooling requirements.

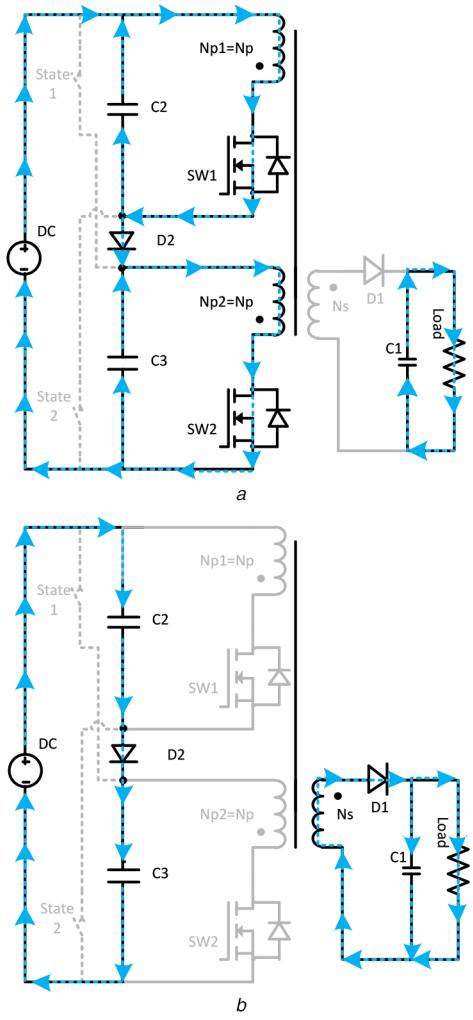

Fig. 3 *DRF current loops in HLM in* ***(a)*** ON interval, ***(b)*** OFF interval

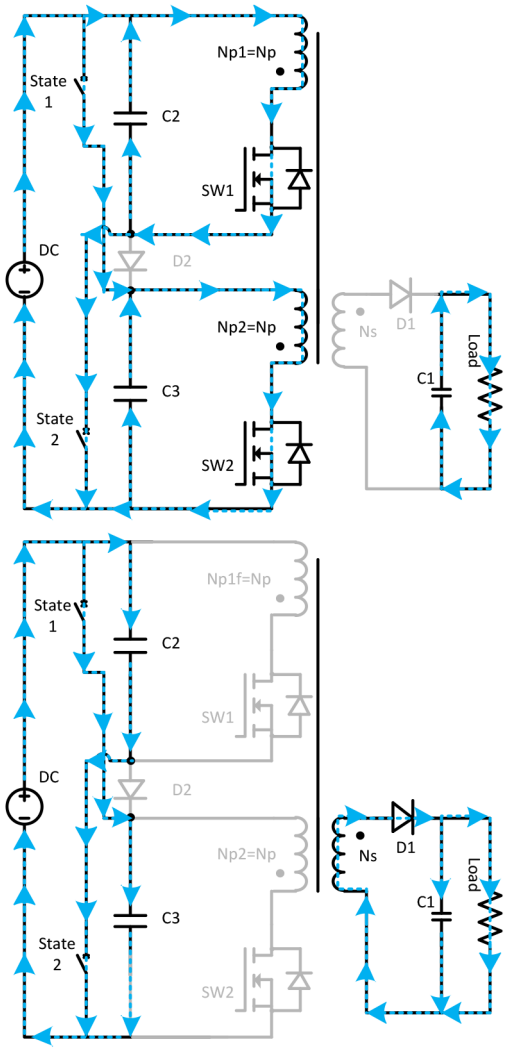

Fig. 4 *DRF current loops in LLM in ON (top) and OFF (bottom) intervals*

3.2 Operating states at the HLM and LLM

To make a comparison, Fig. 1 shows the current loops of the conventional flyback converter at on time and off time For the DRF, as shown in Fig. 3 in the HLM (state switches are OFF), the primary-side input DC loop is closed via D2. The input capacitors are connected in series by D2, which conducts the ripple current. The voltage stress on State1 and State2 are half of the input voltage due to the capacitor voltage balance mechanism, which will be studied in the next sections.

As shown in Fig. 4, in the LLM (state switches are ON), the primary-side input DC loop is divided into two parallel loops, one via State1 and C3 and the other via State2 and C2. The voltage stress on D2 is equal to the rectified DC voltage from the low-voltage AC mains.

The series connection for the HLM and the parallel connection for the LLM offer both low-current and low-voltage requirements of the semiconductor devices and the primary-side input capacitors. The current at the transformer and secondary side are the same as the conventional flyback converter, but the voltage stress on the rectifier is lower. The power loops in both states resemble those of a conventional flyback converter, except that two primary loops are used instead of one. It is possible to switch the power MOSFETs in synchronous or interleaved modes. This paper focuses on the former method due to its lower switching losses and simpler control by using an off-the-shelf flyback controller.

In the HLM, two low-voltage devices are effectively connected in series to reduce the voltage stress. Although the additional diode D2 is in the circuit, the non-switching nature of this diode in the HLM produces no switching loss. For the same power rating, the current is approximately halved in the HLM compared with LLM. Therefore, selecting a simple low-voltage drop diode, regardless of the switching energy, would keep the conduction loss of D2 relatively low. Furthermore, as explained above, the voltage stress on D2 is low.

Similarly, assuming balanced current sharing, in the LLM, each state switch only conducts half of the input current. The non-switching nature of the state switches allows the use of simple low conduction loss devices, regardless of the switching energy. Furthermore, the state switches voltage stress requirement is low as explained above.

Table 2 PSU prototype specification

Section	Parameter	Value
voltage	input LL	110 Vrms (~155 V)
	input HL	220 Vrms (~310 V)
	output	13 V at 60 W
transformer construction	frequency	100 kHz
	maximum flux density	300 mT
	maximum duty cycle	33%
	core	ETD34 at 3C90

4 Simulation and results

4.1 Calculation of device stress

The voltage and current stresses experienced by the parts in the DRF are lower than those of conventional flyback converters due to better utilisation of the device ratings. To illustrate the improvement, a prototype was built. The converter ratings and design specifications are shown in Table 2.

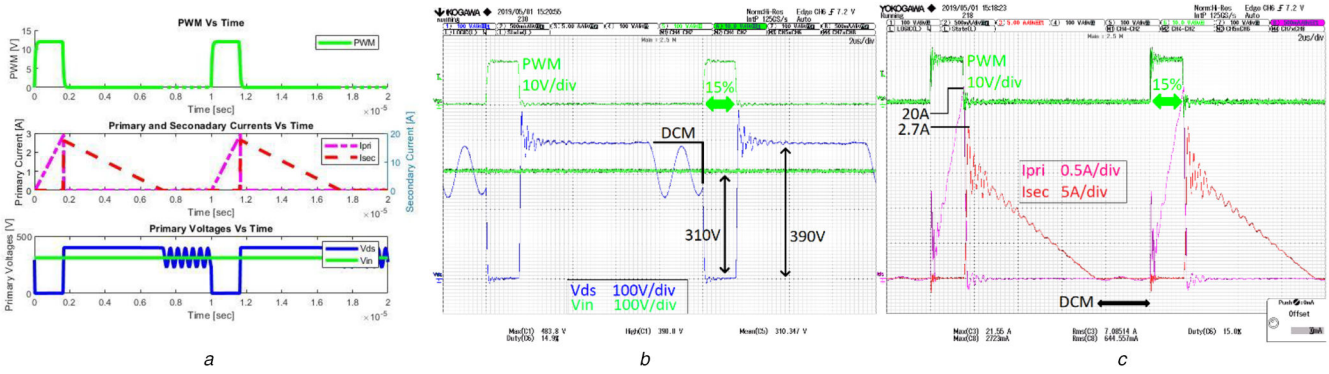

Fig. 5 *Waveforms of conventional flyback converter at HL and full load. Simulated current and voltage waveforms*
(a) Measured current waveforms, ***(b)*** Voltage waveforms, ***(c)*** Operating in DCM. For measurements points, see Fig. 15

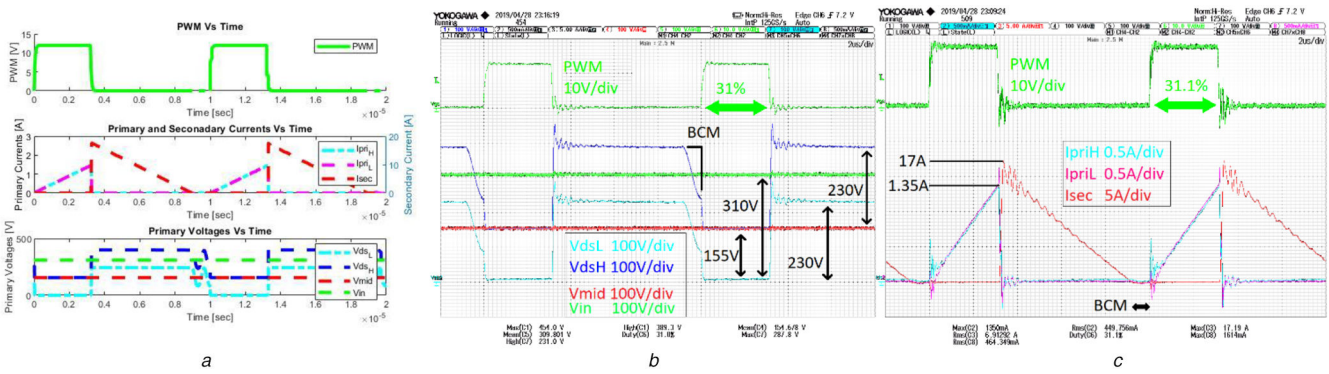

Fig. 6 *Waveforms of DRF converter at HL and full load. Simulated current and voltage waveforms*
(a) Measured current waveforms, ***(b)*** Voltage waveforms, ***(c)*** Operating in BCM. For measurements points, see Fig. 16

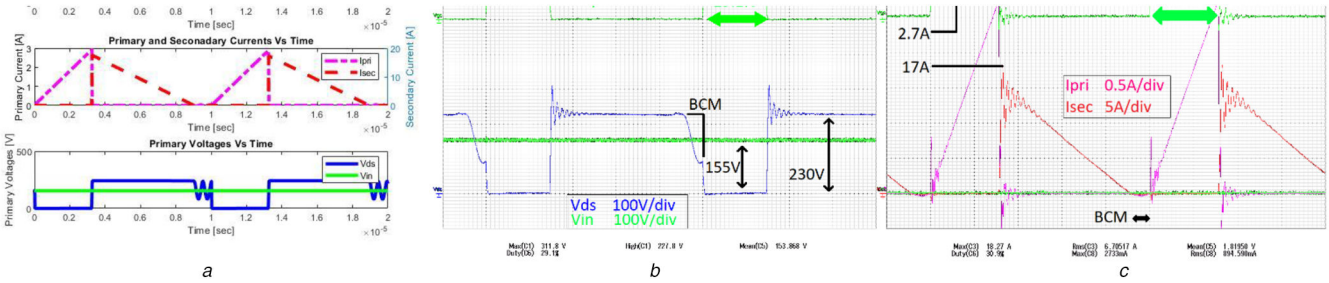

Fig. 7 *Waveforms of conventional flyback converter at LL and full load. Simulated current and voltage waveforms*
(a) Measured current waveforms, ***(b)*** Voltage waveforms, ***(c)*** Operating in BCM. For measurements points, see Fig. 15

In conventional flyback converters, the common practise is to achieve boundary conduction mode (BCM) under LL voltage in order to increase efficiency at nominal load. These requirements, using (3), would set the following transformer parameters: $L_{\text{pri}} = 170\,\mu\text{H}$, $N_{\text{p}} = 30$ and $N_{\text{s}} = 5$. On the basis of the aforementioned design specifications, the stress on power electronic devices, capacitors, rectifiers and magnetics are shown below.

4.2 Simulation of device stress

The proposed circuit has been simulated in the LTspice platform, along with a conventional flyback converter. The simulation waveforms are shown in Figs. 5–8. The results show that the DRF achieves BCM operation as well as constant on time ($D_{\text{on}} = 33\%$) at full load while operating at fixed frequency at both the HL and LL. However, the conventional flyback converter achieves the same condition only at the LL as expected. At HL, the conventional converter operates at deep DCM and a lower on time ($D_{\text{on}} = 15.5\%$) for the same output voltage. It is worth noting that changing the load or input voltage will cause the loss of BCM in both DRF and conventional flyback converters. However, the dual voltage configuration of the DRF allows the current at the DRF being closer to the BCM than that at the conventional counterpart as shown in Figs. 5–8. In terms of the device stress, the simulation shows a similar result to calculation. For example, for the DRF converter, the stress on the power switches, SW1 and SW2, are 233 V and 0.45 A at both HL and LL voltages while the single MOSFET in a conventional flyback converter needs to withstand 388 V (at HL) and 0.9 A (at LL). Similarly, the output rectifier at the HL voltage in the conventional converter operates at 65 V compared with only 39 V in the DRF topology. The simulation verifies the low stresses calculated in the DRF's additional parts (state switches and D2) are about 155 V and 0.25 A_{rms} per device.

4.3 Total devices cost

Although the proposed topology uses more components, the rating of these components is lower than that of a conventional flyback converter, as shown in Table 3, and the total bill of material cost would remain similar. This is validated by cost comparisons shown in Figs. 9 and 10, in which costs of MOSFETs and capacitors at different voltage ratings are compared. All samples from each device are from a single manufacturer. The MOSFETs are supplied by ON semiconductors and the capacitors are from Nichicon. For example, for $R_{\text{ds(on)}} \simeq 0.5\,\Omega$, the cost of two 400 V MOSFETs required in the DRF (£2.75) is similar to one single 650 V MOSFET used in a conventional flyback converter (£2.6). Note

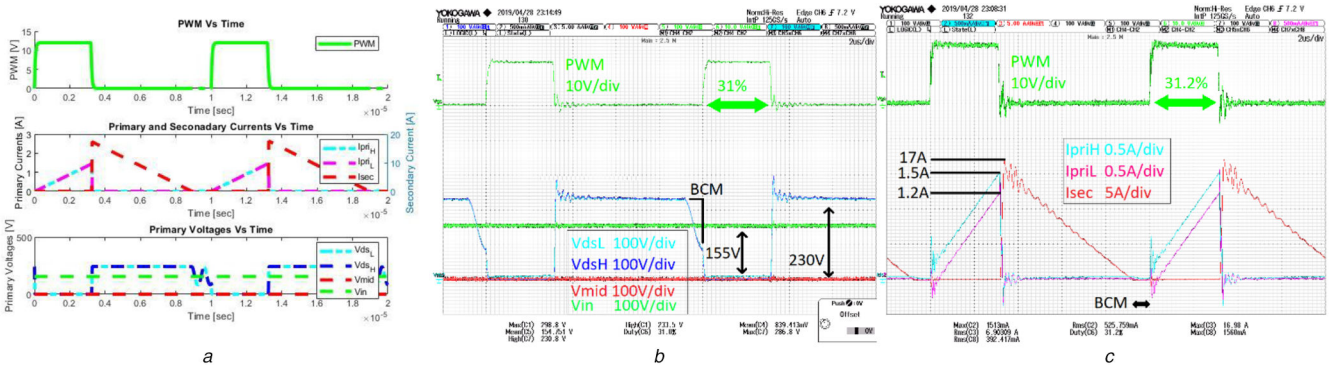

Fig. 8 *Waveforms of DRF converter at LL and full load. Simulated current and voltage waveforms*
(a) Measured current waveforms, ***(b)*** Voltage waveforms, ***(c)*** Operating in BCM. For measurements points, see Fig. 16

Table 3 Device stress comparison between conventional flyback converter and DRF under HL and LLs modes

Devices stress calc/mode	LLM		HLM	
Parameters/converter	Conventional	DRF	Conventional	DRF
on time $D_{on} = L_p I_{pk-tot} F_{sw}/V_{in}$, %	**31**	**31**	*15.5*	**31**
off time $D_{off} = L_p I_{pk-tot} F_{sw} N_s/N_p V_0$, %	62	62	62	**62**
input capacitor voltage, V	**155**	**155**	*310*	**155**
input capacitor peak current $I_{pk} = V_{in} D_{on}/L_p F_{sw}$, A	*2.8*	**1.4***	*2.8*	**1.4***
primary SW's voltage $V_{ds-pri} = V_{in} + V_o N_p/N_s$, V	**233**	**233**	*388*	**233**
primary SW's RMS current $I_{p-rms} = I_{pk}\sqrt{D_{on}/3}$, A	*0.9*	**0.45**[a]	***0.64***	**0.45***
state SW's voltage, V	NA	0	NA	*155*
state SW's current $0.5I_{avg} \simeq 0.5P_{in}/V_{in}$, A	NA	*0.21*[a]	NA	0
input diode voltage, V	NA	*155*	NA	0
input diode current $I_{avg} \simeq P_{in}/V_{in}$, A	NA	0	NA	*0.21*
output rectifier voltage $V_{d-sec} = V_o + V_{in} N_s/N_p$, V	**39**	**39**	*65*	**39**
output rectifier current $I_{p-rms} = I_{pk}\frac{N_p}{N_s}\sqrt{D_{on}/3}$, A	7.7	7.7	7.7	7.7
max field density $B_m = L_p I_{pk-tot}/N_p A_e$, T	0.16	0.16	0.16	0.16

[a]Per device, at the DRF the current divide between capacitors and switches.

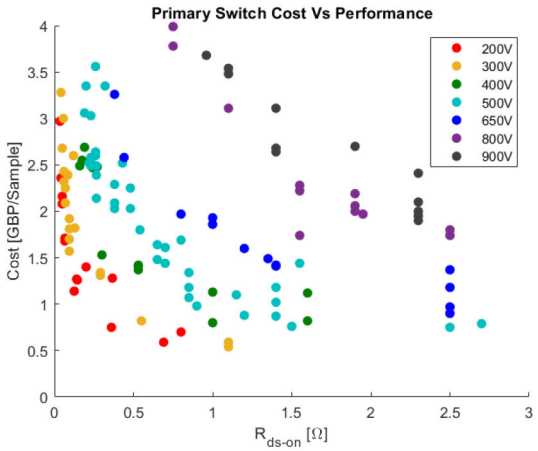

Fig. 9 *OnSemi MOSFET cost data versus $R_{ds(on)}$ for different voltage ratings from DigiKey [25]*

that in this comparison, only one MOSFET package is considered (TO-220) even though the DRF can use smaller and cheaper packages due to the lower stress, and hence lower thermal requirements of each switch. Furthermore, the package of the switch is a major part of its total cost. Therefore, placing both primary MOSFETs in one integrated package would reduce the DRF total cost even more or improve performance for the same cost. The driver for the high side primary switch needs to be added, which will increase the cost of the DRF converter. Note that a simple, low-cost capacitance drive can be considered to minimise this additional cost.

Similarly, for the same capacitance, the cost of two 200 V capacitors is similar to one 400 V capacitor, as shown in Fig. 10. For example, considering a 100 µF capacitance, the cost of the two 200 V capacitors required in the DRF (£2) is cheaper than a single 400 V capacitor used in a conventional flyback converter (£2.5).

The capacitor size is a critical factor in the conventional flyback converter, second only to the size of the magnetic core. The magnetic core used in this DRF prototype is identical to that used in the conventional flyback converters. The winding of the DRF is also identical to that in the conventional by applying similar coupling between the primary windings and secondary windings. The only variation of the transformer is the pinout. The volume of capacitors is also determined by their voltage ratings. With the same capacitance, higher-voltage rating results in larger volume as shown in Fig. 11. For example, for 100 µF capacitance, the volume of two 200 V capacitors required in the DRF (6.5 cm^3) is less than a single 400 V capacitor used in a conventional flyback converter (7.5 cm^3).

The additional parts of the DRF topology, such as the state switches or the input diode, have a very low stress (voltage and current), as shown in Table 3; thus, small and cheap parts [27, 28] can be used without the heatsink. Therefore, the size and cost of the PSU will not be increased significantly. Furthermore, the cost increase of these parts can be easily offset by the output rectifier diode/switch of the DRF converter, which has a lower-voltage rating compared with the conventional flyback converter [29]. Therefore, a lower-cost solution for the same performance can be selected or better performance for the same cost by using low forward voltage drop diodes or a low $R_{ds(on)}$ synchronous rectifier. Note that the state switch speed can be extremely slow without affecting performance, due to the single switch nature of their

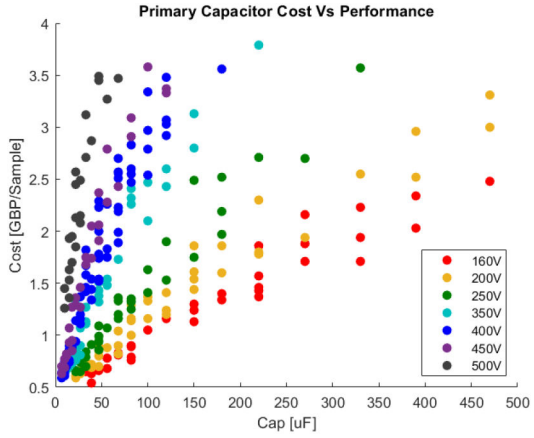

Fig. 10 *Nichicon UCY series capacitors cost data versus capacitance for different voltage ratings from DigiKey [26]*

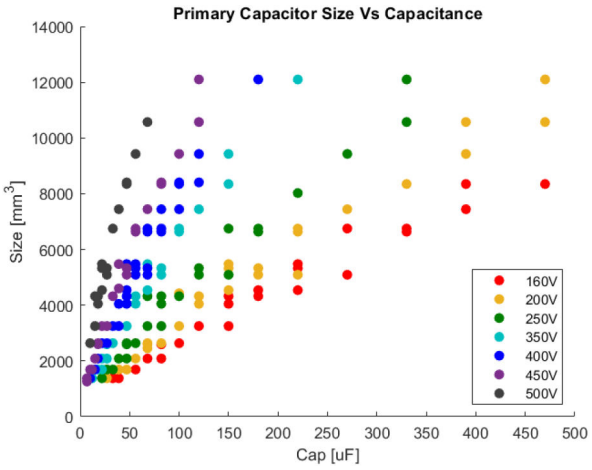

Fig. 11 *Nichicon UCY series capacitors size data for different voltage ratings extracted from DigiKey [26]*

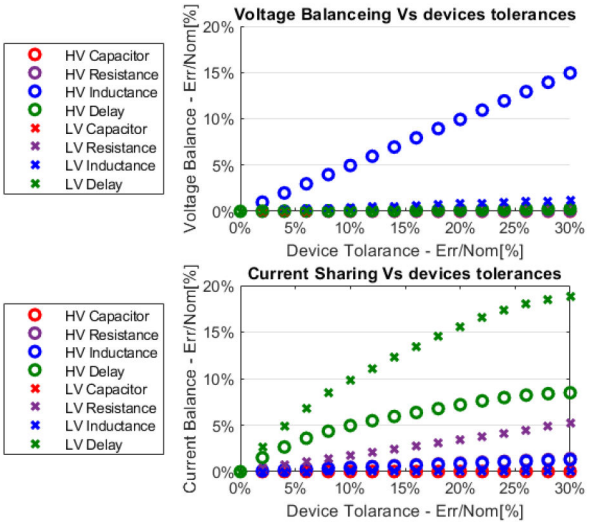

Fig. 12 *DRF voltage balance and current sharing versus devices tolerances in HL and LLs simulation results*

operation. Therefore, a simple gate driver solution could be used minimising the cost and footprint.

4.4 Voltage balancing and current sharing

The DRF topology can use low stress (current and voltage) devices only by ensuring that the voltage balances equally between the input capacitors and that the current is shared evenly between the MOSFETs. At LLM operation, the voltage is always balanced between the capacitors because the state switches force them into a parallel connection. In the HLM operation, the poor balance between the capacitors would create uneven voltage stress on the devices; thus, one of the devices would experience higher-voltage stress. This would reduce the DRF low device stress attractive feature. To study the causes of misbalancing, the DRF converter was simulated with various parameters differing between the two sub-flyback circuits. These parameters include gate drive delay time, transformer primary inductance L_p, input capacitance C_{in} and MOSFET resistance $R_{ds(on)}$. This parameter variation models device tolerance differences between the two circuits. The simulation results show that the dominant parameter in voltage misbalancing, at HLM only, is the primary inductance. The results show that for every 1% deviation of the primary inductor value away from its nominal value $(L_{p1} - L_{p2}/L_{p-nom})$ a 0.5% imbalance of capacitor voltage occurs $(V_{cap1} - V_{cap2}/V_{nom})$. For example, at 10% inductance deviation (instead of two primary inductances of 170 μH: one inductor of 179 μH and the other 161 μH) the capacitor imbalance would be only 5% voltage misbalanced (instead of the 310 V being divided into two equal parts of 155 V, we get 159 and 151 V). The results of the simulation are shown in Fig. 12.

The maximum inductance error (30%) as simulated is extremely high for two windings wound on the same core with the same number of turns. Measurement of the DRF transformers has shown <1% error.

To explain the mechanism of voltage imbalance caused by inductance deviation, two inductances L_{p1} and L_{p2} are assumed for the sub-flyback1 and sub-flyback2, respectively. When both switches are ON, the reflected voltage that sub-flyback1 induces on sub-flyback2 is shown in

$$V_{2-ref} = V_{L_{p1}} \frac{N_{p2}}{N_{p1}} = V_{L_{p1}} \sqrt{\frac{L_{p2}}{L_{p1}}} \tag{4}$$

Assuming X% deviation between the inductances (L_{p1} is X/2% lower than nominal while L_{p2} is X/2% higher) would get

$$V_{L_{p1}} = V_{2-ref} / \sqrt{\frac{L(1 + X/2\%)}{L(1 - X/2\%)}} \tag{5}$$

Similarly, analysing the other sub-flyback circuit reflected voltage would lead to

$$V_{L_{p2}} = V_{1-ref} / \sqrt{\frac{(1 - X/2\%)}{(1 + X/2\%)}}$$

When the switches are ON, the voltage drop on them is negligible. Therefore, the capacitor voltage is approximately the reflected voltage. In consequence, the reflected voltage sum is the input voltage, as shown in

$$V_{in} \simeq V_{cap1} + V_{cap2} \simeq V_{L_{p1}} + V_{L_{p2}} \tag{6}$$

Combining (6) and (5) and assuming $X = 10\%$ would get

$$V_{L_{p1}} \simeq V_{cap1} \simeq V_{in}/2.05 \tag{7}$$

$$V_{L_{p2}} \simeq V_{cap2} \simeq V_{in}/1.95 \tag{8}$$

$$V_{balance} = \frac{V_{cap1} - V_{cap2}}{V_{nom}} 100\% = \frac{(V_{in}/2.05) - (V_{in}/1.95)}{V_{in}/2} = 5\% \tag{9}$$

About the same results as the simulation (at 10% induction tolerance, the misbalance error is 5%). Therefore, any other parameter difference between the sub-flyback circuits, such as capacitance, resistance or gate delay time, would not significantly affect the voltage balancing. The inductance mechanism forces balancing through the means of reflected voltage. The sub-flyback

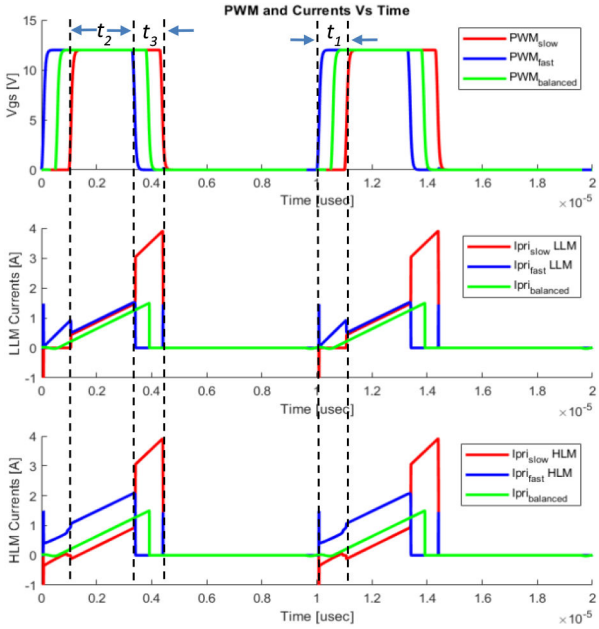

Fig. 13 *Uneven delay time: fast driver (blue), the slow driver (red) and nominal drive (green) time. Top: pulse-width modulation, middle: primary-side LLM currents and bottom: primary-side HLM currents*

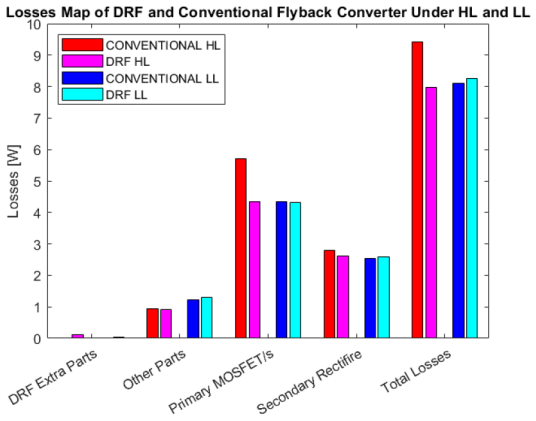

Fig. 14 *Loss maps of DRF and conventional flyback converters in LLM and HLM*

circuit would act according to the reflected voltage (positive or negative current via the MOSFET) until the voltage is balanced.

The gate drive delay parameter, which depends on the driver integrated circuit, the resistance of the route and capacitance between the gate and source of the MOSFET will not cause voltage imbalance as explained above, but will have an effect on current sharing.

As shown in Fig. 13, during the time interval t_1, the sub-flyback with the faster gate drive would conduct the current $I_{\text{pri}_{\text{fast}}}$ before the other sub-flyback with the slower gate drive starts conducting. In this interval, at the HLM, the inductance at the primary side creates a negative current on the other sub-flyback as $I_{\text{pri}_{\text{slow}}}$, forcing a higher $I_{\text{pri}_{\text{fast}}}$ current to compensate. This current flows through the body diode of the MOSFET, causing losses of the converter. At the LLM, the voltage is balanced, thus $I_{\text{pri}_{\text{slow}}} = 0$. Both the devices are ON at the interval t_2 after the delay. At the LLM, the current is equally shared due to the parallel connection if assuming negligible $R_{\text{ds(on)}}$ of two MOSFETs, thus the deviated current at the interval t_1 will be converged to zero. At the HLM, each sub-flyback primary inductance forces current continuity, thus the unbalanced currents keep their deviation in this interval. At the end of the conduction period, the fast system turns off first, leaving the slow sub-flyback MOSFET conducting the peak current and experiencing high-current stress (same current as conventional flyback converter) as shown as the interval t_3. This peak current discharges the input capacitor of the slower gate drive sub-flyback at the HLM. During t_1 the primary inductance would balance that voltage. Therefore, in order to achieve balanced stress on DRF devices, the most critical parameters are the primary inductance; which dictates the voltage balancing, and the driver delay time; which influences the current sharing. The matched parameters between the two sub-flyback circuits enable the voltage and current sharing equally.

4.5 Efficiency and power losses comparison

To compare the efficiency between the DRF and the conventional flyback converters, we first simulated the loss maps of these two converters and plotted them by using PLECS simulation tools. Both simulation and calculation show a similar loss map distribution at full load condition under both HL and LL. The simulation results are shown in Fig. 14. The DRF shows a large loss reduction at the HL operation predominantly caused by lower primary switch losses. This is because, at HL operation, the switching MOSFET's voltage stress in the DRF is lower compared with the conventional flyback converter, resulting in lower clamping and turn-on losses. In addition, the DRF shows moderate loss reduction at both the HL and LL operations due to lower conduction losses in the semiconductors. This is because, with the DRF, the stress on the primary MOSFET and the secondary rectifier is lower, thus enabling the selection of better devices with lower conduction losses for the same price.

Losses of other devices in the DRF, such as the transformer core and the diode bridge, are similar to the conventional flyback converters at both operations. The DRF primary switch turn-off

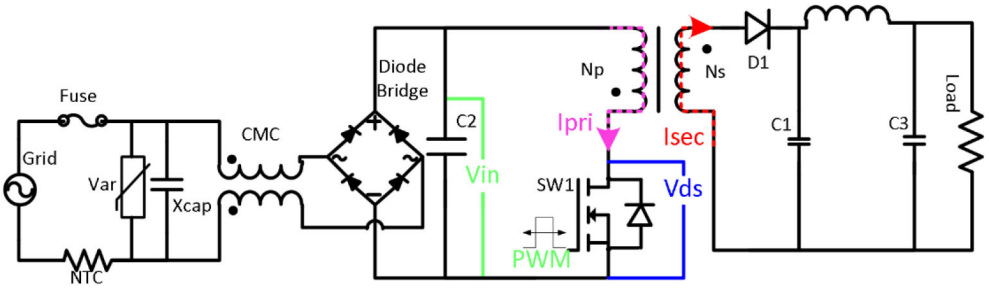

Fig. 15 *Schematic representation, measuring points and variables in EVB and simulation for the conventional flyback converter*

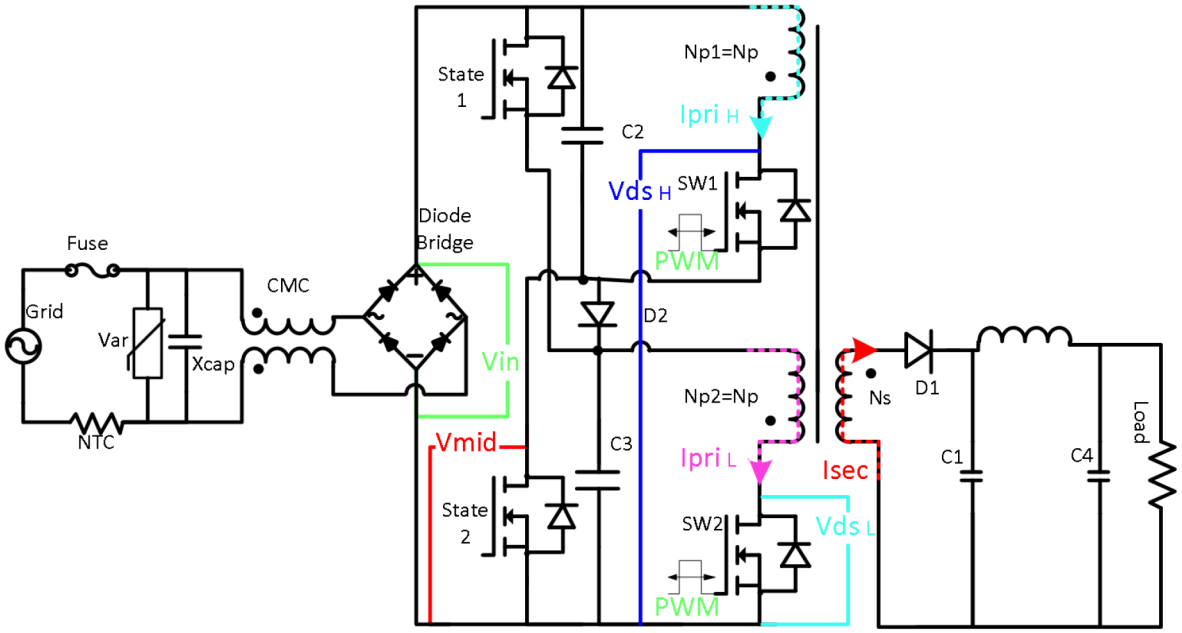

Fig. 16 *Schematic representation, measuring points and variables in EVB and simulation for the DRF converter*

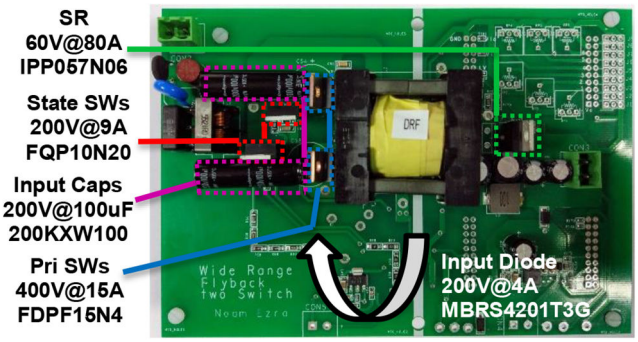

Fig. 17 *EVB and components parameters for the DRF converter*

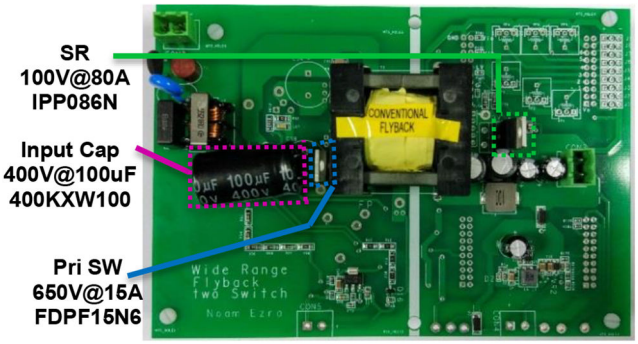

Fig. 18 *EVB and components parameters for the conventional flyback converter*

loss is slightly higher when compared with the conventional flyback converter due to the switching of two MOSFETs instead of one. Nevertheless, these losses are less significant than the clamp and the turn-on losses, in which the DFR shows significant improvement. Overall, the DRF shows higher efficiency when compared with the conventional flyback converter. The losses in the extra parts of the DRF (input diode at HLM or state switches at LLM), shown in the DRF extra parts losses column, are small as explained earlier, and therefore, do not affect the total efficiency. These results support the DRF advantages, such as BCM and constant D_{on}, for designed load, and the ability to use smaller and cheaper devices.

4.6 Experiments results

To experimentally assess the simulation results, a prototype evaluation board (EVB) of the DRF converter was designed and fabricated. A conventional flyback converter was also developed for comparison. The schematic representation of the EVB for both conventional flyback converter and DRF are shown in Figs. 15 and 16, respectively. As shown in Fig. 17, the DRF uses two low-voltage switches and two low-voltage capacitors (400 and 200 V, respectively). In the conventional flyback converter shown in Fig. 18, only one high-voltage switch and one high-voltage capacitor (650 and 400 V, respectively) are used. The output rectifier of the DRF utilises lower-voltage rating devices that operate at 60 V for both HLM and LLM, which are lower than the 100 V of the conventional flyback converter due to lower-voltage stress as calculated above. In the DRF converter, three extra devices rated at 200 V are assembled: the input diode (D2 is surface mounted component (SMC) on the bottom side) and the two-state switches. All the device part numbers are shown in Figs. 18 and 17. To make a fair comparison between the converters, the same magnetic core (ETD34 3C90) were used in the transformers for the DRF and conventional flyback converter.

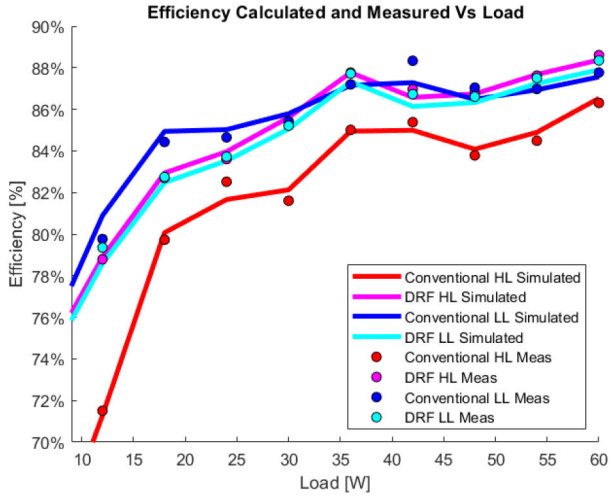

Fig. 19 *Efficiency compare between DRF and conventional flyback converters measured in EVB and PLECS simulation in HLM and LLM*

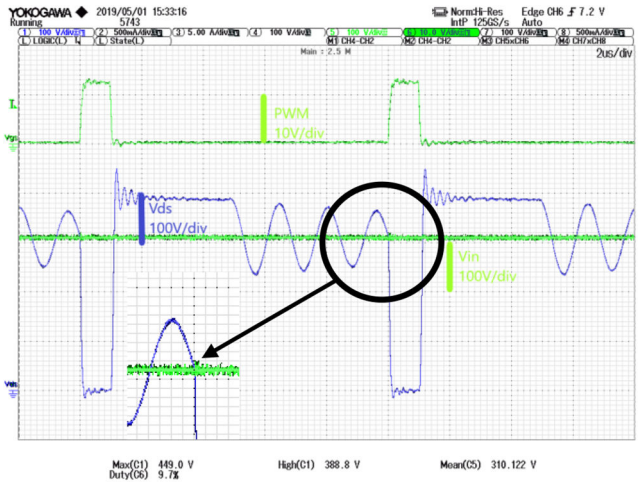

Fig. 20 *Waveforms of conventional flyback at HLM 24 W load with a turn-on voltage of 310 V*

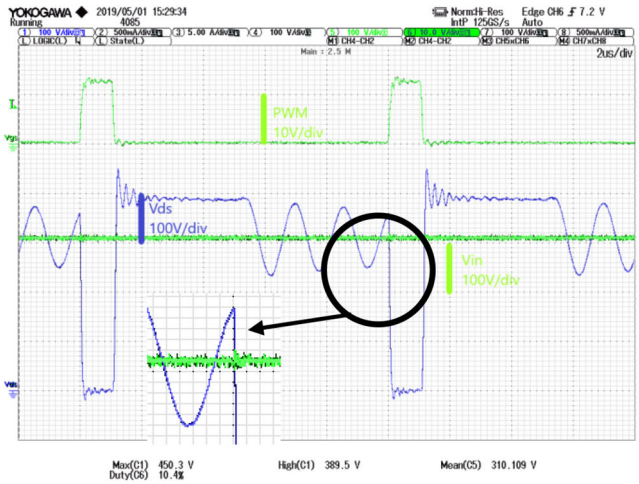

Fig. 21 *Waveforms of conventional flyback at HLM 30 W load with a turn-on voltage of 360 V*

The same amount of copper, i.e. the same length and type of winding wires were used for the transformer, but they were wound differently to accommodate different topologies of the DRF and conventional flyback converter. The primary winding was made using two windings connected in parallel for the conventional flyback converter or divided into two sub-flybacks for the DRF. Therefore, there is no difference between the size or cost of the DRF and the conventional flyback converter transformer, the only difference is the pinout. To include gate drive losses for the total efficiency, the driver power in both designs is supplied by extra auxiliary windings instead of external sources.

The EVB results are divided into two sections: efficiency comparison and operational results:

(i) The efficiency results measured on the EVB at different loads from 10 to 100% compared with the simulated results are shown in Fig. 19. The measured results correlate with the simulated results. In the DRF converter at both HL and LL, the efficiency is similar due to similar devices stress and operation mode (BCM). The conventional flyback converter efficiency at LL is similar to these results, especially on high loads due to similar conditions. However, in the conventional flyback converter at HL, the efficiency performance is lower at any given load, with more than 2% decrease at full load. Therefore, the overall performance of the DRF topology is better compared with the conventional flyback converter.

Note that the efficiency increases with the load increase as expected due to the BCM design at full load. The fluctuations in the efficiency are due to the MOSFET turn-on losses, which vary with the load according to the idle ring. The higher fluctuations occur on conventional flyback converter under HL, which suffers from the highest turn-on losses due to the highest voltage stress on the MOSFET. For example, in the HLM, the efficiency of the conventional flyback converter is higher at 24 W compared with at 30 W even though the former is deeper in DCM. As shown in Fig. 20, at the lighter load, the turn-on voltage 310 V is lower compared with the higher load at 360 V shown in Fig. 21, meaning fewer turn-on losses at the lighter load.

(ii) Steady-state operation waveforms measured on the EVB at ten different loads from 10 to 100%. Figs. 5–8 show the waveforms measured on the EVB and waveform simulated by LTspice at full load for both converters under the HL and LL. The results of the simulation and the measurements are similar. For example, at full load, both the simulation and measurement current peaks are about 1.4 A for the DRF and 2.8 A for the conventional flyback converter. Similarly, the voltage stress and duty cycle in the conventional flyback converter at LL and in the DRF for both lines are 230 V and 31%, respectively, while in the HL conventional flyback converter, the results are 390 V and 15%. Furthermore, the mode of operation (BCM or DCM) in the EVB verify the simulations.

Therefore, it is possible to see the negative current at HLM at the beginning of the cycle due to the balancing mechanism as shown in Fig. 6*b* current waveform. The voltage balancing mechanism is extremely fine, more than 300 Vdc divided into two capacitors with <0.15 V imbalance between them. Furthermore, in Fig. 8*b*, current waveform, the current sharing between the two MOSFETs is not perfect. This is as expected due to a variance in the matching between the two sub-flybacks.

5 Conclusion

This paper introduces a new flyback converter, the DRF converter and its main benefits on increasing the overall efficiency at dual voltage mains. In this paper, the DRF has achieved considerably higher efficiency at 220 Vac as the input compared with a conventional flyback converter and slightly higher efficiency at 110 Vac. The DRF topology is optimised to both high and low mains, while the conventional flyback converter can be optimised only to one of them. The proposed topology enables BCM operation with the same duty cycle (D_{on}) for two different line voltages (110 and 220 Vac), at the full load, while working with a fixed frequency and using low-voltage devices. Although the DRF parts count is higher, the total cost and size are similar to a conventional flyback converter due to a simpler requirement from the parts, which experience less voltage and current stress. Challenges of voltage and current balancing of the DRF have also been assessed and discussed.

The experimental results from the prototype support the calculation and simulation. Comparison between the DFR and

conventional flyback converter also shows the expected benefits from the DRF. The results show that the proposed topology has lower losses and less stress on the parts when compared with the conventional flyback converter and this DRF could replace the conventional flyback for universal AC mains, i.e. both the 220 and 110 Vac.

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