Dynamic Logic and Latches II:

Practical Implementation Methods and Circuits Examples used on the ALPHA 21164

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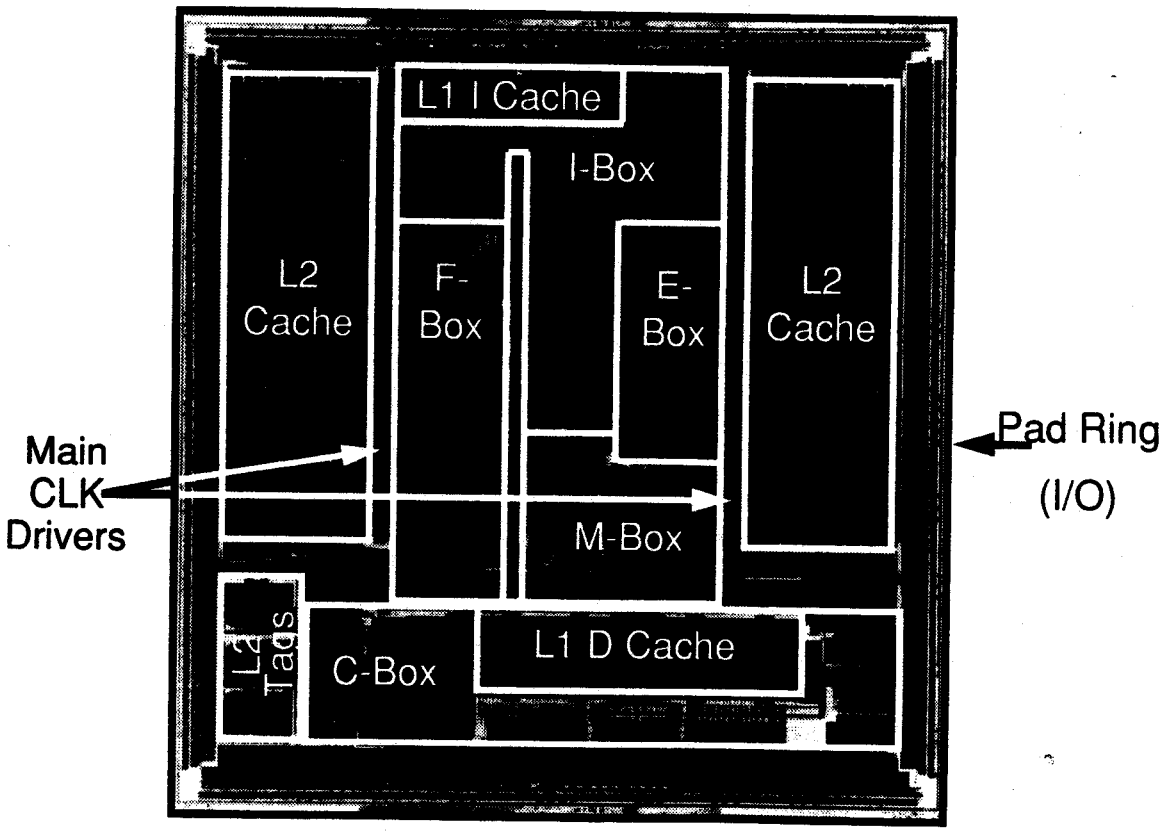
Outline

- introduction to ALPHA 21164
- Latching
- Clocking
  - Distribution
  - Analysis
- Dynamic Logic
  - Single-rail
  - Dual-rail
- Circuit Examples.

Introduction to ALPHA **21164**

- ❒ Second generation design
- ❒ Quad-issue, in-order execution
- ❒ 14 gates per cycle including latches

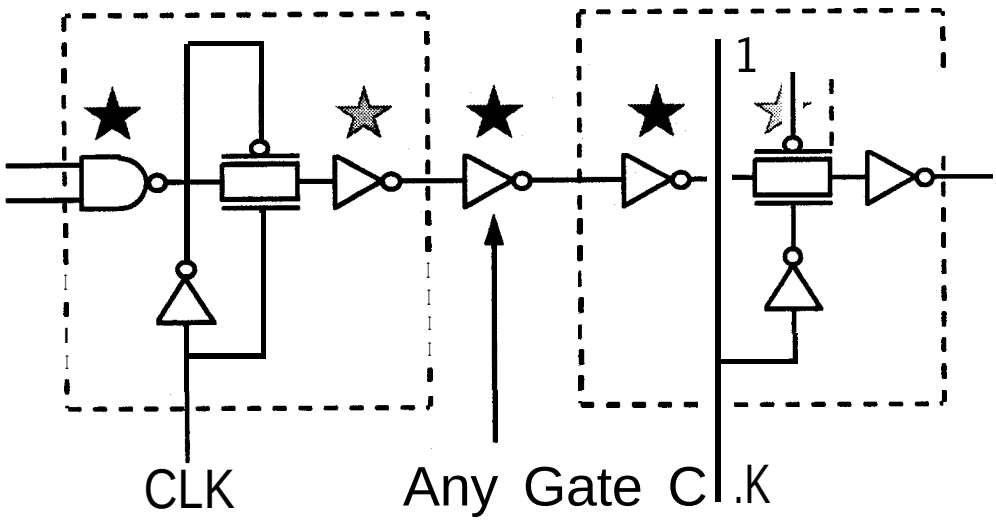
	Ø.5 µm process	0.35 µm process
Transistor Count	**9.3 Million**	**9.66 Million**
Die Size	16.5 mm x 18.1 mm	14.4 mm x 14.5 mm
Power Supply	**3.3V external**	**3.3V external**
	3.3V internal	**2.0V internal**
WC Power Dissipation	**50W @ 300 MHz**	**25W @ 433 MHz**
Target Cycle Time	**300 MHz**	**433 MHz**



Latching - Overview

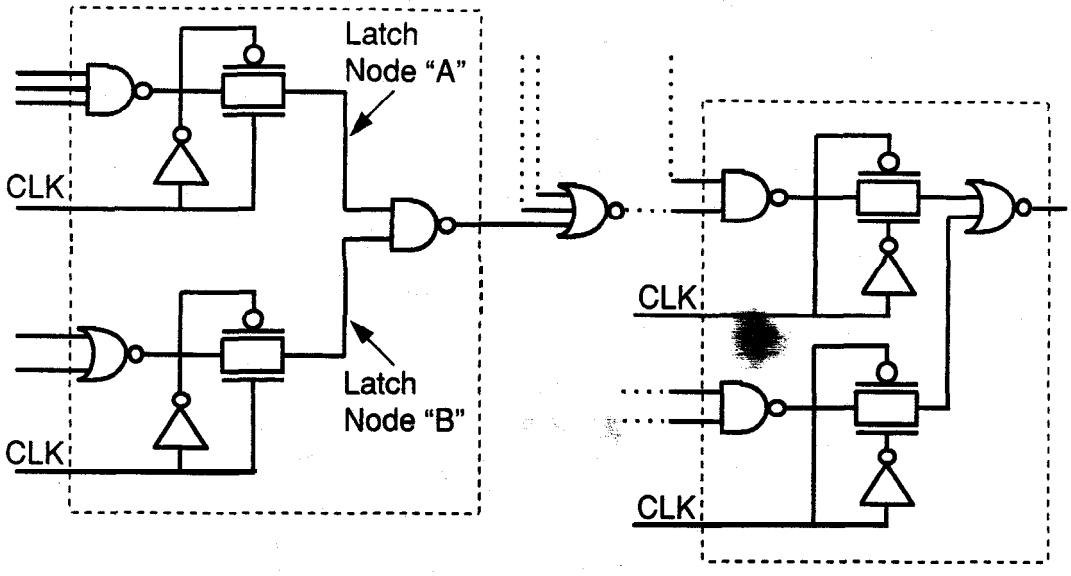
- ❒ Level-sensitive design
- ❒ Dynamic latches
  - Faster
  - Less area
  - Required to function at 1/10th speed
- ❒ General purpose library
  - Fully characterized
  - Emphasis on speed

Latching - Latch Implementation



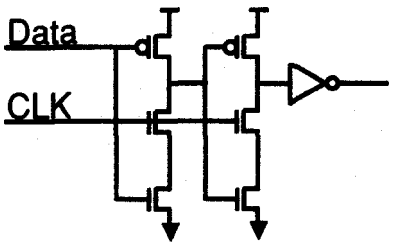
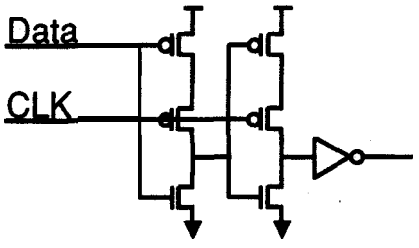
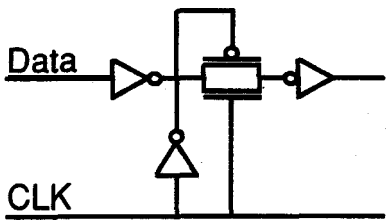
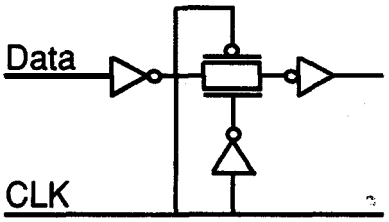
Minimum one gate between any two latching points required

Latching - Embedding Logic

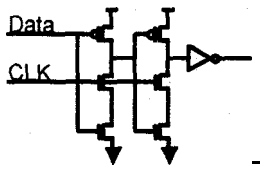
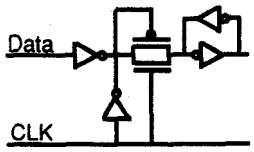
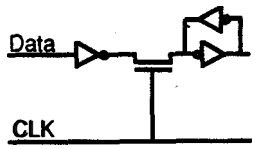
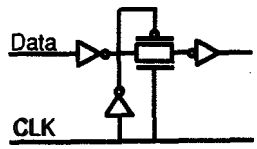


Latching costs only 2 pass gates per cycle

Latching - Circuit Implementation

	CLK-HI Version	CLK-LO Version
21064 Latches:		
21164 Latches:		

Latching - Comparison

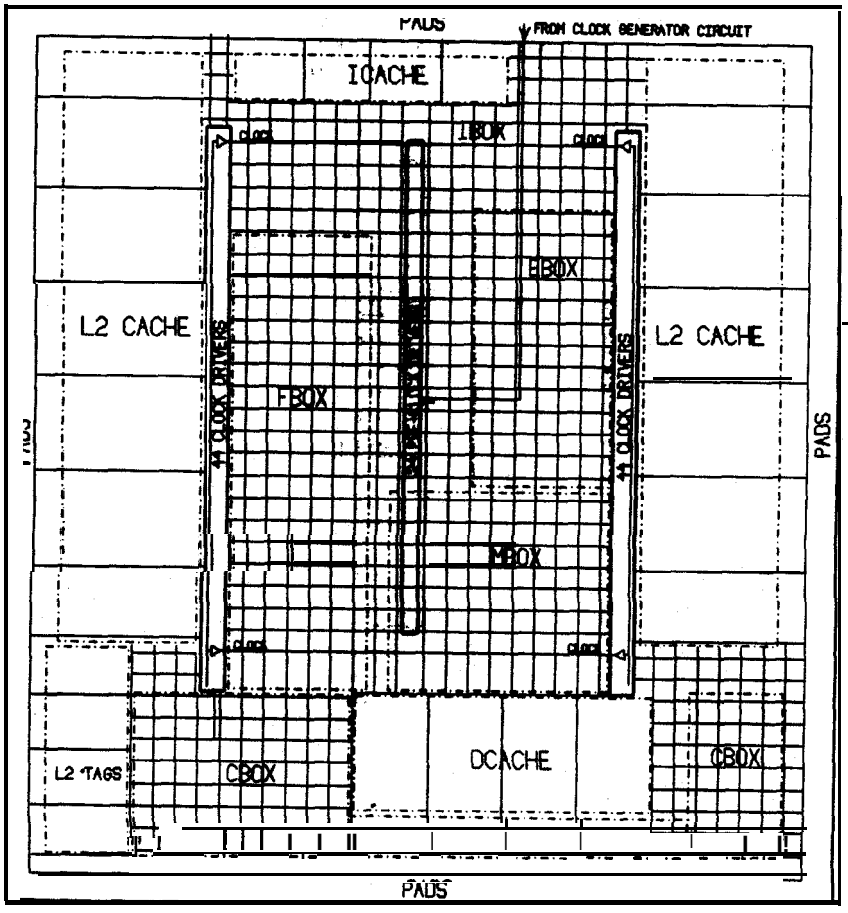
	Area	Speed	Race	Clock Load
	1.25	1.2	- CLK edge rate	4
	1.25	1.2	- CLK edge rate - CLK buffer delay	1.0
	1.0	1.3	- CLK edge rate	0.5
	1.0	1.0	- CLK edge rate - CLK buffer delay	1.0

Latching - Verification Issues

- Race verification
  - Race speed analysis (SPICE)
  - Custom race tool specific to design methodology
  - Latch size checks
  - Minimum/maximum clock edge rate
  - Clock buffer not shared
  - At least one gate delay between latches
  - Latch driven by clock or deskewed
- Functional verification (for static latches)
  - DC noise margin analysis (SPICE)
  - DC writeability analysis (SPICE)
- Full dynamic logic verification

Clocking - Overview

- Single-wire, two phase clocking scheme
- Single global clock grid
- Limited use of conditional clocks
- Clock statistics (0.5 µm design)
  - **Clock load = 3.75 nF**
  - Size of final clock inverter = 58 cm
  - Edge rate = 0.5 ns
  - Clocking consumes 40% of chip power
  - Decoupling capacitance near clocks = 35 nF
  - di/dt = 50 **A**

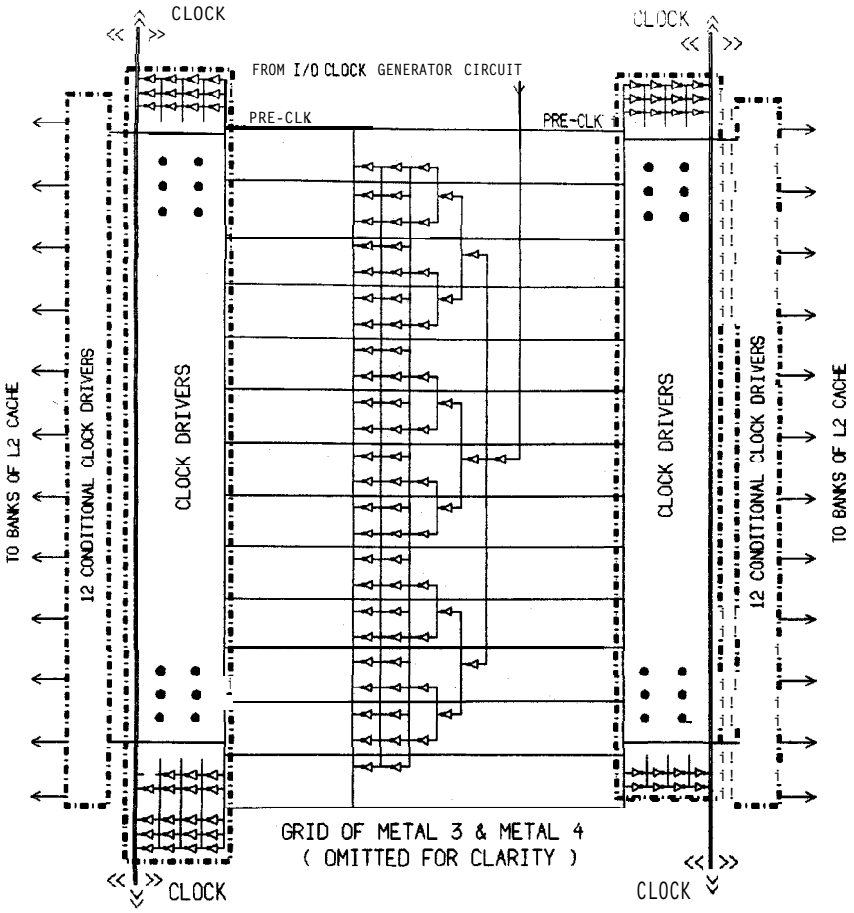


Clocking interconnect

Total Capacitance	3.75 **nF**
Global Interconnect	**1.00 nF**
Local Interconnect	**0.95 nF**
Gate Capacitance	**1.20 nF**
self Loading	**0.60 nF**

At best, save 20% with H tree (global interconnect)

Clocking Distribution



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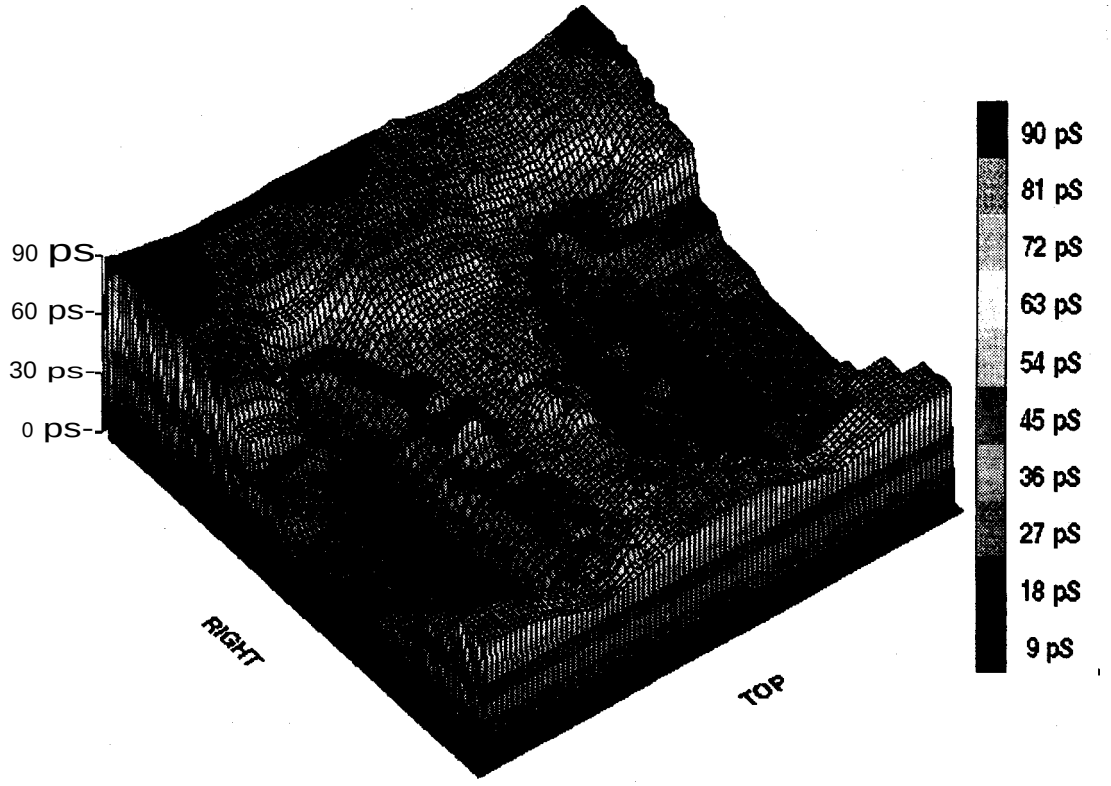
Clocking - Analysis

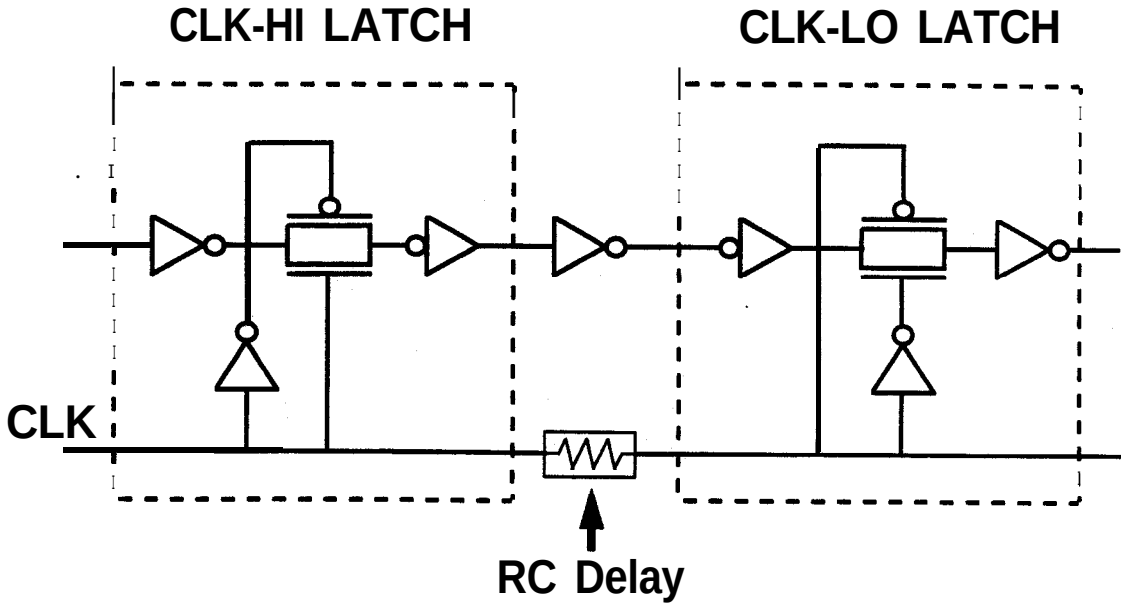
- Clock generation. and driver network evaluated using SPICE
  - VSS and VDD supply noise
  - Device variations across the chip
- RC delay of global clock interconnect evaluated using extracted R and C data
  - Global clock skew can limit speed
  - Local clock skew can create race-through problems

200ps pred.cld

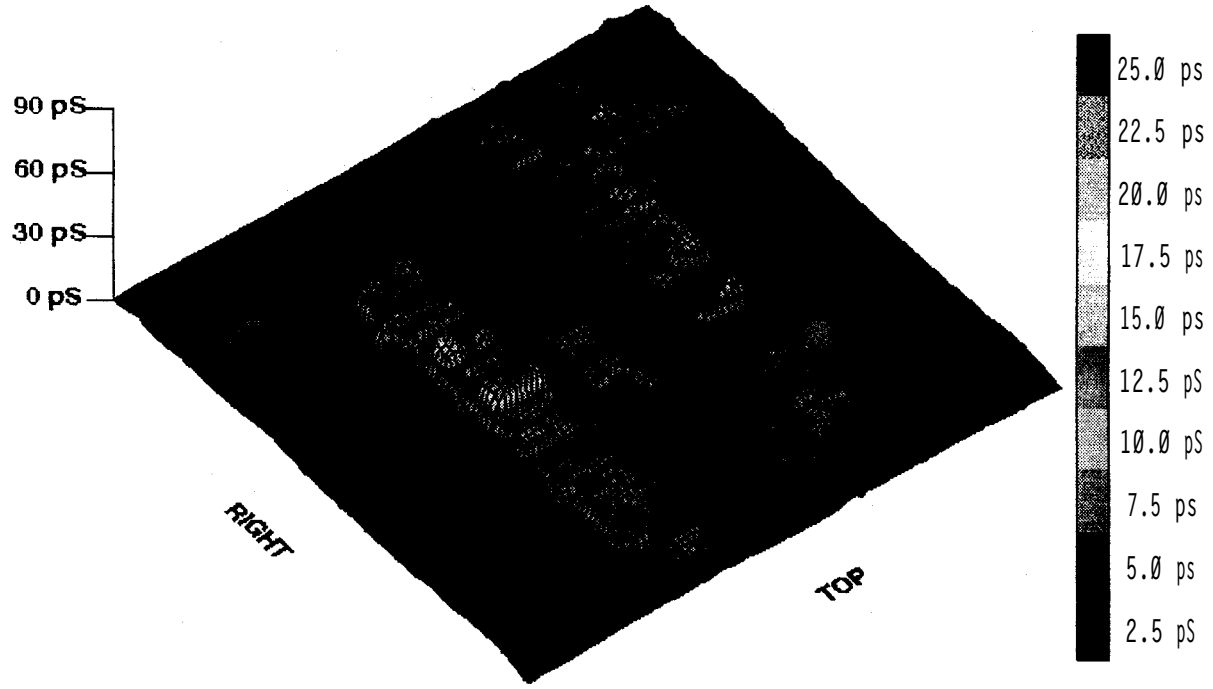
Clocking - Global Clock Skew



Clocking - Skew Sensitive Circuit



Clocking - Local Clock Skew

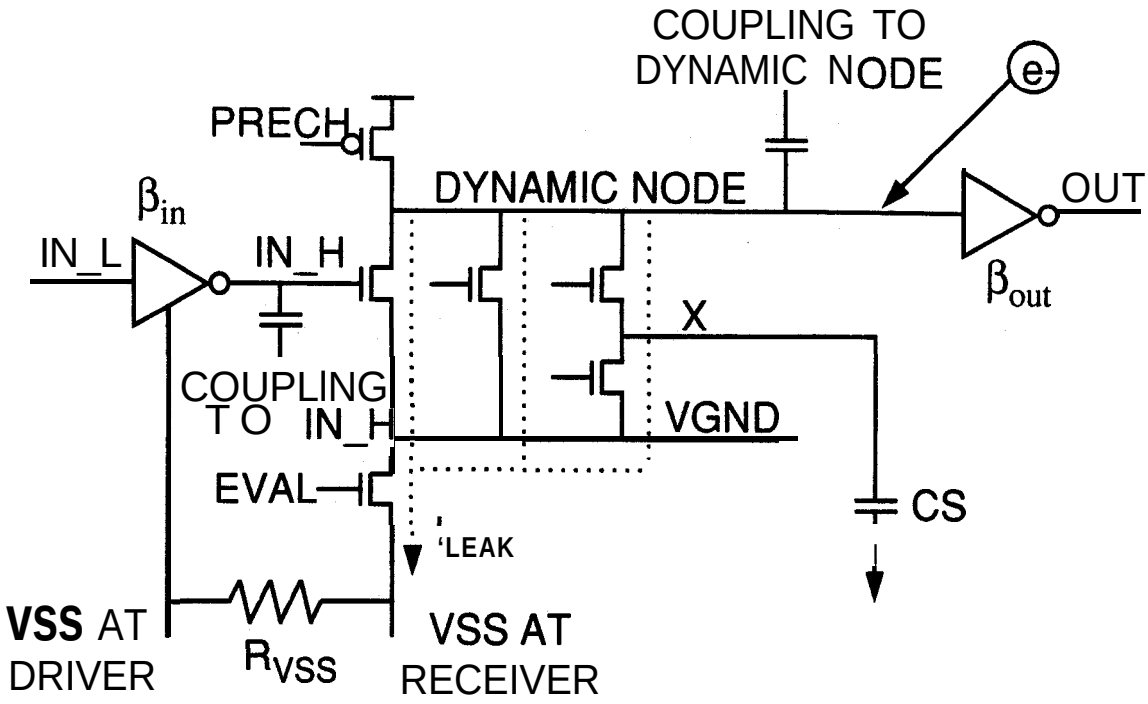


Dynamic Logic - Overview

Dynamic logic requires significantly more electrical verification than static logic.

- Capacitive coupling and charge sharing
- Subthreshold leakage
- Charge injection
  - -Minority carrier collection
  - -Latch-up
- Alpha particle immunity
- VDD/VSS noise and resistance

Dynamic Logic - Circuit Diagram

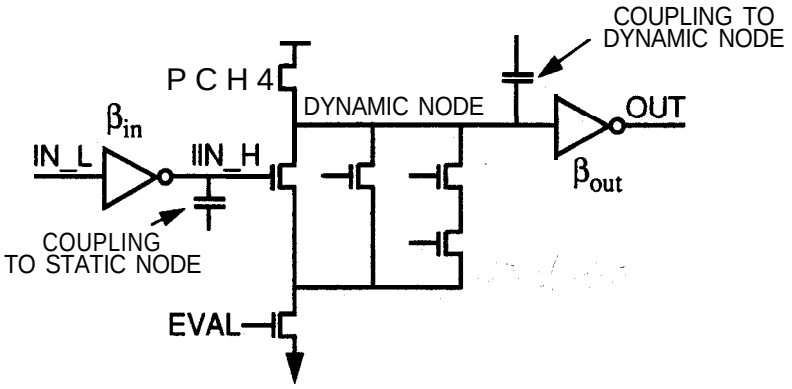


Dynamic Logic - General Rules

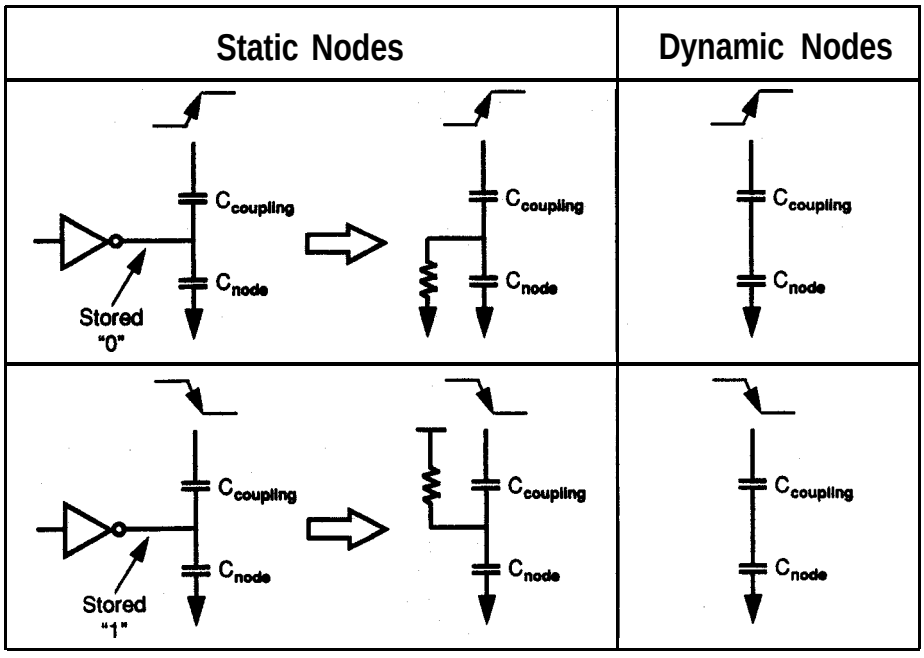
- Dynamic logic can only be driven by complementary gates
- Complementary gates must be close to dynamic structure
  - Global nodes received by gates with standard β ratio (noise margin)
  - Local nodes can be received by gates with a skewed β ratio (for speed)
- Precharge controlled by clock
  - Delayed precharge not typically used
  - Domino or ripple precharge not typically used

Dynamic Logic - Coupling

- Coupling is difficult to analyze precisely
  - What capacitance should be used?
  - When do “aggressor” signals change?
  - What is the rise/fall time of “aggressor” signals?



Dynamic Logic - Coupling Circuit Diagram

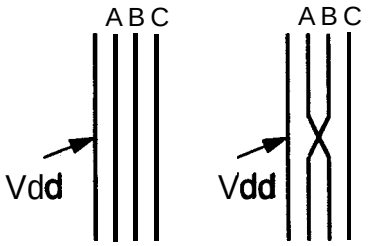


Note: High-up coupling on stored “1” nodes and Low-down coupling on stored “0” nodes can be a problem as well.

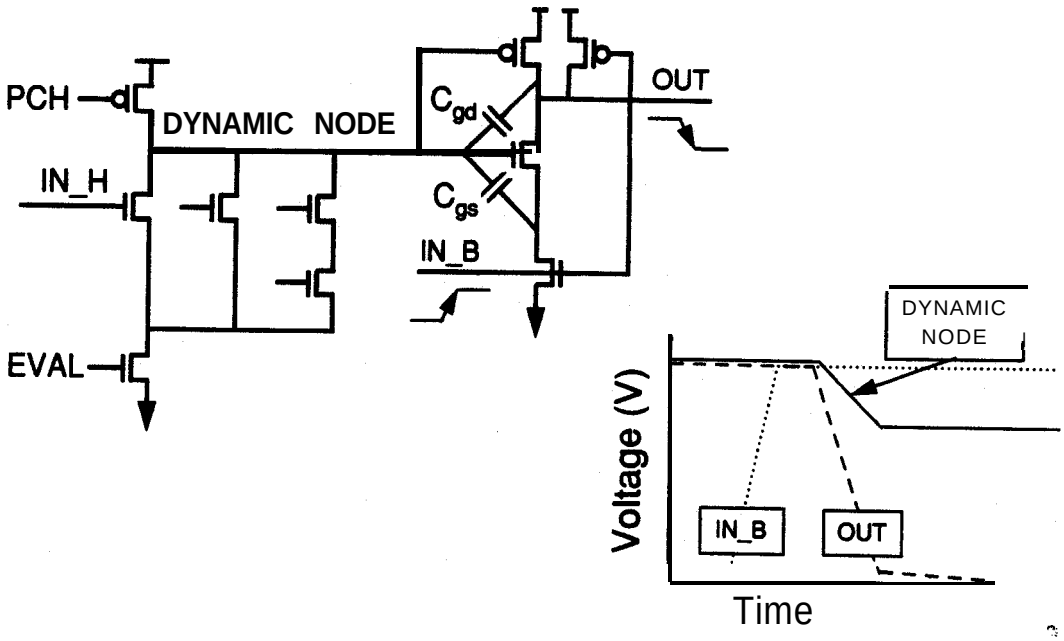
Dynamic Logic - Coupling Solutions

1. **Set limits on** maximum allowable coupling and input and output beta ratio ranges to ensure acceptable noise margin.
2. Account for canceling coupling events - be careful!
3. Shield and/or isolate dynamic nodes where possible.
4. Increase overall "good" (fixed) capacitance to reduce the impact of "bad" coupling capacitance.
5. In datapaths, examine bus ordering (see below).

   - "Twist" lines (as shown at right) to take advantage of power rails
   - Route dynamic lines between mutually exclusive or complementary lines

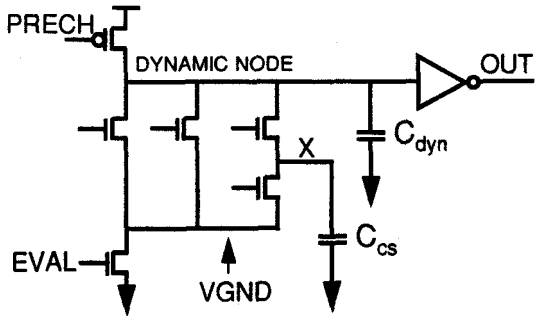


Dynamic Logic - Coupling Example

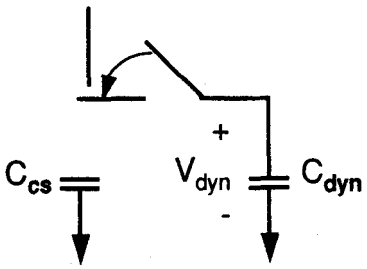


Dynamic **Logic -** Charge Share

Charge sharing can occur when internal nodes (node X) are not adequately precharged.



$$V_{dyn} = \frac{V_{dd} * C_{dyn}}{C_{dyn} + C_{cs}}$$

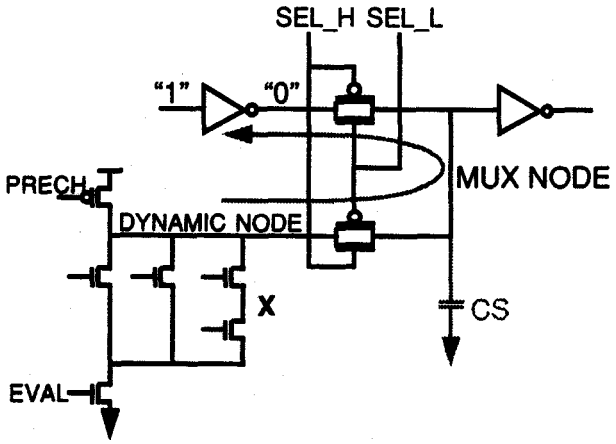


Dynamic Logic - Charge Share

Solutions:

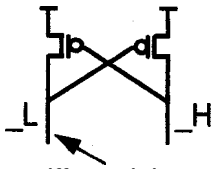
1. Minimize diffusion capacitance on charge share node
2. Precharge "X" with nmos device
   + less area for precharge
   + faster
   - buffered clock required
3. Precharge "X" with pmos device

Another Example:

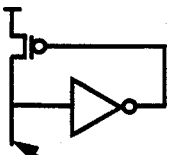


Dynamic Logic - Subthreshold Leakage

- Subthreshold leakage may be a problem for dynamic nodes where $\Sigma W_{eff} / C_{node}$ is large.
- Determine leakage time:
  - $t_{leak} = C_{node} * V_{node} / i_{leak}$
- Circuit solutions:
  - Increase channel length
  - Add weak "leakers"

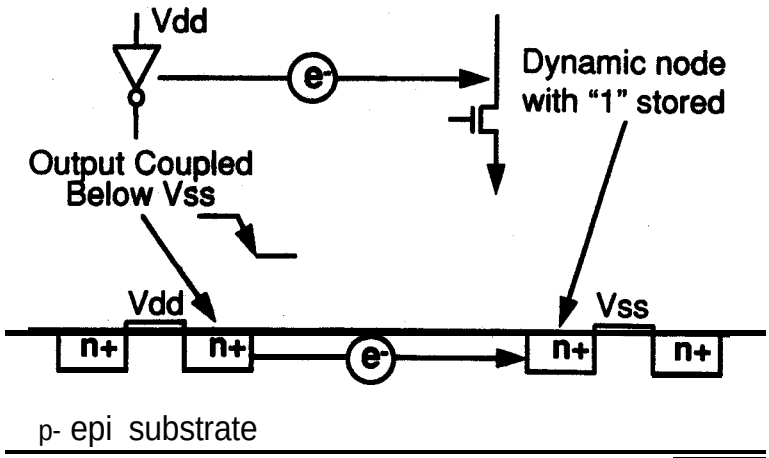


Differential Bus

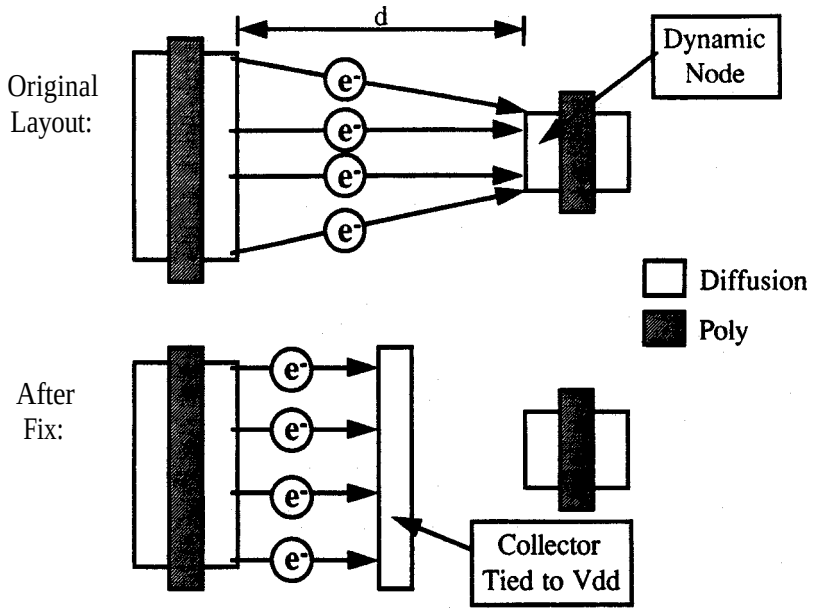

Dynamic Node

Dynamic Logic - Charge Injection

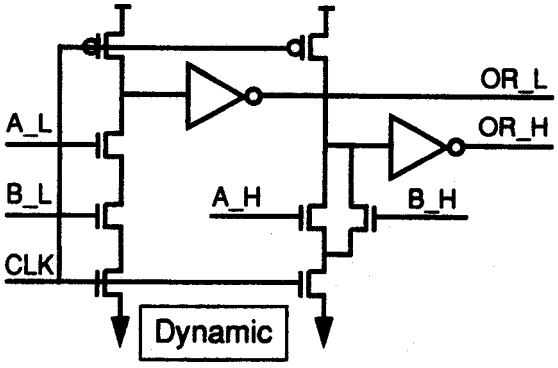
- Latch-up
- Minority carrier charge injection/collection

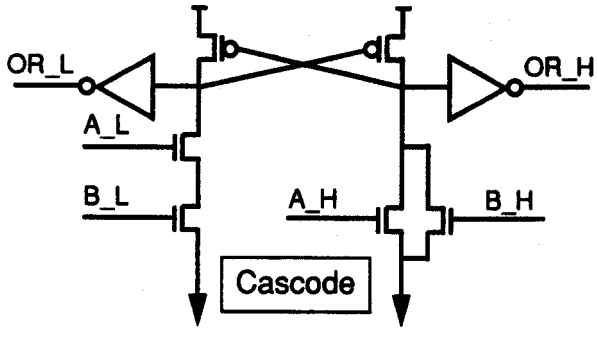


Dynamic Logic - Charge Injection



Dynamic Logic - Dual-rail Design





Advantages

❶ Fast - use sense amp to detect small voltage swing on output or skew the beta ratio of output complementary gates.

❷ Complex logic functions can be easily generated as true and complement of all signals available.

❸ Since both outputs (OR_L and OR_H) start low after precharge, can sense when logic is complete by detecting 01 or 10.

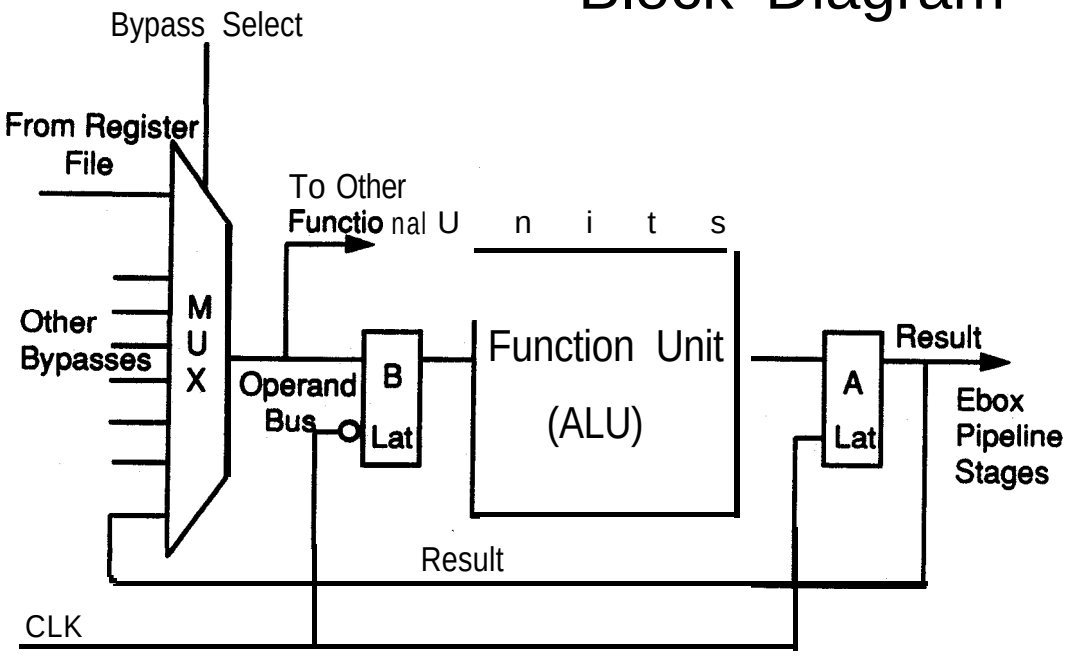
Dynamic Logic - Dual-rail Design

Design Issues

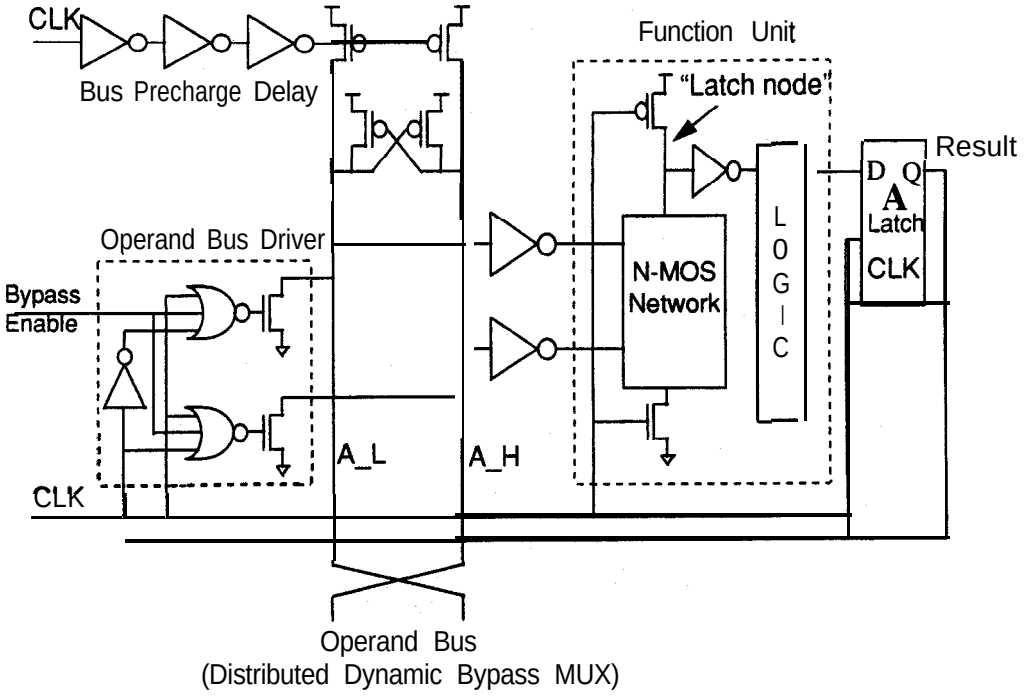
1. Power dissipation. One side of the logic is always evaluated.
2. Area. Requires roughly twice the area of single-rail design.
3. Coupling may be an issue, especially in datapath structures
   - Twisted bit lines
   - Bus ordering
   - Encode Lines (HP PA8000 Floating Point Unit - see references)

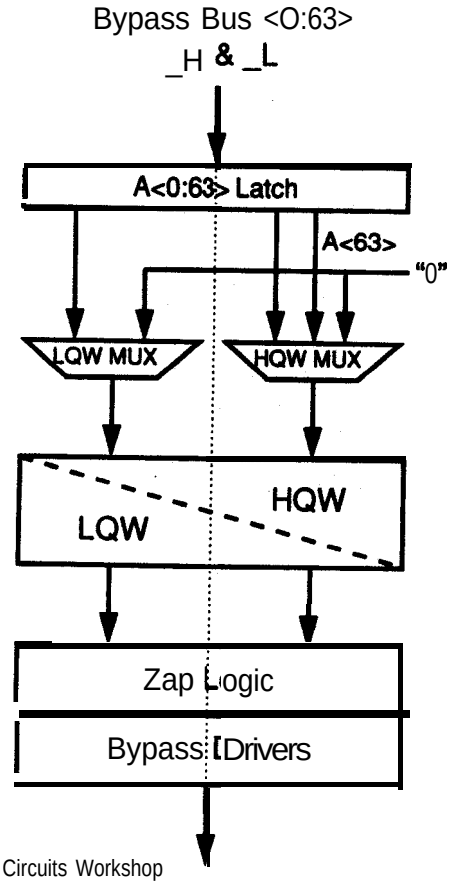
Inputs	Dual-rail inputs				Encoded inputs			
A B	A_H	A_L	B_H	B_L	AB3	AB2	AB1	AB0
0	0	0	1	0	1	0	0	0
0	1	0	1	1	0	0	0	1
1	0	1	0	0	1	0	0	0
1	1	1	0	1	0	0	0	0

Circuit Example #1 - E-Box Bypass Block Diagram



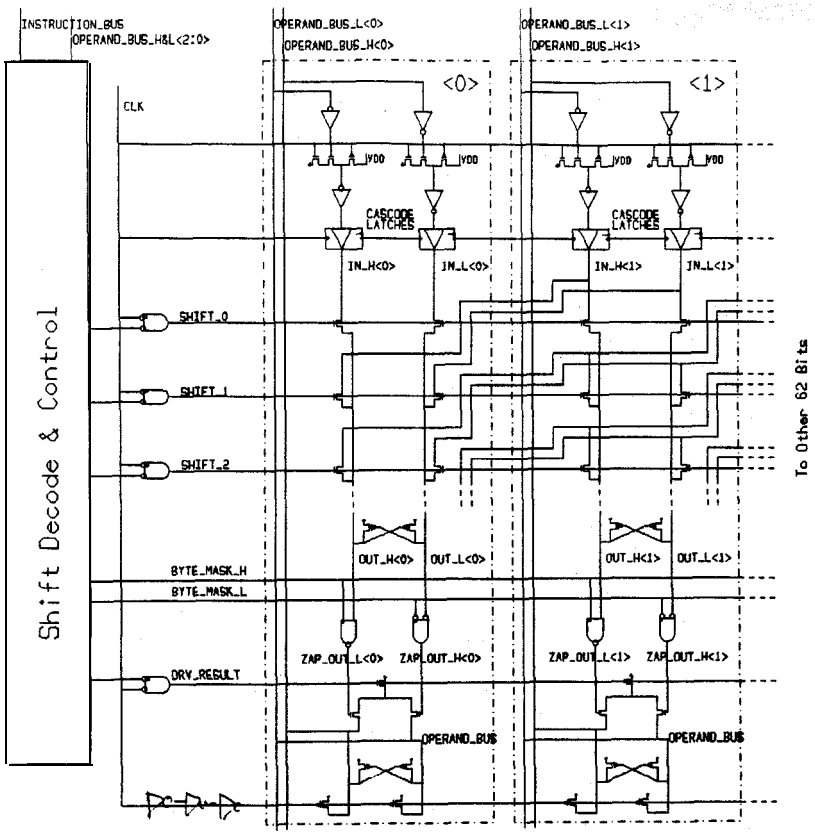
E-box Bypass - Circuit Diagram





Circuit Example #2 - E-Box Shifter Block Diagram

E-box Shifter
Circuit Schematic



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