ECE 111 (Winter 2019)

- http://cwcserv.ucsd.edu/~billlin/classes/ECE111/index.php
- Professor Bill Lin
  - Office hours: Mon 1:00-1:50p, 4310 Atkinson Hall
- Lectures:
  - Section A00: MW 2:00-3:20p, EBU1-2315
  - Section B00: MW 3:30p-4:50p, EBU1-2315
- No regular discussion sections (only schedule if needed)
- TAs:
  - Jianling Liu, Justin Law, Dylan Vizcarra, Yu Huang and Ping Yin
  - Office hours: TBD
  - Note: You may get help from any TA during their office hours.

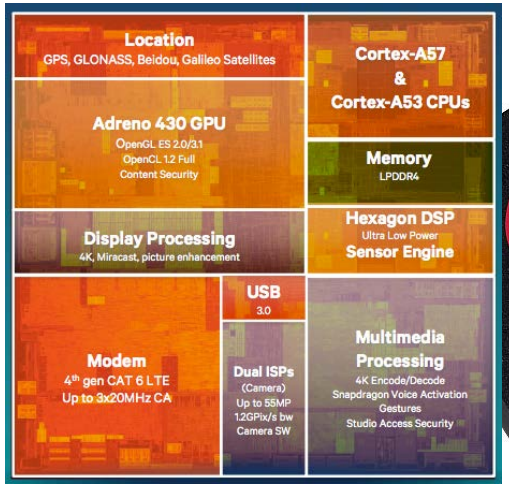
Introduction

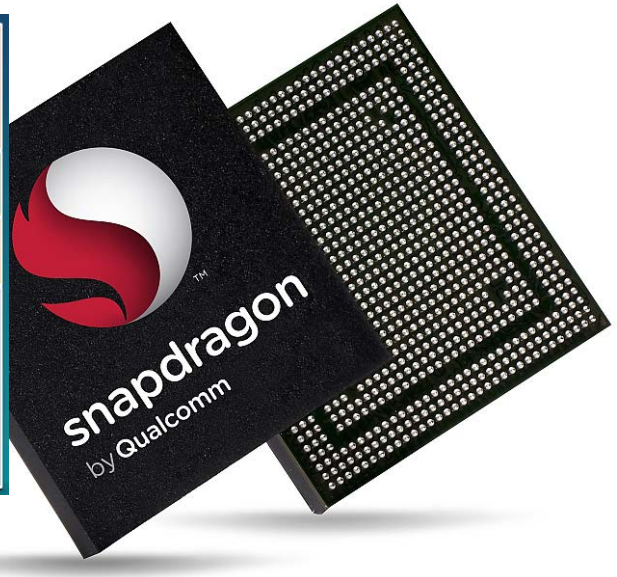
- Goal: Learn Verilog-based chip design
- In particular, we will be using the Hardware Description Language (HDL) SystemVerilog, which is a "superset" of Verilog:
  - Verilog, IEEE standard (1364) in 1995
  - SystemVerilog, extended in 2005, current version is IEEE Standard 1800-2012
- The name "SystemVerilog" is confusing because it still describes hardware at the same level as "Verilog", but SystemVerilog adds a number of enhancements and improved syntax.
- SystemVerilog files have a ".sv" extension so that the compiler knows that the file is in SystemVerilog rather than Verilog.

Why Learn Verilog/SystemVerilog

- Most EE jobs are Verilog/SystemVerilog based chip designs

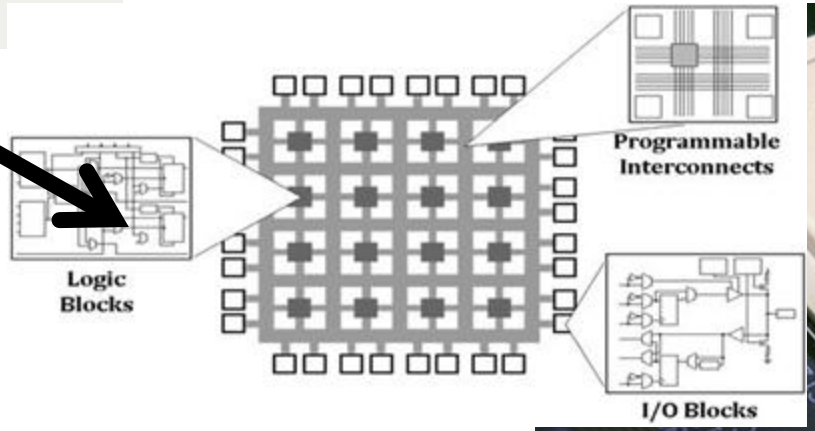
ASIC Design





SystemVerilog

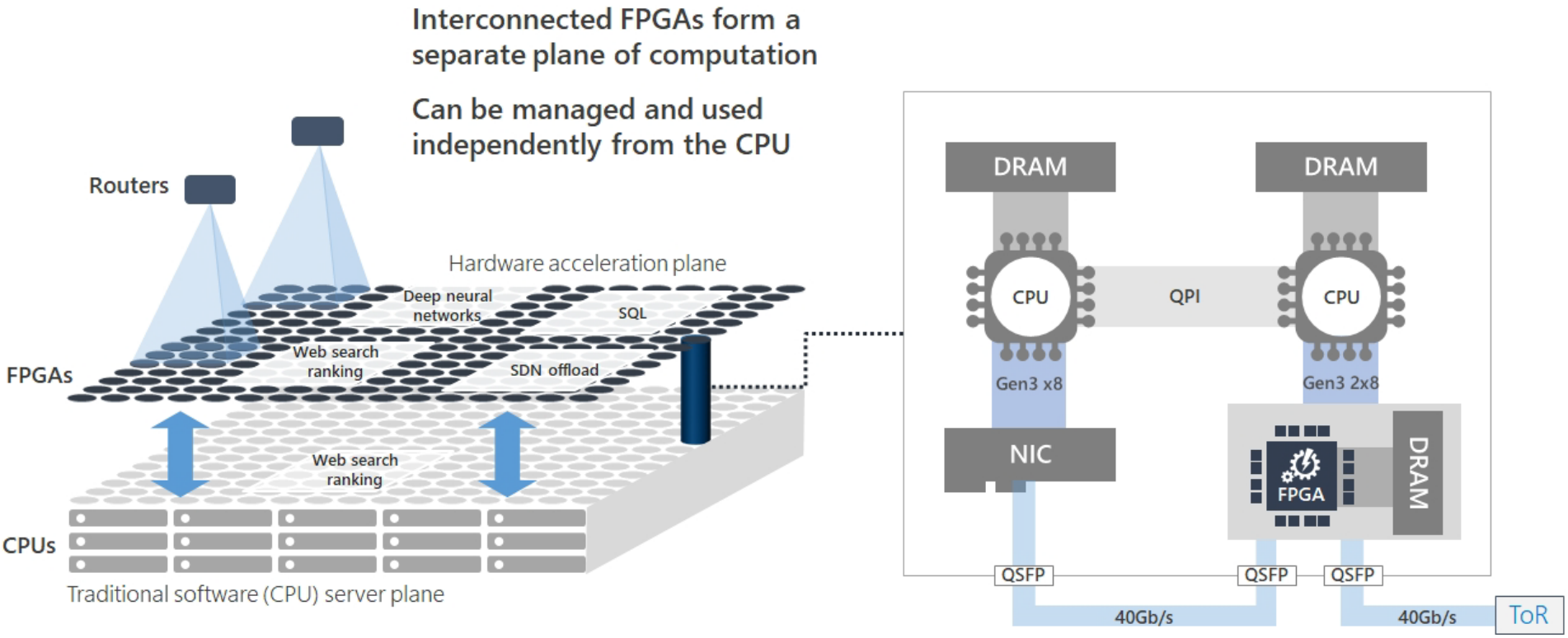
FPGA Design



Why Learn Verilog/SystemVerilog

- Emergence of the FPGA Cloud

Example: Microsoft's Catapult Project deployed worldwide

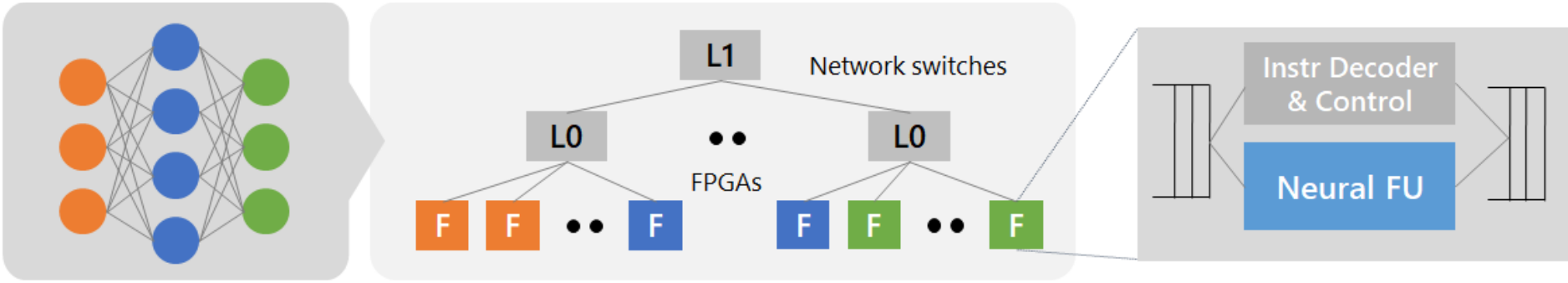


[Credit: Microsoft, MICRO'16]

Why Learn Verilog/SystemVerilog

- Emergence of the FPGA Cloud

Example: Microsoft's Project BrainWave



Each FPGA implements many Soft DPUs

[Credit: Microsoft, Hot Chips'17]

Other FPGA Clouds

FPGA Cloud Applications

- Bing search engine implemented in Microsoft's FPGA cloud
- Machine learning/AI
- High-speed frequency trading
- Bioinformatics (e.g. DNA sequencing)

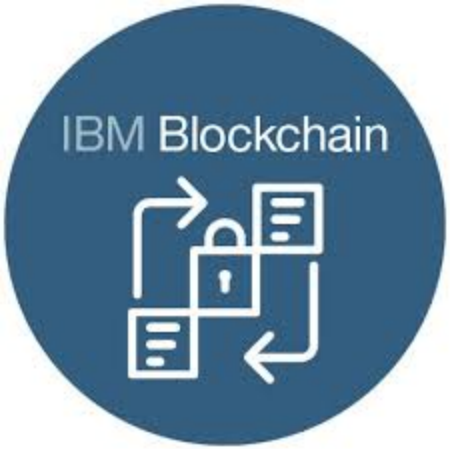
Class Project

- Final project on Bitcoin mining
- Great deal of interest in cryptocurrencies

Class Project

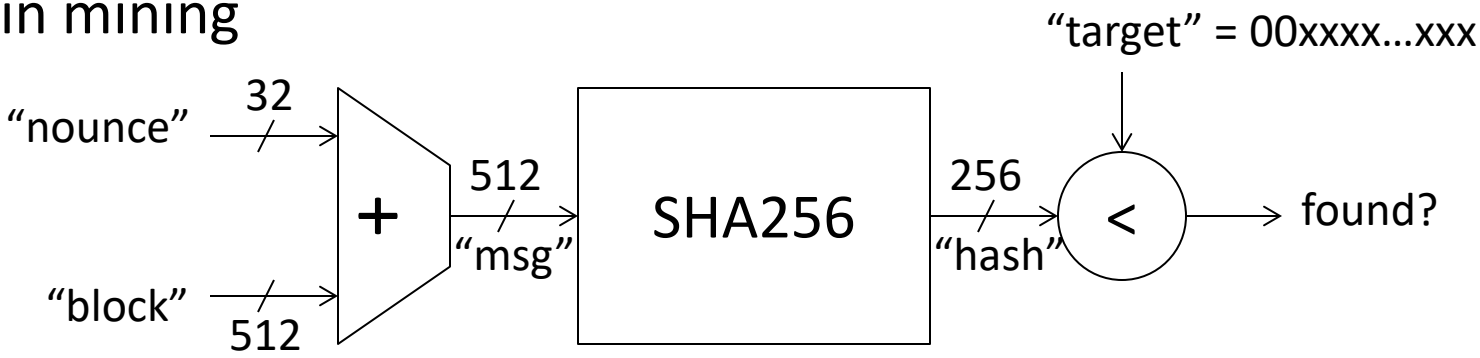
- Blockchain is the underlying technology for cryptocurrencies, which provides authenticated global ledger (tamper-proof global transaction record)

- Blockchain is finding many applications: e.g.,



Class Project

- Bitcoin mining



- Every "msg" will produce different 256-bit hash. Changing "nounce" will change "msg" and produce different 256-bit hash.
- Find "nounce" such that SHA256(nounce + block) < "target"
- If "target" has 1 leading 0, then chances of success every 2 tries. If 2 leading 0's, every 4 tries, 30 leading 0's, every billion tries, etc.
- Bitcoin by design makes "target" increasingly difficult after certain number of bitcoins have been mined.

Class Project

- Final project based on how fast can your design evaluate “nonces” (equivalent to how fast you can mine a Bitcoin). i.e., final project grade based on performance only.

- You can use the entire FPGA to create as many instancs of SHA256 as you like, and you can greatly improve the performance of each SHA256 unit using techniques like pipelining, etc.

- Intermediate project: Design of a SHA256 unit.

- Projects done in teams of 2 (you have the option of working alone). Your partner can be in the other section.

Software

- See Software Downloads Page

http://cwcserv.ucsd.edu/~billlin/classes/ECE111/software.php

which links to this:
http://fpgasoftware.intel.com/18.1/?edition=lite

- Quartus Prime Lite Edition
  - Quartus Prime (earlier versions were called Quartus II)
  - ModelSim-Intel FPGA Edition
- Arria II device support
- Available for Windows and Linux
- For Macs, you can use Bootcamp to dual-boot Windows
- Windows Machines with software setup also available in **EBU1-4309**. You should be able to get the door code from here: https://sdacs.ucsd.edu/~icc/index.php

Software

- Class website has a tutorial page on Quartus and ModelSim

http://cwcserv.ucsd.edu/~billlin/classes/ECE111/Quartus_ModelSim_Tutorial/quartus_modelsim_tutorial.html

More Information

- Recommended textbook
  - Digital Design and Computer Architecture, Second Edition, by David Harris and Sarah Harris
  - We will only be using Chapter 4 of this book, which provides a good overview of SystemVerilog with good examples.
  - Make sure you get the 2nd Edition since the 1st Edition uses Verilog instead of SystemVerilog
  - Book recommended, but not required.

Honor Code

- The UCSD Student Conduct Code

  https://students.ucsd.edu/sponsor/student-conduct/regulations/22.00.html

- Violations will be reported to the Student Conduct Office (as well as failing the class)