ECE 255, MOSFET Circuits

8 February 2018

In this lecture, MOSFET will be further studied.

1 Current-Voltage Characteristics of MOSFET

1.1 Circuit Symbols

Here, the n-channel enhancement-type MOSFET will be considered. The circuit symbols for MOSFET in shown in Figure 1. In Figure 1(a), an arrow is shown in the terminal B, or the body terminal. This indicates that it is an NMOS, or the body is of p type. Hence, a current can be driven into the device with a positive voltage at B if the drain (D) and the source (S) are grounded.

Even though a MOSFET is a symmetrical device, for better book keeping, it is better to designate one of the terminals as source (S) and the other terminal as (D). For NMOS, the current flows out of the source, as indicated by an arrowhead in Figure 1(b). By convention, the current always flows from top to down, and clearly indicating that this is an NMOS device; hence, the arrowhead in B can be omitted. Also, for NMOS, the drain is always at a higher potential than the source. Sometimes the symbol for B is completely omitted as shown in Figure 1(c).

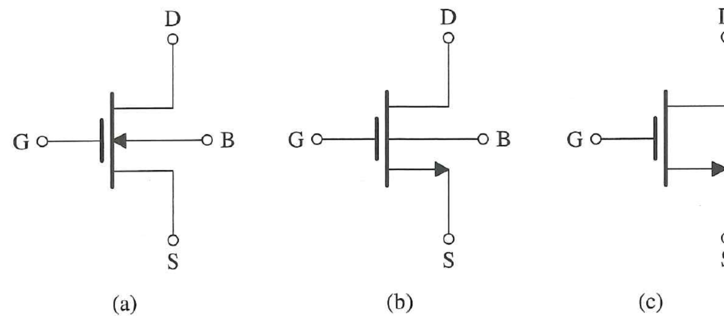

Figure 1: Different circuit symbols for enahancement-type NMOS. The sign of the arrows show that this is an NMOS device (Courtesy of Sedra and Smith).

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A variety of other circuit symbols are used in practice as shown in Figure 2, but in this course, only those in Figure 1 shall be used.

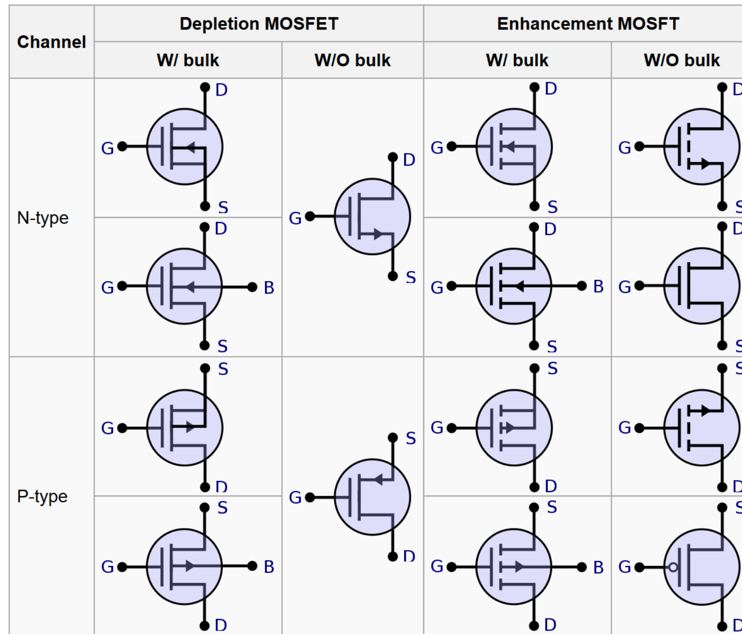

Figure 2: Different symbols for MOSFET used in practice. “Bulk” here refers to “body”. Body electrodes are shown when “bulk” is included. Dotted lines are used to denote conduction channel (Courtesy of WIKICHIP).

1.2 i_D-v_{DS} Characteristics

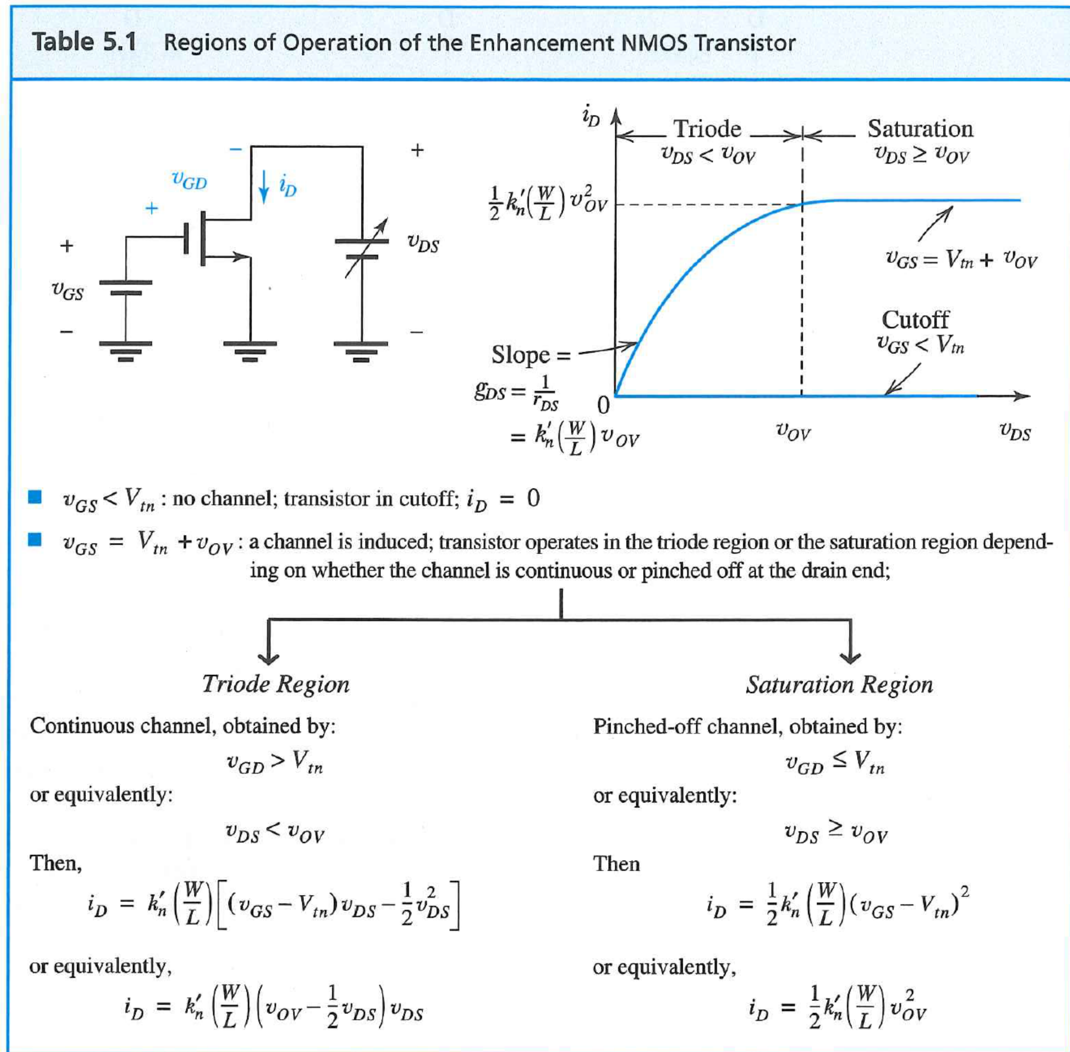

Table 5.1 Regions of Operation of the Enhancement NMOS Transistor

- $v_{GS} < V_{tn}$: no channel; transistor in cutoff; $i_D = 0$
- $v_{GS} = V_{tn} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched off at the drain end;

Triode Region

Continuous channel, obtained by:

$$v_{GD} > V_{tn}$$

or equivalently:

$$v_{DS} < v_{OV}$$

Then,

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

or equivalently,

$$i_D = k_n'\left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{GD} \leq V_{tn}$$

or equivalently:

$$v_{DS} \geq v_{OV}$$

Then

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

or equivalently,

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$$

Figure 3: Regions of operation of the NMOS transistor and summary of important formulas for their respective regions (Courtesy of Sedra and Smith).

Figure 3 (Table 5.1 of the textbook) shows the operation characteristics of an NMOS transistor. The transistor characteristics are shown in the cutoff region ($v_{GS} < V_{tn}$), triode region ($0 < v_{DS} < v_{OV}$), and the saturation region ($v_{DS} > v_{OV}$).

When $v_{GS} < V_{tn}$,[1] the transistor is in the off or cutoff mode, since no channel is formed and no current can flow. When $v_{GS} > V_{tn}$ or $v_{GS} = V_{tn} + v_{OV}$, the transistor is in the on mode, and the i_D-v_{DS} curve is as shown. The transistor can be either in the triode region or saturation region.

The transistor is in the saturation region if v_{DS} is larger than the overdrive voltage v_{OV}. This is also the case when the channel is pinched off. Increasing the v_{GS} beyond v_{OV} increases the depletion region, causing the excess voltage to drop across the depletion region. This is indicated in Figure 4.

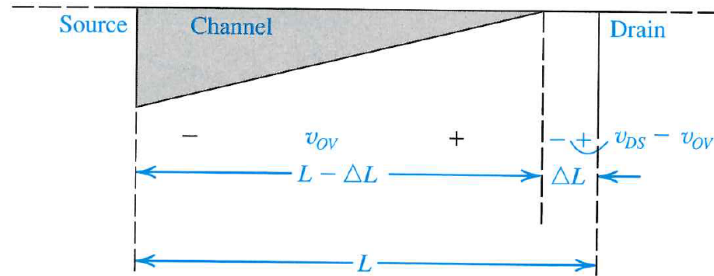

Figure 4: The channel region when the transistor is in the saturation mode when $v_{DS} > V_{OV}$. It is to be reminded that the vertical axis represents the charge density in the channel, not the depth (Courtesy of Sedra and Smith).

To be in the triode region, there should be no pinch-off in the channel. As indicated in Figure 5 (reproduced here from the previous lecture), v_{GD} has to be larger that V_{tn}. Keeping this in mind, Figure 6 shows the different regimes of operation of the NMOS transistor. Please be noted that the saturation region is analogous to the active region in the BJT, while the triode region is analogous to the saturation region in the BJT.

[1] Here, V_{tn} is the threshold voltage for NMOS.

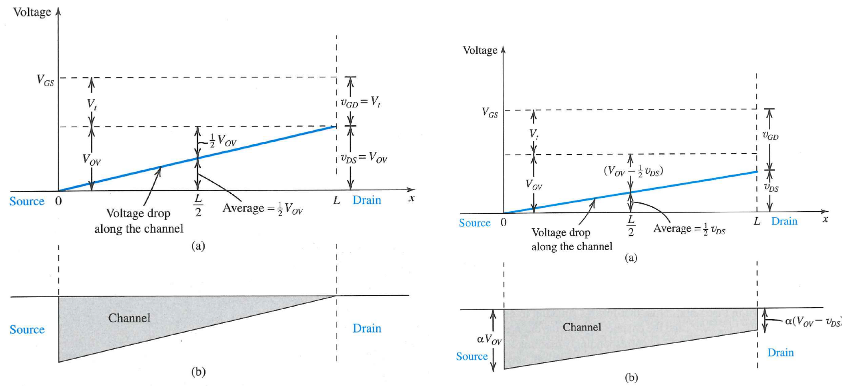

Figure 5: (Left) The shape of the channel of NMOS in the just before it enters the saturation regime. (Right) Reminder picture showing the channel in the triode regime (Courtesy of Sedra and Smith).

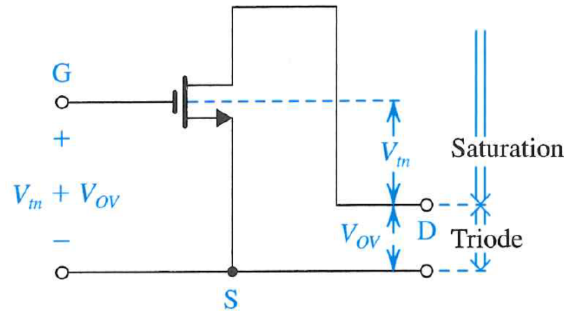

Figure 6: Different regimes of operation of the NMOS transistor. The saturation regime here is analogous to the active regime in BJT, while the triode regime corresponds to the saturation regime in BJT (Courtesy of Sedra and Smith).

Using the fact that at the boundary between triode and saturation regions, $v_{DS} = v_{OV}$, then

$$i_{D\text{sat}} = \frac{k_n'}{2}\frac{W}{L}v_{OV}^2 \tag{1.1}$$

As seen from above formula, the cross-over points from triode region to the saturation region is marked by a parabola as shown in Figure 7 where $v_{DS} = v_{OV}$ at these points.

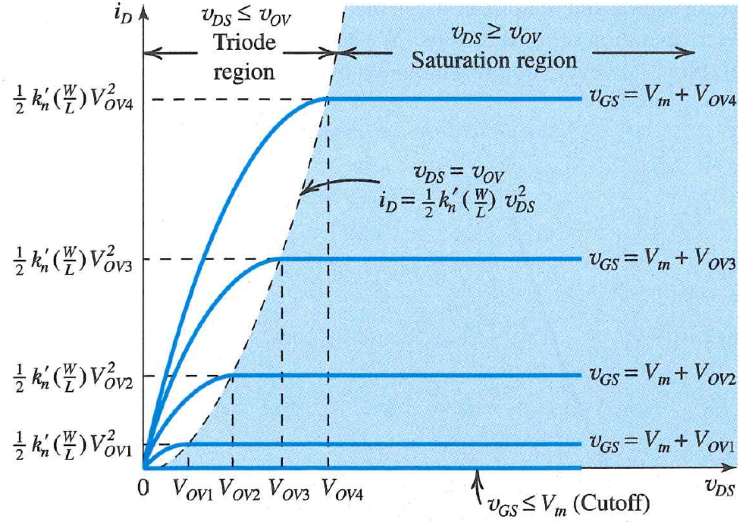

Figure 7: The i_D-v_{DS} curves of an NMOS transistor for different V_{OV} (Courtesy of Sedra and Smith).

1.3 i_D-v_{GS} Characteristics

When used as an amplifier, the NMOS transistor operates in the saturation regime (analogous to the active regime in BJT). In this regime, as shown before

$$i_{D\text{sat}} = \frac{k_n'}{2}\frac{W}{L}(v_{GS} - V_{tn})^2 = \frac{k_n'}{2}\frac{W}{L}v_{OV}^2 \tag{1.2}$$

Here, i_D remains constant when $v_{DS} > v_{OV}$. The i_D-v_{GS} relation of the transistor is shown in Figure 8. The current i_D grows algebraically when v_{GS} exceeds V_{tn}. This is less dramatic and unlike the BJT case where the current grows exponentially fast with respect to the v_{BE} voltage. This represents an important difference between a BJT and a MOSFET: this algebraic growth makes the MOSFET more nonlinear than a BJT.

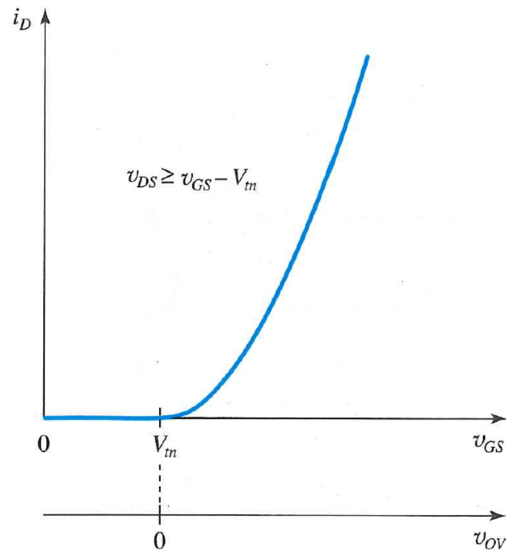

Figure 8: The i_D-v_{GS} curves of an NMOS transistor indicating its algebraic growth rather than the exponential growth of a BJT as shown by equation (1.2) (Courtesy of Sedra and Smith).

Since the current i_D does not change for different v_{DS} (mark of a current source), it can be modeled as a voltage-controlled current source in this regime. This is shown in Figure 9.

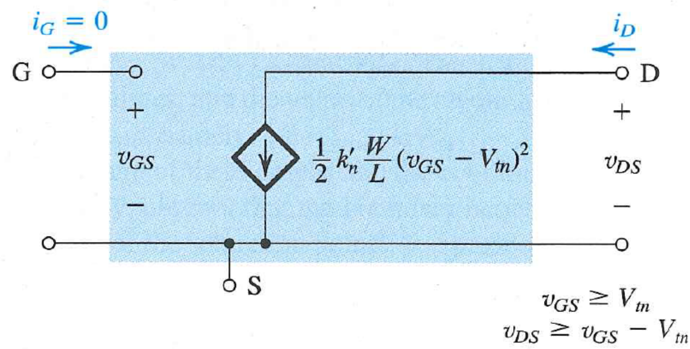

Figure 9: Equivalent circuit model of a NMOS transistor as a voltage controlled current source in the saturation regime of the transistor (Courtesy of Sedra and Smith).

1.4 Finite Output Resistance in Saturation

When v_{DS} is larger than V_{OV},[2] the depletion region around the drain region grows in size. This is because the *pn* junction near the drain is in reverse bias while the *pn* junction near the source is in forward bias. So most of the excess voltage is dropped across the depletion region near the drain region, and the channel length becomes shorter as shown in Figure 4. As the channel length becomes shorter, the electric field, which is proportional to v_{DS}/L, becomes larger. Consequently, the drift current increases, and i_D increases with increasing v_{DS} as shown in Figure 10. This effect is called the **channel-length modulation** effect (also called Early effect as in the BJT case attributed to J.M. Early). This effect can be incorporated by including a factor of $(1 + v_{DS}/V_A)$ giving rise to a formula for the drain current as

$$i_D = \frac{1}{2}k'_n\frac{W}{L}(v_{GS} - V_{tn})^2(1 + \frac{v_{DS}}{V_A}) \tag{1.3}$$

where V_A is a measure of how sensitive this channel-length modulation is to v_{DS}. The negative intercept of the i_D-v_{DS} curve is at $-V_A$. Here, V_A is referred to as the Early voltage as in BJT. Notice that the smaller V_A is, the more pronounced is the Early effect.

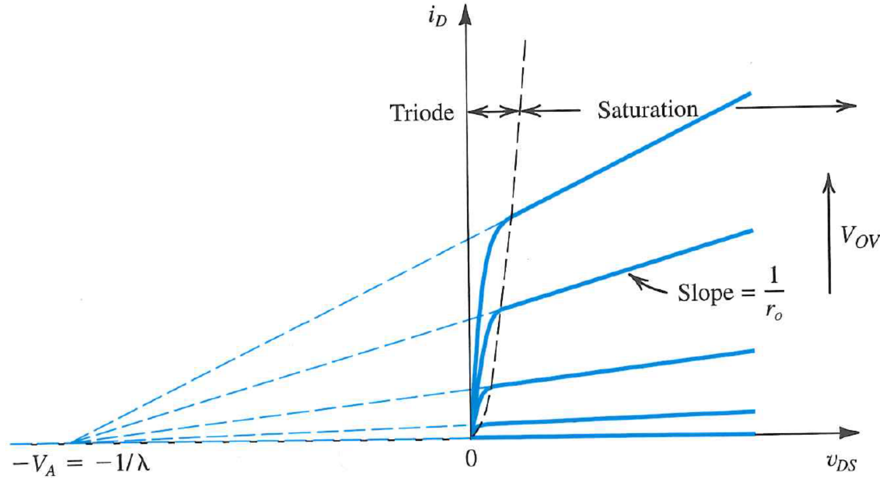

Figure 10: The channel-length modulation effect causes the i_D-v_{DS} characteristics to change for different V_{OV}. As v_{DS} becomes larger, the channel length becomes smaller, and i_D becomes larger (Courtesy of Sedra and Smith).

It is found empirically that V_A becomes smaller with decreasing channel length L (device dimensions are of the order of 14 nm now). As device gets

[2]Again, it is to be reminded that the textbook uses capital letter to denote DC values.

smaller, the channel length becomes smaller. Therefore, it is prudent to define

$$V_A = V_A' L \tag{1.4}$$

so that V_A' is independent of device size. The above formula together with the plots in Figure 10 indicates that this channel-length modulation effect is stronger for smaller device dimensions. The reason is that the excess v_{DS} voltage drop is shouldered by the depletion region, and the width of the depletion region grows with this excess voltage. Also, switching voltages in circuits are about 1 to 5 V, remaining about constant when device dimensions becomes smaller as predicted by Moore's law. Therefore, percentage-wise, the effect of the depletion region growth becomes more pronounced with decreased device dimensions.

Because of the non-zero slope of the i_D-v_{DS} curve, an incremental resistance can be defined as

$$r_o = \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1}_{v_{GS}=\text{constant}} \tag{1.5}$$

The above can be derived to be

$$r_o = \left[\lambda \frac{k_n'}{2}\frac{W}{L}(v_{GS} - V_{tn})^2\right]^{-1} \tag{1.6}$$

where $\lambda = 1/V_A$. One can rewrite the above as

$$r_o = \frac{V_A}{I_D'} \tag{1.7}$$

with

$$I_D' = \frac{k_n'}{2}\frac{W}{L}(V_{GS} - V_{tn})^2 \tag{1.8}$$

The equivalent circuit model of NMOS is then given in Figure 11. One can show this to be the case by rewriting (1.3) as

$$i_D = \frac{k_n'}{2}\frac{W}{L}(v_{GS} - V_{tn})^2(1 + \frac{v_{DS}}{V_A}) = \frac{k_n'}{2}\frac{W}{L}(v_{GS} - V_{tn})^2 + \frac{v_{DS}}{r_o} \tag{1.9}$$

The above can be represented as a voltage current source in parallel with the resistor r_o.

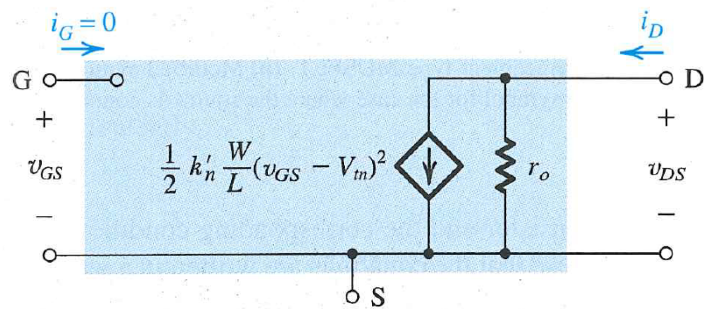

Figure 11: The equivalent circuit for an NMOS transistor when the Early effect is accounted for by including an output resistance r_o. As a result, i_D becomes larger when v_{DS} increases (Courtesy of Sedra and Smith).

The following example is from Sedra and Smith.

Example 5.2

Consider an NMOS transistor fabricated in a 0.18-μm process with $L = 0.18$ μm and $W = 2$ μm. The process technology is specified to have $C_{ox} = 8.6$ fF/μm^2, $\mu_n = 450$ cm^2/V·s, and $V_{tn} = 0.5$ V.

(a) Find V_{GS} and V_{DS} that result in the MOSFET operating at the edge of saturation with $I_D = 100$ μA.
(b) If V_{GS} is kept constant, find V_{DS} that results in $I_D = 50$ μA.
(c) To investigate the use of the MOSFET as a linear amplifier, let it be operating in saturation with $V_{DS} = 0.3$ V. Find the change in i_D resulting from v_{GS} changing from 0.7 V by +0.01 V and by −0.01 V.

Solution

First we determine the process transconductance parameter k_n',

$$\begin{aligned} k_n' &= \mu_n C_{ox} \\ &= 450 \times 10^{-4} \times 8.6 \times 10^{-15} \times 10^{12} \text{ A/V}^2 \\ &= 387 \ \mu\text{A/V}^2 \end{aligned}$$

and the transistor transconductance parameter k_n,

$$\begin{aligned} k_n &= k_n'\left(\frac{W}{L}\right) \\ &= 387\left(\frac{2}{0.18}\right) = 4.3 \text{ mA/V}^2 \end{aligned}$$

(a) With the transistor operating in saturation,

$$I_D = \frac{1}{2} k_n V_{OV}^2$$

Thus,

$$100 = \frac{1}{2} \times 4.3 \times 10^3 \times V_{OV}^2$$

which results in

$$V_{OV} = 0.22 \text{ V}$$

Thus,

$$V_{GS} = V_{tn} + V_{OV} = 0.5 + 0.22 = 0.72 \text{ V}$$

and since operation is at the edge of saturation,

$$V_{DS} = V_{OV} = 0.22 \text{ V}$$

Example 5.2 *continued*

(b) With V_{GS} kept constant at 0.72 V and I_D reduced from the value obtained at the edge of saturation, the MOSFET will now be operating in the triode region, thus

$$I_D = k_n\left[V_{OV}V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$50 = 4.3 \times 10^3\left[0.22V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

which can be rearranged to the form

$$V_{DS}^2 - 0.44V_{DS} + 0.023 = 0$$

This quadratic equation has two solutions

$$V_{DS} = 0.06 \text{ V} \quad \text{and} \quad V_{DS} = 0.39 \text{ V}$$

The second answer is greater than V_{OV} and thus is physically meaningless, since we know that the transistor is operating in the triode region. Thus we have

$$V_{DS} = 0.06 \text{ V}$$

(c) For $v_{GS} = 0.7$ V, $V_{OV} = 0.2$ V, and since $V_{DS} = 0.3$ V, the transistor is operating in saturation and

$$\begin{aligned} I_D &= \frac{1}{2}k_n V_{OV}^2 \\ &= \frac{1}{2} \times 4300 \times 0.04 \\ &= 86 \ \mu\text{A} \end{aligned}$$

Now for $v_{GS} = 0.710$ V, $v_{OV} = 0.21$ V and

$$i_D = \frac{1}{2} \times 4300 \times 0.21^2 = 94.8 \ \mu\text{A}$$

and for $v_{GS} = 0.690$ V, $v_{OV} = 0.19$ V, and

$$i_D = \frac{1}{2} \times 4300 \times 0.19^2 = 77.6 \ \mu\text{A}$$

Thus, with $\Delta v_{GS} = +0.01$ V, $\Delta i_D = 8.8$ μA; and for $\Delta v_{GS} = -0.01$ V, $\Delta i_D = -8.4$ μA.

We conclude that the two changes are almost equal, an indication of almost-linear operation when the changes in v_{GS} are kept small. This is just a preview of the "small-signal operation" of the MOSFET studied in Chapter 7.