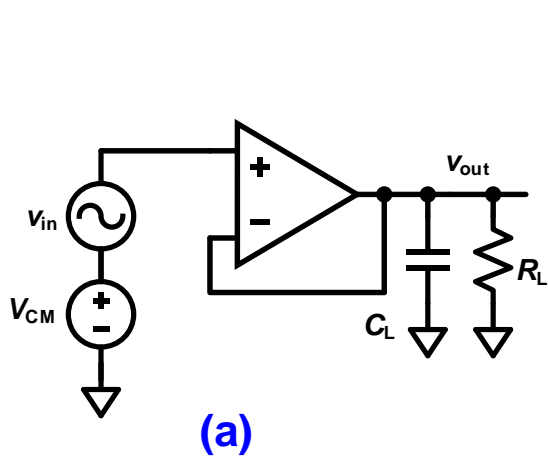


ECE 415/515 –ANALOG INTEGRATED CIRCUIT DESIGN

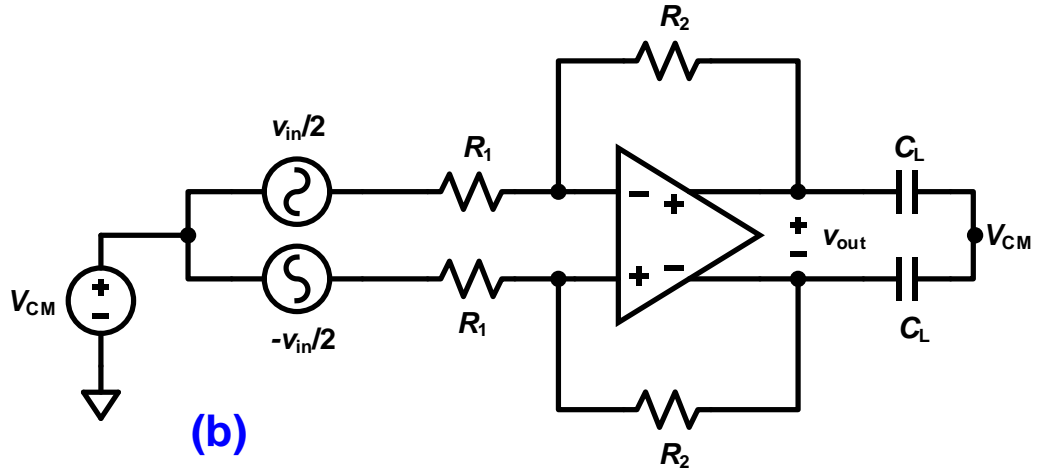
OPAMP DESIGN AND SIMULATION



OPAMP DESIGN PROJECT



ECE415/EO



ECE515



DESIGN SPECIFICATIONS

Parameter	Spec. for ECE 415	Spec. for ECE 515
Technology	TSMC 180n CMOS	
Supply voltage, V_{DD}	1.8V	
Common-mode voltage, V_{CM}	0.9V	
Typical load	$100k\Omega 1pF$	$C_L = 1pF$
Unit gain frequency (f_{un})	$> 50 MHz$	—
Open-loop gain (A_{OL})	$> 60 dB$	—
Closed-loop gain (A_{CL})	≥ 1	2
Closed-loop bandwidth ($f_{3dB,CL}$)	—	$> 20 MHz$
Slew-rate (SR)	$> 100 \frac{V}{\mu s}$	
Phase margin (ϕ_M)	60°	
Output swing	$> 0.75V_{DD}$	$> 1.5 \cdot V_{DD}$
Power consumption	Minimum possible	



TWO-STAGE OPAMP

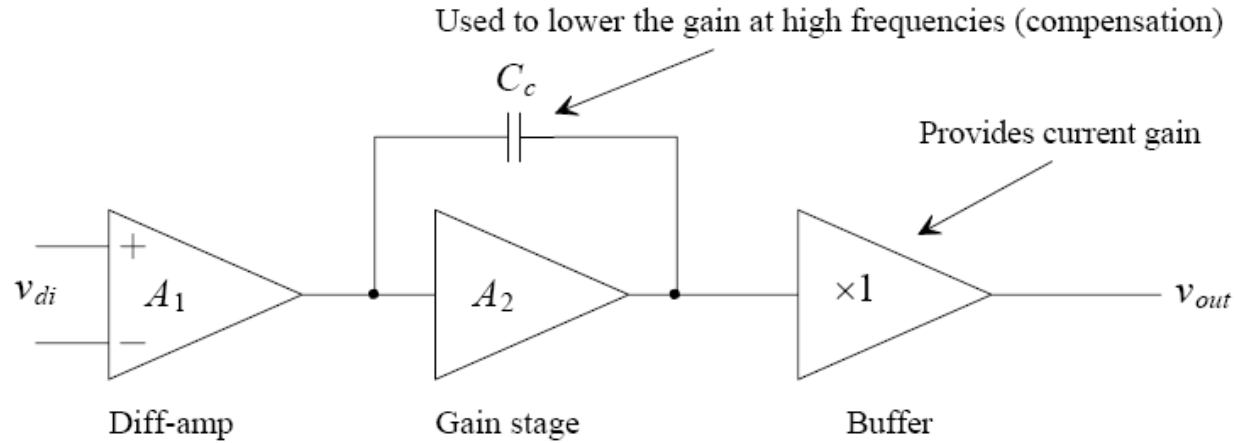
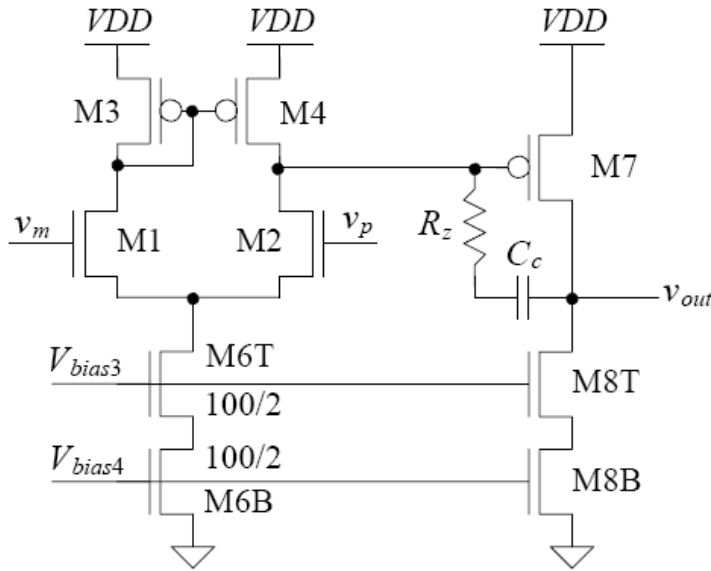
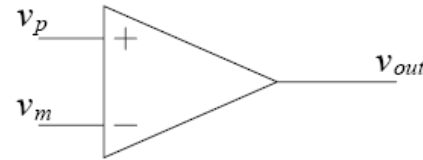


Figure 24.1 Block diagram of two-stage op-amp with output buffer.

TWO-STAGE OPAMP: MILLER COMPENSATION



Parameters from Table 9.2
with biasing circuit from
Fig. 20.47. Unlabeled NMOS
are 50/2 and PMOS are 100/2.
Scale factor is 50 nm.

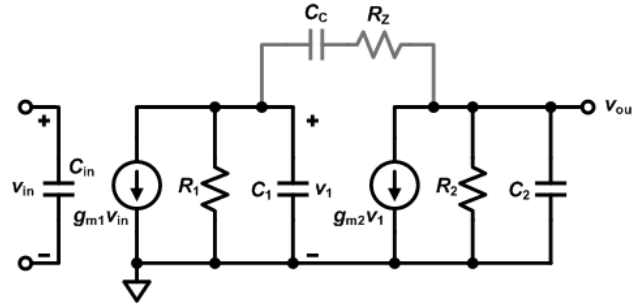


Op-amp schematic symbol

Figure 24.2 Basic two-stage op-amp.



MILLER COMPENSATION EQUATIONS



$$A_v = g_{m1}R_1g_{m2}R_2$$

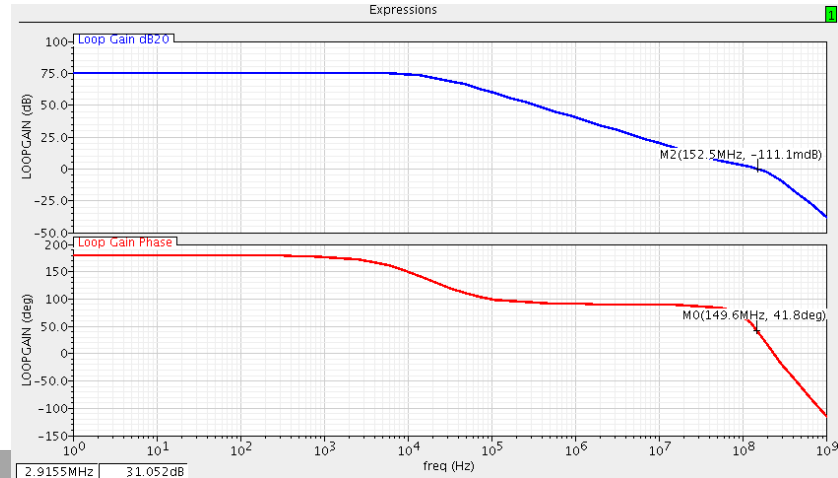
$$\omega_{p1} \approx \frac{1}{g_{m2}R_2R_1C_c}$$

$$\omega_{p2} \approx \frac{g_{m2}C_c}{C_2(C_1+C_c)+C_cC_1} = f\left(\frac{g_{m2}}{C_2}\right)$$

$$\omega_z \approx \frac{g_{m2}}{C_c}$$

$$\omega_{un} \approx \frac{g_{m1}}{C_c}$$

$$\omega_{z, nulling-R} \approx \frac{1}{\left(\frac{1}{g_{m2}-R_z}\right)C_c}$$



TWO-STAGE OPAMP: ZERO-NULLING R

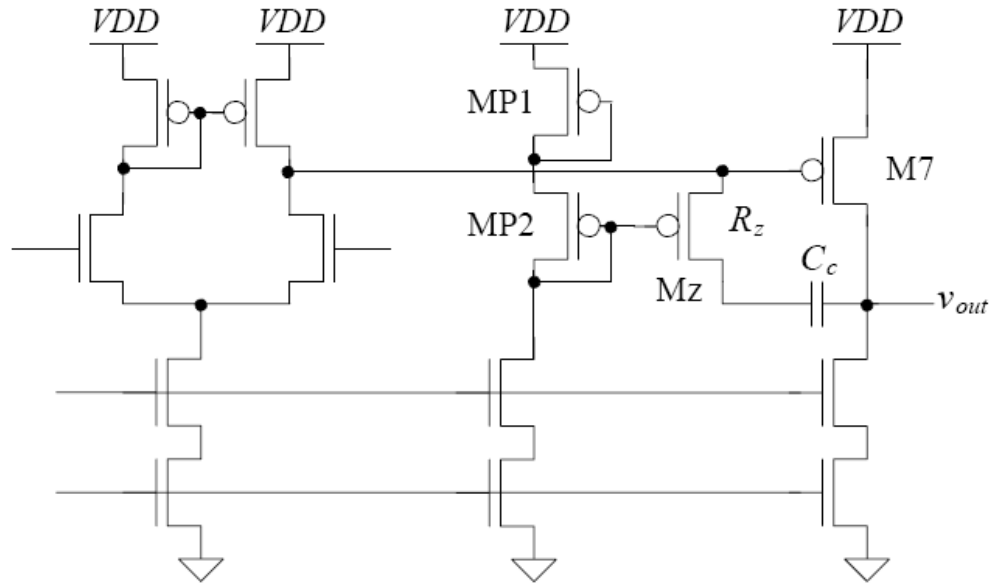


Figure 24.15 Making the zero-nulling resistor process independent.



VOLTAGE BUFFER COMPENSATION

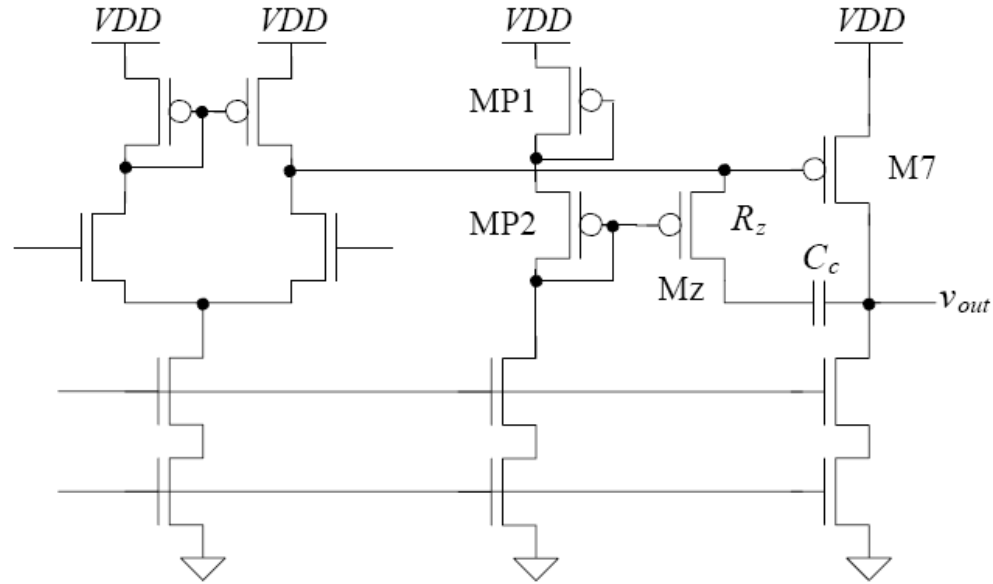


Figure 24.15 Making the zero-nulling resistor process independent.

COMMON-GATE COMPENSATION

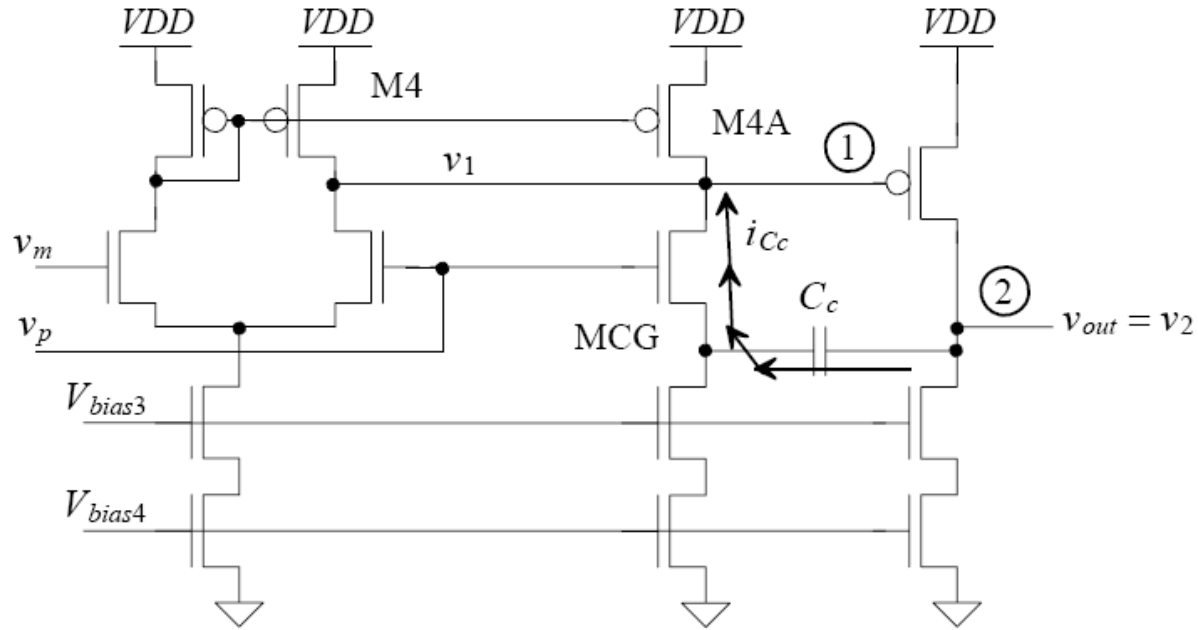
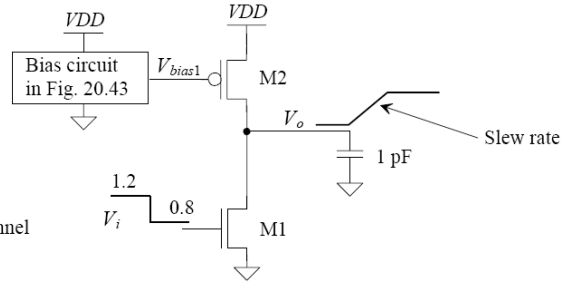


Figure 24.17 Feeding back a current indirectly to avoid the RHP zero.

CLASS-A STAGE: SLEWING



Use the long-channel sizes and biasing seen in Table 9.1.

Figure 21.18 Slew rate limitations in a class A amplifier.

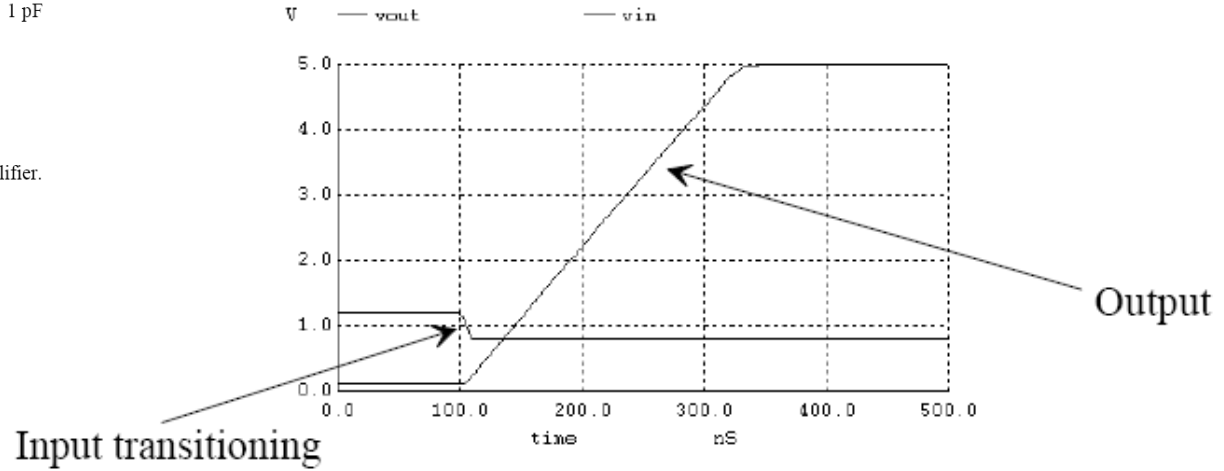
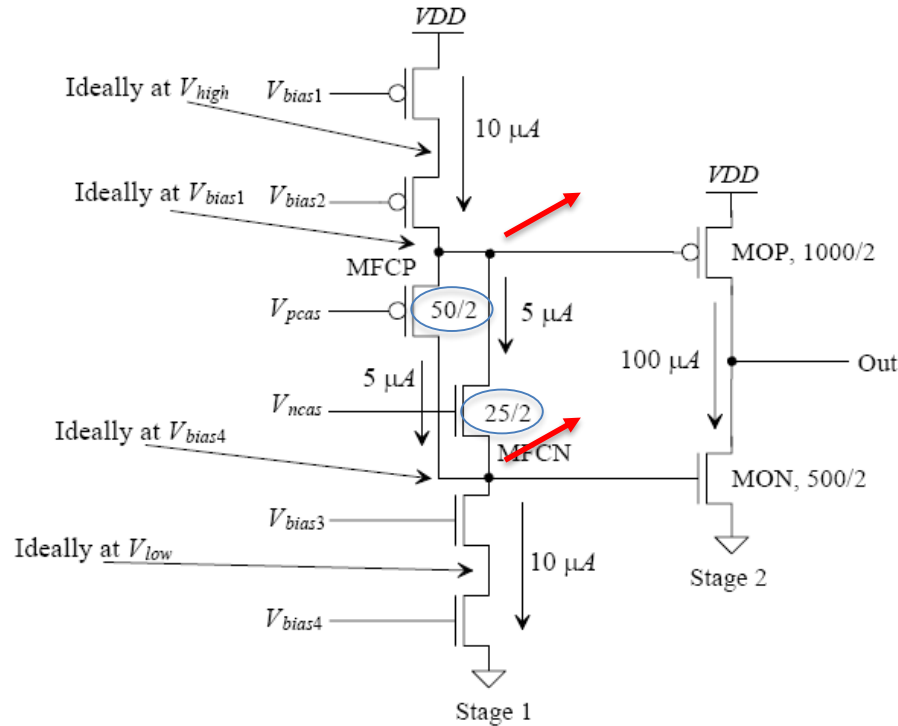


Figure 21.19 Verifying the results in Ex. 21.5



CLASS-AB STAGE: FLOATING MIRROR



Bias voltages come from Fig. 20.47 (short-channel parameters in Table 9.2). Unlabeled NMOS are 50/2, while unlabeled PMOS are 100/2.

Figure 20.49 Biasing with a floating current source.



TELESCOPIC+CLASS-AB STAGE

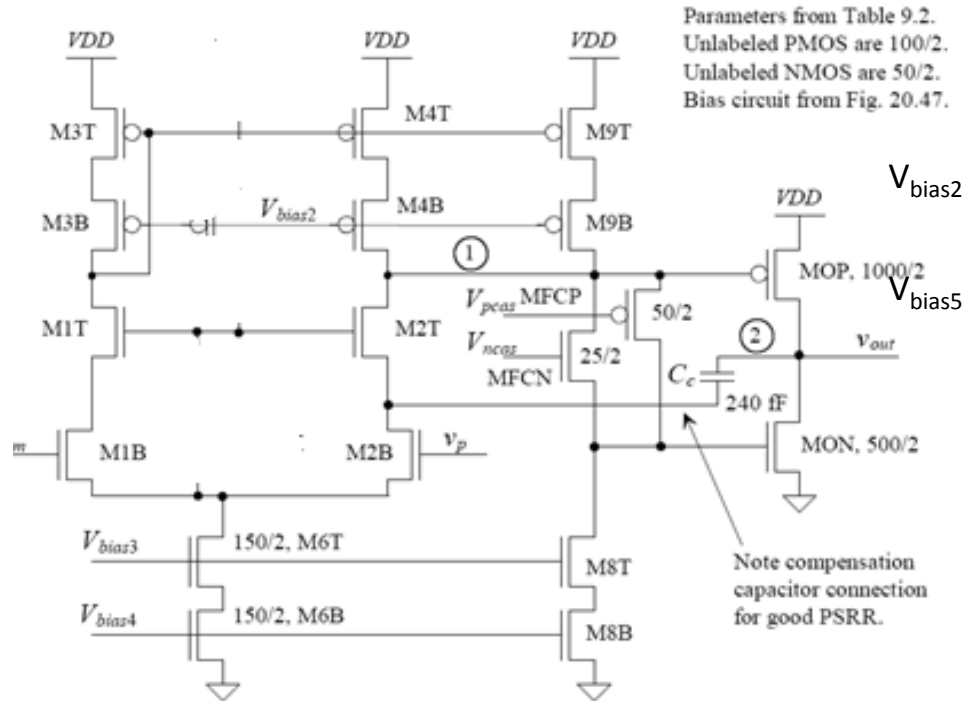


Figure 24.29 A CMOS op-amp with output buffer.

- Note that in this schematic, Indirect compensation is used.
 - C_c is connected between v_{out} and an internal low-impedance node
- For Miller compensation, connect C_c between nodes 1 and 2.
- V_{bias5} is generated using a replica bias circuit

FOLDED-CASCODE STAGE

Biasing from Fig. 20.47.
Sizes given in Table 9.2.

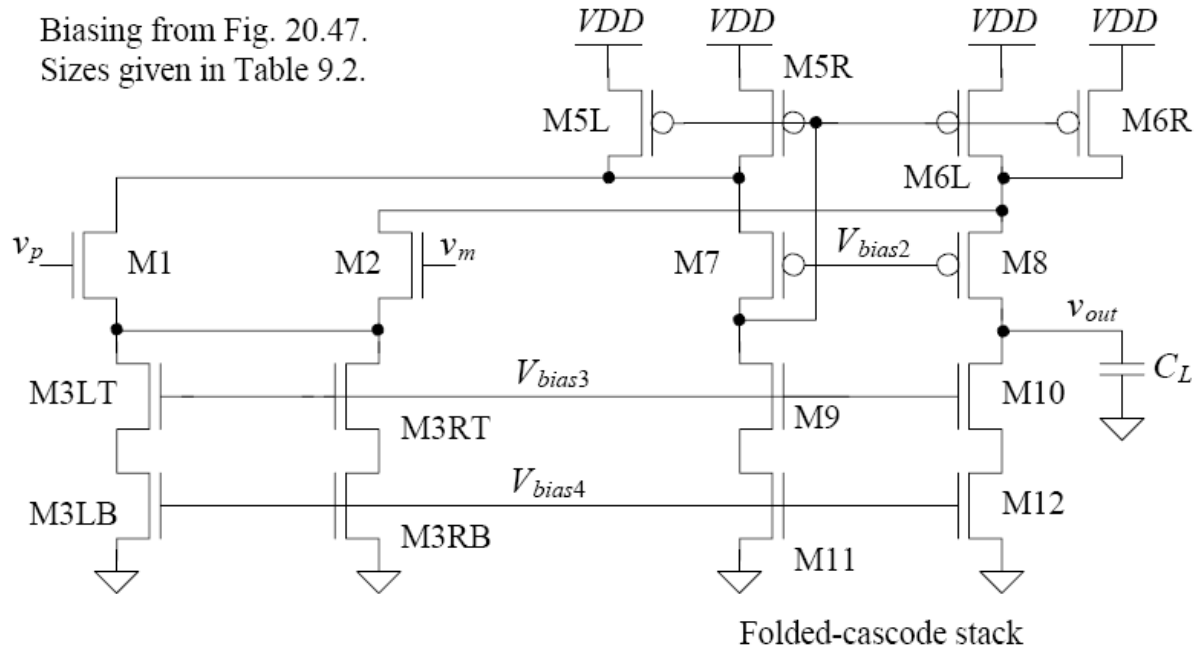
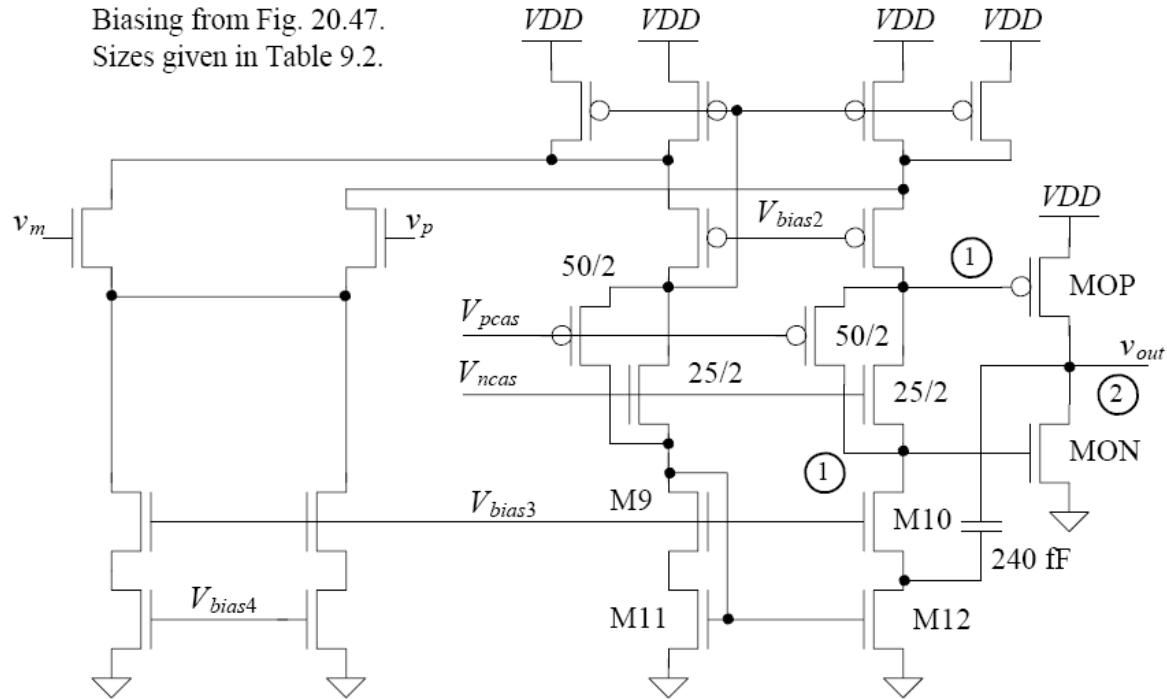


Figure 24.42 A folded-cascode OTA.



FOLDED-CASCODE WITH CLASS-AB OUTPUT

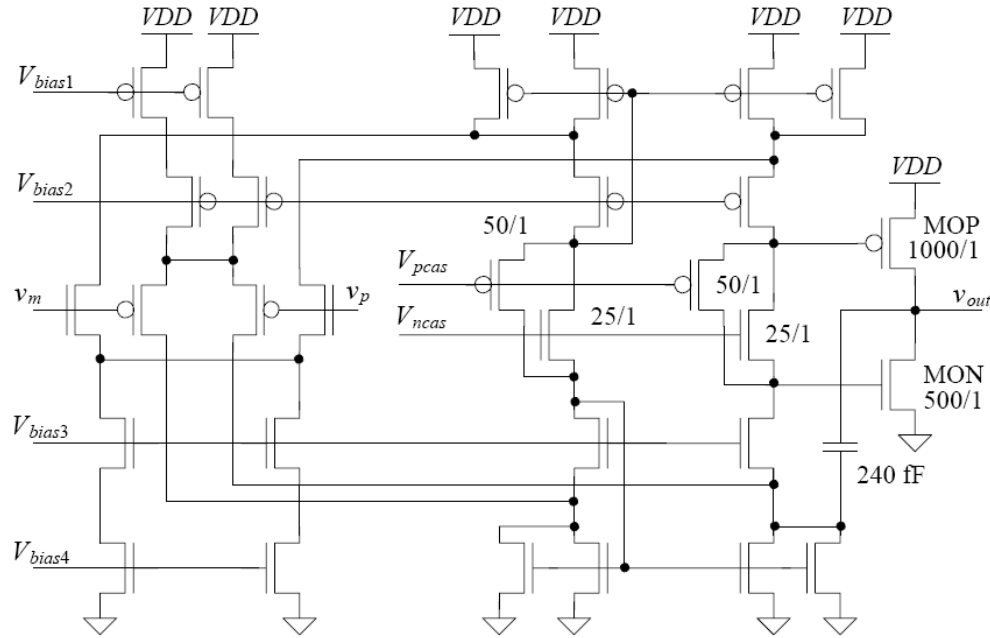
Biasing from Fig. 20.47.
Sizes given in Table 9.2.



- Note that in this schematic, Indirect compensation is used.
 - C_c is connected between v_{out} and an internal low-impedance node
- For Miller compensation, connect C_c between nodes 1 and 2.

Figure 24.44 Folded-cascode op-amp with class AB output buffer.

FC+CLASS-AB+RAIL-TO-RAIL INPUT



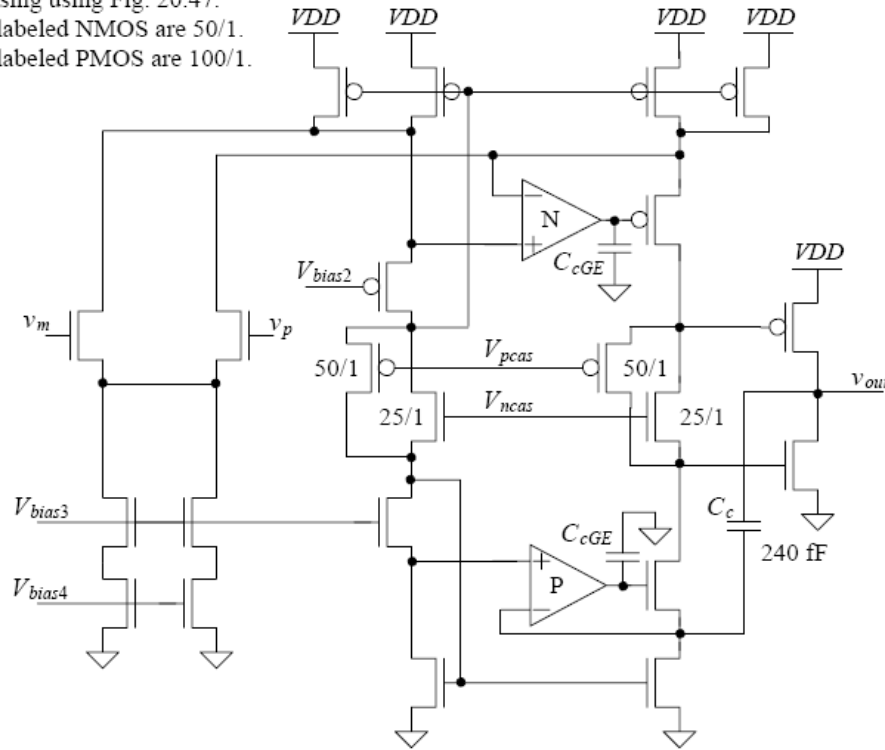
Biasing from Fig. 20.47.
 Unlabeled NMOS are 50/1.
 Unlabeled PMOS are 100/1.

Figure 24.48 An op-amp with an input common-mode range that extends beyond the power supply rails and that can drive heavy loads.



GAIN ENHANCEMENT

Biasing using Fig. 20.47.
Unlabeled NMOS are 50/1.
Unlabeled PMOS are 100/1.



- Note that in this schematic, Indirect compensation is used.
 - C_c is connected between v_{out} and an internal low-impedance node
- For Miller compensation, connect C_c between nodes 1 and 2.

Figure 24.51 Folded-cascode op-amp with class AB output buffer and gain-enhancement.



CADENCE SPECTRE STB ANALYSIS

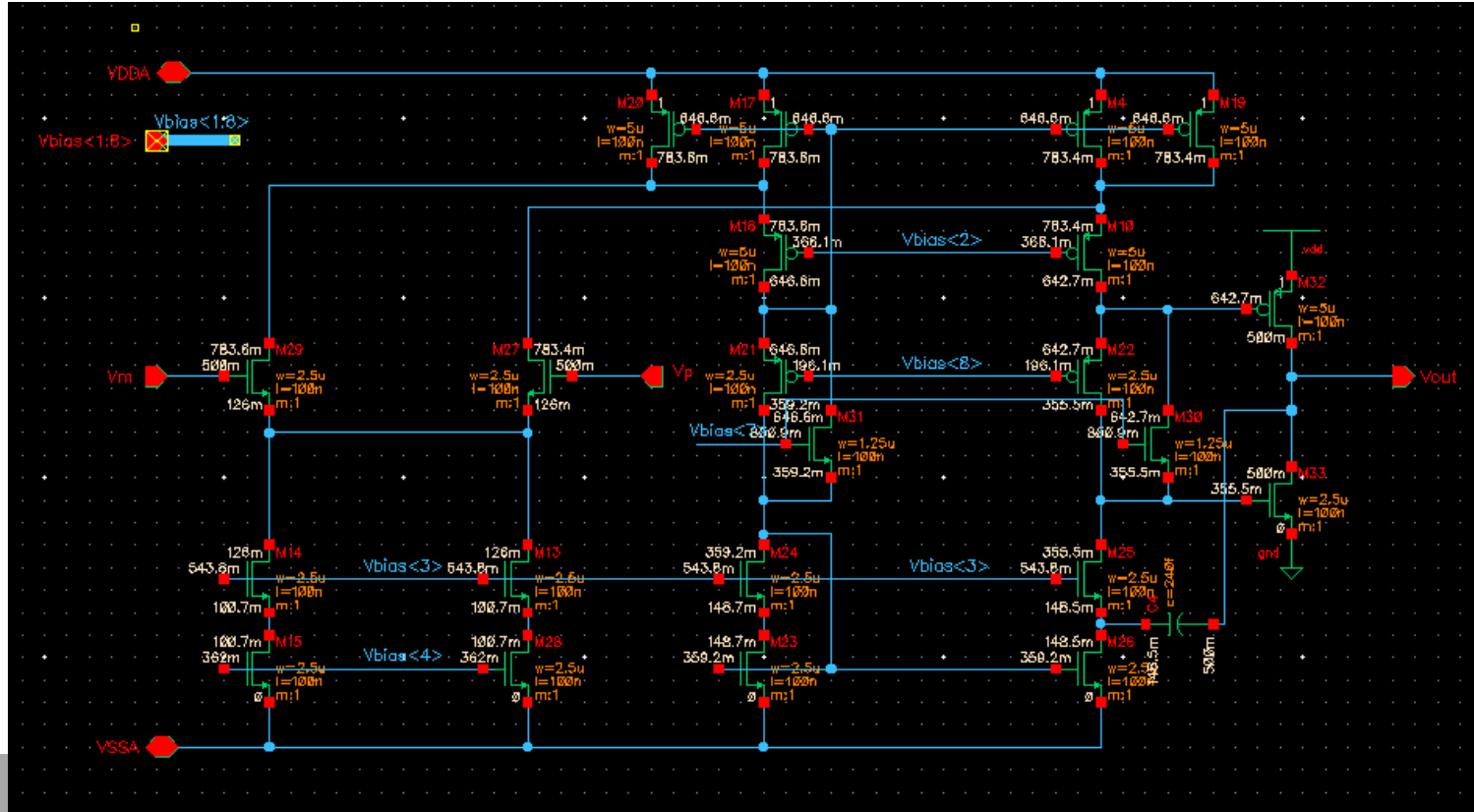


SPECTRE STB ANALYSIS

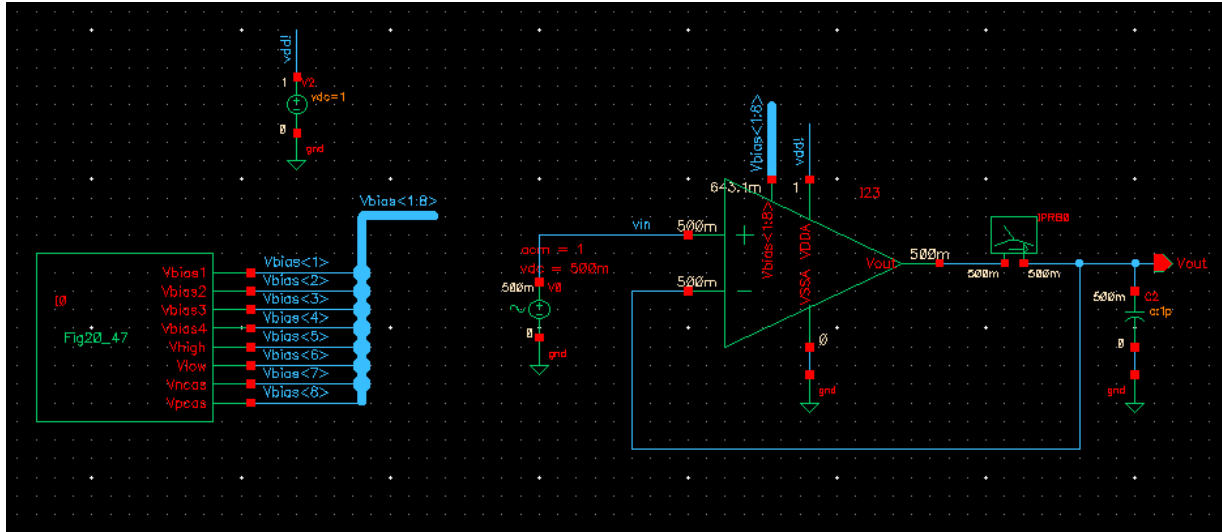
- The STB analysis linearizes the circuit about the DC operating point and computes the loop-gain, gain and phase margins (if the sweep variable is frequency), for a feedback loop or a gain device [1].
- Refer to the Spectre Simulation Reference [1] and [2] for details.



EXAMPLE SINGLE-ENDED OPAMP SCHEMATIC



STB ANALYSIS TEST BENCH



- Pay attention to the **iprobe** component (from **analogLib**)
 - Acts as a short for DC, but breaks the loop in **stb** analysis
- Place the probe at a point where it completely breaks (all) the loop(s).



DC ANNOTATION

The screenshot shows the Cadence Virtuoso Schematic Editor interface. The main window displays a circuit schematic for an Opamp1. A context menu is open over the schematic, listing options like 'DC Node Voltages', 'DC Operating Points', 'Model Parameters', 'Transient Node Voltages...', 'Transient Operating Points', 'Net Names', 'Component Parameters', 'Design Defaults', 'Show Parasitics', and 'Hide Parasitics'. The 'DC Node Voltages' option is selected. In the foreground, a results window titled 'Results in /tmp/simulation/vsaxena/Opamp1_AC/spectre/schematic' shows the following data:

Node	Voltage	Current
U18	783.6m	100n
U17	846.9m	100n
U14	646.9m	100n
U10	783.4m	100n
U19	842.7m	100n
U22	842.7m	100n
U21	846.9m	100n
U20	846.9m	100n
U15	846.9m	100n
U13	842.7m	100n
U25	359.2m	100n
U24	359.2m	100n
U23	148.7m	100n
U28	148.5m	100n
U26	359.2m	100n
U27	359.2m	100n
U16	100.7m	100n
U12	100.7m	100n
U11	100.7m	100n
U9	100.7m	100n
U8	100.7m	100n
U7	100.7m	100n
U6	100.7m	100n
U5	100.7m	100n
U4	100.7m	100n
U3	100.7m	100n
U2	100.7m	100n
U1	100.7m	100n

- Annotating the node voltages and DC operating points of the devices helps debug the design
 - Check device **gds** to see if its in triode or saturation regions



SIMULATION SETUP

Virtuoso® Analog Design Environment (1) - Opamp_test1 Opamp1_AC schematic

Session Setup Analyses Variables Outputs Simulation Results Tools Help **cadence**

Status: Ready T=27 C Simulator: spectre State: spectre_state1

Design Variables

Name	Value
------	-------

Analyses

Type	Enable	Arguments
1 dc	<input checked="" type="checkbox"/>	t
2 stb	<input checked="" type="checkbox"/>	1 1G /IPRBO Automatic Start-Stop

Outputs

Name/Signal/Expr	/alut	Plot	Save	Save Options
1 Loop Gain Phase	wave	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
2 Loop Gain dB20	wave	<input checked="" type="checkbox"/>	<input type="checkbox"/>	

Plotting mode: Replace

> Results in /tmp/simulation/vsaxena/Opamp1_AC/spectre/schematic
16 Netlist and Run

Choosing Analyses -- Virtuoso® Analog Design E

Analysis tran dc ac noise
 xf sens dcmatch stb
 pz sp envlp pss
 pac pstb pnoise pxf
 psp qpss qpac qpnoise
 qpxf qpsp

Stability Analysis

Sweep Variable
 Frequency
 Design Variable
 Temperature
 Component Parameter
 Model Parameter

Sweep Range
 Start-Stop Start: 1 Stop: 1G
 Center-Span

Sweep Type
Automatic

Add Specific Point

Probe Instance: /IPRBO Select

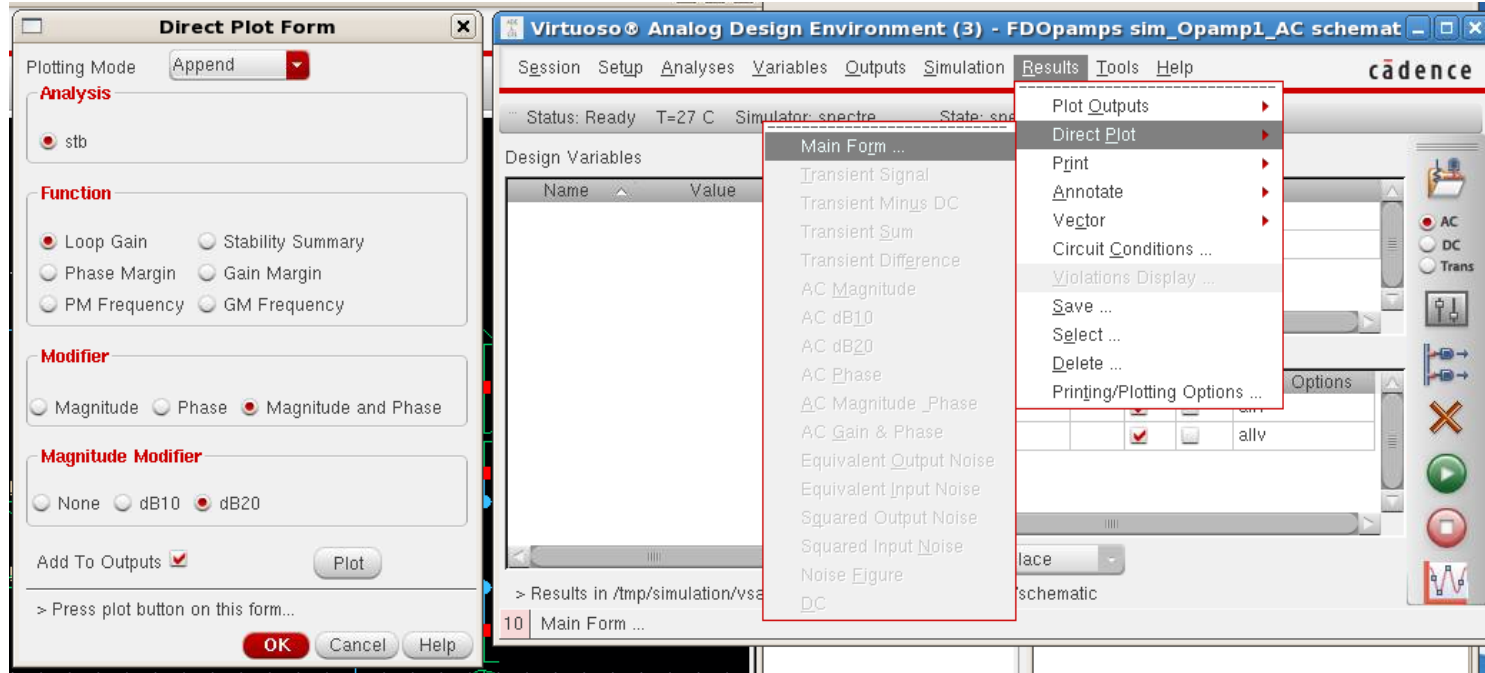
Enabled Options...

OK Cancel Defaults Apply Help



5) Could not get a license for ADE L. Trying a higher-tiered license
6) Checked out the license for ADE XL to run ADE L

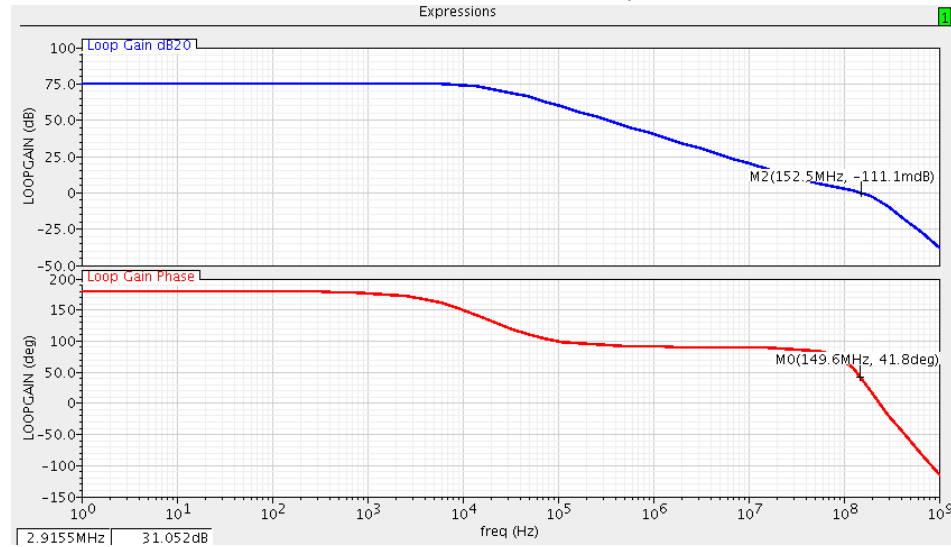
BODE PLOT SETUP



- Results->Direct Plot-> Main Form



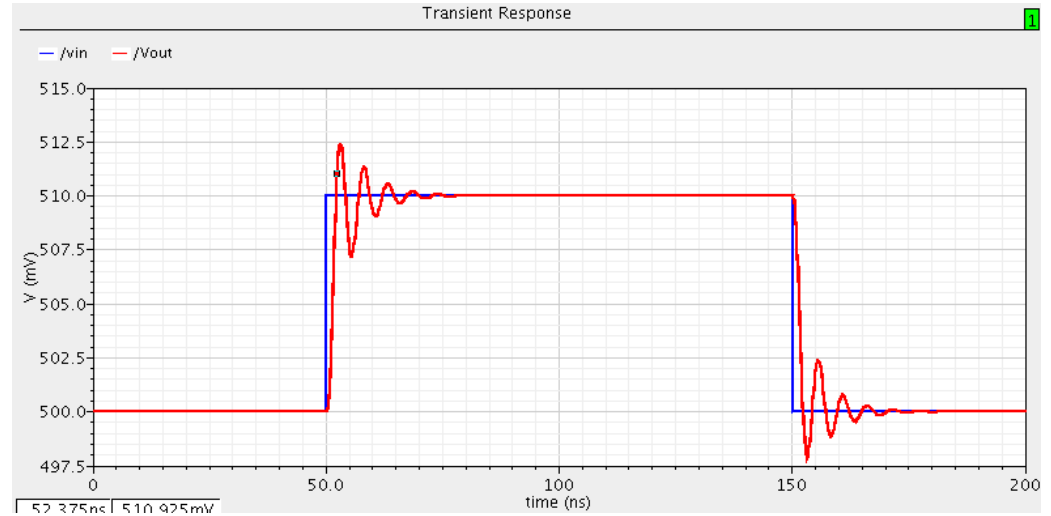
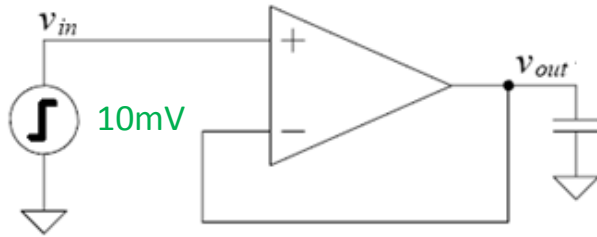
OPEN-LOOP RESPONSE (BODE PLOTS)



- Here, $f_{un} = 152.5$ MHz, $PM = 41.8^\circ$
- Best to use the stb analysis with circuit is in the desired feedback configuration
 - Break the loop with realistic DC operation points



SMALL STEP RESPONSE

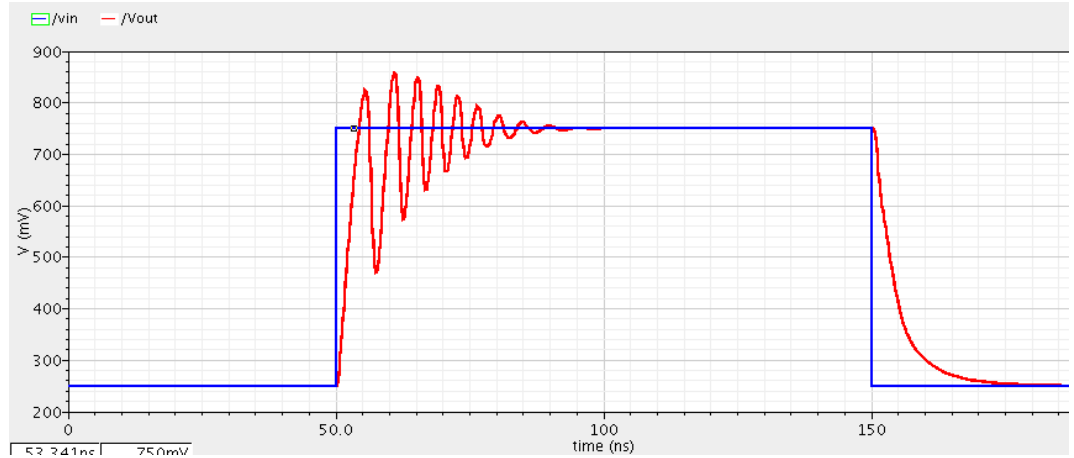
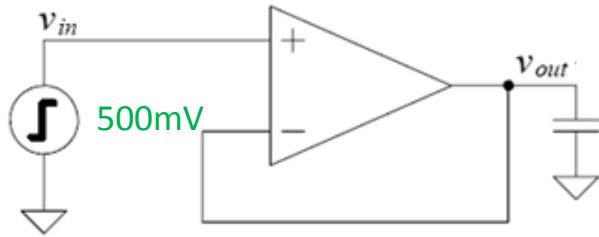


Observe the ringing (PM was 41°)

- Compensate more ($\uparrow C_c$ and/or $\uparrow g_{m2}$)



LARGE STEP RESPONSE



Note the slewing in the output

- Class-A: I_2/C_L
- Class-AB: I_{SS}/C_C



XF ANALYSIS (FOR CMRR, PSRR)

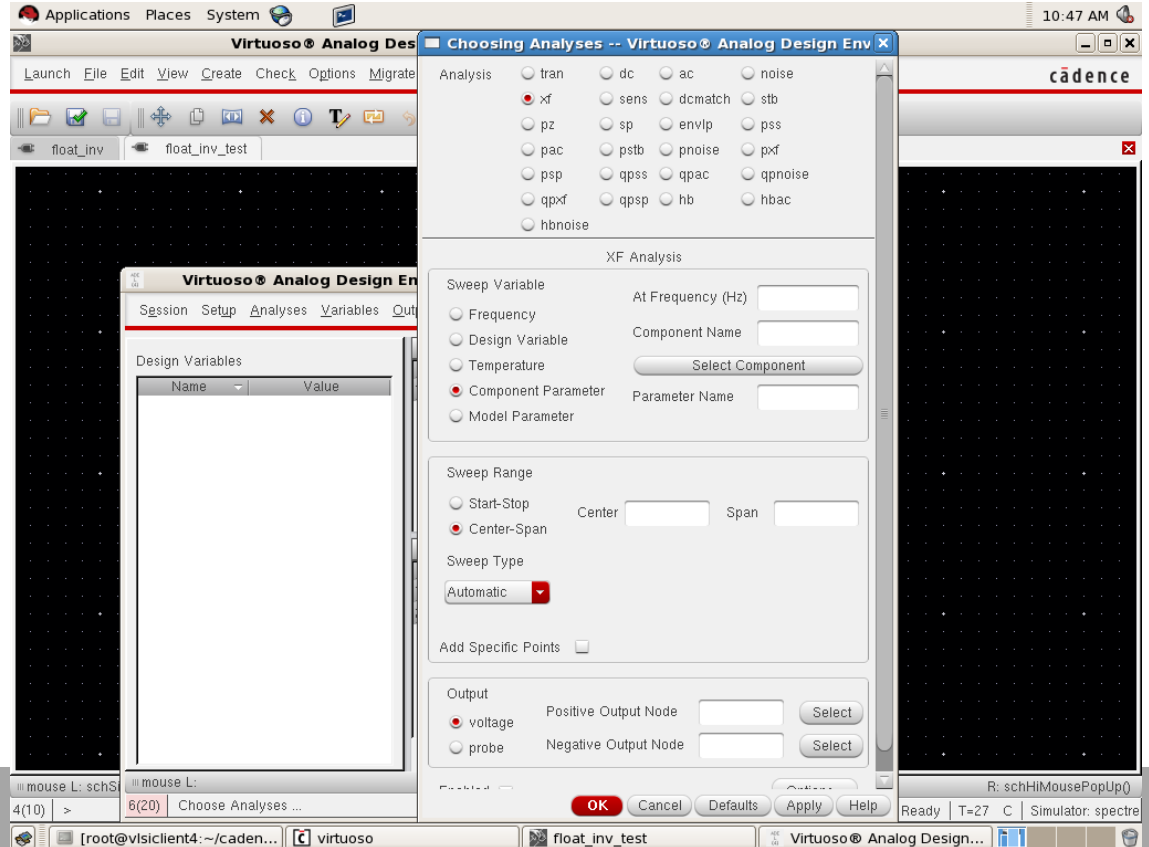
- For CMRR and PSRR plots, you can use **xf** analysis.
- Set up your testbench sources for the supplies (of course), but also a source representing the common mode voltage.
- Then run an **xf** analysis and tell it where the output of the circuit.
- You can then plot the transfer function from every source to the differential output of the circuit.

<http://www.designers-guide.org/books/dg-spice/ch3.pdf>



XF ANALYSIS

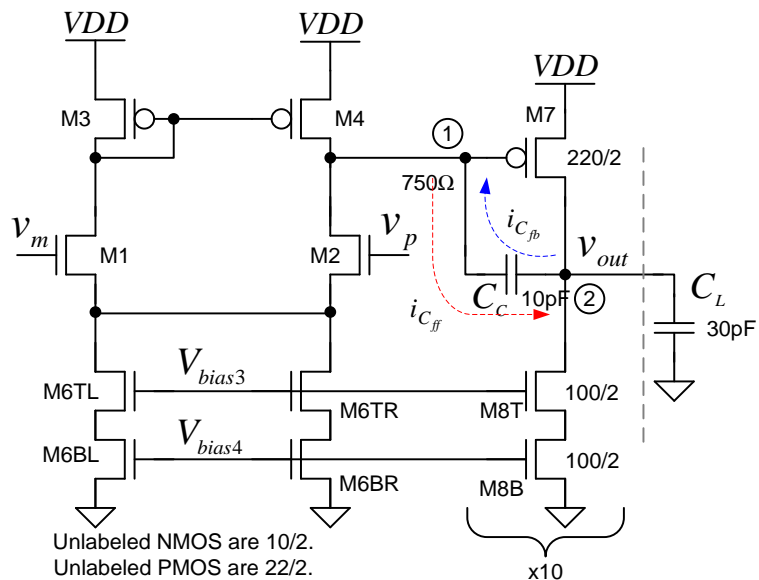
- XF analysis simultaneously computes individual transfer functions from every independent source to a single output.



TWO-STAGE OPAMP COMPENSATION TECHNIQUES



MILLER COMPENSATION



Compensation capacitor (C_c) between the output of the gain stages causes pole-splitting and achieves dominant pole compensation.

An RHP zero exists at $z_1 = \frac{g_{m2}}{C_c}$

- Due to feed-forward component of the compensation current (i_c).

The second pole is located at $-\frac{g_{m2}}{C_1 + C_2}$

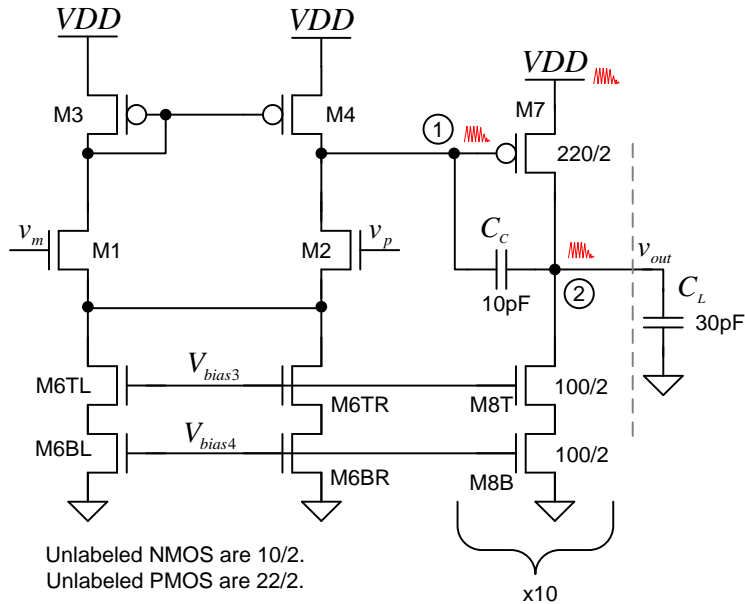
The unity-gain frequency is $f_{un} = \frac{g_{m1}}{2\pi C_c}$

A benign undershoot in step-response due to the RHP zero

❖ All the op-amps presented have been designed in AMI C5N 0.5 μ m CMOS process with scale=0.3 μ m and $L_{min}=2$. The op-amps drive a 30pF off-chip load offered by the test-setup.



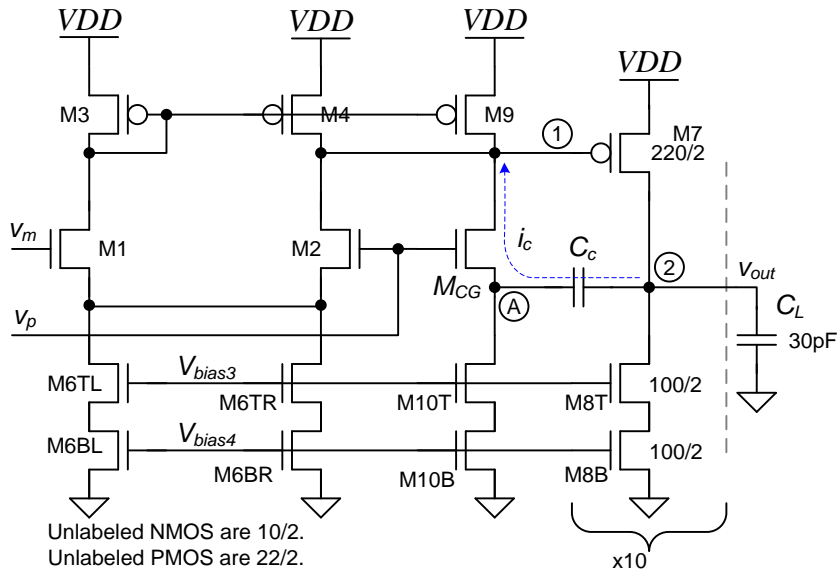
DRAWBACKS OF MILLER COMPENSATION



- The RHP zero decreases phase margin
 - Requires large C_c for compensation (10pF here for a 30pF load!).
- Slow-speed for a given load, C_L .
- Poor PSRR
 - Supply noise feeds to the output through C_c .
- Large layout size.



INDIRECT (AHUJA) COMPENSATION

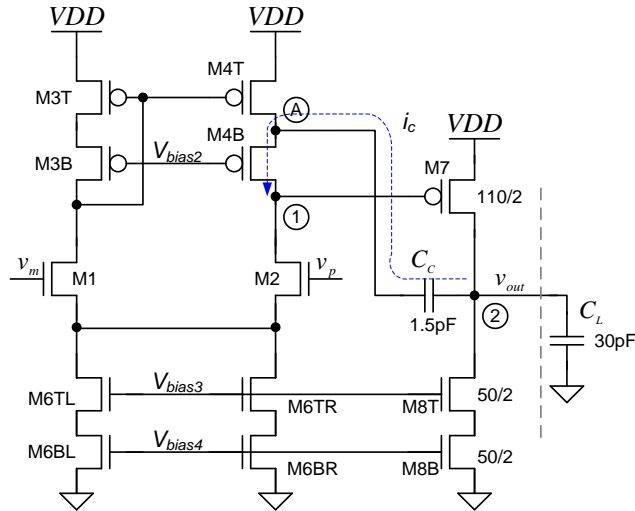


An indirect-compensated op-amp using a common-gate stage.

- The RHP zero can be eliminated by blocking the feed-forward compensation current component by using
 - A common gate stage,
 - A voltage buffer,
 - Common gate “embedded” in the cascode diff-amp, or
 - A current mirror buffer.
- Now, the compensation current is fed-back from the output to node-1 indirectly through a low-Z node-A.
- Since node-1 is not loaded by C_c , this results in higher unity-gain frequency (f_{un}).

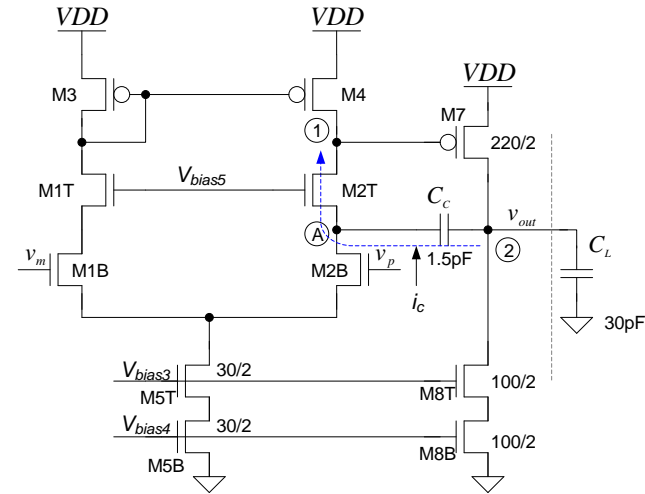


INDIRECT (CASCODE) COMPENSATION



Unlabeled NMOS are 10/2.
Unlabeled PMOS are 44/2.

Indirect-compensation using cascoded current mirror load.



Unlabeled NMOS are 10/2.
Unlabeled PMOS are 22/2.

Indirect-compensation using cascoded diff-pair.

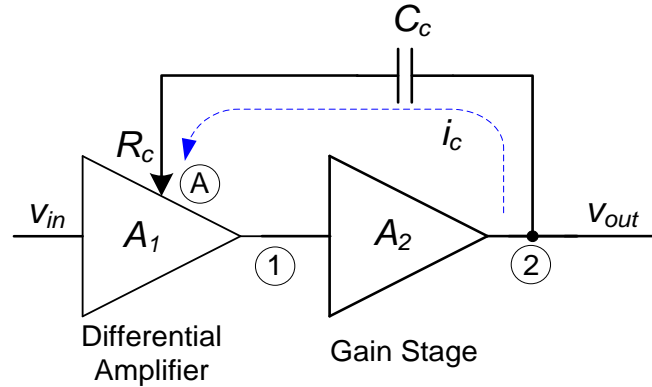
Employing the common gate device “embedded” in the cascode structure for indirect compensation avoids a separate buffer stage.

✓ Lower power consumption.

✓ Also voltage buffer reduces the swing which is avoided here.

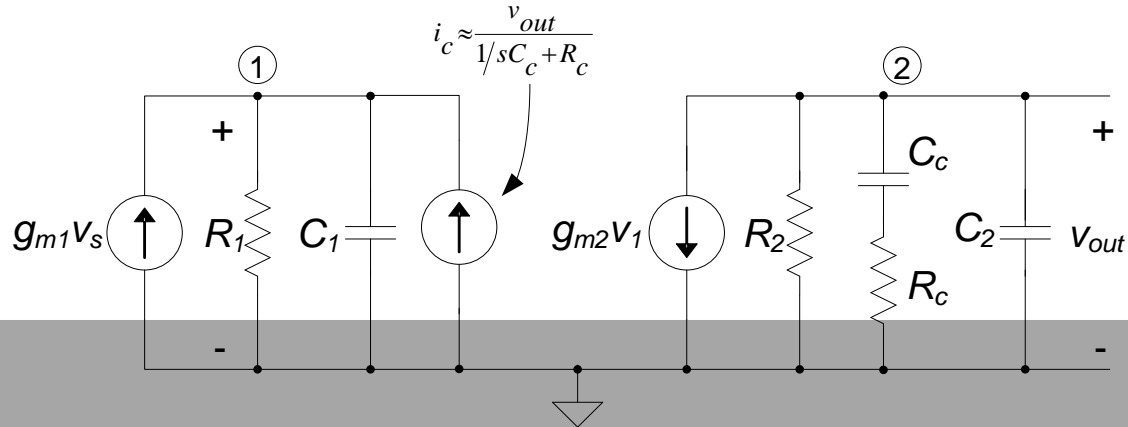


INDIRECT COMPENSATION: MODELING



The compensation current (i_c) is indirectly fed-back to node-1.

Block Diagram

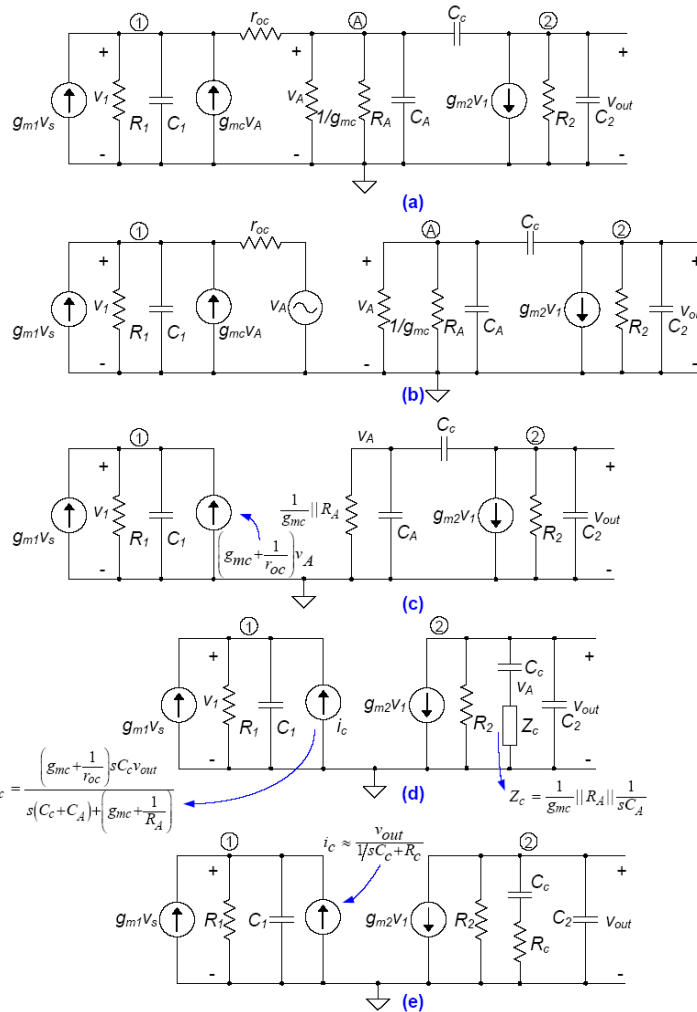


R_C is the resistance attached to node-A.

Small signal analytical model



Resistance r_{oc} is assumed to be large.



The small-signal model for a common gate indirect compensated op-amp topology is approximated to the simplified model seen in the last slide.

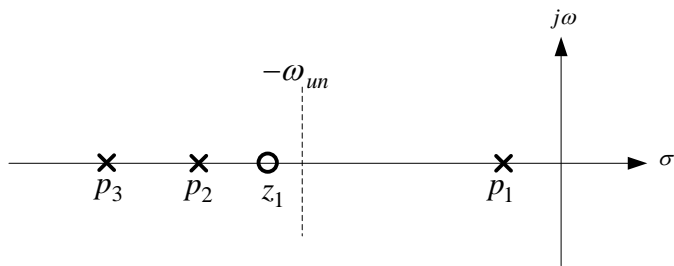
$$g_{mc} \gg r_{oc}^{-1}, R_A^{-1}, C_C \gg C_A$$

$$i_c = \frac{\left(g_{mc} + \frac{1}{r_{oc}}\right) s C_c V_{out}}{s(C_c + C_A) + \left(g_{mc} + \frac{1}{R_A}\right)}$$

$$i_c \approx \frac{V_{out}}{1/s C_c + R_c}$$



INDIRECT COMPENSATION: EQUATIONS



- Pole p_2 is much farther away from f_{un} .
 - Can use smaller $g_{m2} \Rightarrow$ less power!
- LHP zero improves phase margin.
- Much faster op-amp with lower power and smaller C_C .
- Better slew rate as C_C is smaller.

$$\frac{v_{out}}{v_s} = -A_v \left(\frac{1 + b_1 s}{1 + a_1 s + a_2 s^2 + a_3 s^3} \right)$$

$$z_1 \approx -\frac{1}{R_c C_c} \quad \text{LHP zero}$$

$$p_1 \approx -\frac{1}{a_1} = -\frac{1}{g_{m2} R_2 R_1 C_c}$$

$$p_2 \approx -\frac{a_1}{a_2} = -\frac{g_{m2} R_1 C_c}{C_2 (R_c C_c + R_1 C_1)} \approx -\frac{g_{m2} C_c}{C_L C_1}$$

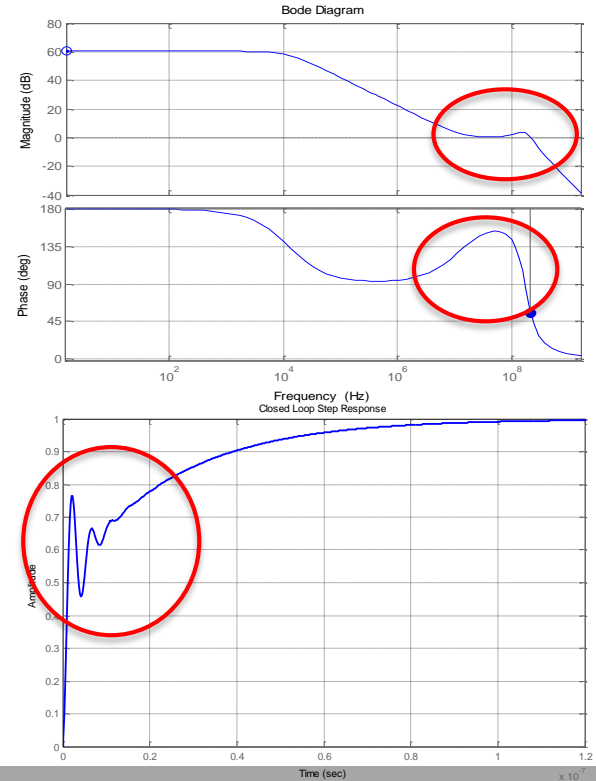
$$p_3 \approx -\frac{a_2}{a_3} = -\left[\frac{1}{R_c C_c} + \frac{1}{R_1 C_1} \right]$$

$$f_{un} = \frac{|p_1| A_v}{2\pi} \approx \frac{g_{m1}}{2\pi C_c}$$



EFFECT OF LHP ZERO ON SETTLING

- In certain cases with indirect compensation, the LHP-zero ($\omega_{z,LHP}$) shows up near f_{un} .
 - Causes gain flattening and degrades PM
 - Hard to push out due to topology restrictions
- Ringing in closed-loop step response
 - Used to be a benign undershoot with the RHP zero, here it can be pesky
 - Is this settling behavior acceptable?
- Watch out for the $\omega_{z,LHP}$ for clean settling behavior!
- When using indirect compensation be aware of the LHP-zero induced transient settling issues



REFERENCES

1. The Designer's Guide to SPICE and Spectre: <http://www.designers-guide.org/books/dg-spice/>
2. Spectre User Simulation Guide, pages 160-165: <http://www.designers-guide.org/Forum/YaBB.pl?num=1170321868>
3. M. Tian, V. Viswanathan, J. Hangtan, K. Kundert, "Striving for Small-Signal Stability: Loop-based and Device-based Algorithms for Stability Analysis of Linear Analog Circuits in the Frequency Domain," *Circuits and Devices*, Jan 2001. <http://www.kenkundert.com/docs/cd2001-01.pdf>
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7. Saxena V., Baker R.J., “Indirect compensation techniques for three-stage fully-differential op-amps,” IEEE MWSCAS 2010.
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