#### Department of Electrical and Computer Engineering

College of Engineering and Applied Sciences

WESTERN MICHIGAN UNIVERSITY



# ECE 4510/5530 Microcontroller Applications

Week 7

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#### MISC Stuff

- Project Progress?
  - Complete by end of next week (Friday)
  - Lab open this Saturday @ noon thank Lalith
- Lab 5 reports
  - Complete by end of spring break
- Lab 6
  - Code for operating uC/OS-II has been prepared and tested by Lalith Narasimhan. It is on the lab web site as Lab6\_Code
- 5x7 Display Code revisited
- Direct Digital Synthesis

# Optional Required Reading

Reminiscences of the VLSI Revolution:

How a series of failures triggered a paradigm shift in digital design

By Lynn Conway

IEEE SOLID-STATE CIRCUITS MAGAZINE, vol.4, no.4, pp.8-31,

Dec. 2012

• <a href="http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6393023">http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6393023</a>

# **5x7 Display Revisited**

#### Text Keypad Code Function

```
if(display5x7 advance flag)
                                                                                         // 1 cycle load column bit
                                                                                         // 15 cycles load row data shift column bit and enable
          display5x7 advance flag = FALSE;
                                                                                         // 1 cycle shift column bit to 16th/empty column
         PORTA = 0x08;
                                                 // Output disable row source
                                                                                         // Operational rate approx. 60 Hz * 17 \sim 1020 Hz
         switch(display count)
                                                                                         // Using rti @ 1.024 msec => 976 Hz
          case 0:
                                                                                         // or 57.4 complete scans/sec
                 PORTA = 0x10;
                                                 // Set one into the first shift register
                 PORTA = 0x20;
                                                 // shift register clock rise
                                                 // shift register clock fall, remove input data
                 PORTA &= \sim (0x30);
                                                 // The next clock will cause the 1st column to be active
                 display count++;
                                                 // increment counter
                 break;
          case 1:case 2:case 3:case 4:case 5:case 6:case 7:case 8:case 9:
          case 10:case 11:case 12:case 13:case 14:case 15:
                 row location = display count + offset - 1;
                                                                  // row index
                 row load(row data array[row location]);
                                                                  // load the row value
                 PORTA = 0x20;
                                                                  // shift register clock rise
                 PORTA &= \sim (0x08);
                                                         // Output enable row source
                 PORTA &= \sim (0x20);
                                                         // shift register clock fall
                  display count++;
                                                         // increment counter
                 break;
                  default:
                  PORTA = 0x20;
                                                 // shift register clock rise
                 PORTA &= \sim(0x20); // shift register clock fall
                  display count = 0;
                 break;
ECE end display5x7_advance
```

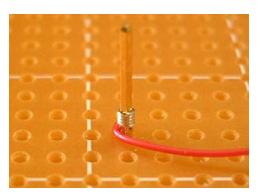
4510/5530

#### C-Library

- Tested and corrected code from the keypad and 5x7 display has been added to the C-library zip file on the course web site.
  - Thanks to Lalith for testing and correcting my original musings.

#### Wire Wrap Prototypes

- Lost Knowledge: Wire-wrapping
- By Gareth Branwyn, 2009/07/27 @ 3:16 pm
- <a href="http://blog.makezine.com/2009/07/27/lost-knowledge-wire-wrapping/">http://blog.makezine.com/2009/07/27/lost-knowledge-wire-wrapping/</a>





- For a nice wire wrap job, see
- http://blog.imakecircuits.com/category/breadboard-freaks/

#### PC Board and Wire Wrap Sockets

- PC BOARD 4"X5" UNCLAD 0.1"
- Twin Industries, Part Number 7100-45
- Digikey Part Number 438-1019-ND, \$4.68
- IC SOCKET MACH PIN WW 8/14/16POS GOLD
- Assmann WSW Components
  - AR08-HZW/T-R
  - AR14-HZW/T-R
  - AR16-HZW/T-R
- Digikey Part Number
  - AE10046-ND, \$1.45
  - AE10047-ND, \$2.55
  - AE10048-ND, \$2.69







## Wire Wrap Tool and Wire

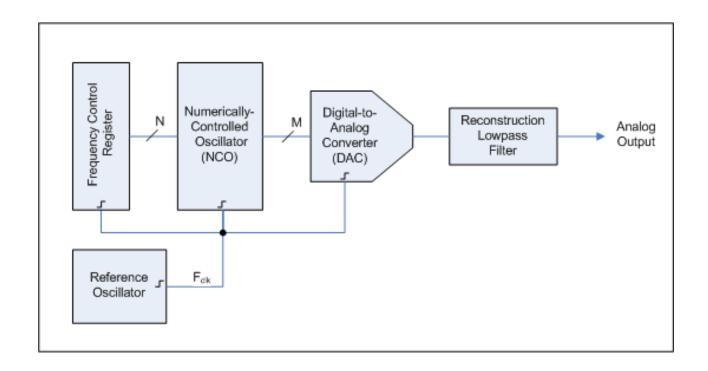
- TOOL WRAP/STRIP/UNWRAP MOD 30AWG
- OK Industries/Div of Jonard Ind Corp, WSU-30M
- Digikey Part Number K105-ND
- \$31.85
- Wire Wrap Wire 30 Gauge
- Digikey Part Number K229-ND
- 30 foot roll for \$9.65



# Direct Digital Synthesis - something to do with DACs

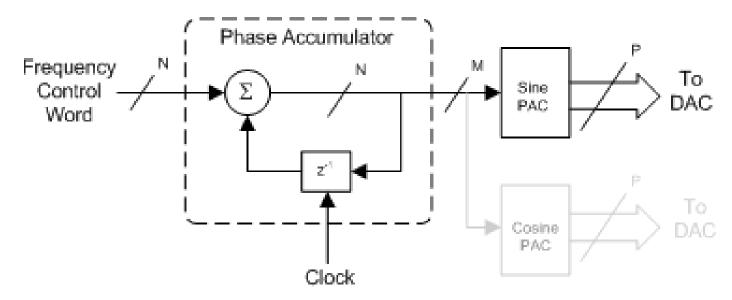
## Direct Digital Synthesis

- From Wikipedia, the figure works great ...
  - http://en.wikipedia.org/wiki/Direct digital synthesizer
  - Implementation: digital logic, DAC and analog filter.



#### Numerically Controlled Oscillator

- The NCO forms time samples of the waveform desired.
  - Wikipedia again: <a href="http://en.wikipedia.org/wiki/Numerically\_controlled\_oscillator">http://en.wikipedia.org/wiki/Numerically\_controlled\_oscillator</a>



- A phase accumulator/summer: generate  $\theta$
- Sinusoidal output generators/ROM:  $sin(\theta)$  or  $cos(\theta)$

## Drawback of Microprocessors

- The sound is subject to the periodicity of the outputs
  - The sample rate should be constant.
  - The loading of the DAC should be periodic ... using a counter/timer channel at a constant output frequency
  - The waveform samples are loaded into the DAC and then output using the periodicity of the timer channel.
- Alternative: A Xilinx device makes an excellent NCO and sin/cos table lookup with clock based periodicity.
  - Microcontroller adjusts the frequency control word or instantaneous phase that sill be accumulated.

#### Xilinx DDS

- DDS V5.0, DS246, April 28, 2005
  - http://www.xilinx.com/support/documentation/ip\_documentation/dds.pdf

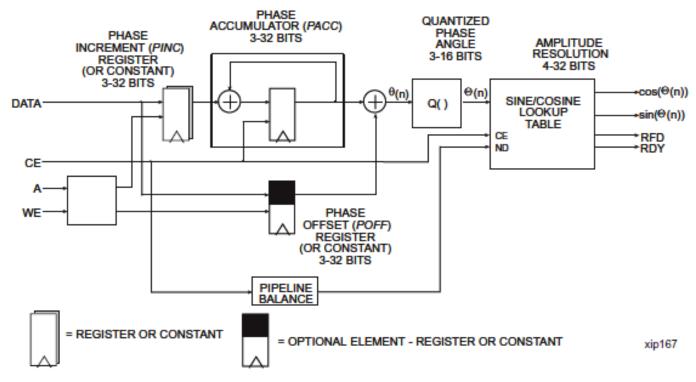


Figure 16: DDS Core (Detailed View)

## Example Output

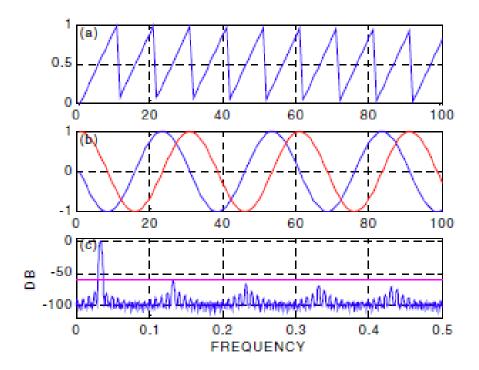


Figure 17: DDS plots showing (a) phase error time series, (b) complex output time series, (c) output spectrum. 1024 deep lookup table, 16-bit samples, output frequency is 0.333 Hz.

#### Frequency Modulated Waveform

- If the phase increment register is constant
  - A single frequency results
- If the phase increment register is linearly incremented
  - A chirp waveform is generated
- If the phased increment register changes with the input from a microphone with a constant offset
  - A frequency modulated waveform results
  - This is a simple way to make FM

# Wavetable Synthesis

- another way to make sound

#### Generate a Waveform Table

- Collect one cycle of a waveform desired.
   We did not have to use a sine or cosine table!
  - Imagine that it is stored in a circular buffer that can be continuously read out ... a continuous waveform results.
  - It can be played back at any desired sample rate resulting in different frequencies of the same waveform.
  - If the waveform was sampled at a very high sample rate, not all samples need to be produced you could "step across" the waveform with different "time steps" to increase or decrease the output frequency.
- Multiple waveforms can be summed and "processed" using DSP

#### Extending to Radios

• Components of a software radio

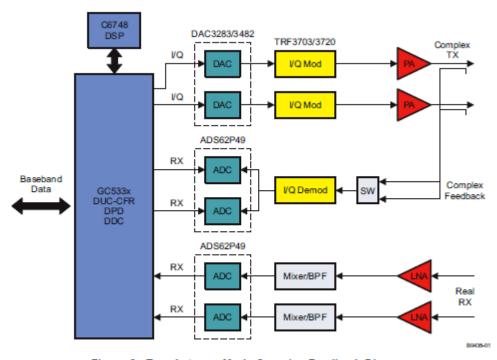
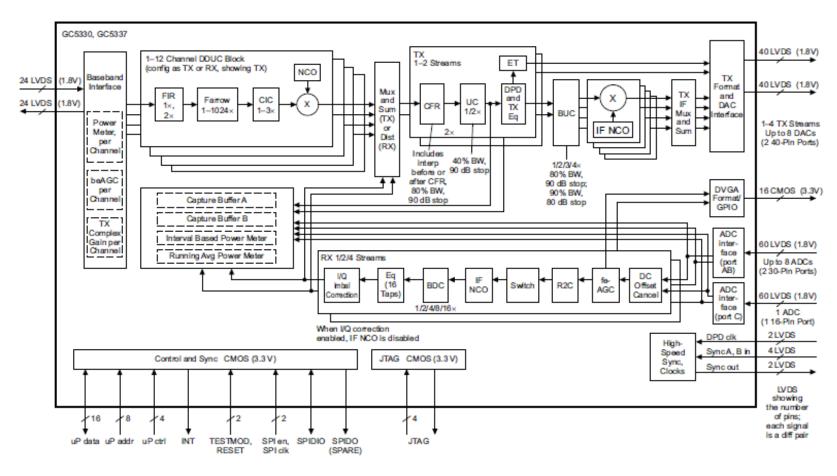


Figure 3. Two-Antenna-Mode Complex-Feedback Diagram

Texas Instruments, Wideband Transmit-Receive Digital Signal Processors, GC5330 and GC5337

#### GC5330/GC5337



B0445-01

NOTE: UC1 and UC2 are for CFR interpolation; UC2 can only be used if UC1 is also used.

Figure 6. GC533x Block Diagram