ECE520 – VLSI Design

Lecture 0: Introduction to VLSI Technology

Payman Zarkesh-Ha

Office: ECE Bldg. 230B
Office hours: Wednesday 2:00-3:00PM or by appointment
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Course Objectives

- We will focus mainly on ***CMOS integrated circuits***
- There will be a design project assigned including:
  - Schematic design using S-Edit
  - Spice simulations and design verification
  - Layout design using L-Edit (including LVS and DRC)
  - Circuit extract and spice simulation (again)
- Project will be done by groups of 3 students
- Project grade will be based on:
  - Quality of report
  - Performance (speed/delay)
  - Power dissipation
  - Layout area
- There will be a 10% extra credit for any design that beats certain criteria for layout area, performance, or power consumption

Textbook and References

- **Main textbook:**
  - **"Digital Integrated Circuits" by J. M. Rabaey et al. (2nd edition)**
- **Other reference books:**
  - **"Physical Design of CMOS Integrated Circuits Using L-Edit" by J. Uyemura**
  - **"Design of High-Performance Microprocessor Circuits", by A. Chandrakasan**
- **Lecture Notes: combination of slides and discussions**
  - **Slides will be posted on the class webpage**
  - **Class webpage: *www.unm.edu/~pzarkesh/ECE520***
- **Reference papers posted on the class webpage**

Grading Policy

- Your grade in the course will be comprised of:
  - Homework (25%)
  - Project (25%)
  - Midterm Exam (25%)
  - Final Exam (25%)
- Final letter grade will be based on curve and class performance
- No makeup exam

Homework Policy

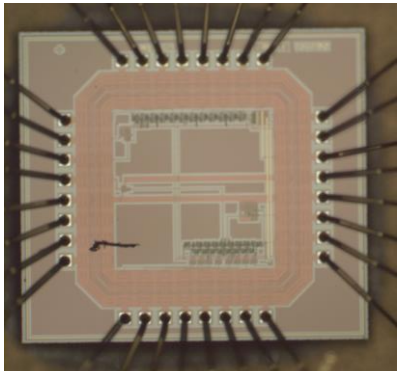
- Homework will be on weekly basis and is setup for the project
  - Learn CAD tools and basic circuits
  - Require lab work
- Solutions will be posted on the class website as soon as I can
- Late homework and projects have 20% per day credit penalty

Class Project & Tools

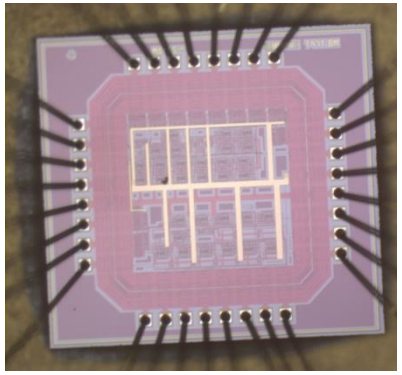
- Use of CAD tools will be required for most assignments. Get yourself familiarized with the tools from today!
- This is a project oriented course. Be prepared for extensive lab work!
- We will be using L-Edit for our VLSI project
  - all Tanner tools including L-Edit, S-Edit, T-SPICE, LVS, and W-Edit are installed on all machines in ECE 211 Lab
  - The tools can also be installed on your own computer for the project use
  - for more information about these tools, please visit class website
- We will be using ON Semiconductor 0.5um for our project
  - Selected projects will be submitted for manufacturing by MOSIS
  - for more information about this process please visit https://www.mosis.com/vendors/view/on-semiconductor/c5

Projects Manufactured by MOSIS in 2009

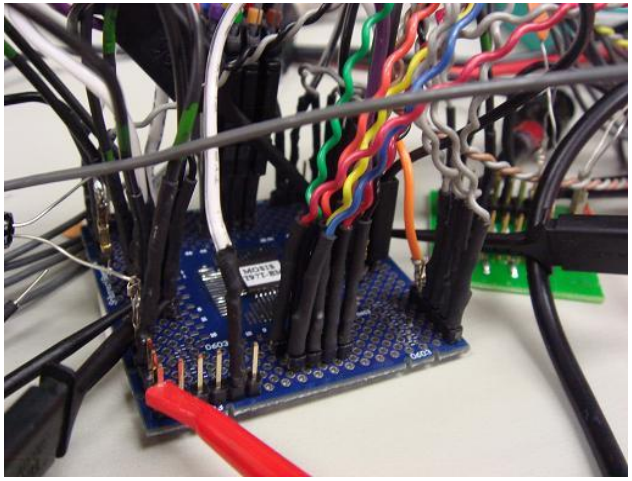
Test Chip 1	Test Chip 2
Thomas Leboeuf John (Colby) Hoffman	Kevin Fox Srinivasan Sridhar Shawn Levesque

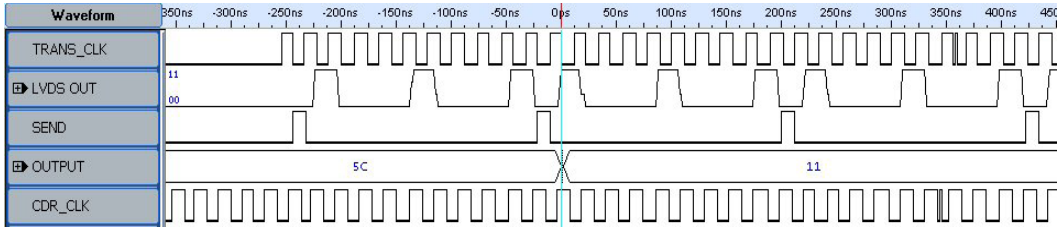


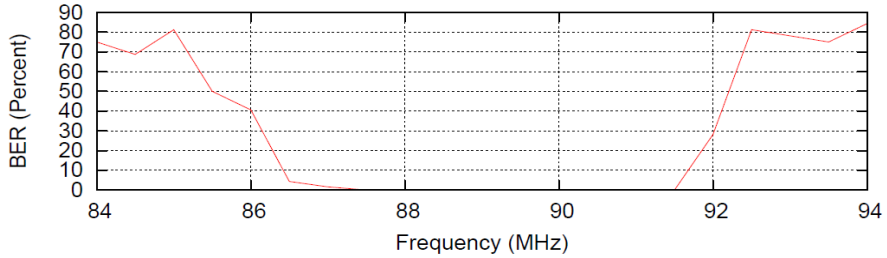
Test Chip 1



Test Chip 2

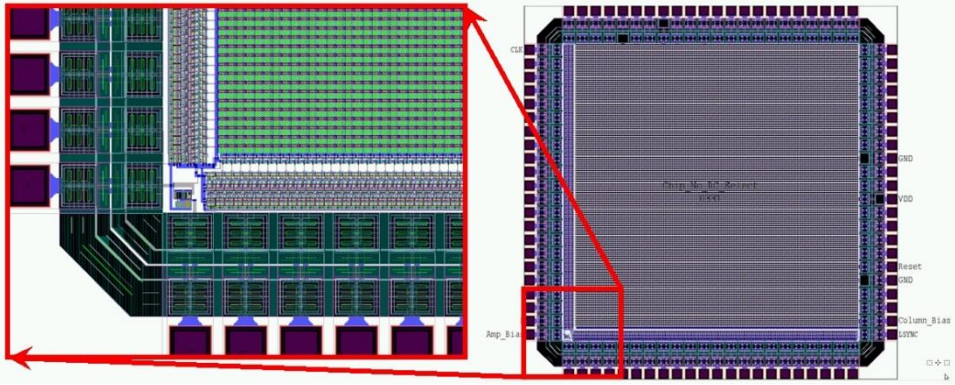


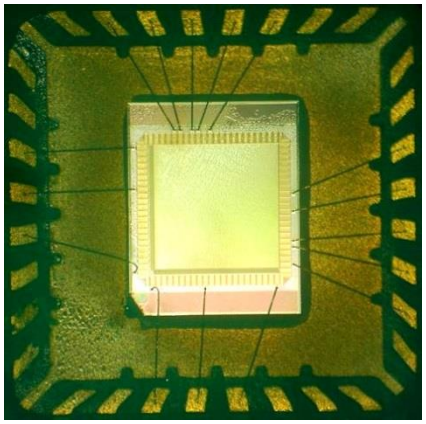




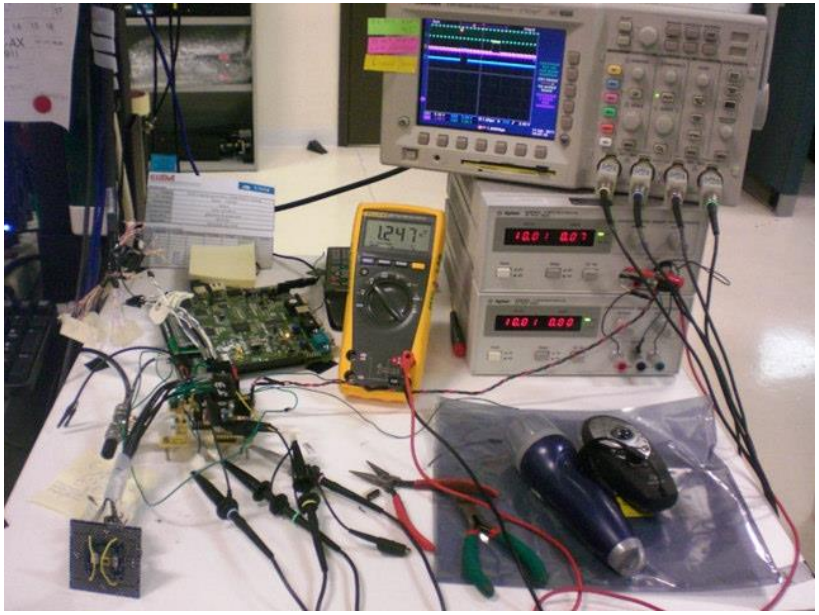
Projects Manufactured by MOSIS in 2010

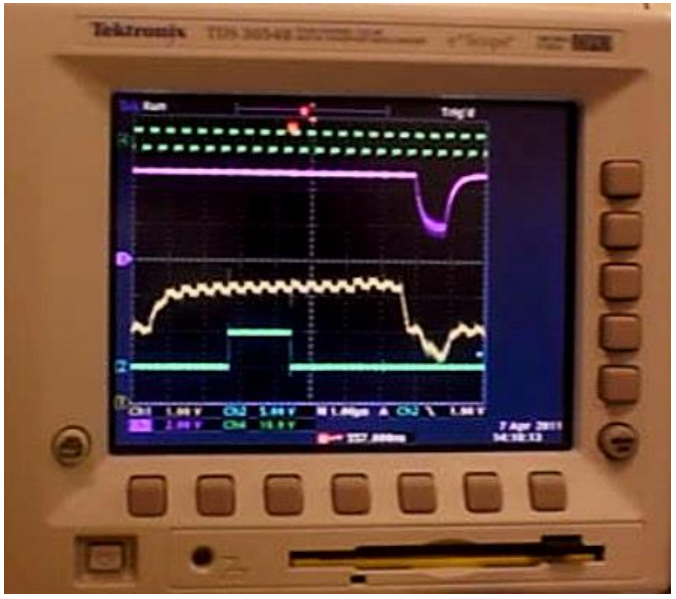
Selected Design By: Cesar Mendez Ruiz and Ethan Tanner





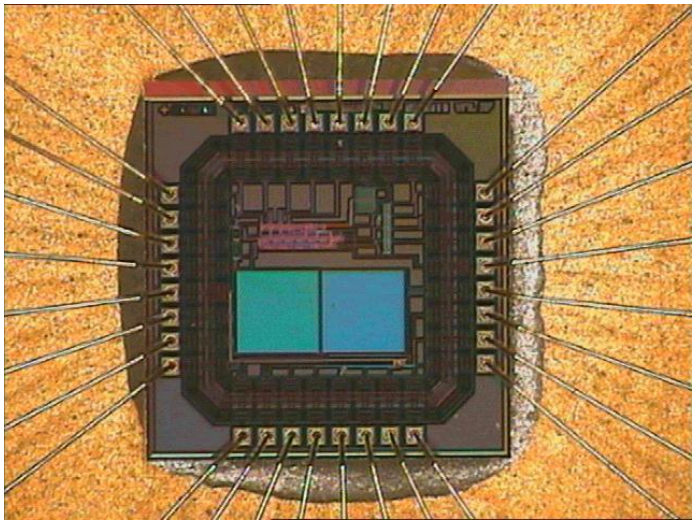
Die Photograph of the Test Chip



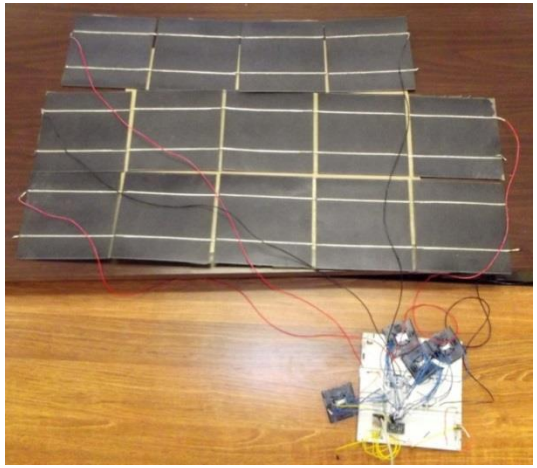


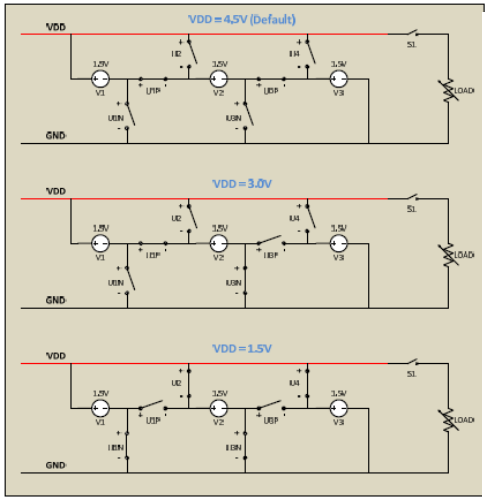
Projects Manufactured by MOSIS in 2011

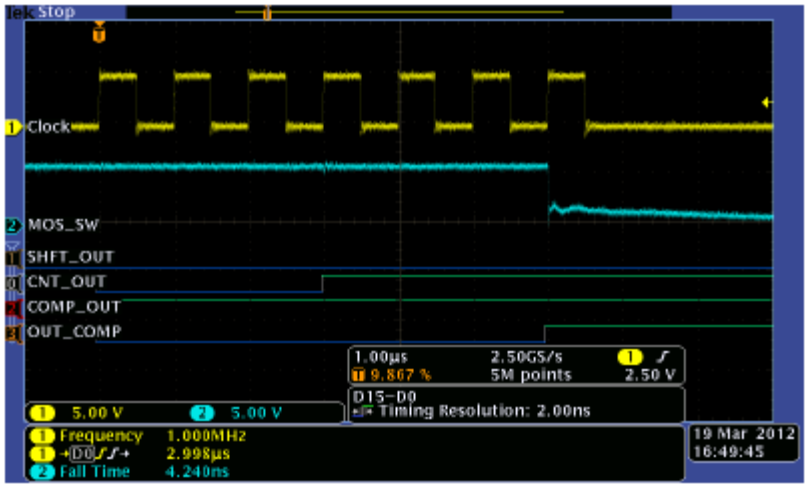
Design 1	Design 2
Mike Echert Roger Flateau	William Cavanaugh Jing Ju Kanamu Pupuhi



Die Photograph of the Test Chip 2

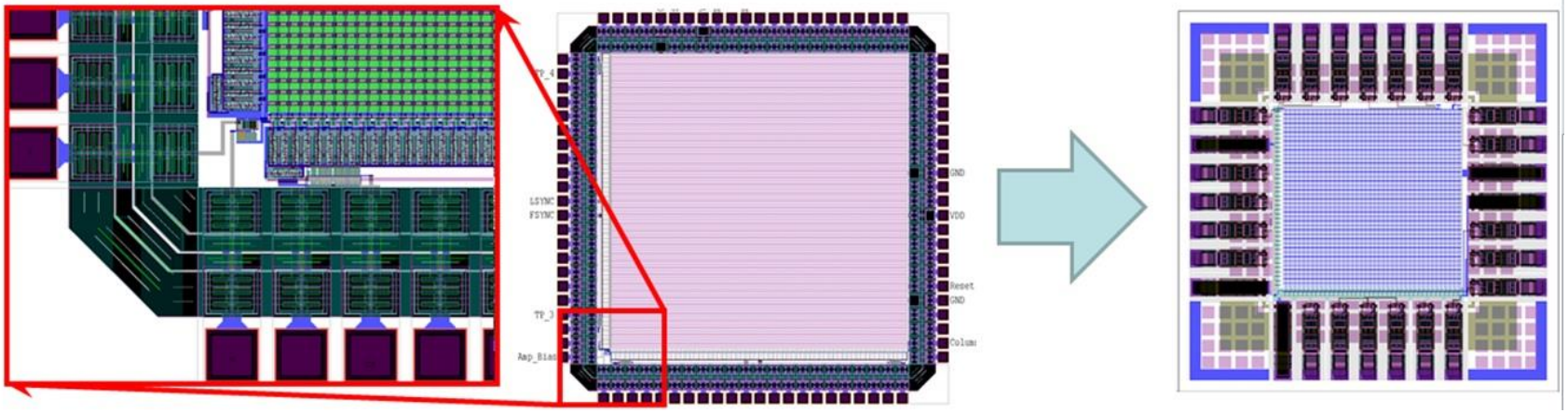


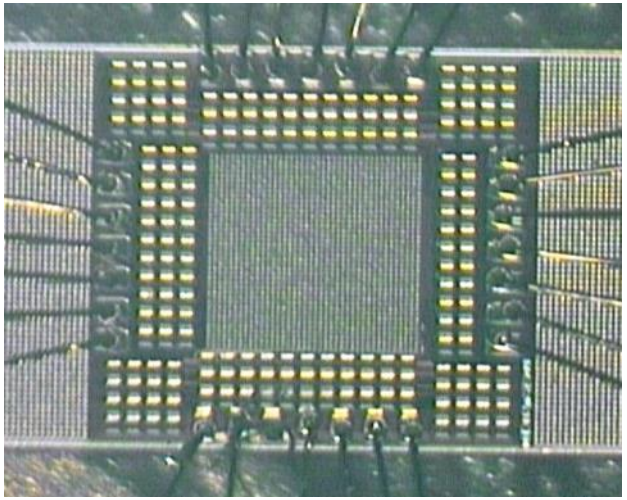


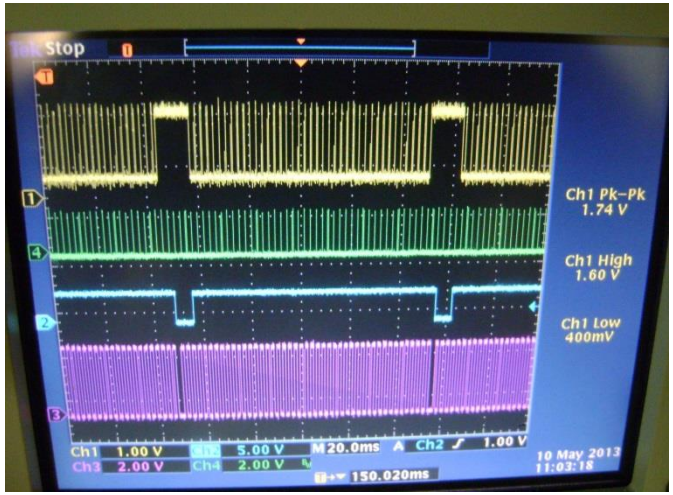


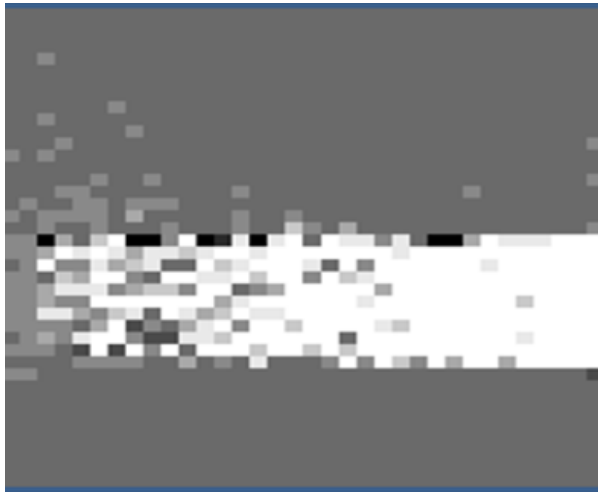
Projects Manufactured by MOSIS in 2012

Selected Design By: Javad Ghasemi

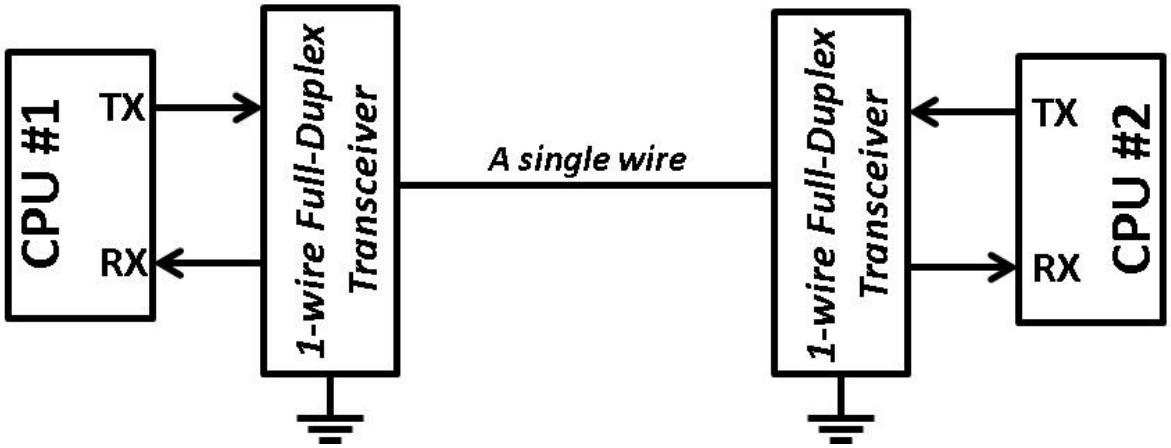


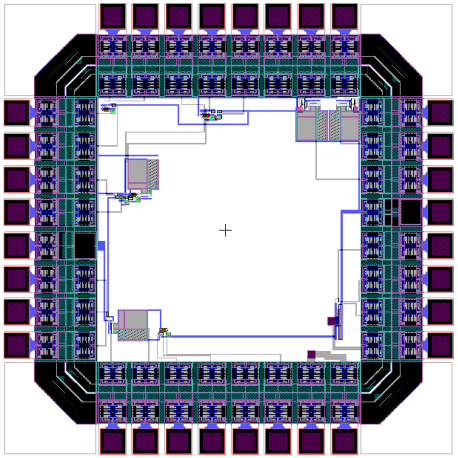


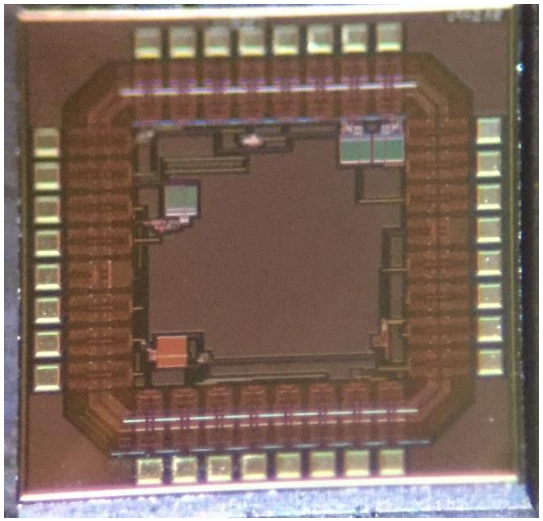




Projects Manufactured by MOSIS in 2019







Class Schedule

Warning: Lecture schedule subject to change!!

Date	Day	Topic	Reading Coverage	Quiz Questions	Supporting Documents
January 19	Tue	Introduction to VLSI Technology	1.1-1.3	No Quiz	Video 0 (1 min)
January 21	Thr	Basic MOS Physics I (static)	3.2	Quiz 1 (due on 1/20/21)	Video 1 Discussion notes 1
January 26	Tue	Basic MOS Physics II (dynamic)	3.3	Quiz 2 (due on 1/25/21)	Video 2 Discussion notes 2
January 28	Thr	Device Scaling Issues	3.4-3.5	Quiz 3 (due on 1/27/21)	Video 3 Discussion notes 3
February 2	Tue	Device Scaling Issues - cont.	3.4-3.5	Quiz 4 (due on 2/1/21)	Video 4 Discussion notes 4
February 4	Thr	Basic CMOS Inverter	5.1.4	Quiz 5 (due on 2/3/21)	Video 5 Discussion notes 5
February 9	Tue	Basic CMOS Inverter - cont.	5.1-5.4	Quiz 6 (due on 2/8/21)	Video 6 Discussion notes 6
February 11	Thr	Dynamic Behavior of CMOS Inverter	5.4-5.6	Quiz 7 (due on 2/10/21)	Video 7 Discussion notes 7
February 16	Tue	CMOS Manufacturing Process	2.1-2.3, 2.4 (review), 2.5	Quiz 8 (due on 2/15/21)	Video 8 Discussion notes 8
February 18	Thr	Interconnect Manufacturing & Modeling	4.1-4.5	Quiz 9 (due on 2/17/21)	Video 9 Discussion notes 9
February 23	Tue	Design Rules	2.3, insert A	Quiz 10 (due on 2/22/21)	Video 10 Discussion notes 10
February 25	Thr	Layout Techniques & L-Edit Demo	handouts	Quiz 11 (due on 2/24/21)	Video 11 Discussion notes 11
March 2	Tue	Combinational Static Logic	6.1-6.2	Quiz 12 (due on 3/1/21)	Video 12 Discussion notes 12
March 4	Thr	Gate Sizing (Inverter Chain)	5.4	Quiz 13 (due on 3/3/21)	Video 13 Discussion notes 13
March 9	Tue	Gate Sizing (Inveter Chain) - cont.	5.4	Quiz 14 (due on 3/8/21)	Video 14 Discussion notes 14
March 11	Thr	Midterm Exam	-	-	-
March 16	Tue	Spring Break	-	-	-
March 18	Thr	Spring Break	-	-	-
March 23	Tue	Logical Effort	6.1 - 6.2	Quiz 15 (due on 3/22/21)	Video 15 Discussion notes 15
March 25	Thr	Logical Effort - cont.	6.1 - 6.2	Quiz 16 (due on 3/24/21)	Video 16 Discussion notes 16
March 30	Tue	Pseudo Logic and Pass-Transistor Logic	6.2	Quiz 17 (due on 3/29/21)	Video 17 Discussion notes 17
April 1	Thr	Project Review	-	Quiz 18 (due on 3/31/21)	Video 18 Discussion notes 18
April 6	Tue	Dynamic Logic	6.3	Quiz 19 (due on 4/5/21)	Video 19 Discussion notes 19
April 8	Thr	Advanced topics: Power Reduction	Handout	Quiz 20 (due on 4/7/21)	Video 20 Discussion notes 20
April 13	Tue	Sequential Logic	7.1-7.2	Quiz 21 (due on 4/12/21)	Video 21 Discussion notes 21
April 15	Thr	Sequential Logic - cont.	7.1-7.2	Quiz 22 (due on 4/14/21)	Video 22 Discussion notes 22
April 20	Tue	Timing Issues	10.1-10.2	Quiz 23 (due on 4/19/21)	Video 23 Discussion notes 23
April 22	Thr	Clock Distribution - PLL	10.3	Quiz 24 (due on 4/21/21)	Video 24 Discussion notes 24
April 27	Tue	Power Distribution & I/O Circuits	9.1-9.4	Quiz 25 (due on 4/26/21)	Video 25 Discussion notes 25
April 29	Thr	Memories	12.1-12.2	Quiz 26 (due on 4/28/21)	Video 26 Discussion notes 26
May 4	Tue	Nonvolatile Memories	12.2	Quiz 27 (due on 5/3/21)	Video 27 Discussion notes 27
May 6	Thr	SRAM Memories & Review for Final	Project Due	Quiz 28 (due on 5/5/21)	Video 28 Discussion notes 28
May 11	Tue	Final Exam (12:30-2:30PM)	-		

Reading Assignment

- **Today we will review Chapter 1 and some more**
  - **Introduction and history**
- **Our next class will be on Chapter 3 (MOS Physics)**
  - **Skim through Diodes but focus on Section 3.2.3 (diode transient behavior)**
  - **Study Section 3.3 (MOS transistor) *thoroughly***
- **We will get back to Chapter 2 (Manufacturing Process) later**

VLSI Design Flow

- **The goal of VLSI designers is to design a circuit block that meets the following objectives:**
  - **Maximize speed or performance**
  - **Minimize power consumption**
  - **Minimize area**
  - **Maximized robustness**
- **Methods that they use are:**
  - **Circuit design, transistor sizing**
  - **Use of new architectures, clock gating, etc**
  - **Choice of circuit style, efficient layout design**
  - **Interconnect design and optimization**

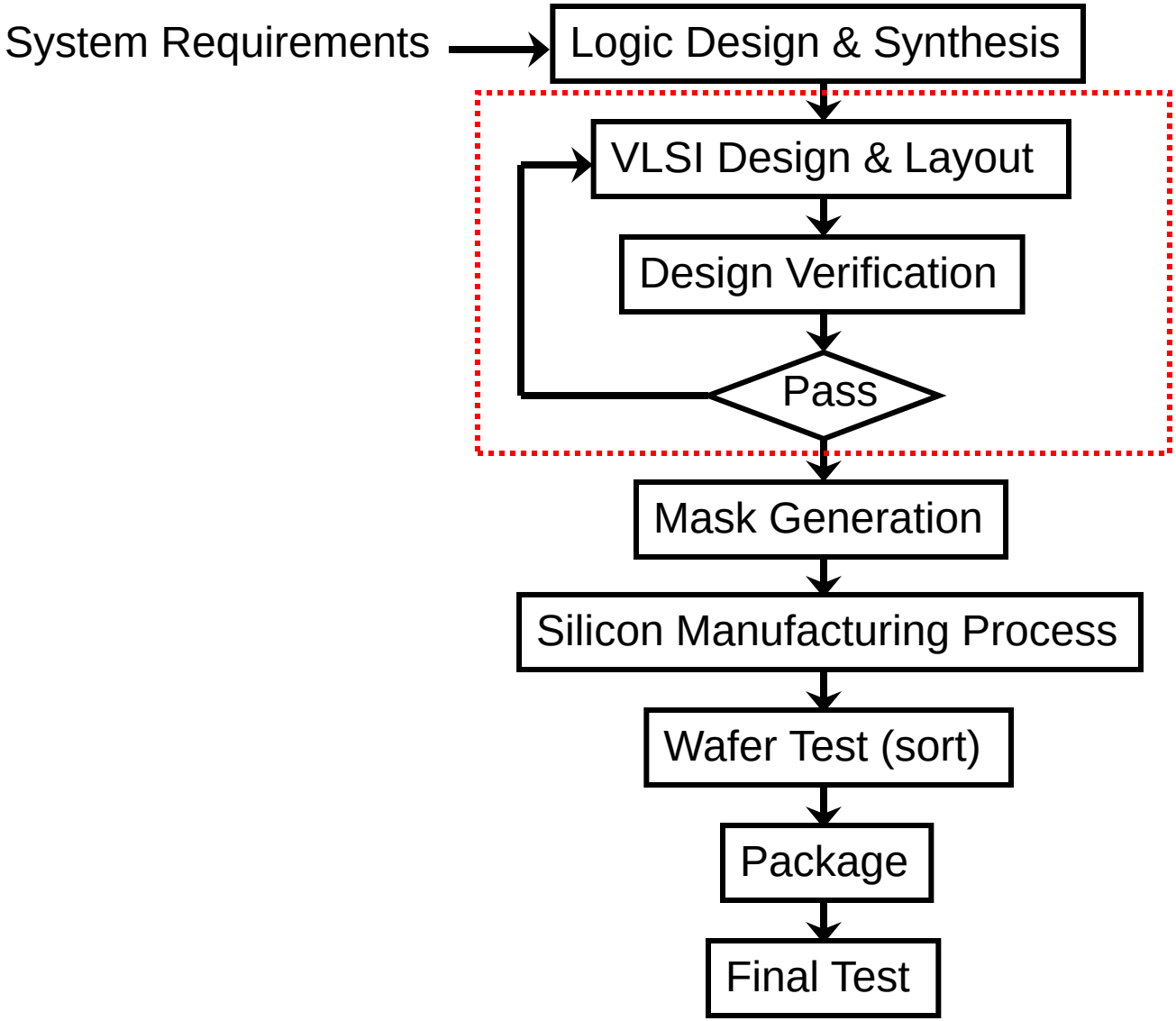
VLSI Design Approaches

- **Gate Arrays (Old technology, but still attractive)**
  - Pre-fabricated chips containing transistors and local wiring
  - Upper level wires added to implement design
  - Rapid design, but very sub-optimal, slow, and usually high power consumption
- **Standard Cells (Used for ASIC design)**
  - Cells in a library with fixed sizes
  - Cells pre-characterized for delay and power
  - Design is fast and layout is done automatically
  - Better performance, in the range of several 100's MHz
- **Custom Design (Used for Microprocessor design)**
  - Optimal circuit design and sizes
  - Extensive design verification required
  - Slowest, but densest layout design
  - Best performance, in the range of 1-5 GHz

VLSI Design Tools

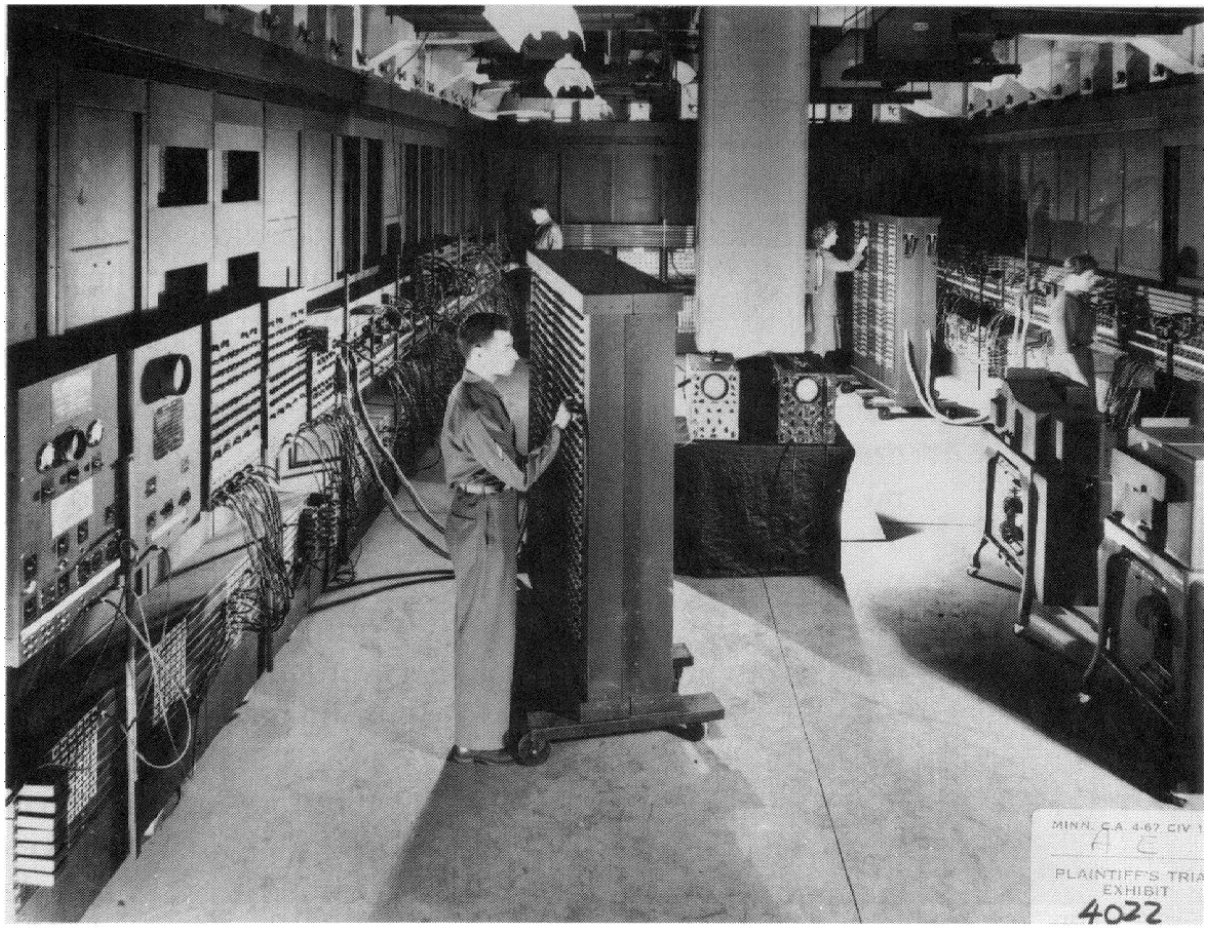
- **Synthesis**
  - Logic, micro-architecture, automatic physical generation
- **Static Analysis**
  - Design rule checking (DRC)
  - Circuit extraction
  - Timing analysis
  - Test generation (ATPG)
- **Dynamic Analysis**
  - Architectural simulation
  - Logic simulation
  - Circuit simulation (SPICE)
  - Test verification

High Level VLSI Design Steps



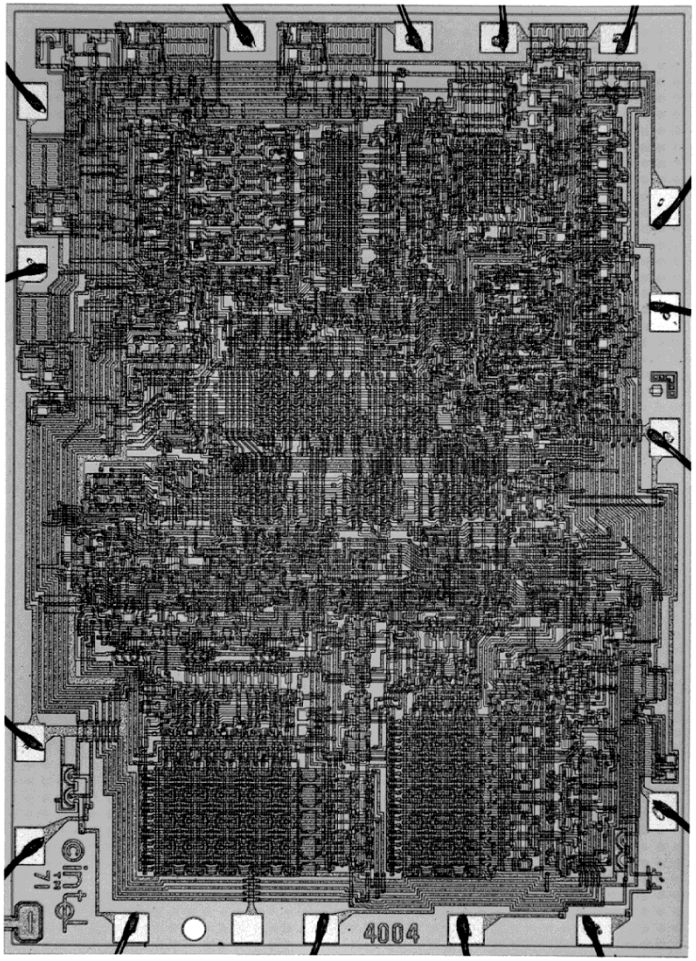
Introduction

Beginning of the Computer: ENIAC, the first electronic computer (1946)



- 333 integer multiplication/second
- A six-week run was equivalent to 100 person-years of manual computation
- Program resides in the wired connections

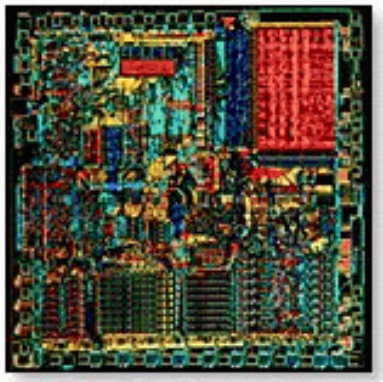
Intel 4004 Microprocessor



- 1971
- 10 um NMOS-only
- 2300 transistors
- 1 MHz

Intel Technology Advancement

Processor Comparison



Intel® i8088

Year: 1981
29,000 transistors

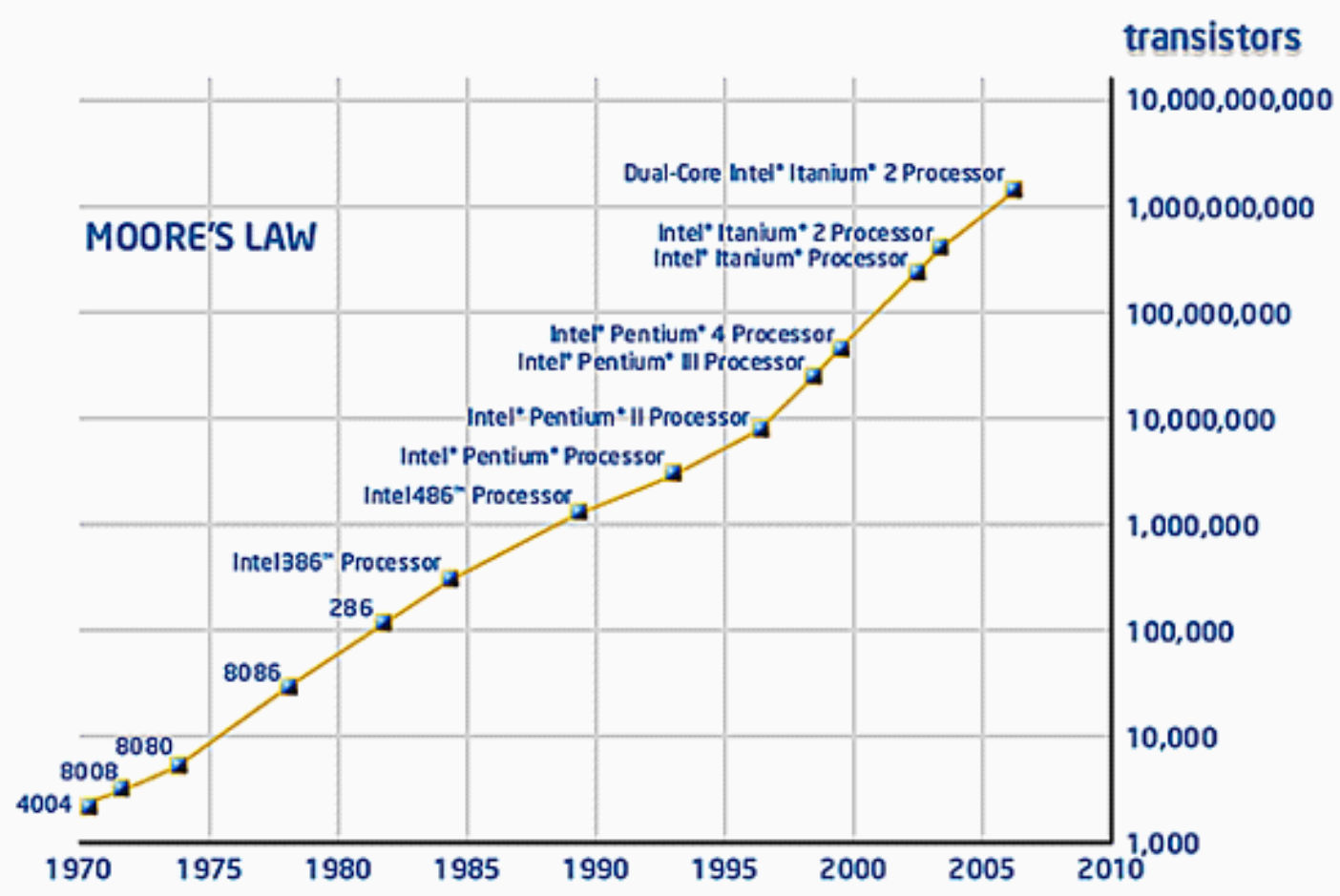
Intel® Pentium® 4 Processor with HT Technology

Year: 2004
125,000,000 transistors

Moore's Law

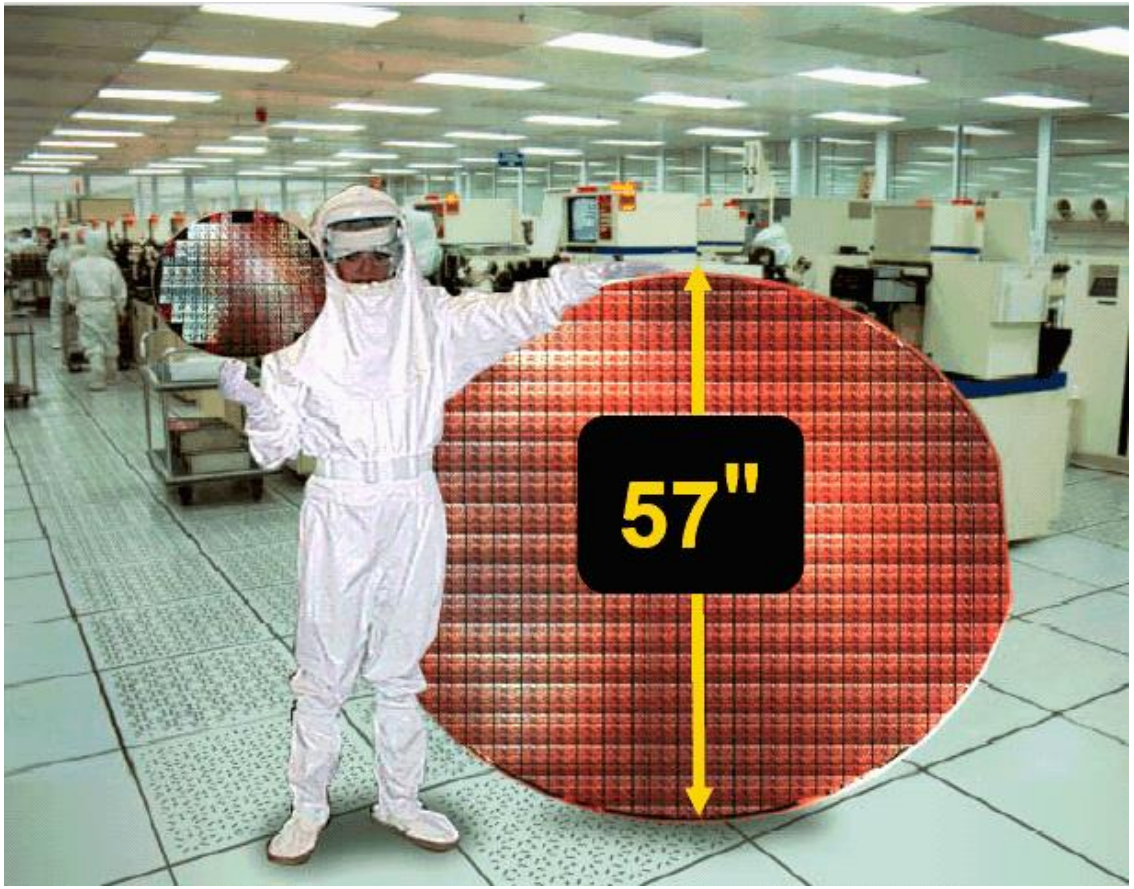
- In 1965, Gordon Moore (founder of Intel) had a very interesting observation. He noticed that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology would double its effectiveness every 18 months.

Moore's Law for Intel Microprocessors



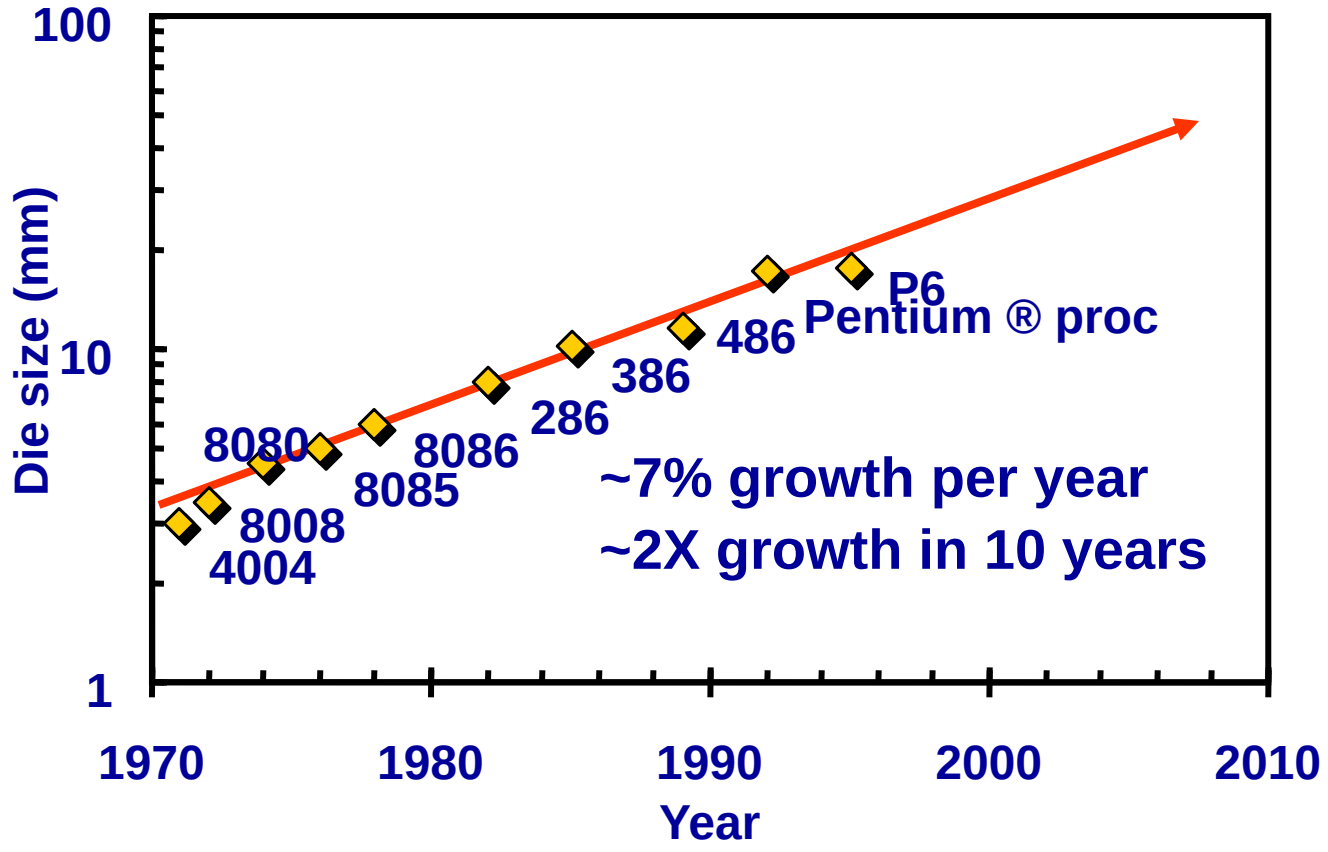
Source: www.intel.com

Projected Wafer in 2000, circa 1975



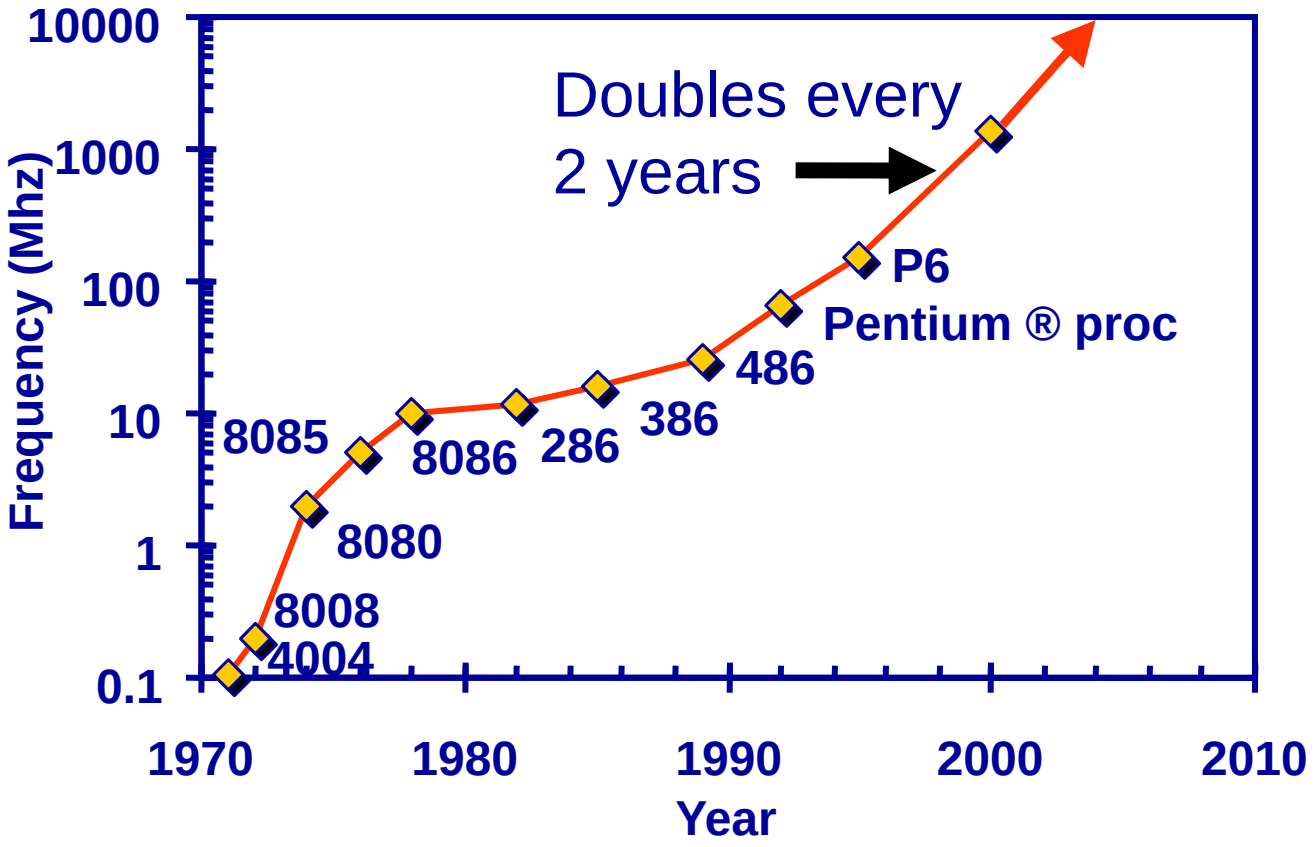
Moore was not always accurate

Die Size Growth



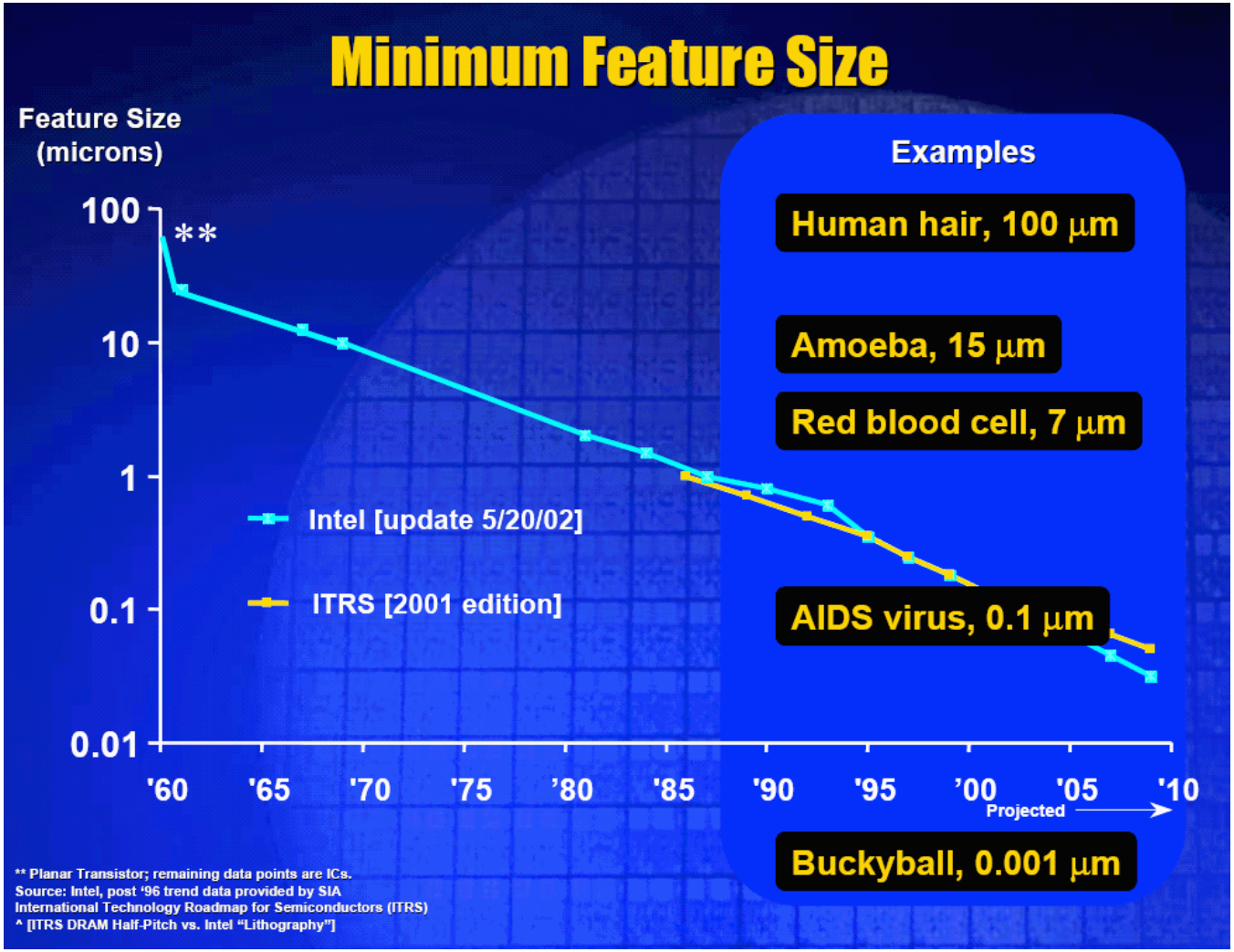
Die size has grown by 14% to satisfy Moor's law, BUT the growth is almost stopped because of manufacturing and cost issues

Clock Frequency



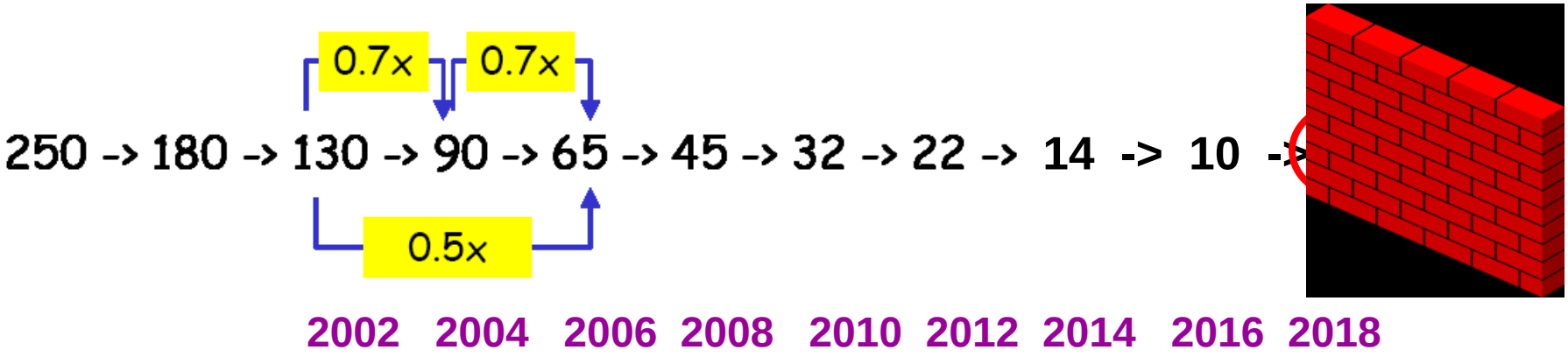
Lead microprocessors frequency doubles every 2 year, BUT the growth is slower because of power dissipation issue

CMOS Scaling Scenario

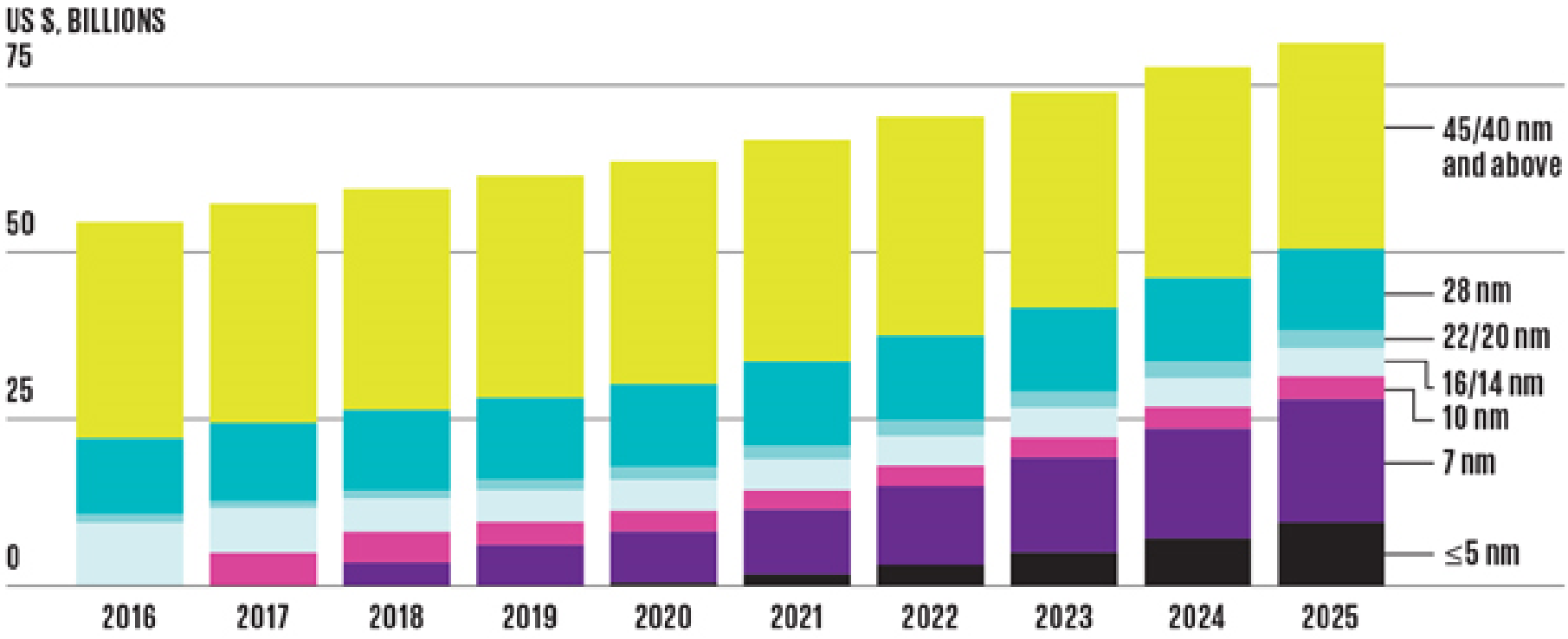


CMOS Scaling Calculation

Scaling Calculator



The Evolution of Foundry Market



Cost of Design versus Technology Node