

ECEN620: Network Theory Broadband Circuit Design Fall 2022

Lecture 3: Phase-Locked Loop Systems



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Announcements

- HW1 due Sept 22, 11:59PM
 - Turn in via Canvas
- HW2 due Oct 6
 - Requires transistor-level design
 - For 90nm CMOS device models, see https://people.engr.tamu.edu/spalermo/ecen689/cadence_90nm_2021.pdf
 - Can use other technology models if they are a 90nm or more advanced CMOS node

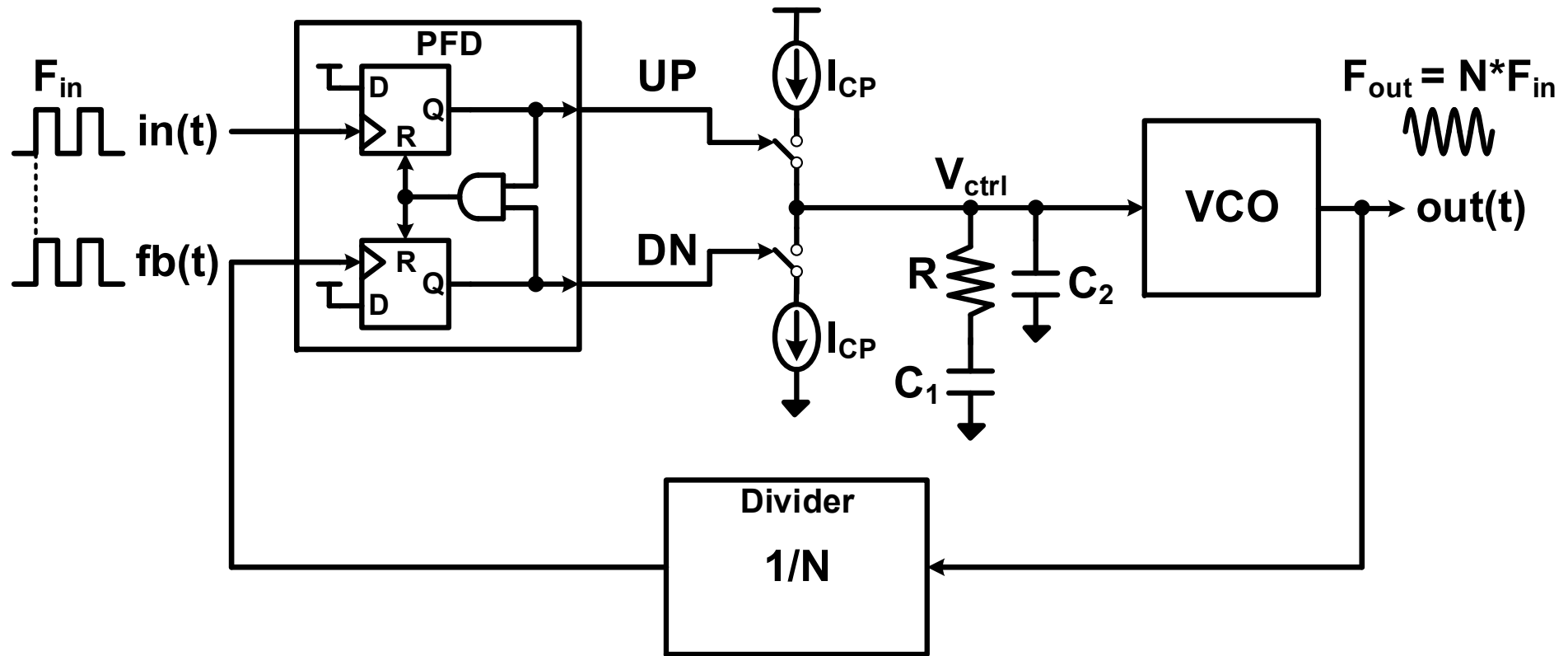
Reading/References

- Chapter 2, 3, 5, & 12 of *Phaselock Techniques*, F. Gardner, John Wiley & Sons, 2005.
 - <https://onlinelibrary.wiley.com/doi/book/10.1002/0471732699>
- Charge-Pump PLL Design Procedure Paper (OSU)
- Chapter 1-3.4 of “Low-Power Low-Jitter On-Chip Clock Generation,” M. Mansuri, Ph.D. thesis, UCLA, 2003.
 - Posted on website
- Other references
 - M. Perrott, *High Speed Communication Circuits and Systems Course*, MIT Open Courseware
 - Chapter 2 of *Phase-Locked Loops, 3rd Ed.*, R. Best, McGraw-Hill, 1997.
 - Chapter 4 of *Phase-Locked Loops for Wireless Communications*, D. Stephens, Kluwer, 2002.

Agenda

- PLL Overview
- PLL Linear Model
- PLL Stability
- Analog Charge Pump PLL Design Procedure
- PLL Noise Transfer Functions
- PLL Transient Behavior
- PLL Time Domain Modeling

PLL Block Diagram

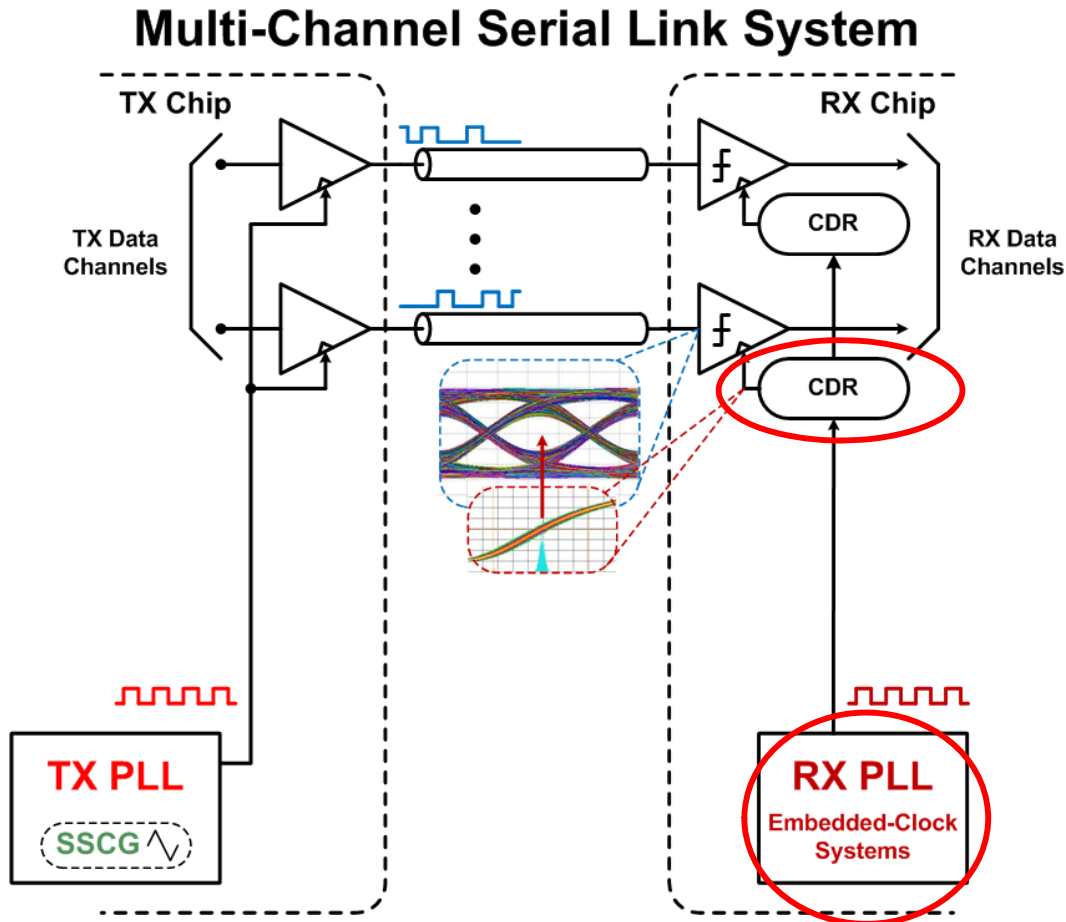


- A phase-locked loop (PLL) is a negative feedback system where an oscillator-generated signal is phase AND frequency locked to a reference signal

PLL Applications

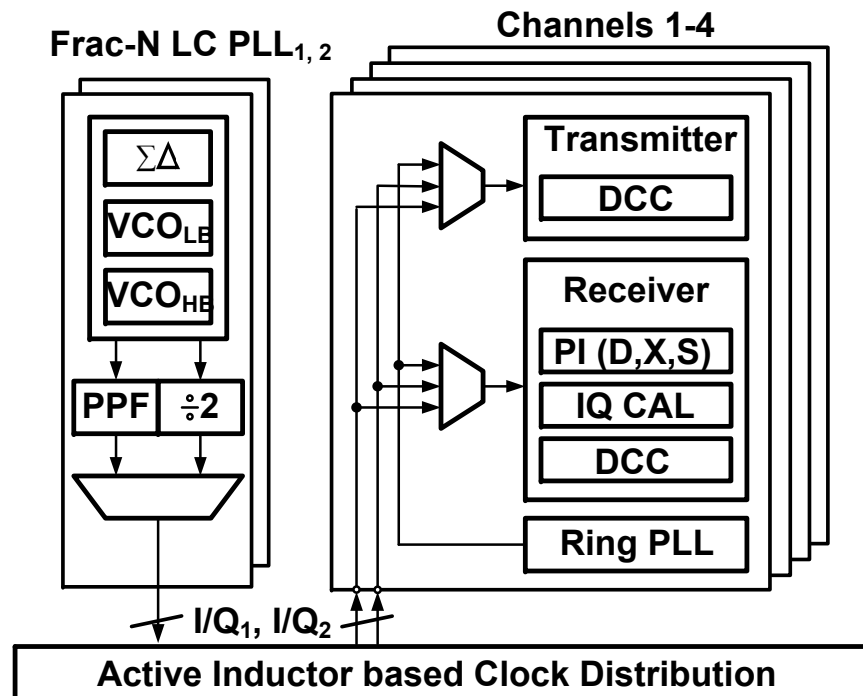
- PLLs applications
 - Frequency synthesis
 - Multiplying a 100MHz reference clock to 10GHz
 - Skew cancellation
 - Phase aligning an internal clock to an I/O clock
 - Clock recovery
 - Extract from incoming data stream the clock frequency and optimum phase of high-speed sampling clocks
 - Modulation/De-modulation
 - Wireless systems
 - Spread-spectrum clocking

Embedded Clock (CDR) I/O Circuits



- TX PLL
- TX Clock Distribution
- CDR
 - Per-channel PLL-based
 - Dual-loop w/ Global PLL &
 - Local DLL/PI
 - Local Phase-Rotator PLLs
 - Global PLL requires RX clock distribution to individual channels

Xilinx 0.5-32Gb/s Transceiver Clocking



Technology	CMOS 16nm FinFET
Power Supply (V_{avcc} , V_{avtt} , V_{aux})	0.9 V, 1.2 V, 1.8 V
Frequency range	500 Mb/s – 32.75 Gb/s
Transceiver Quad area	2.625 mm × 2.218 mm
LC PLL range	8-16.375 GHz
Ring PLL range	2-6.25 GHz
TX PRBS7 jitter at 32.75Gb/s	TJ: 5.39 ps, RJ: 190 fs
32.75Gb/s RX JTOL @ 30MHz @ 100MHz	0.45 UI 0.6 UI
Channel loss at 32.75Gb/s	30 dB
Measured BER at 32.75Gb/s	< 10 ⁻¹⁵
Power at 32.75Gb/s with DFE	577mW/ch (17.6pJ/b)

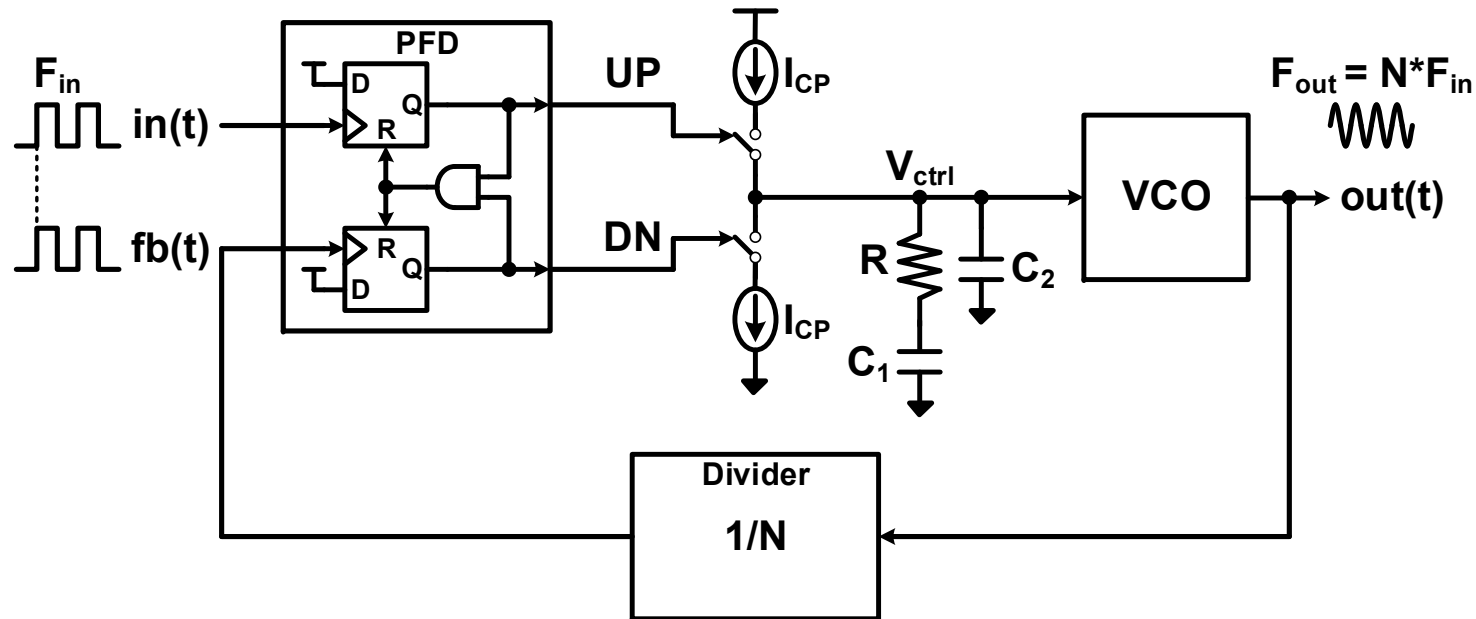
[Upadhyaya VLSI 2016]

- LC-PLL with 2 LC-VCOs used to cover high data rates (8-32Gb/s)
- Ring-PLL used for lower data rates
- CML clock distribution with active inductive loads used for low jitter

Agenda

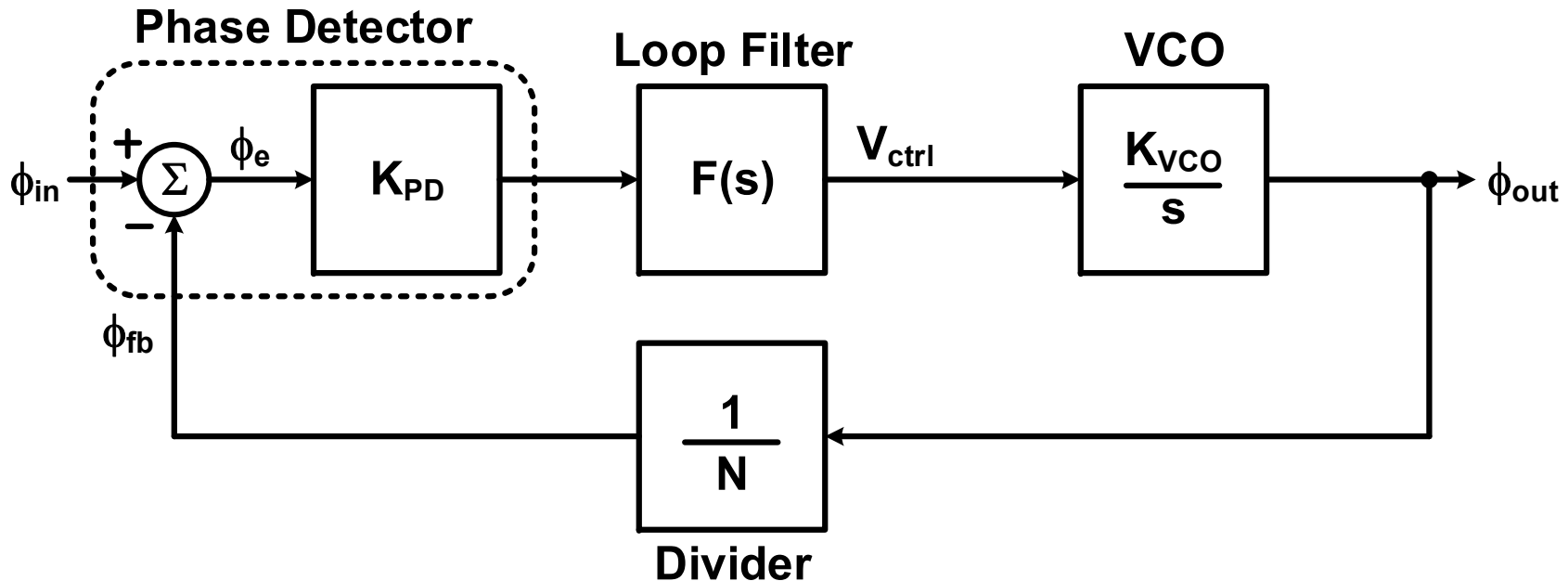
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Charge Pump PLL



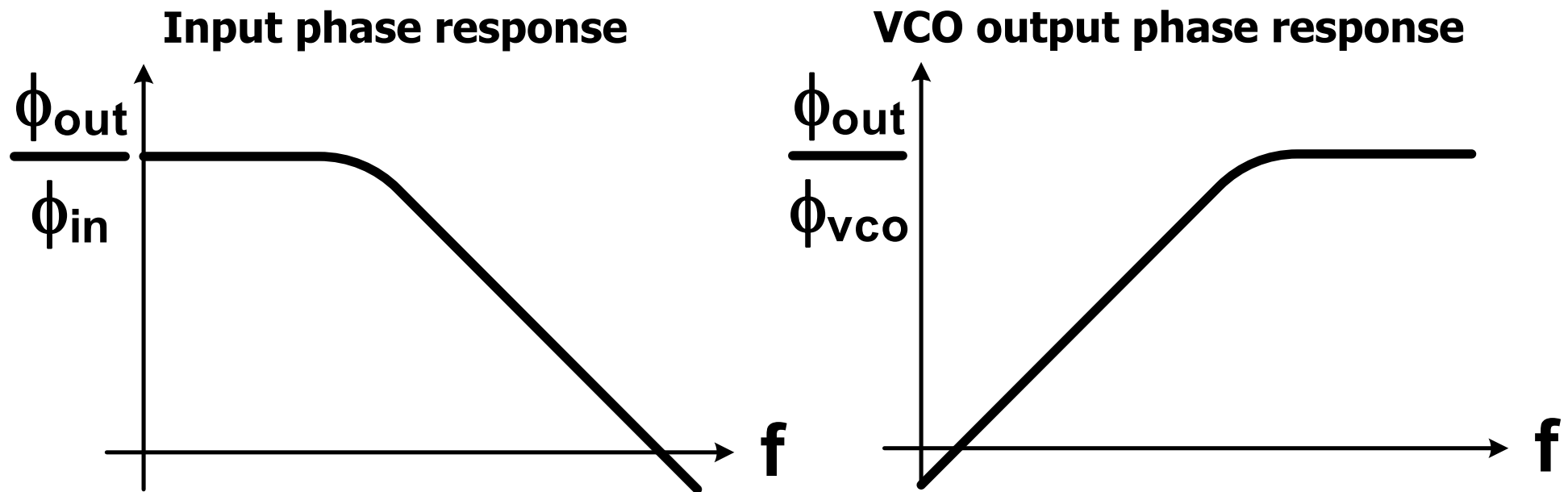
- Charge pump PLL is a common implementation
- Type-2 (2 integrators) allows for ideally zero phase error between the input and feedback phase
- Requires a stabilizing zero that is realized with the filter resistor
- A secondary capacitor C_2 is often added for additional filtering to reduce reference spurs
- Modeled as a third-order system

Linear PLL Model



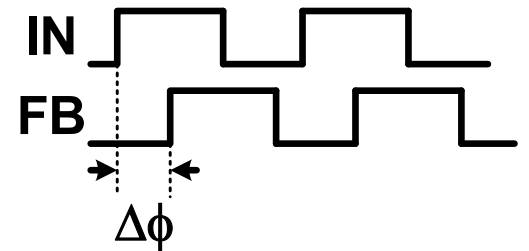
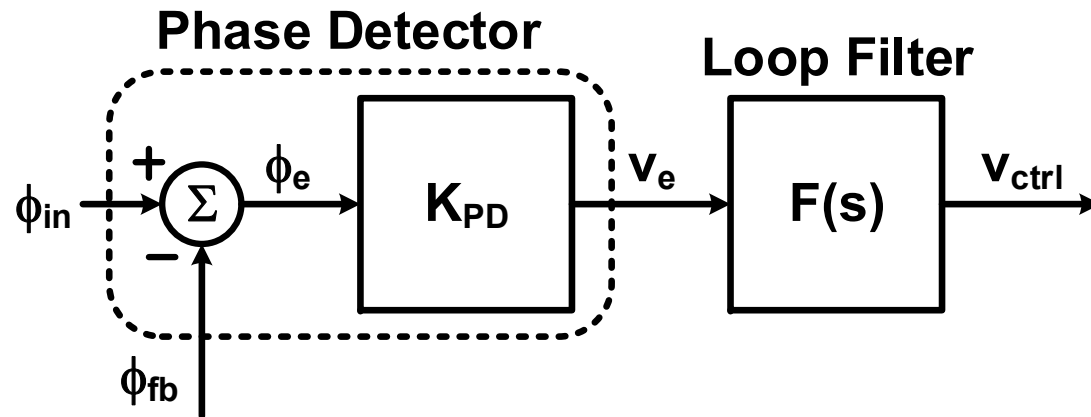
- Phase is the key variable of interest
 - Output phase response to a stimulus injected at a given point in the loop
 - Phase error response is also informative
- Linear “small-signal” analysis is useful for understand PLL dynamics if
 - PLL is locked (or near lock)
 - Input phase deviation amplitude is small enough to maintain operation in lock range

Understanding PLL Frequency Response



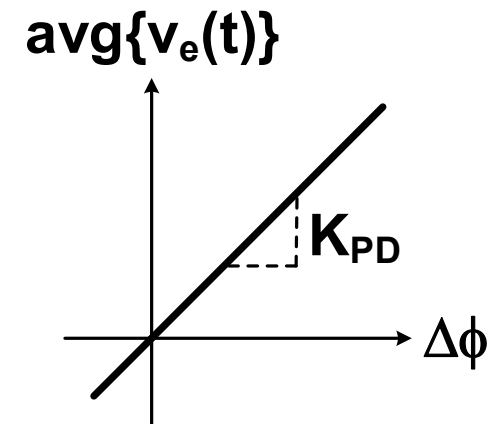
- Frequency domain analysis can tell us how well the PLL tracks the input phase as it changes at a certain frequency
- PLL transfer function is different depending on which point in the loop the output is responding to

Phase Detector



$$\text{avg}\{v_e(t)\} = K_{PD}\Delta\phi$$

- Detects phase difference between feedback clock and reference clock
- The loop filter will filter the phase detector output, thus to characterize phase detector gain, extract average output voltage
- The K_{PD} factor can change depending on the specific phase detector circuit



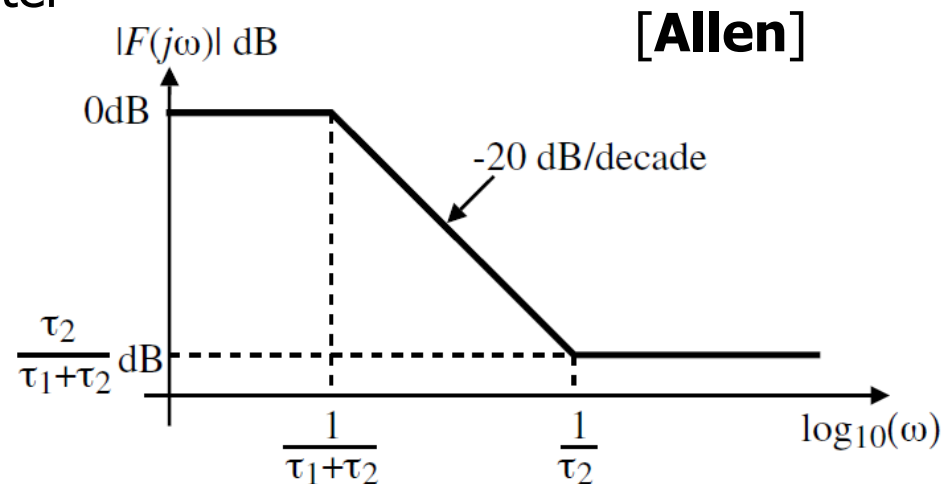
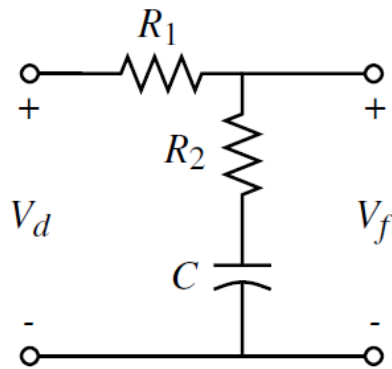
K_{PD} units are V/rad when used with a dimension - less filter

K_{PD} units are rad^{-1} (averaged) or A/rad when combined with the charge - pump

when used with a impedance filter

Dimension-Less Loop Filter

Example: Passive Lag-Lead Loop Filter



[Allen]

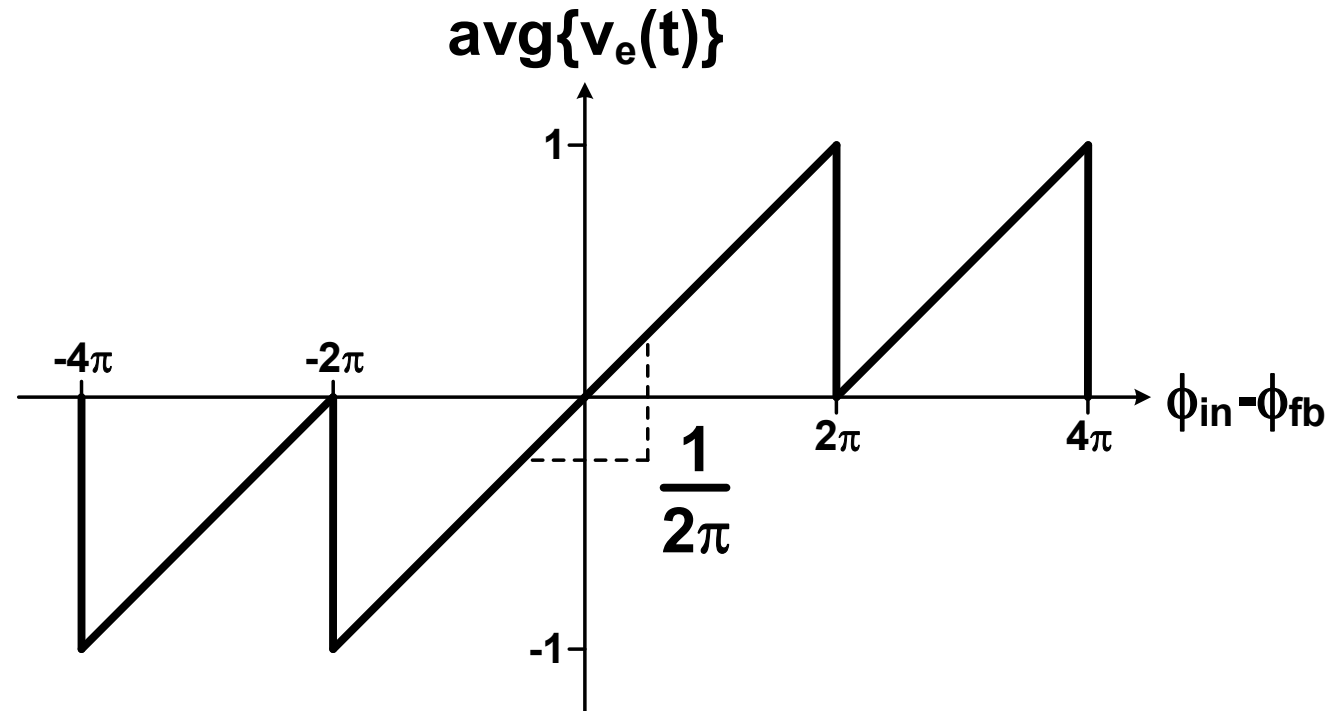
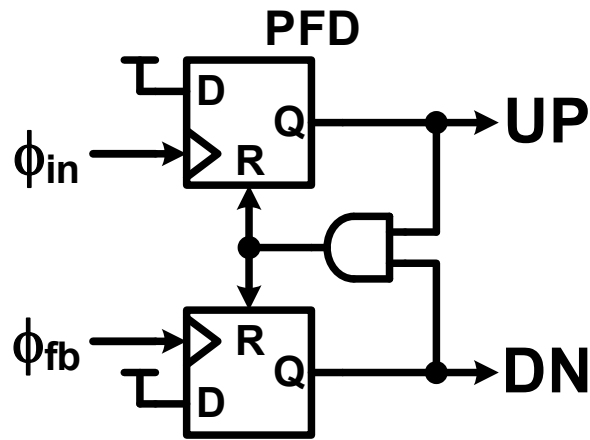
$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)}$$

$$\tau_1 = R_1 C \quad \tau_2 = R_2 C$$

- Lowpass filter extracts average of phase detector signal
- No units for the dimension-less loop filter

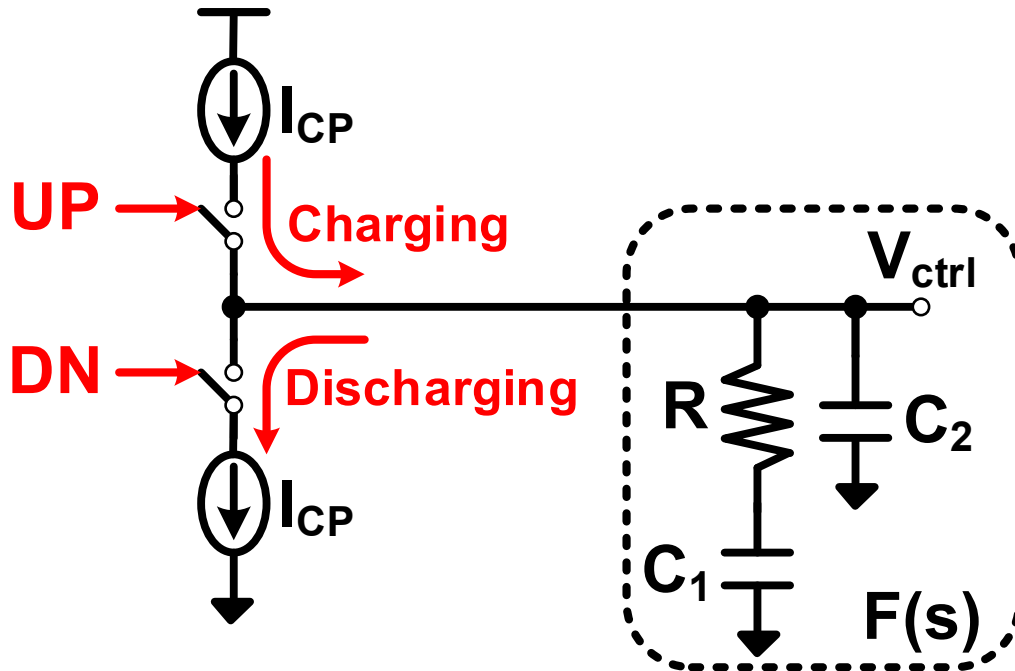
Averaged PFD Transfer Characteristic

UP=1 & DN=-1



- Constant slope and polarity asymmetry about zero phase allows for wide frequency range operation
- The averaged PFD gain is $1/(2\pi)$ with units of rad^{-1}

Charge Pump



- Converts PFD output signals to charge
- Charge is proportional to PFD pulse widths

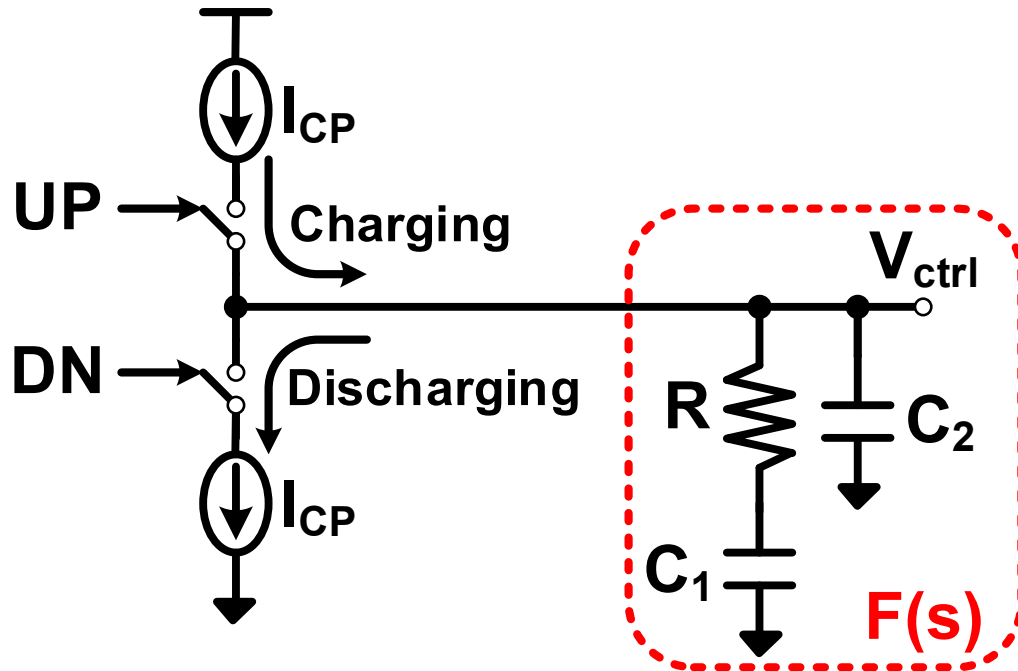
$$\text{Un - Averaged Charge - Pump Gain} = I_{CP} \text{ (Amps)}$$

$$\text{Averaged Charge - Pump Gain} = \frac{I_{CP}}{2\pi} \left(\frac{\text{Amps}}{\text{rad}} \right)$$

$$\text{Total PFD \& Charge - Pump Gain} = \frac{I_{CP}}{2\pi} \left(\frac{\text{Amps}}{\text{rad}} \right)$$

This gain can vary if a different phase detector is used

Loop Filter



w/o C_2

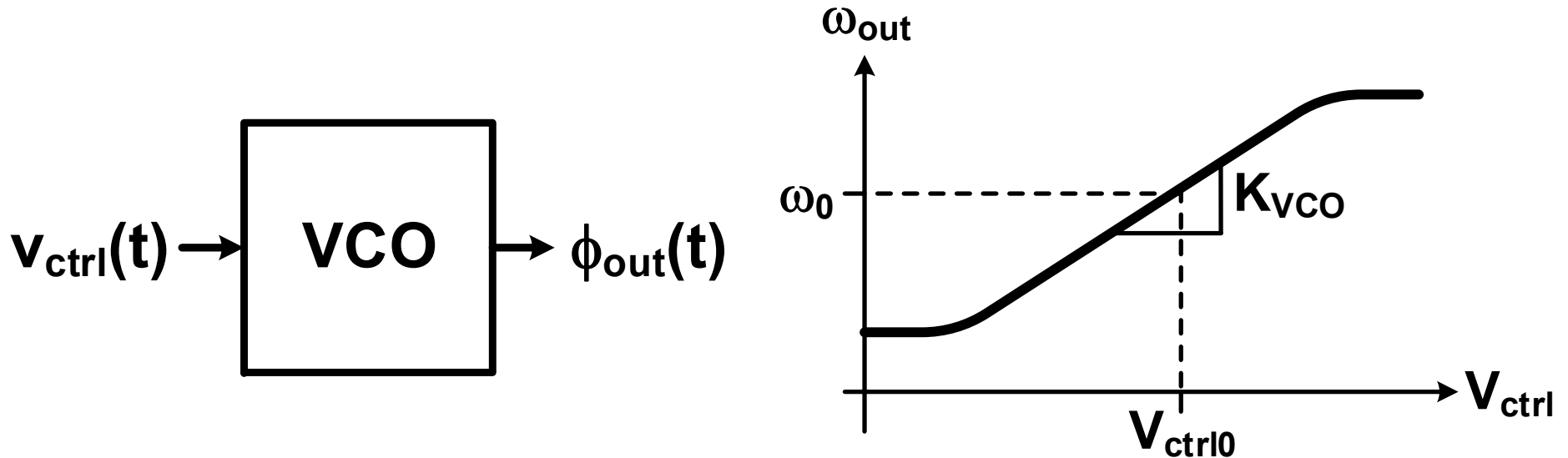
$$F(s) = \frac{R \left(s + \frac{1}{RC_1} \right)}{s}$$

w/ C_2

$$F(s) = \frac{\left(\frac{1}{C_2} \right) \left(s + \frac{1}{RC_1} \right)}{s \left(s + \frac{C_1 + C_2}{RC_1 C_2} \right)}$$

- Lowpass filter extracts average of phase detector error pulses
- The units of the filter are ohms

Voltage-Controlled Oscillator



$$\omega_{out}(t) = \omega_0 + \Delta\omega_{out}(t) = \omega_0 + K_{VCO}v_{ctrl}(t)$$

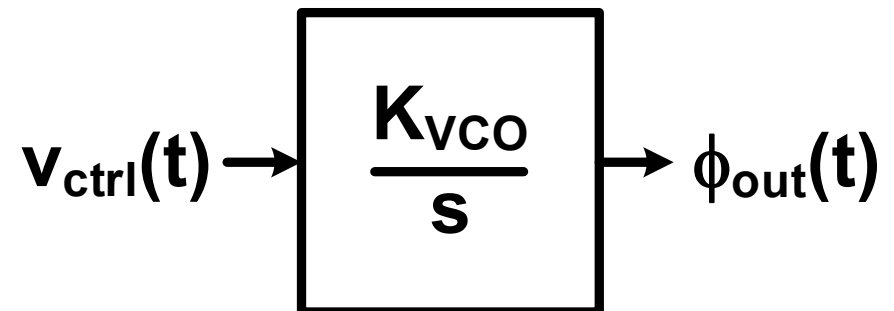
- Time-domain phase relationship

$$\phi_{out}(t) = \int \Delta\omega_{out}(t)dt = \int K_{VCO}v_{ctrl}(t)dt$$

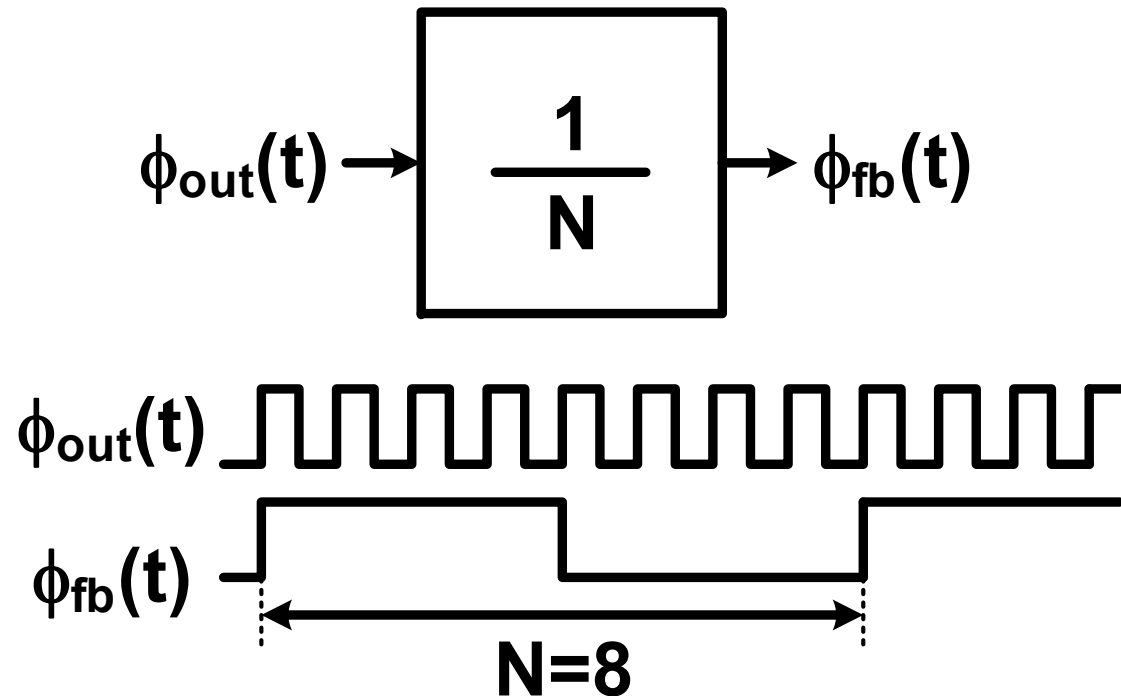
$$K_{VCO} \text{ units are } \frac{\text{rad}}{\text{s} \cdot \text{V}}$$

$$\frac{2\pi(1\text{MHz})}{\text{V}} = 2\pi \times 10^6 \frac{\text{rad}}{\text{s} \cdot \text{V}}$$

Laplace Domain Model



Loop Divider



- Time-domain model

$$\omega_{fb}(t) = \frac{1}{N} \omega_{out}(t)$$

$$\phi_{fb}(t) = \int \frac{1}{N} \omega_{out}(t) dt = \frac{1}{N} \phi_{out}(t)$$

- The loop divider is dimension-less in the PLL linear model

Phase & Frequency Relationships

Angular Frequency is the first derivative (rate of change vs time) of phase

$$\frac{d\phi(t)}{dt} = \omega(t)$$

$$\phi(t) = \int_0^t \omega(\tau) d\tau$$

Consider a sinusoid $u_1(t)$ with angular frequency $\omega_1(t)$ and phase $\phi_1(t)$

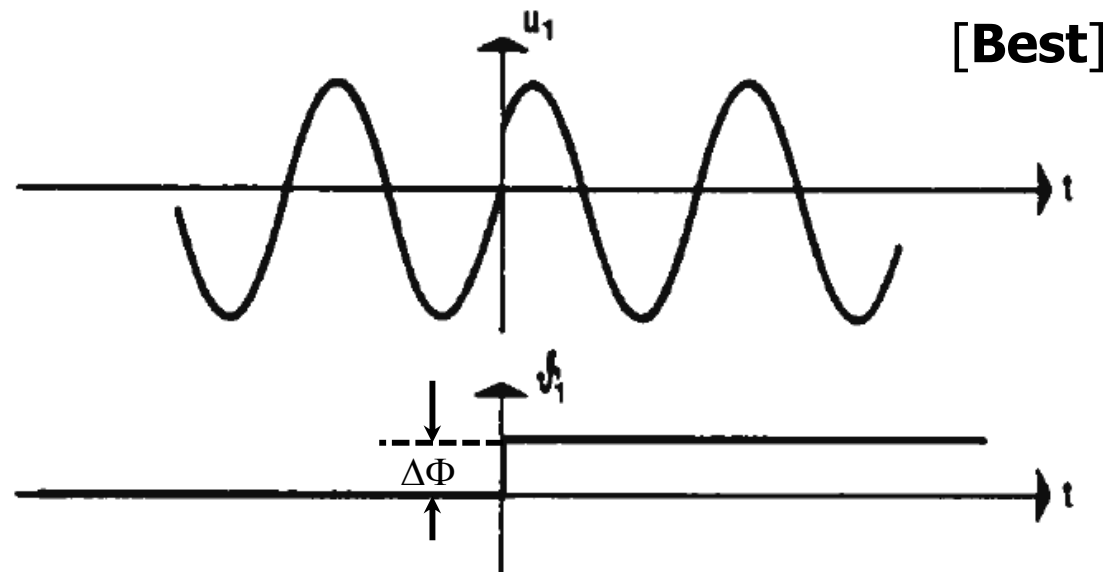
$$u_1(t) = \sin(\omega_1(t)t + \phi_1(t))$$

- Phase Step

$$\phi_1(t) = \Delta\Phi u(t)$$

$$u_1(t) = \sin(\omega_1(t) + \Delta\Phi u(t))$$

No change in frequency



Phase & Frequency Relationships

- Frequency Step

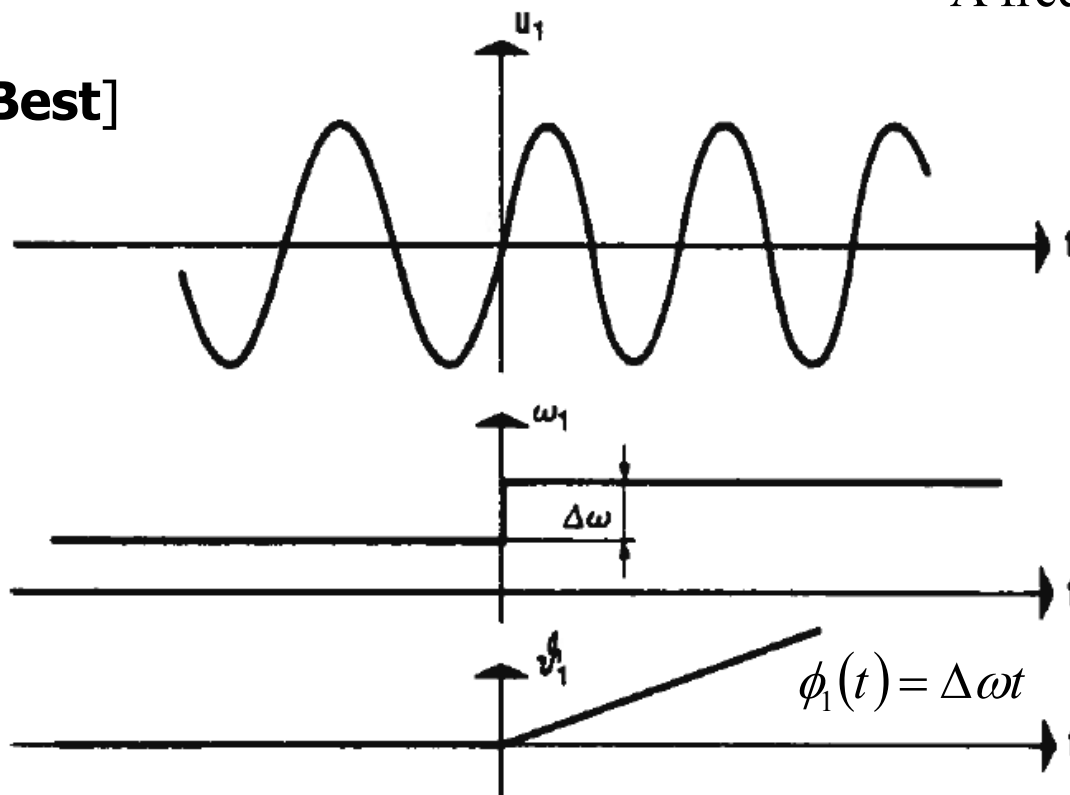
$$\omega_1(t) = \omega_0 + \Delta\omega$$

$$u_1(t) = \sin(\omega_0 t + \Delta\omega t) = \sin(\omega_0 t + \phi_1(t))$$

$$\text{where } \phi_1(t) = \Delta\omega t$$

A frequency step produces a ramp in phase

[Best]



Phase & Frequency Relationships

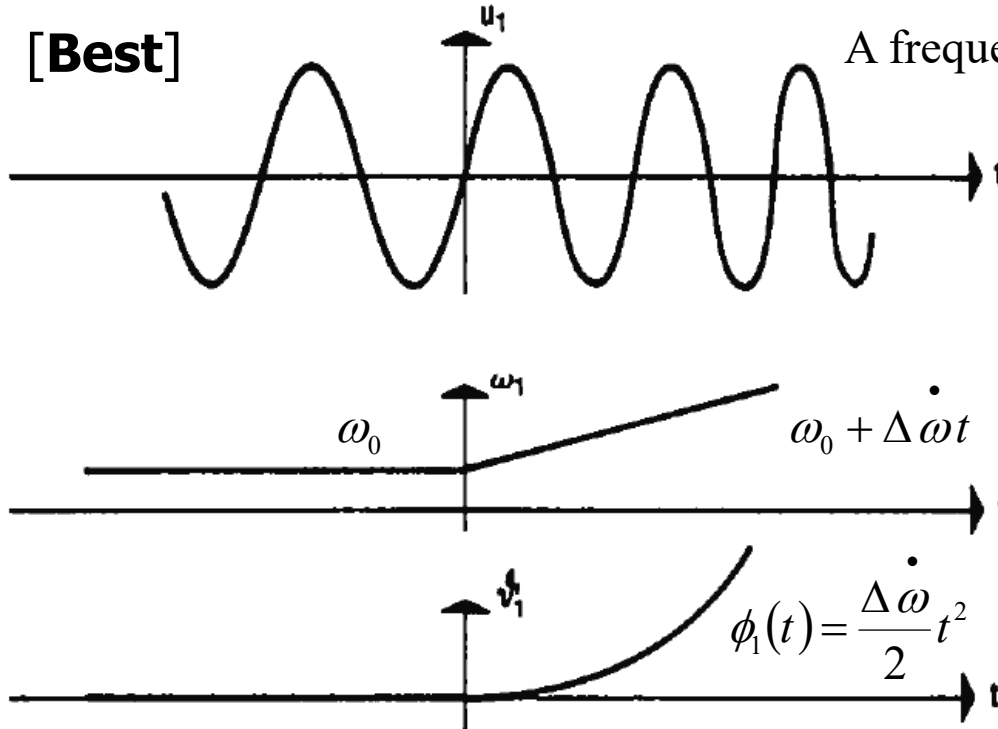
- Frequency Ramp

$$\omega_1(t) = \omega_0 + \Delta \dot{\omega} t$$

$$u_1(t) = \sin\left(\int_0^t (\omega_0 + \Delta \dot{\omega} \tau) d\tau\right) = \sin\left(\omega_0 t + \frac{\Delta \dot{\omega}}{2} t^2\right) = \sin(\omega_0 t + \phi_1(t))$$

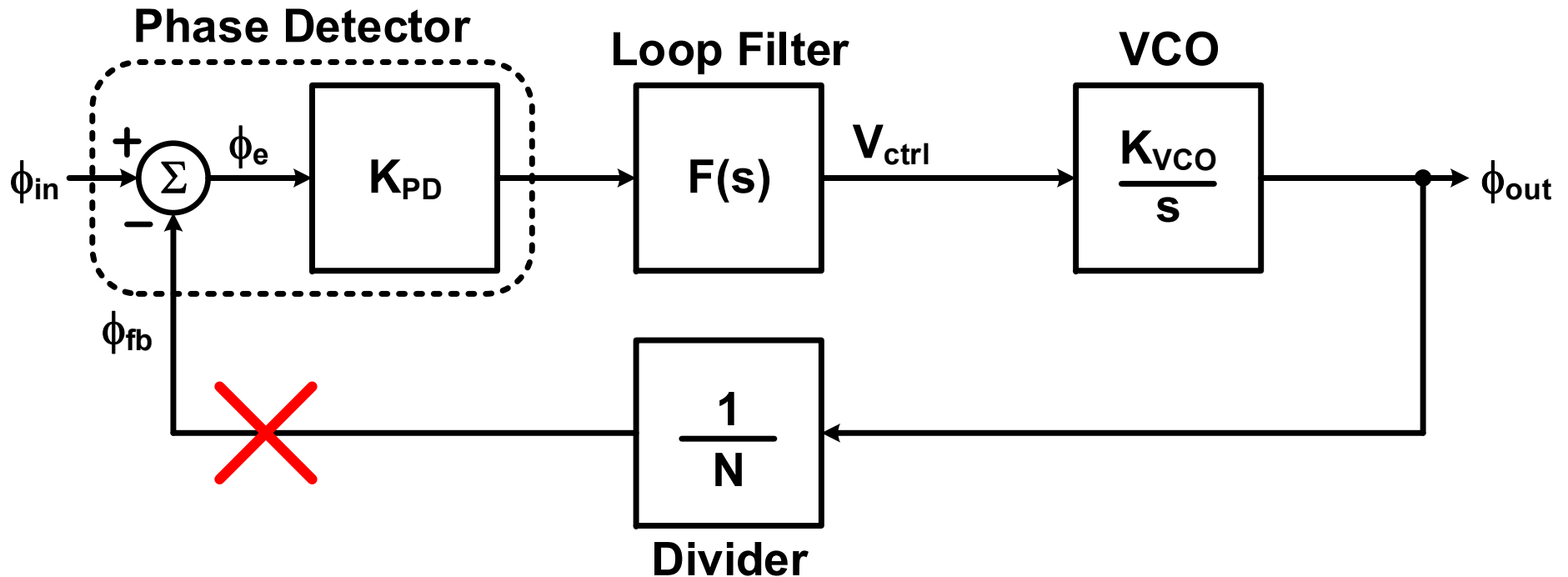
$$\text{where } \phi_1(t) = \frac{\Delta \dot{\omega}}{2} t^2$$

[Best]



A frequency ramp produces a quadratic change in phase

Open-Loop PLL Transfer Function

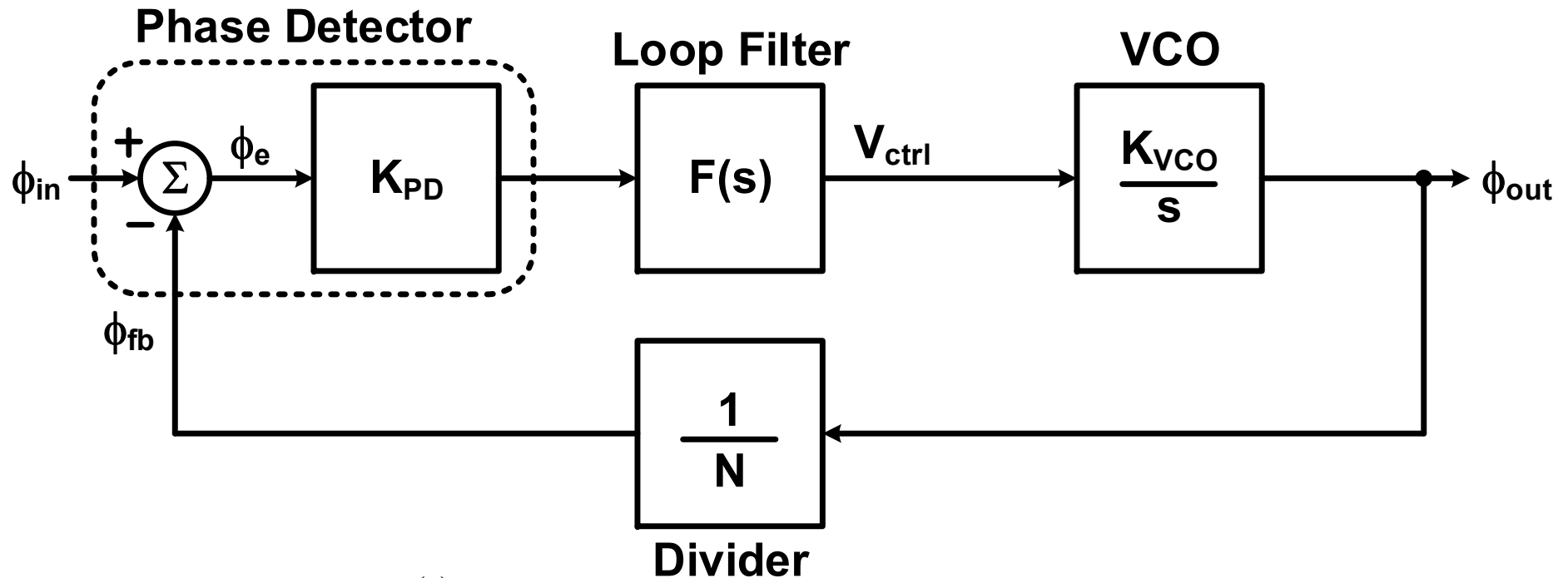


$$\text{Forward Path Gain: } G(s) = \frac{\Phi_{out}(s)}{\Phi_e(s)} = \frac{K_{PD}K_{VCO}F(s)}{s}$$

$$\text{Open-Loop Response: } \frac{G(s)}{N} = \frac{K_{PD}K_{VCO}F(s)}{sN}$$

- Open-loop response generally decreases with frequency

Closed-Loop PLL Transfer Function



Loop Gain

$$l_1 = -\frac{K_{PD}K_{VCO}F(s)}{sN} = -\frac{G(s)}{N}$$

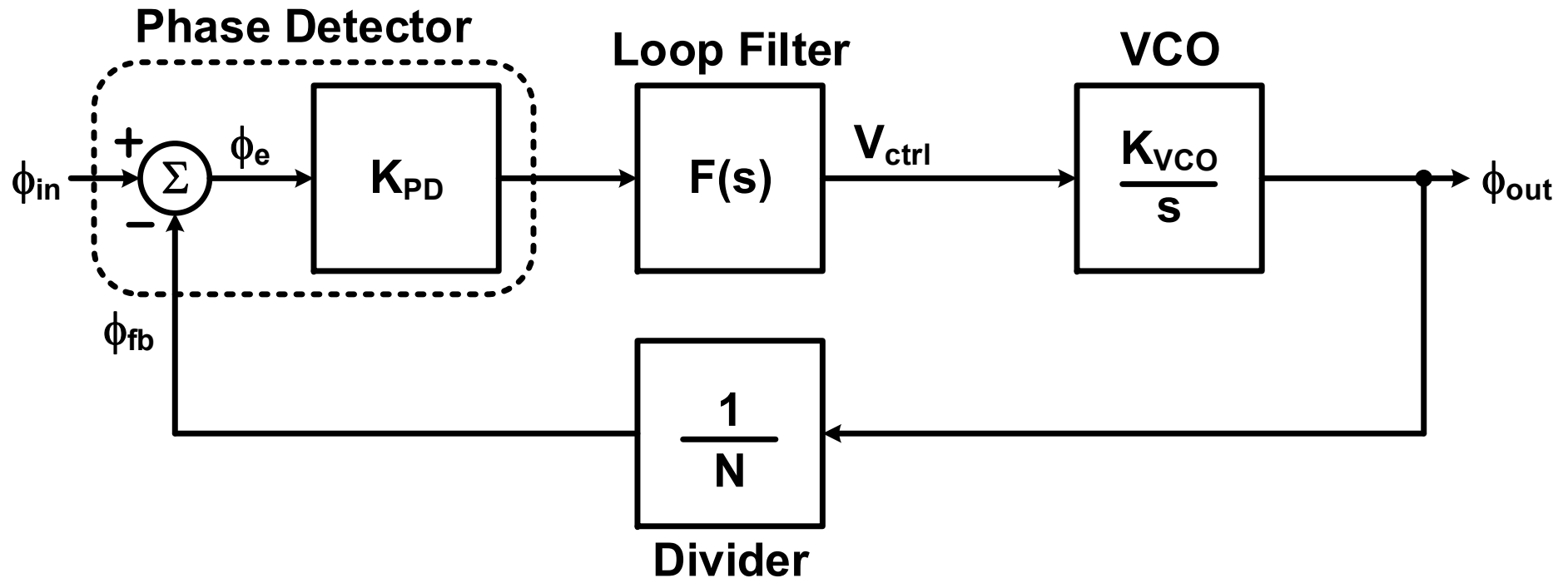
Forward Path Determinant $\Delta_1 = 1 - 0 = 1$

$$\text{System Determinant } \Delta = 1 - \left(-\frac{G(s)}{N} \right) + 0 = 1 + \frac{G(s)}{N}$$

$$H(s) = \frac{\Phi_{out}(s)}{\Phi_{ref}(s)} = \frac{G(s)}{1 + \frac{G(s)}{N}} = \frac{K_{PD}K_{VCO}F(s)}{s + \frac{K_{PD}K_{VCO}F(s)}{N}}$$

- Low-pass response whose overall order is set by $F(s)$

PLL Error Transfer Function



$$l_1 = -\frac{K_{PD}K_{VCO}F(s)}{sN} = -\frac{G(s)}{N}$$

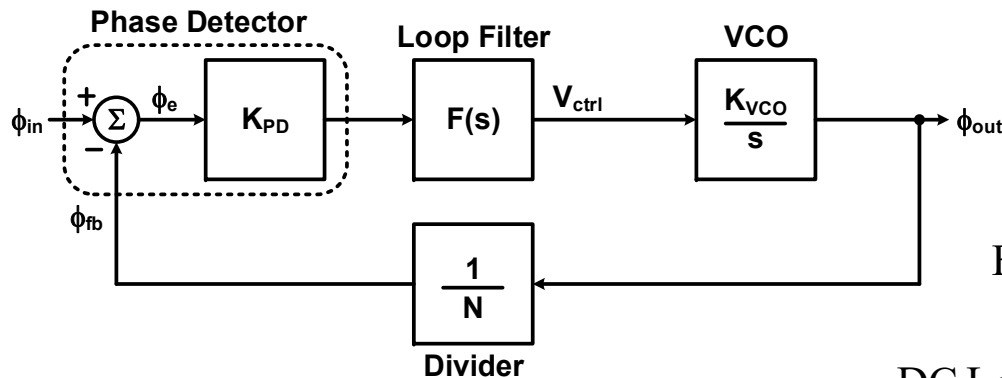
$$E(s) = \frac{\Phi_e(s)}{\Phi_{ref}(s)} = \frac{1}{1 + \frac{G(s)}{N}} = \frac{s}{s + \frac{K_{PD}K_{VCO}F(s)}{N}}$$

- Ideally, we want this to be zero
- Phase error generally increases with frequency due to this high-pass response

PLL Order and Type

- The PLL order refers to the number of poles in the closed-loop transfer function
 - This is typically one greater than the number of loop filter poles
- The PLL type refers to the number of integrators within the loop
 - A PLL is always at least Type 1 due to the VCO integrator
- Note, the order can never be less than the type

First-Order PLL



$$F(s) = K_1$$

$$\text{Forward Path Gain : } G(s) = \frac{K_{PD}K_{VCO}K_1}{s} = \frac{NK_{DC}}{s}$$

$$\text{DC Loop Gain Magnitude : } K_{DC} = \lim_{s \rightarrow 0} \left| \frac{sG(s)}{N} \right| = \frac{K_{PD}K_{VCO}K_1}{N}$$

$$\text{Transfer Function : } H(s) = \frac{K_{PD}K_{VCO}K_1}{s + \frac{K_{PD}K_{VCO}K_1}{N}} = \frac{N\omega_{3dB}}{s + \omega_{3dB}} = \frac{NK_{DC}}{s + K_{DC}}$$

$$\text{Closed - Loop Bandwidth : } \omega_{3dB} = \frac{K_{PD}K_{VCO}K_1}{N} = K_{DC}$$

$$\text{Error Function : } E(s) = \frac{s}{s + \frac{K_{PD}K_{VCO}K_1}{N}} = \frac{s}{s + \omega_{3dB}} = \frac{s}{s + K_{DC}}$$

- Simple first-order low-pass transfer function
- Closed-loop bandwidth is equal to the DC loop gain magnitude
- Note, the "DC Loop Gain Magnitude" is not simply the PLL open-loop gain evaluated at $s=0$. It is

$$K_{DC} = \lim_{s \rightarrow 0} \left| \frac{sG(s)}{N} \right|.$$

- This expression cancels the VCO DC pole and allows a comparison between PLLs of different orders and types. It is useful to predict the steady-state phase error. See Gardner 2.2.3 and 5.1.1.

First-Order PLL Tracking Response

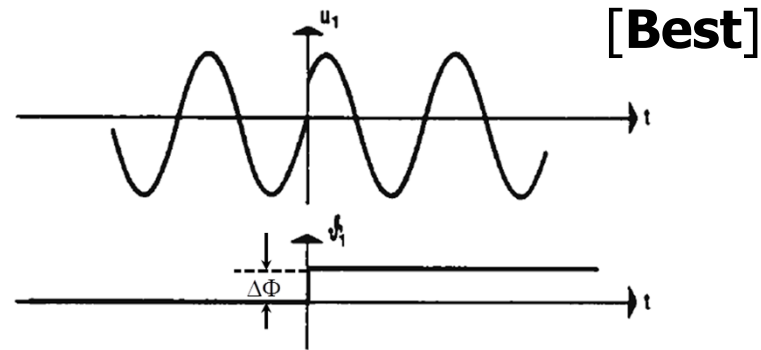
- The PLL's tracking behavior, or how the phase error responds to an input phase change, varies with the PLL type

- Phase Step Response

$$\phi_1(t) = \Delta\Phi u(t)$$

$$u_1(t) = \sin(\omega_1(t) + \Delta\Phi u(t))$$

No change in frequency



- The final value theorem can be used to find the steady-state phase error

$$\lim_{s \rightarrow 0} \left(\frac{\Delta\Phi}{s} \right) (sE(s)) = \lim_{s \rightarrow 0} \frac{\Delta\Phi s}{s + K_{DC}} = 0$$

- All PLLs should have no steady-state phase error with a phase step error
 - Note, this assumes that the frequency of operation is the same as the VCO center frequency ($V_{ctrl}=0$). Working at a frequency other than the VCO center frequency is considered having a frequency offset (step).

First-Order PLL Tracking Response

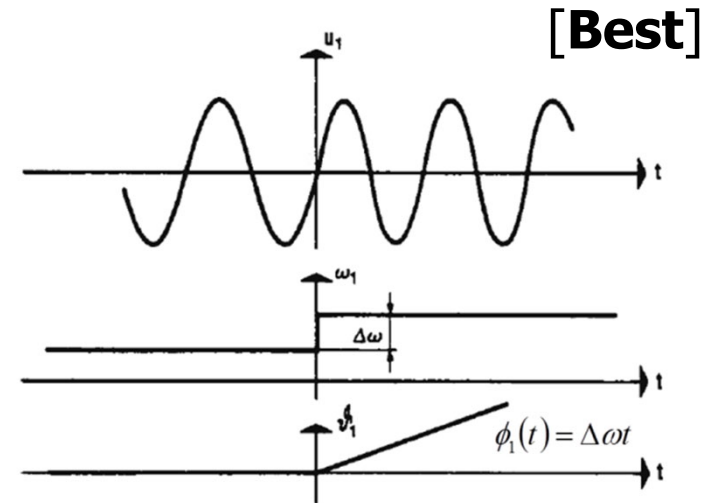
- Frequency Offset (Step)

$$\omega_1(t) = \omega_0 + \Delta\omega$$

$$u_1(t) = \sin(\omega_0 t + \Delta\omega t) = \sin(\omega_0 t + \phi_1(t))$$

$$\text{where } \phi_1(t) = \Delta\omega t$$

A frequency step produces a ramp in phase



- The final value theorem can be used to find the steady-state phase error

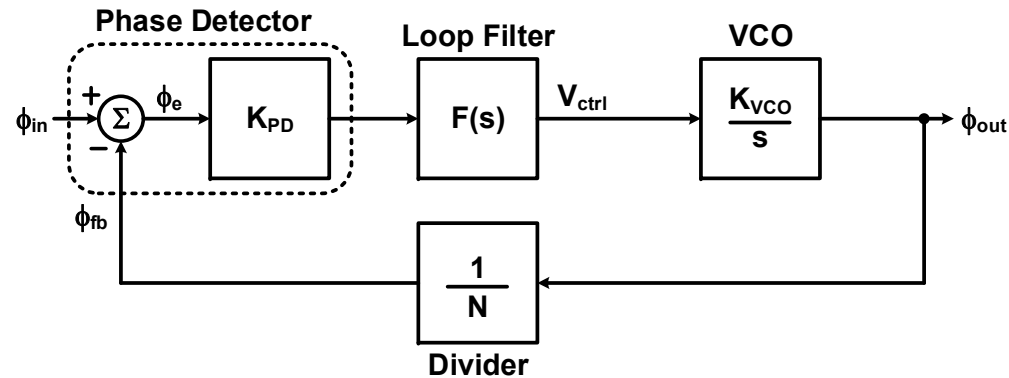
$$\lim_{s \rightarrow 0} \left(\frac{\Delta\omega}{s^2} \right) (sE(s)) = \lim_{s \rightarrow 0} \frac{\Delta\omega}{s + K_{DC}} = \frac{\Delta\omega}{K_{DC}}$$

- With a frequency offset (step), a first-order PLL will lock with a steady-state phase error that is inversely proportional to the loop gain

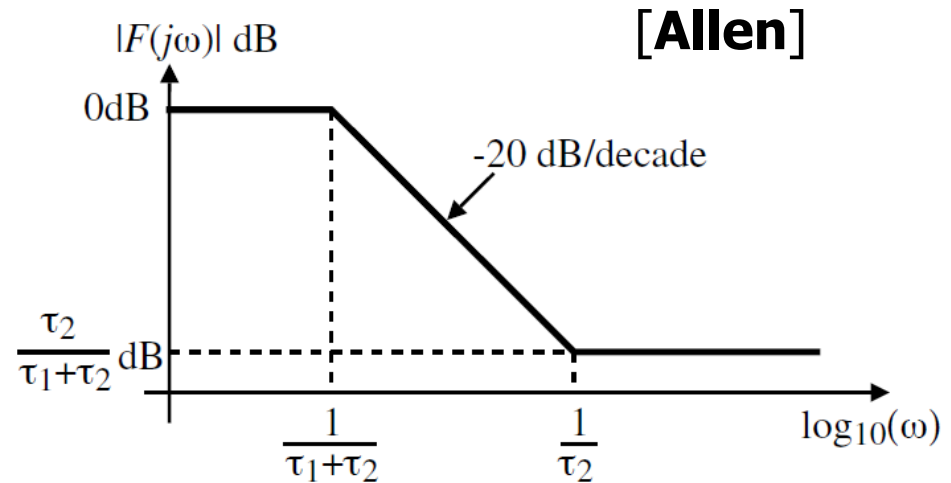
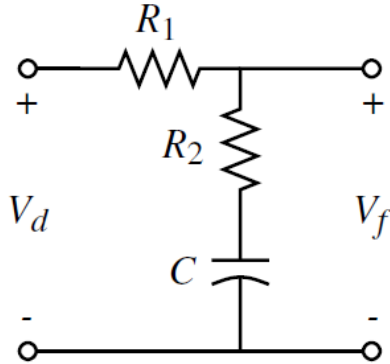
First-Order PLL Issues

- The DC loop gain directly sets the PLL bandwidth
 - No degrees of freedom
- In order to have low phase error, a large loop gain is necessary, which implies a wide bandwidth
 - This may not be desired in applications where we would like to filter input reference clock phase noise
- First-order PLLs offer no filtering of the phase detector output
 - Without this filtering, the PD may not be well approximated by a simple K_{PD} factor
 - Multiplier PDs have a “second-harmonic” term
 - Digital PDs output square pulses that need to be filtered

Second-Order Type-1 PLL w/ Passive Lag-Lead Filter



Passive Lag-Lead Loop Filter



[Allen]

$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)}$$

$$\tau_1 = R_1 C \quad \tau_2 = R_2 C$$

Second-Order Type-1 PLL w/ Passive Lag-Lead Filter

$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)} \quad \text{Forward Path Gain : } G(s) = \frac{K_{PD}K_{VCO}(1 + s\tau_2)}{s(1 + s(\tau_1 + \tau_2))} = \frac{NK_{DC} \left(\frac{\tau_2}{\tau_1 + \tau_2} \right) \left(s + \frac{1}{\tau_2} \right)}{s \left(s + \frac{1}{\tau_1 + \tau_2} \right)}$$

$$\tau_1 = R_1C \quad \tau_2 = R_2C$$

$$\text{DC Loop Gain Magnitude : } K_{DC} = \lim_{s \rightarrow 0} \left| \frac{sG(s)}{N} \right| = \frac{K_{PD}K_{VCO}}{N}$$

$$\text{Transfer Function : } H(s) = \frac{\frac{K_{PD}K_{VCO}\tau_2}{\tau_1 + \tau_2} \left(s + \frac{1}{\tau_2} \right)}{s^2 + \left(\frac{1 + K_{PD}K_{VCO}\tau_2/N}{\tau_1 + \tau_2} \right) s + \frac{K_{PD}K_{VCO}}{N(\tau_1 + \tau_2)}} = N \frac{\omega_n \left(2\zeta - \frac{N\omega_n}{K_{PD}K_{VCO}} \right) s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$= N \frac{K_{DC} \left(\frac{\tau_2}{\tau_1 + \tau_2} \right) \left(s + \frac{1}{\tau_2} \right)}{s^2 + \left(\frac{1 + K_{DC}\tau_2}{\tau_1 + \tau_2} \right) s + \frac{K_{DC}}{\tau_1 + \tau_2}}$$

$$\text{Natural Frequency : } \omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{N(\tau_1 + \tau_2)}}$$

$$\text{Damping Factor : } \zeta = \frac{\omega_n}{2} \left(\tau_2 + \frac{N}{K_{PD}K_{VCO}} \right)$$

$$\text{Note : } \zeta = \frac{1}{2Q}$$

$$\text{Error Function : } E(s) = \frac{s \left(s + \frac{N\omega_n^2}{K_{PD}K_{VCO}} \right)}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

Second-Order Type-1 PLL Tracking Response

- Phase Step Response

$$\lim_{s \rightarrow 0} \left(\frac{\Delta \Phi}{s} \right) (sE(s)) = \lim_{s \rightarrow 0} \frac{\Delta \Phi s \left(s + \frac{N\omega_n^2}{K_{PD}K_{VCO}} \right)}{s^2 + 2\zeta\omega_n s + \omega_n^2} = 0$$

Again, phase error should be zero with a phase step

- Frequency Offset (Step)

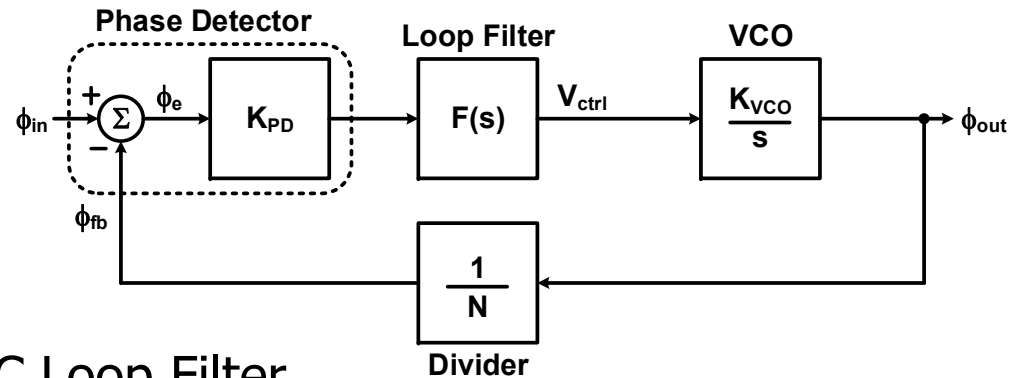
$$\lim_{s \rightarrow 0} \left(\frac{\Delta \omega}{s^2} \right) (sE(s)) = \lim_{s \rightarrow 0} \frac{\Delta \omega \left(s + \frac{N\omega_n^2}{K_{PD}K_{VCO}} \right)}{s^2 + 2\zeta\omega_n s + \omega_n^2} = \frac{\Delta \omega}{K_{DC}}$$

- A second-order type-1 PLL will still lock with a phase error if there is a frequency offset!

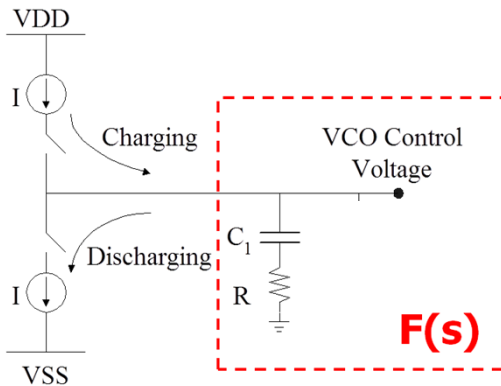
Second-Order Type-1 PLL Properties

- While the second-order type-1 PLL will still lock with a phase error with a frequency offset, it is much more useful than a first-order PLL
- There are sufficient design parameters (degrees of freedom) to independently set ω_n , ζ , and K_{DC}
- The loop filter conditions the phase detector output for proper VCO control
- Loop stability needs to be considered for the second-order system

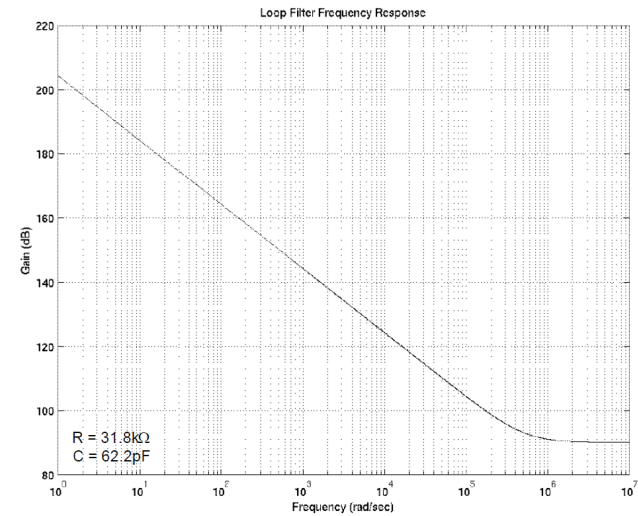
Second-Order Type-2 PLL w/ Passive Series-RC Lag-Lead Filter



Passive Series-RC Loop Filter



$$F(s) = \frac{R \left(s + \frac{1}{RC} \right)}{s}$$



- Note, this type of loop filter is typically used with a charge-pump driving it. Thus, the filter transfer function is equal to the impedance.

Second-Order Type-2 PLL w/ Passive Series-RC Lag-Lead Filter

$$F(s) = \frac{R\left(s + \frac{1}{RC}\right)}{s}$$

$$\text{Forward Path Gain : } G(s) = \frac{K_{PD}K_{VCO}R\left(s + \frac{1}{RC}\right)}{s^2}$$

$$\text{DC Loop Gain Magnitude : } K_{DC} = \lim_{s \rightarrow 0} \left| \frac{sG(s)}{N} \right| = \infty$$

$$\text{Transfer Function : } H(s) = \frac{K_{PD}K_{VCO}R\left(s + \frac{1}{RC}\right)}{s^2 + \left(\frac{K_{PD}K_{VCO}R}{N}\right)s + \frac{K_{PD}K_{VCO}}{NC}} = \frac{N2\zeta\omega_n\left(s + \frac{\omega_n}{2\zeta}\right)}{s^2 + 2\zeta\omega_ns + \omega_n^2}$$

$$\text{Natural Frequency : } \omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{NC}}$$

$$\text{Damping Factor : } \zeta = \frac{\omega_n}{2}RC$$

$$\text{Error Function : } E(s) = \frac{s^2}{s^2 + 2\zeta\omega_ns + \omega_n^2}$$

Second-Order Type-2 PLL Tracking Response

- Phase Step Response

$$\lim_{s \rightarrow 0} \left(\frac{\Delta\Phi}{s} \right) (sE(s)) = \lim_{s \rightarrow 0} \frac{\Delta\Phi s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} = 0$$

Again, phase error should be zero with a phase step

- Frequency Offset (Step)

$$\lim_{s \rightarrow 0} \left(\frac{\Delta\omega}{s^2} \right) (sE(s)) = \lim_{s \rightarrow 0} \frac{\Delta\omega s}{s^2 + 2\zeta\omega_n s + \omega_n^2} = 0$$

- A second-order type-2 PLL will lock with no phase error with a frequency offset!

Second-Order Type-2 PLL Properties

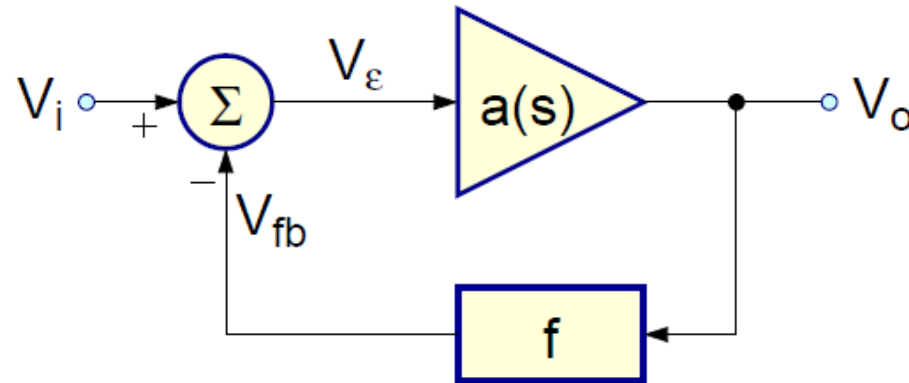
- A big advantage of the type-2 PLL is that it has zero phase error even with a frequency offset
 - This is why type-2 PLLs are very popular
- A type-2 PLL requires a zero in the loop filter for stability.
 - Note, this is not required in a type-1 PLL
- This zero can cause extra peaking in the frequency response
 - Important to minimize this in some applications, such as cascaded CDR systems

Agenda

- PLL Overview
- PLL Linear Model
- PLL Stability
- Analog Charge Pump PLL Design Procedure
- PLL Noise Transfer Functions
- PLL Transient Behavior
- PLL Time Domain Modeling

Feedback Configuration

[Karsilayan]



Here f = feedback factor

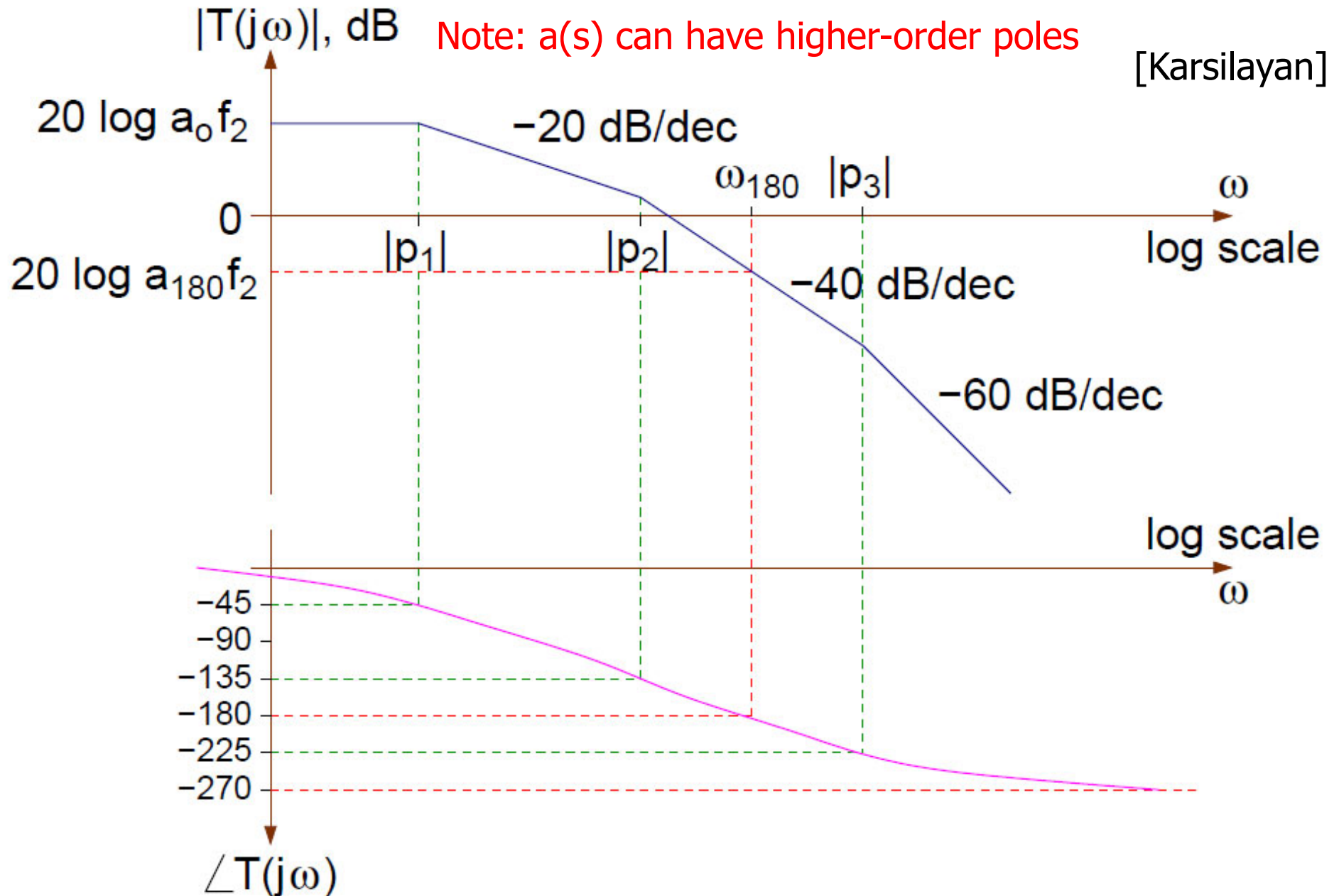
$$a(s) = \frac{V_o}{V_\epsilon}(s) = \frac{a_0}{1 + \frac{s}{p_1}}$$

$$A_{CL}(s) = \frac{V_o}{V_i}(s) = \frac{a(s)}{1 + a(s)f} = \frac{\frac{a_0}{1 + a_0 f}}{1 + \frac{s}{(1 + a_0 f)p_1}}$$

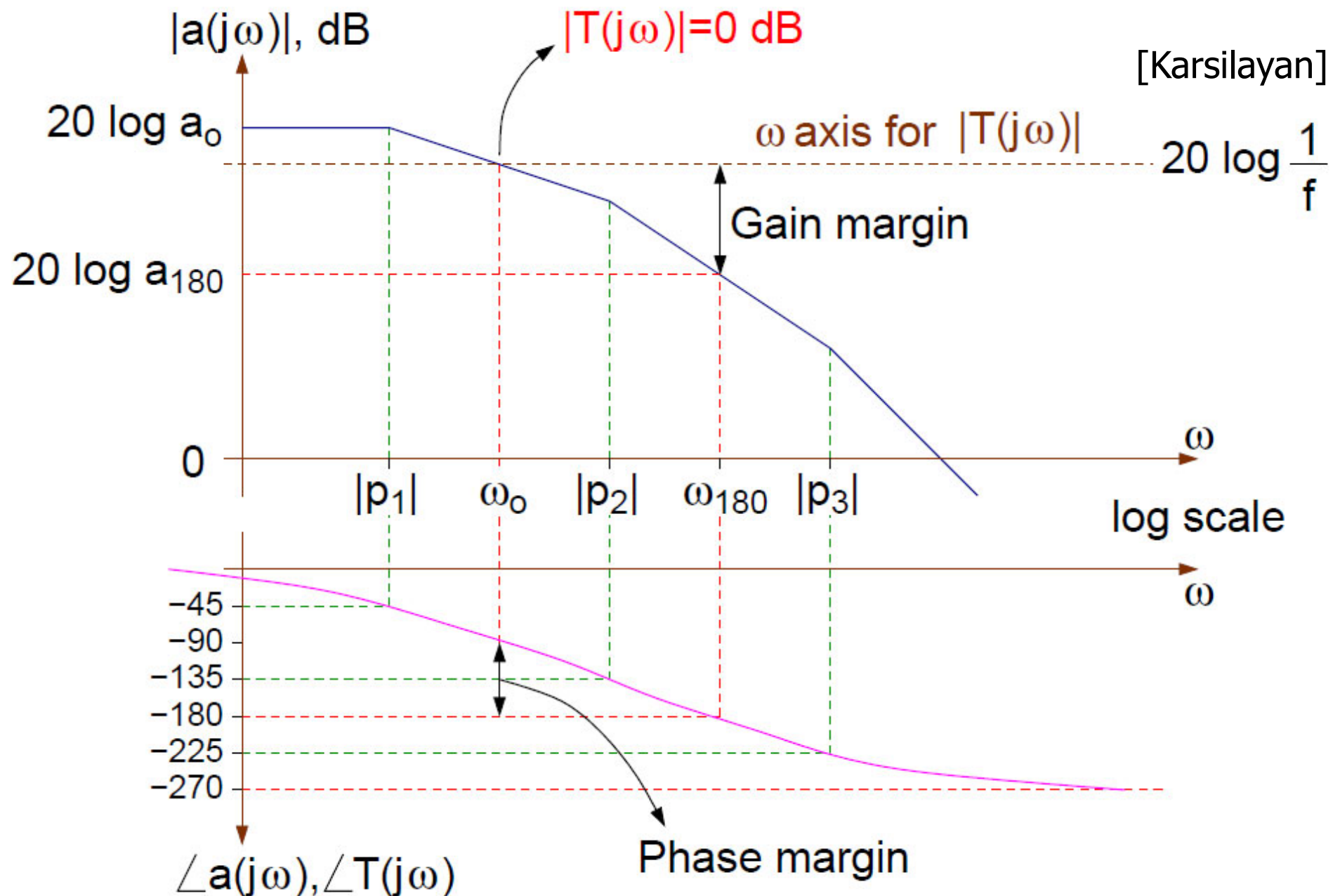
$$\text{If } a_0 \text{ is large: } A_{CL}(0) \approx \frac{1}{f} \quad \omega_p \approx a_0 p_1 f$$

Magnitude & Phase

$$T(s) = a(s)f_2$$



Gain & Phase Margin



Stability Criteria

Nyquist:

$$|T(j\omega_{180})| = a_{180}f < 1 \Rightarrow \text{Stable}$$

[Karsilayan]

Gain Margin (**GM**):

$$GM = 20 \log \frac{1}{|T(j\omega_{180})|} = -20 \log |T(j\omega_{180})|$$

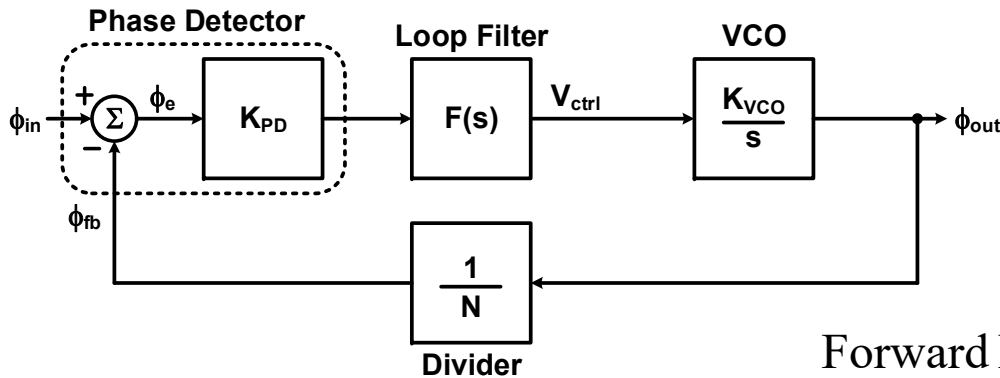
$$GM > 0 \Rightarrow \text{Stable}$$

Phase Margin (**PM**):

$$PM = 180^\circ + \angle T(j\omega_o)$$

$$PM > 0 \Rightarrow \text{Stable}$$

First-Order PLL



$$F(s) = K_1$$

$$\text{Forward Path Gain : } G(s) = \frac{K_{PD}K_{VCO}K_1}{s} = \frac{NK_{DC}}{s}$$

$$\text{DC Loop Gain Magnitude : } K_{DC} = \lim_{s \rightarrow 0} \left| \frac{sG(s)}{N} \right| = \frac{K_{PD}K_{VCO}K_1}{N}$$

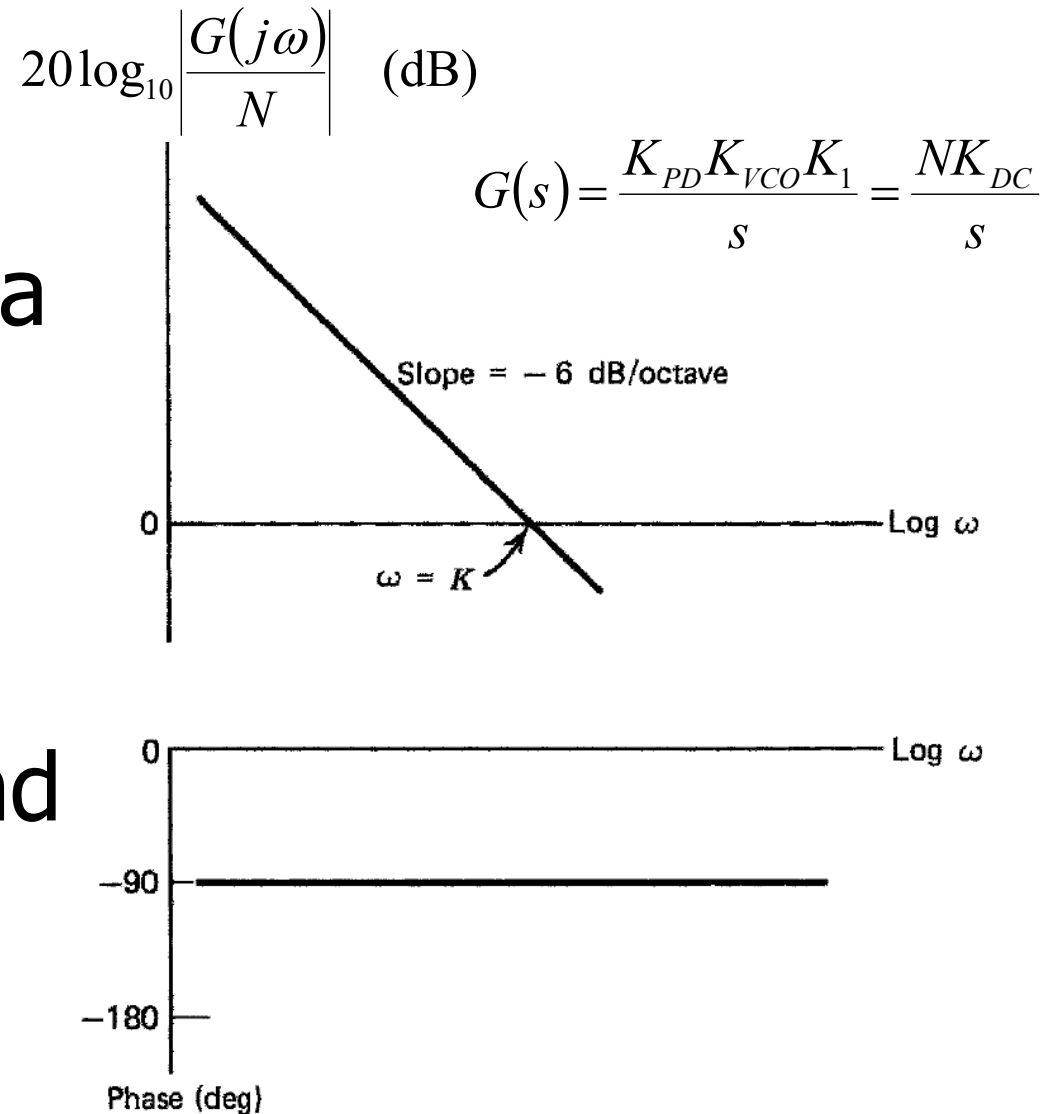
$$\text{Transfer Function : } H(s) = \frac{K_{PD}K_{VCO}K_1}{s + \frac{K_{PD}K_{VCO}K_1}{N}} = \frac{N\omega_{3dB}}{s + \omega_{3dB}} = \frac{NK_{DC}}{s + K_{DC}}$$

$$\text{Closed - Loop Bandwidth : } \omega_{3dB} = \frac{K_{PD}K_{VCO}K_1}{N} = K_{DC}$$

$$\text{Error Function : } E(s) = \frac{s}{s + \frac{K_{PD}K_{VCO}K_1}{N}} = \frac{s}{s + \omega_{3dB}} = \frac{s}{s + K_{DC}}$$

First-Order PLL Stability

- Open-loop Bode plots are useful for checking stability via the phase margin
- A first-order PLL is inherently stable and always has 90° phase margin



Second-Order Type-1 PLL w/ Passive Lag-Lead Filter

$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)} \quad \text{Forward Path Gain : } G(s) = \frac{K_{PD}K_{VCO}(1 + s\tau_2)}{s(1 + s(\tau_1 + \tau_2))} = \frac{NK_{DC}\left(\frac{\tau_2}{\tau_1 + \tau_2}\right)\left(s + \frac{1}{\tau_2}\right)}{s\left(s + \frac{1}{\tau_1 + \tau_2}\right)}$$

$$\tau_1 = R_1C \quad \tau_2 = R_2C$$

$$\text{DC Loop Gain Magnitude : } K_{DC} = \lim_{s \rightarrow 0} \left| \frac{sG(s)}{N} \right| = \frac{K_{PD}K_{VCO}}{N}$$

$$\begin{aligned} \text{Transfer Function : } H(s) &= \frac{\frac{K_{PD}K_{VCO}\tau_2}{\tau_1 + \tau_2}\left(s + \frac{1}{\tau_2}\right)}{s^2 + \left(\frac{1 + K_{PD}K_{VCO}\tau_2/N}{\tau_1 + \tau_2}\right)s + \frac{K_{PD}K_{VCO}}{N(\tau_1 + \tau_2)}} = N \frac{\omega_n \left(2\zeta - \frac{N\omega_n}{K_{PD}K_{VCO}}\right)s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \\ &= N \frac{K_{DC}\left(\frac{\tau_2}{\tau_1 + \tau_2}\right)\left(s + \frac{1}{\tau_2}\right)}{s^2 + \left(\frac{1 + K_{DC}\tau_2}{\tau_1 + \tau_2}\right)s + \frac{K_{DC}}{\tau_1 + \tau_2}} \end{aligned}$$

$$\text{Natural Frequency : } \omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{N(\tau_1 + \tau_2)}}$$

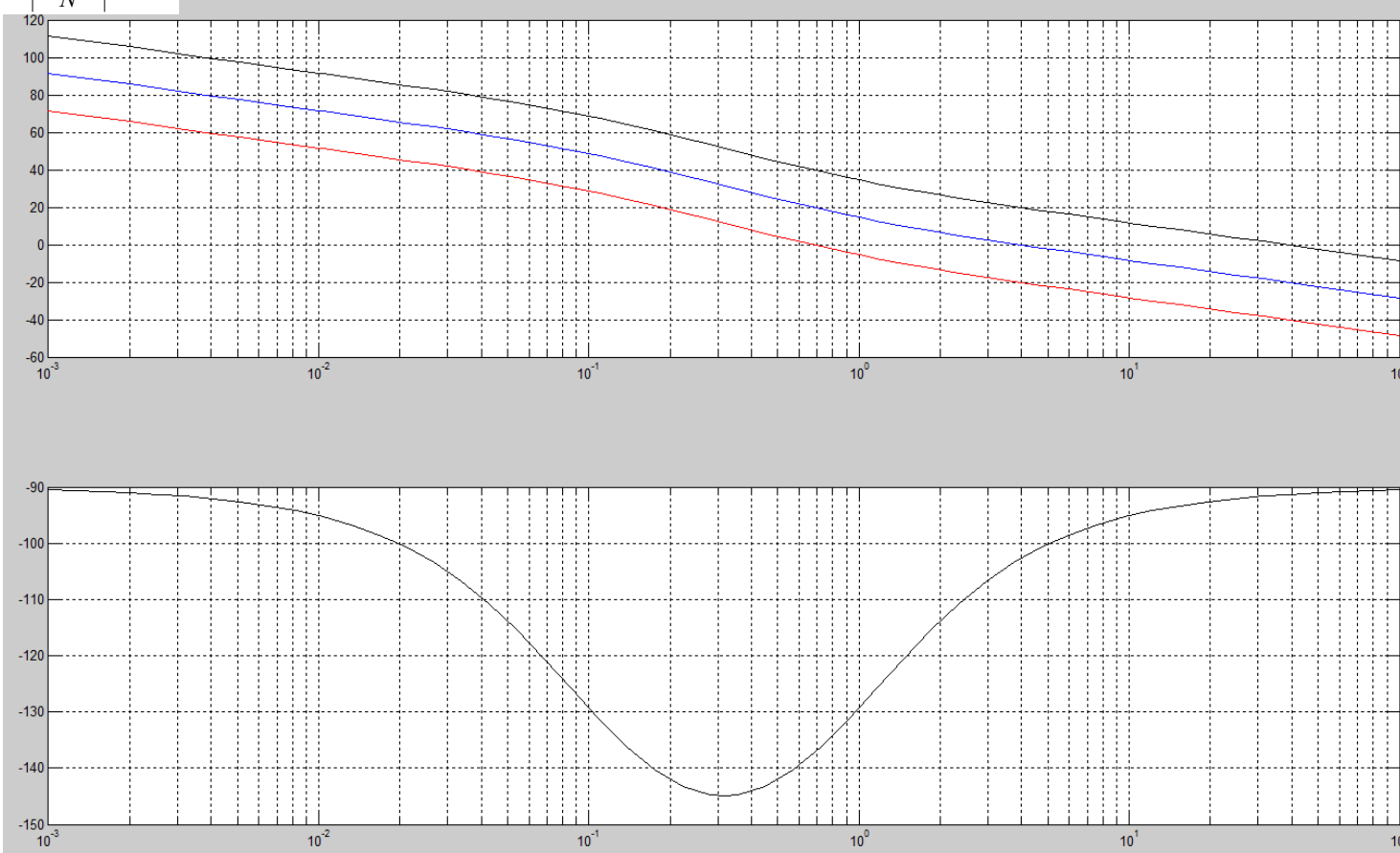
$$\text{Damping Factor : } \zeta = \frac{\omega_n}{2} \left(\tau_2 + \frac{N}{K_{PD}K_{VCO}} \right)$$

$$\text{Error Function : } E(s) = \frac{s\left(s + \frac{N\omega_n^2}{K_{PD}K_{VCO}}\right)}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

Second-Order Type-1 PLL w/ Lag-Lead Filter Stability

- Assuming a decade spacing between filter pole and zero

$20\log_{10}\left|\frac{G(j\omega)}{N}\right|$ (dB)



$$G(s) = \frac{NK_{DC} \left(\frac{\tau_2}{\tau_1 + \tau_2} \right) \left(s + \frac{1}{\tau_2} \right)}{s \left(s + \frac{1}{\tau_1 + \tau_2} \right)}$$

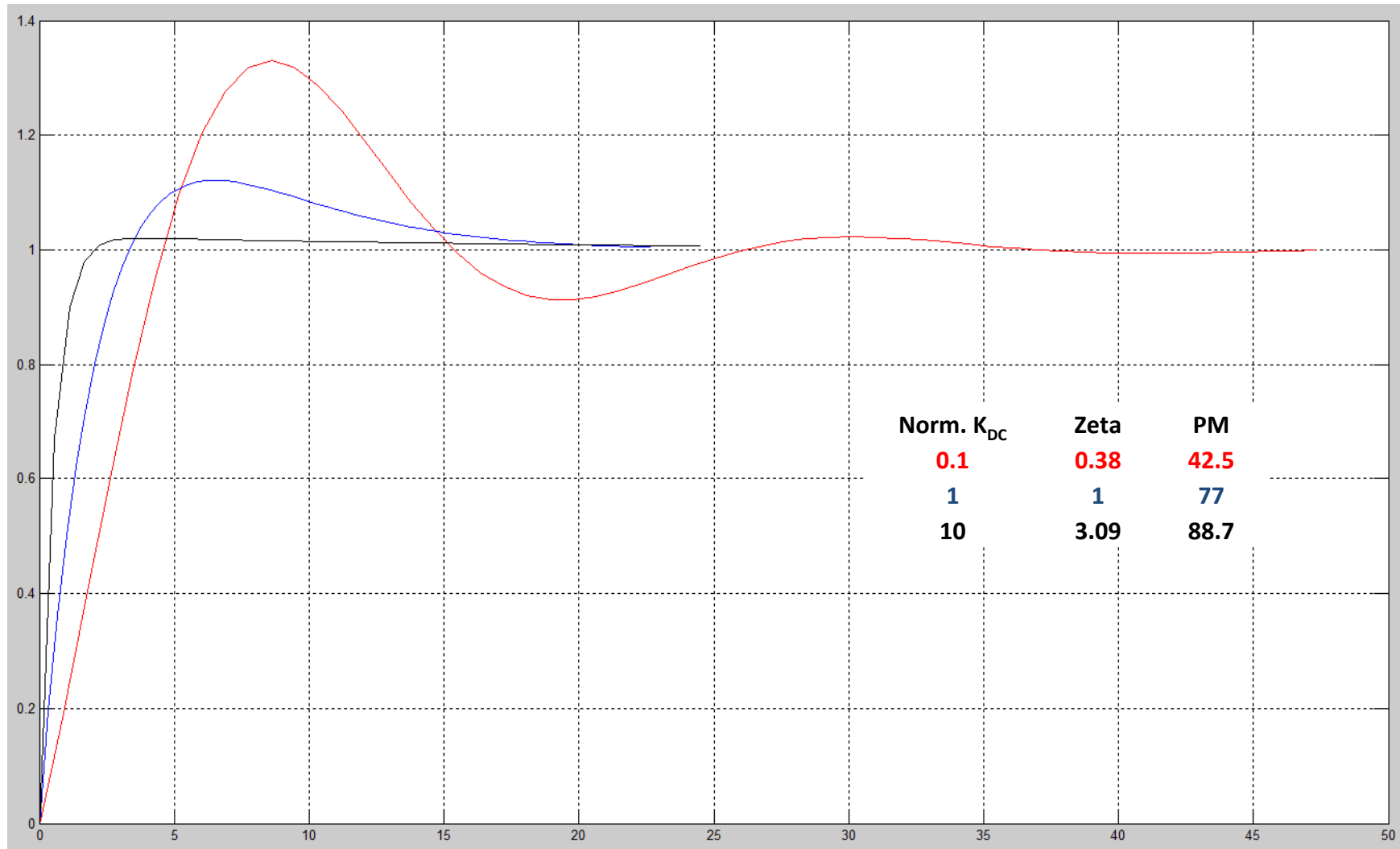
Normalizing
 K_{DC} for $\zeta=1$

Norm. KDC	Zeta	PM
0.1	0.38	42.5
1	1	77
10	3.09	88.7

- A larger K_{DC} provide a more stable system

Second-Order Type-1 PLL w/ Lag-Lead Filter

Output Response w/ Phase Step



- Note, time axis is scaled by $\sqrt{K_{DC}}$ in order to view the phase step plots on one graph

Root Locus

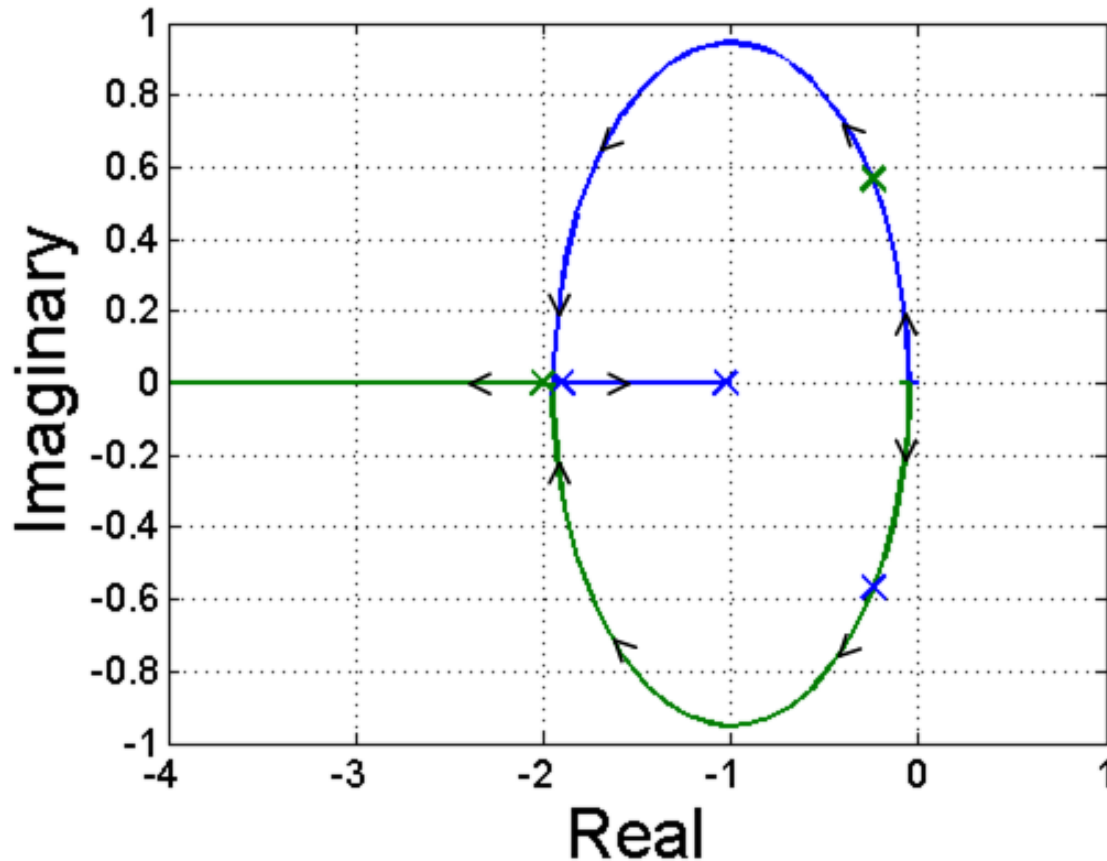
- A Root-Locus Plot is a plot of the closed-loop poles in the complex s -plane as the loop gain changes from zero to very large
- Useful in visualizing system stability and sensitivity to variations in loop gain
- For stability, all poles should lie within the left-half plane, i.e no poles should be in the right-half plane
- A good design ensures that the poles have sufficient margin from the imaginary axis for proper stability, damping, and acceptable gain peaking

Second-Order Type-1 PLL w/ Passive Lag-Lead Filter Root Locus

$$\text{Open - Loop: } \frac{G(s)}{N} = \frac{K_{DC} \left(\frac{\tau_2}{\tau_1 + \tau_2} \right) \left(s + \frac{1}{\tau_2} \right)}{s \left(s + \frac{1}{\tau_1 + \tau_2} \right)}$$

$$\text{Closed - Loop: } H(s) = N \frac{K_{DC} \left(\frac{\tau_2}{\tau_1 + \tau_2} \right) \left(s + \frac{1}{\tau_2} \right)}{s^2 + \left(\frac{1 + K_{DC} \tau_2}{\tau_1 + \tau_2} \right) s + \frac{K_{DC}}{\tau_1 + \tau_2}}$$

$$\tau_2 = 1, \tau_1 = 9$$



- Initial pole values with zero loop gain are the open-loop poles

$$p_1 = 0 \quad p_2 = -\frac{1}{\tau_1 + \tau_2} = -0.1$$

- Final pole values with infinite loop gain are the open-loop zeros

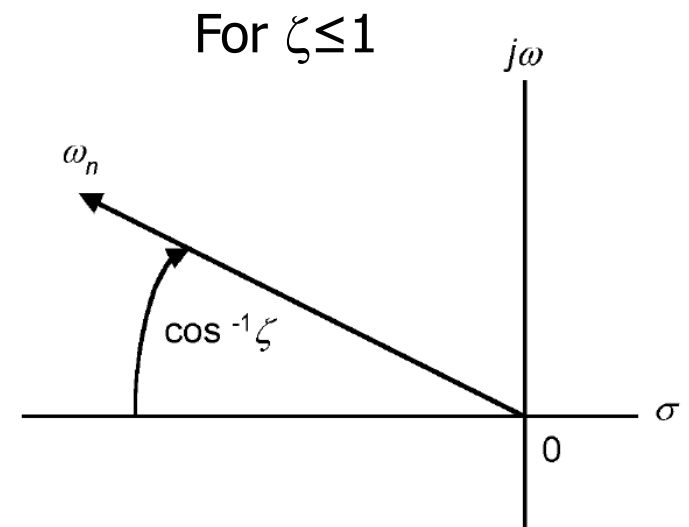
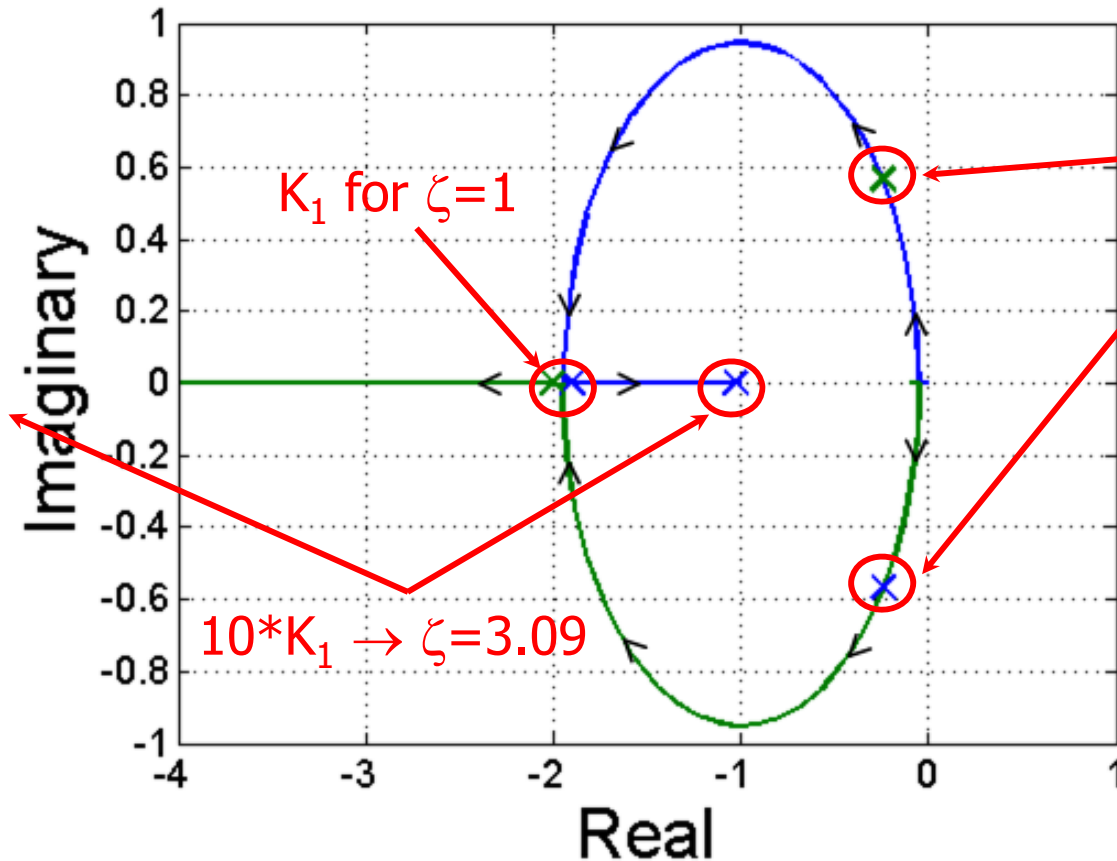
$$p_1 = -\frac{1}{\tau_2} = -1 \quad p_2 = -\infty$$

Second-Order Type-1 PLL w/ Passive Lag-Lead Filter Root Locus

$$\text{Open - Loop: } \frac{G(s)}{N} = \frac{K_{DC} \left(\frac{\tau_2}{\tau_1 + \tau_2} \right) \left(s + \frac{1}{\tau_2} \right)}{s \left(s + \frac{1}{\tau_1 + \tau_2} \right)}$$

$$\text{Closed - Loop: } H(s) = N \frac{K_{DC} \left(\frac{\tau_2}{\tau_1 + \tau_2} \right) \left(s + \frac{1}{\tau_2} \right)}{s^2 + \left(\frac{1 + K_{DC}\tau_2}{\tau_1 + \tau_2} \right) s + \frac{K_{DC}}{\tau_1 + \tau_2}}$$

$$\tau_2=1, \tau_1=9$$

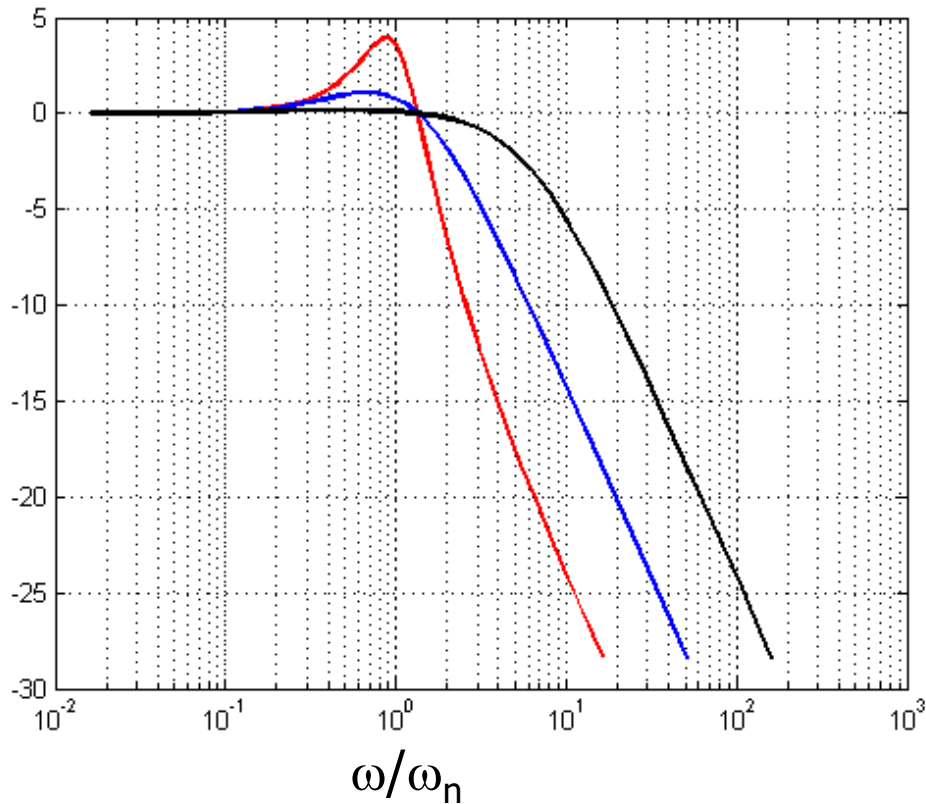


Second-Order Type-1 PLL w/ Passive Lag-Lead Filter Closed-Loop Response

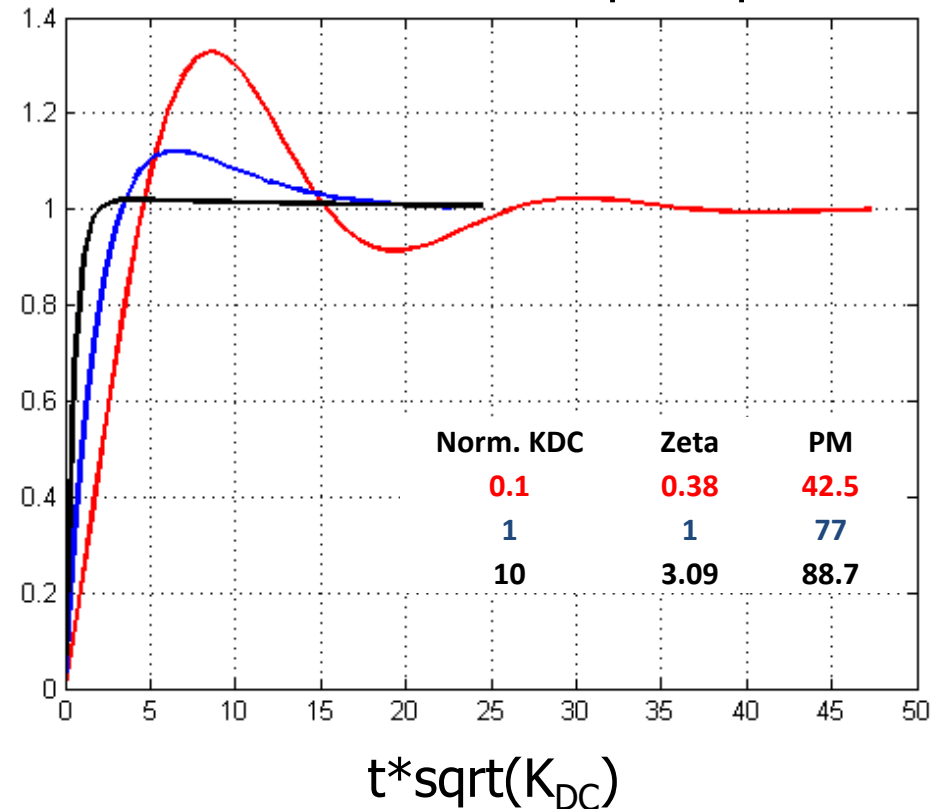
$$\text{Open - Loop: } \frac{G(s)}{N} = \frac{K_{DC} \left(\frac{\tau_2}{\tau_1 + \tau_2} \right) \left(s + \frac{1}{\tau_2} \right)}{s \left(s + \frac{1}{\tau_1 + \tau_2} \right)}$$

$$\text{Closed - Loop: } H(s) = N \frac{K_{DC} \left(\frac{\tau_2}{\tau_1 + \tau_2} \right) \left(s + \frac{1}{\tau_2} \right)}{s^2 + \left(\frac{1 + K_{DC}\tau_2}{\tau_1 + \tau_2} \right) s + \frac{K_{DC}}{\tau_1 + \tau_2}}$$

$20 \cdot \log_{10} |H(j\omega)|$



Normalized Phase Step Response



- A larger K_{DC} provide a more stable system and wider loop bandwidth

Second-Order Type-2 PLL w/ Passive Series-RC Lag-Lead Filter

$$F(s) = \frac{R\left(s + \frac{1}{RC}\right)}{s}$$

Define a loop gain factor $K = \frac{K_{PD}K_{VCO}R}{N}$

Forward Path Gain : $G(s) = \frac{K_{PD}K_{VCO}R\left(s + \frac{1}{RC}\right)}{s^2} = \frac{NK\left(s + \frac{1}{RC}\right)}{s^2}$

Transfer Function : $H(s) = \frac{K_{PD}K_{VCO}R\left(s + \frac{1}{RC}\right)}{s^2 + \left(\frac{K_{PD}K_{VCO}R}{N}\right)s + \frac{K_{PD}K_{VCO}}{NC}} = \frac{N2\zeta\omega_n\left(s + \frac{\omega_n}{2\zeta}\right)}{s^2 + 2\zeta\omega_ns + \omega_n^2} = \frac{NK\left(s + \frac{1}{RC}\right)}{s^2 + Ks + \frac{K}{RC}}$

Natural Frequency : $\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{NC}} = \sqrt{\frac{K}{RC}}$

Damping Factor : $\zeta = \frac{\omega_n}{2} RC = \frac{1}{2} \sqrt{KRC}$

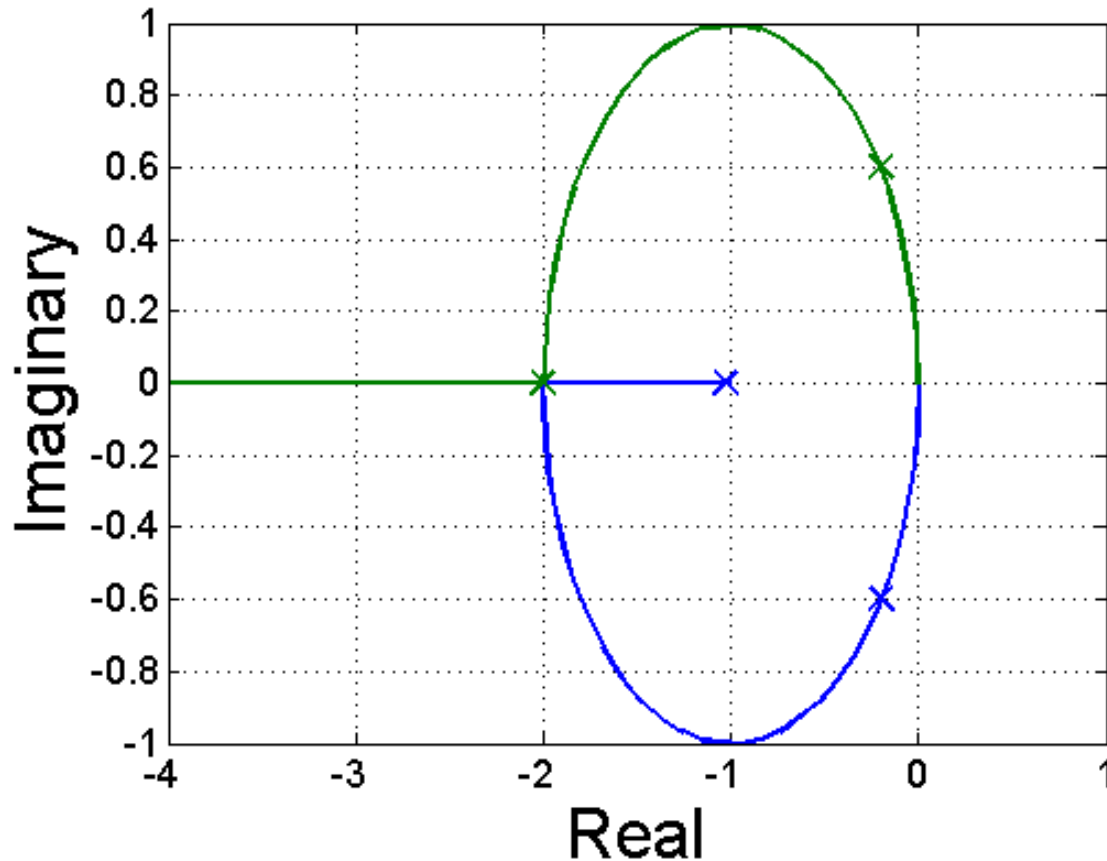
Error Function : $E(s) = \frac{s^2}{s^2 + 2\zeta\omega_ns + \omega_n^2}$

Second-Order Type-2 PLL w/ Passive Series-RC Lag-Lead Filter Root Locus

$$\text{Open - Loop: } \frac{G(s)}{N} = \frac{K \left(s + \frac{1}{RC} \right)}{s^2}$$

$$\text{Closed - Loop: } H(s) = \frac{NK \left(s + \frac{1}{RC} \right)}{s^2 + Ks + \frac{K}{RC}}$$

R=1, C=1



- Initial pole values with zero loop gain are the open-loop poles

$$p_1 = 0 \quad p_2 = 0$$

- Final pole values with infinite loop gain are the open-loop zeros

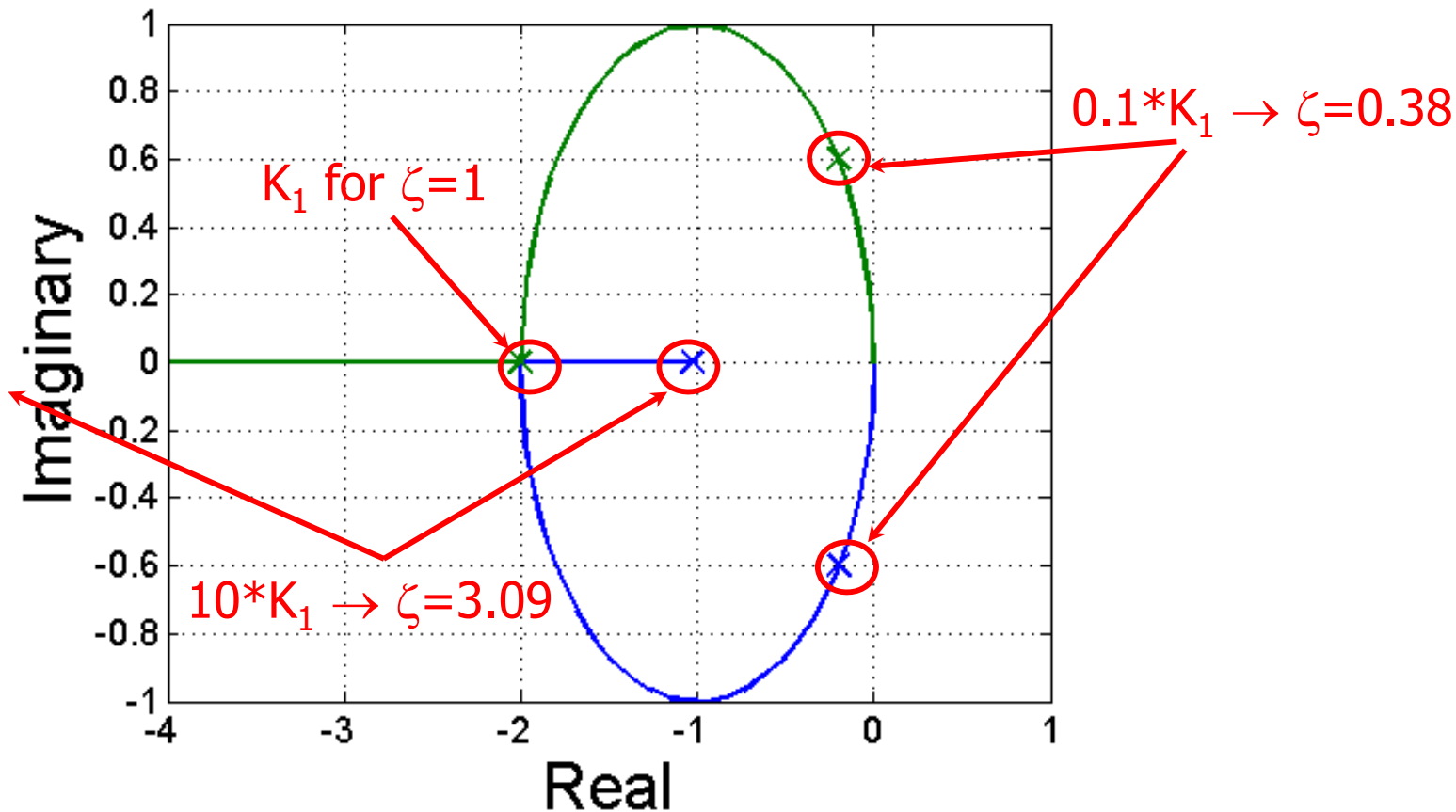
$$p_1 = -\frac{1}{RC} = -1 \quad p_2 = -\infty$$

Second-Order Type-2 PLL w/ Passive Series-RC Lag-Lead Filter Root Locus

$$\text{Open - Loop: } \frac{G(s)}{N} = \frac{K \left(s + \frac{1}{RC} \right)}{s^2}$$

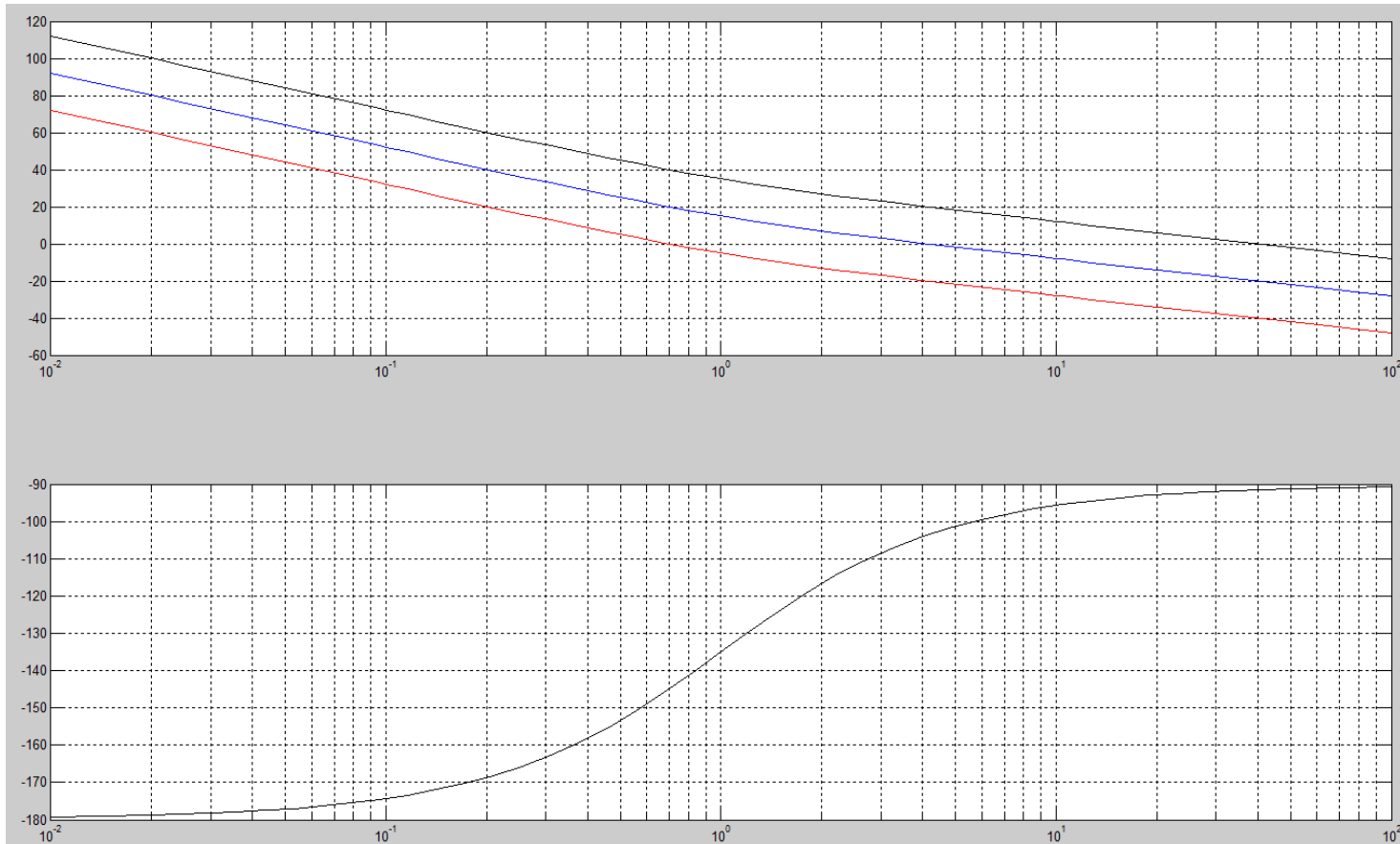
$$\text{Closed - Loop: } H(s) = \frac{NK \left(s + \frac{1}{RC} \right)}{s^2 + Ks + \frac{K}{RC}}$$

R=1, C=1



Second-Order Type-2 PLL w/ Passive Series-RC Lag-Lead Filter Stability

$20\log_{10}\left|\frac{G(j\omega)}{N}\right|$ (dB)



$$G(s) = \frac{NK\left(s + \frac{1}{RC}\right)}{s^2}$$

Normalizing K
for $\zeta=1$

Norm. K_{DC}	Zeta	PM
0.1	0.38	35
1	1	76.2
10	3.09	88.6

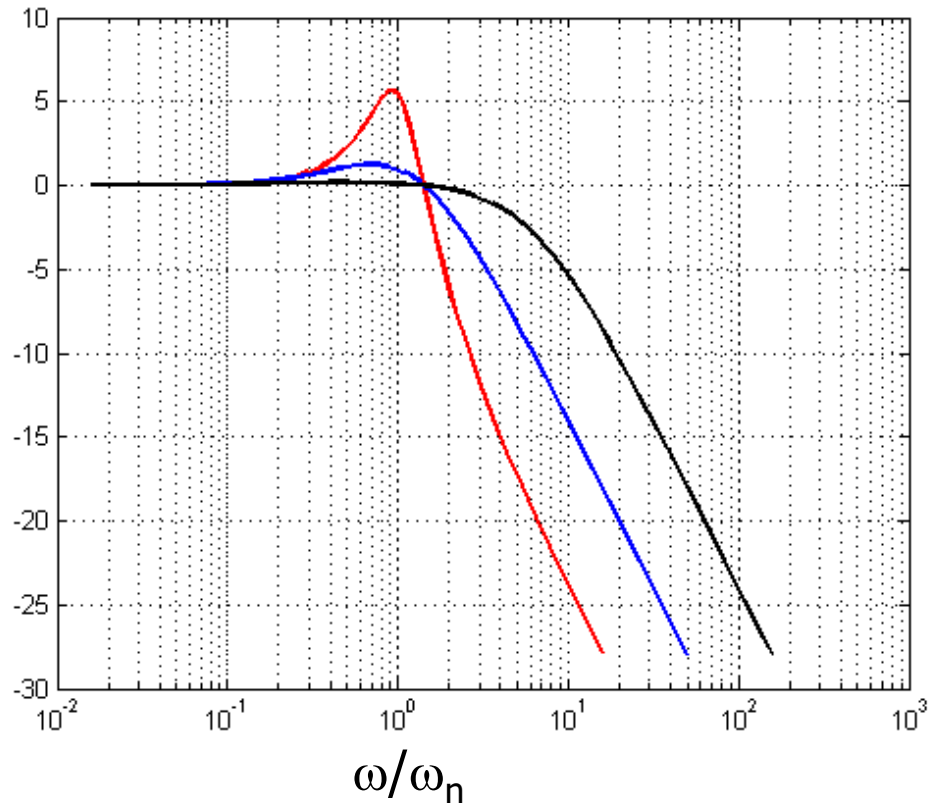
- A larger K provide a more stable system

Second-Order Type-2 PLL w/ Passive Series-RC Lag-Lead Filter Closed-Loop Response

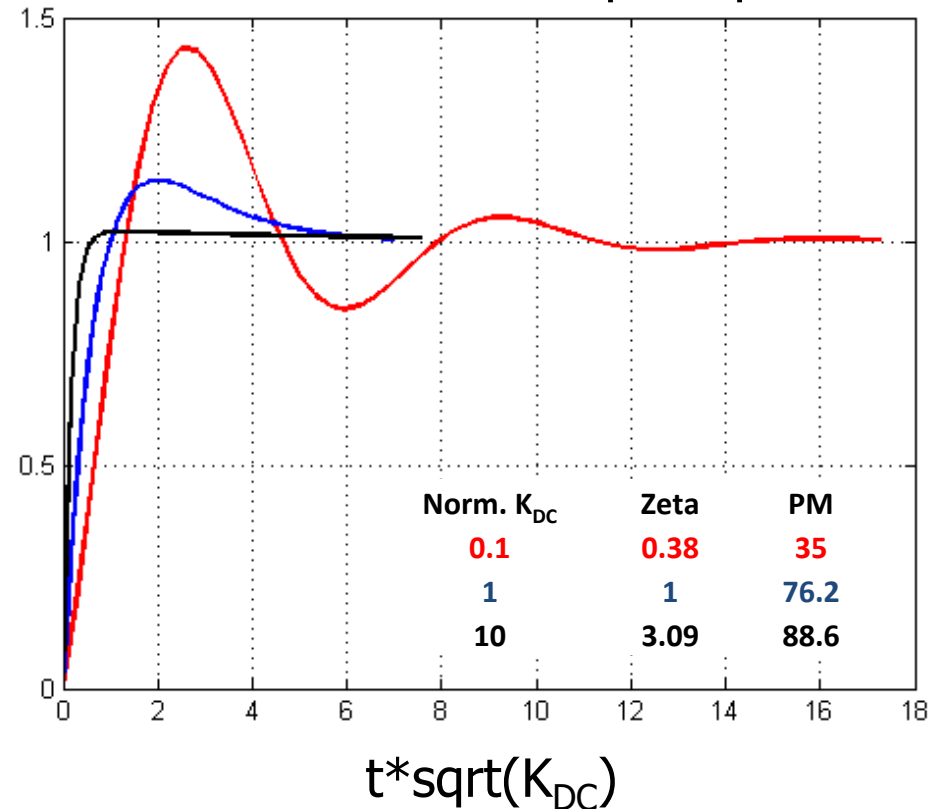
$$\text{Open - Loop: } \frac{G(s)}{N} = \frac{K \left(s + \frac{1}{RC} \right)}{s^2}$$

$$\text{Closed - Loop: } H(s) = \frac{NK \left(s + \frac{1}{RC} \right)}{s^2 + Ks + \frac{K}{RC}}$$

$20 \cdot \log_{10} |H(j\omega)|$

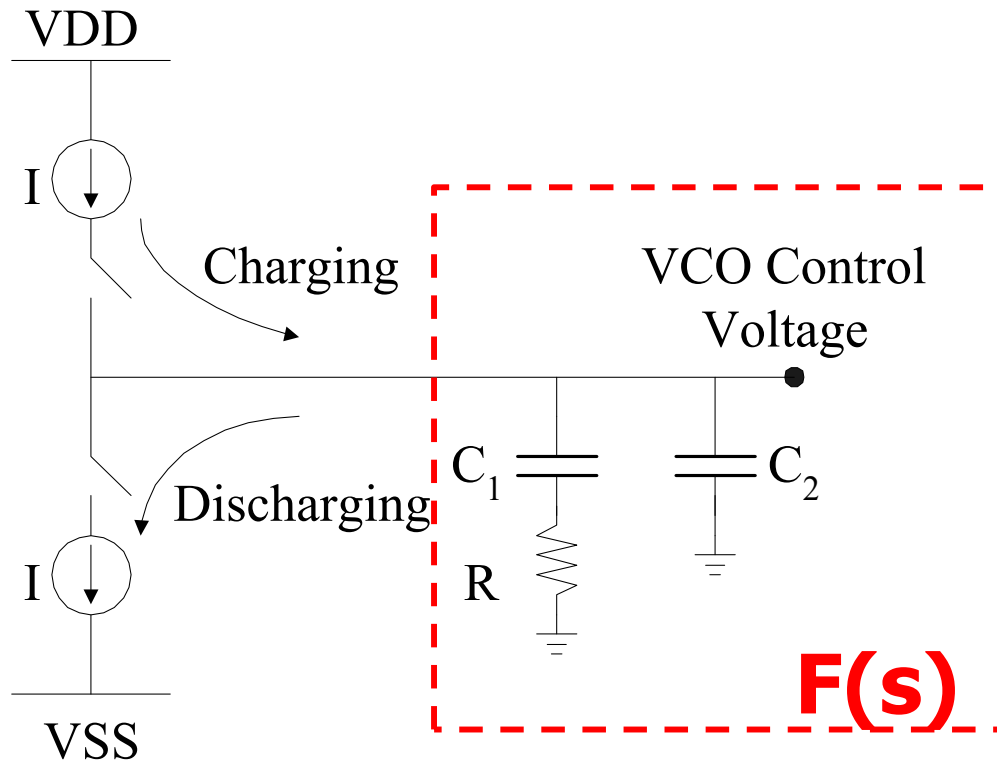


Normalized Phase Step Response



- A larger K_{DC} provide a more stable system and wider loop bandwidth

Typical Charge-Pump PLL Loop Filter



$$\text{w/o } C_2$$

$$F(s) = \frac{R \left(s + \frac{1}{RC_1} \right)}{s}$$

$$\text{w/ } C_2$$

$$F(s) = \frac{\left(\frac{1}{C_2} \right) \left(s + \frac{1}{RC_1} \right)}{s \left(s + \frac{C_1 + C_2}{RC_1 C_2} \right)}$$

- A secondary capacitor C_2 is often added for additional filtering to reduce reference spurs
- This introduces an extra pole and potential stability concerns

Third-Order Type-2 PLL w/ Passive Series-RC Lag-Lead Filter & Additional Pole

$$F(s) = \frac{\left(\frac{1}{C_2}\right)\left(s + \frac{1}{RC_1}\right)}{s\left(s + \frac{C_1 + C_2}{RC_1C_2}\right)}$$

Define a loop gain factor $K = \frac{K_{PD}K_{VCO}R}{N}$

$$\text{Forward Path Gain : } G(s) = \frac{K_{PD}K_{VCO}\left(\frac{1}{C_2}\right)\left(s + \frac{1}{RC_1}\right)}{s^2\left(s + \frac{C_1 + C_2}{RC_1C_2}\right)} = \frac{NK\left(s + \frac{1}{RC_1}\right)}{RC_2s^2\left(s + \frac{C_1 + C_2}{RC_1C_2}\right)}$$

$$\text{Transfer Function : } H(s) = \frac{K_{PD}K_{VCO}\left(\frac{1}{C_2}\right)\left(s + \frac{1}{RC_1}\right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1C_2}\right)s^2 + \left(\frac{K_{PD}K_{VCO}}{NC_2}\right)s + \frac{K_{PD}K_{VCO}}{NRC_1C_2}} = \frac{NK\left(s + \frac{1}{RC_1}\right)}{RC_2s^3 + \left(\frac{C_1 + C_2}{C_1}\right)s^2 + Ks + \frac{K}{RC_1}}$$

$$\text{Error Function : } E(s) = \frac{s^2\left(s + \frac{C_1 + C_2}{RC_1C_2}\right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1C_2}\right)s^2 + \left(\frac{K_{PD}K_{VCO}}{NC_2}\right)s + \frac{K_{PD}K_{VCO}}{NRC_1C_2}} = \frac{RC_2s^2\left(s + \frac{C_1 + C_2}{RC_1C_2}\right)}{RC_2s^3 + \left(\frac{C_1 + C_2}{C_1}\right)s^2 + Ks + \frac{K}{RC_1}}$$

If the third - pole is at a high frequency, can approximate as a second - order system with

$$\text{Natural Frequency : } \omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{NC_1}} = \sqrt{\frac{K}{RC_1}}$$

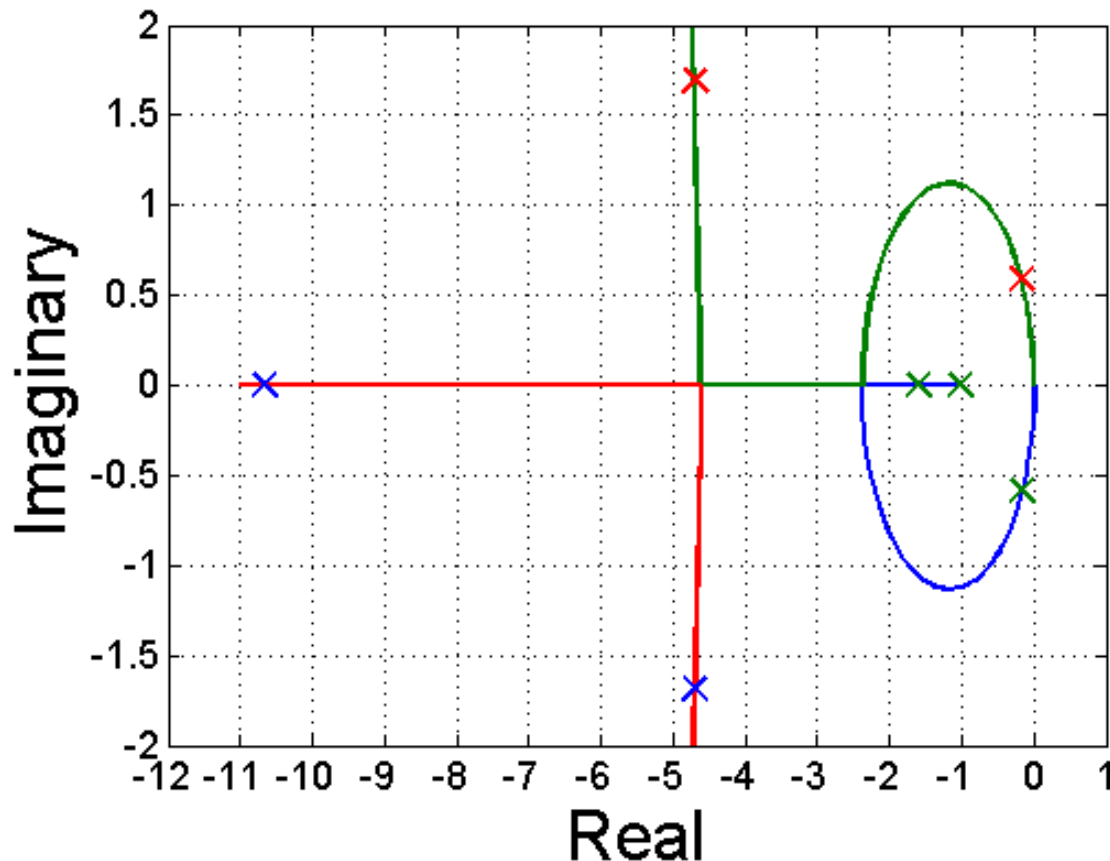
$$\text{Damping Factor : } \zeta = \frac{\omega_n}{2} RC_1 = \frac{1}{2} \sqrt{KRC_1}$$

Third-Order Type-2 PLL w/ Passive Series-RC Lag-Lead Filter & Additional Pole Root Locus

$$\text{Open-Loop: } \frac{G(s)}{N} = \frac{K \left(s + \frac{1}{RC_1} \right)}{RC_2 s^2 \left(s + \frac{C_1 + C_2}{RC_1 C_2} \right)}$$

$$\text{Closed-Loop: } H(s) = \frac{NK \left(s + \frac{1}{RC_1} \right)}{RC_2 s^3 + \left(\frac{C_1 + C_2}{C_1} \right) s^2 + Ks + \frac{K}{RC_1}}$$

$$R=1, C_1=1, C_2=0.1$$



- Initial pole values with zero loop gain are the open-loop poles

$$p_1 = 0 \quad p_2 = 0 \quad p_3 = -\frac{C_1 + C_2}{RC_1 C_2} = -11$$

- Final pole values with infinite loop gain

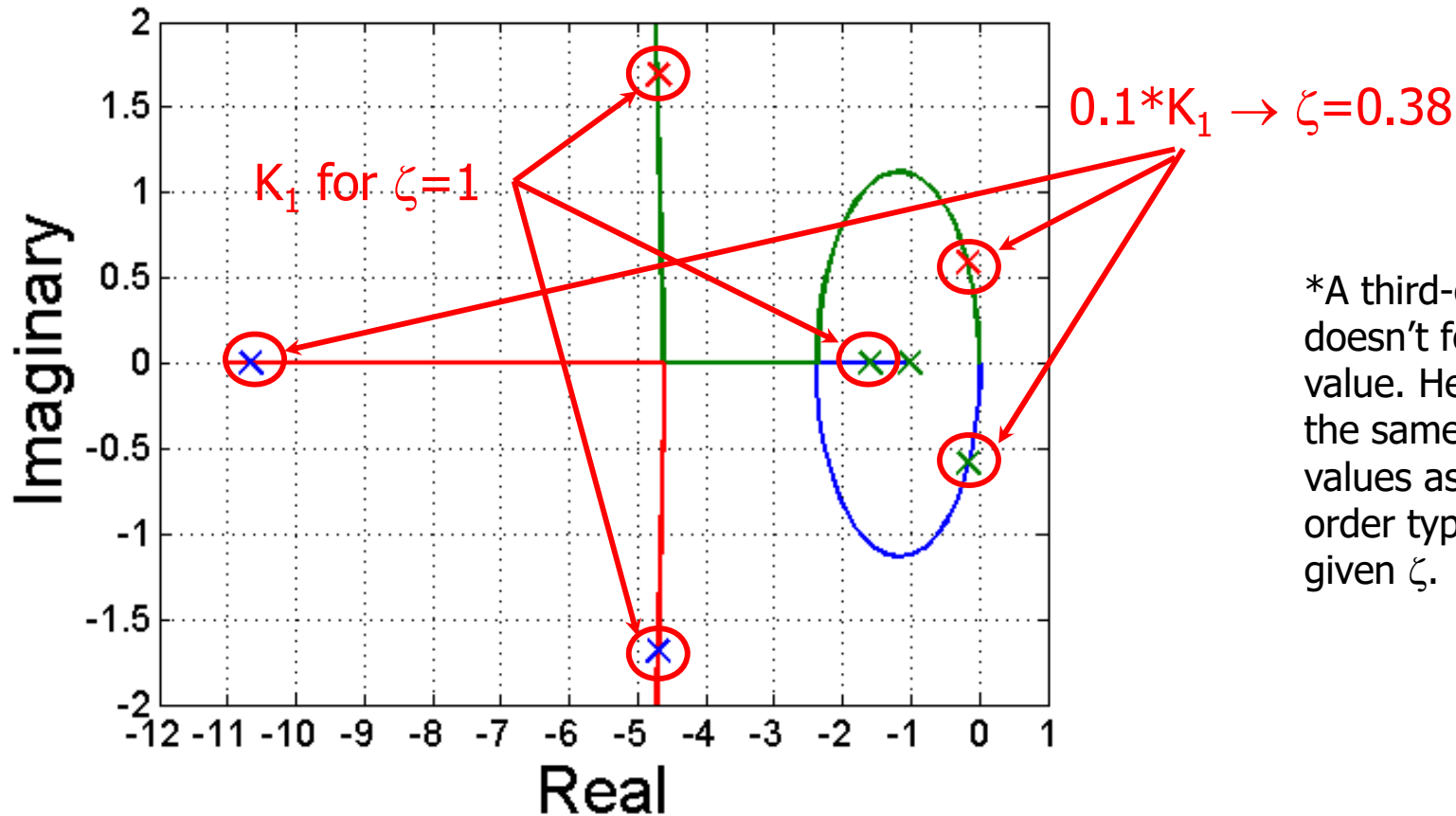
$$p_1 = -\frac{1}{RC} = -1 \quad p_{2,3} = -5 \pm j\infty$$

Third-Order Type-2 PLL w/ Passive Series-RC Lag-Lead Filter & Additional Pole Root Locus

$$\text{Open-Loop: } \frac{G(s)}{N} = \frac{K \left(s + \frac{1}{RC_1} \right)}{RC_2 s^2 \left(s + \frac{C_1 + C_2}{RC_1 C_2} \right)}$$

$$\text{Closed-Loop: } H(s) = \frac{NK \left(s + \frac{1}{RC_1} \right)}{RC_2 s^3 + \left(\frac{C_1 + C_2}{C_1} \right) s^2 + Ks + \frac{K}{RC_1}}$$

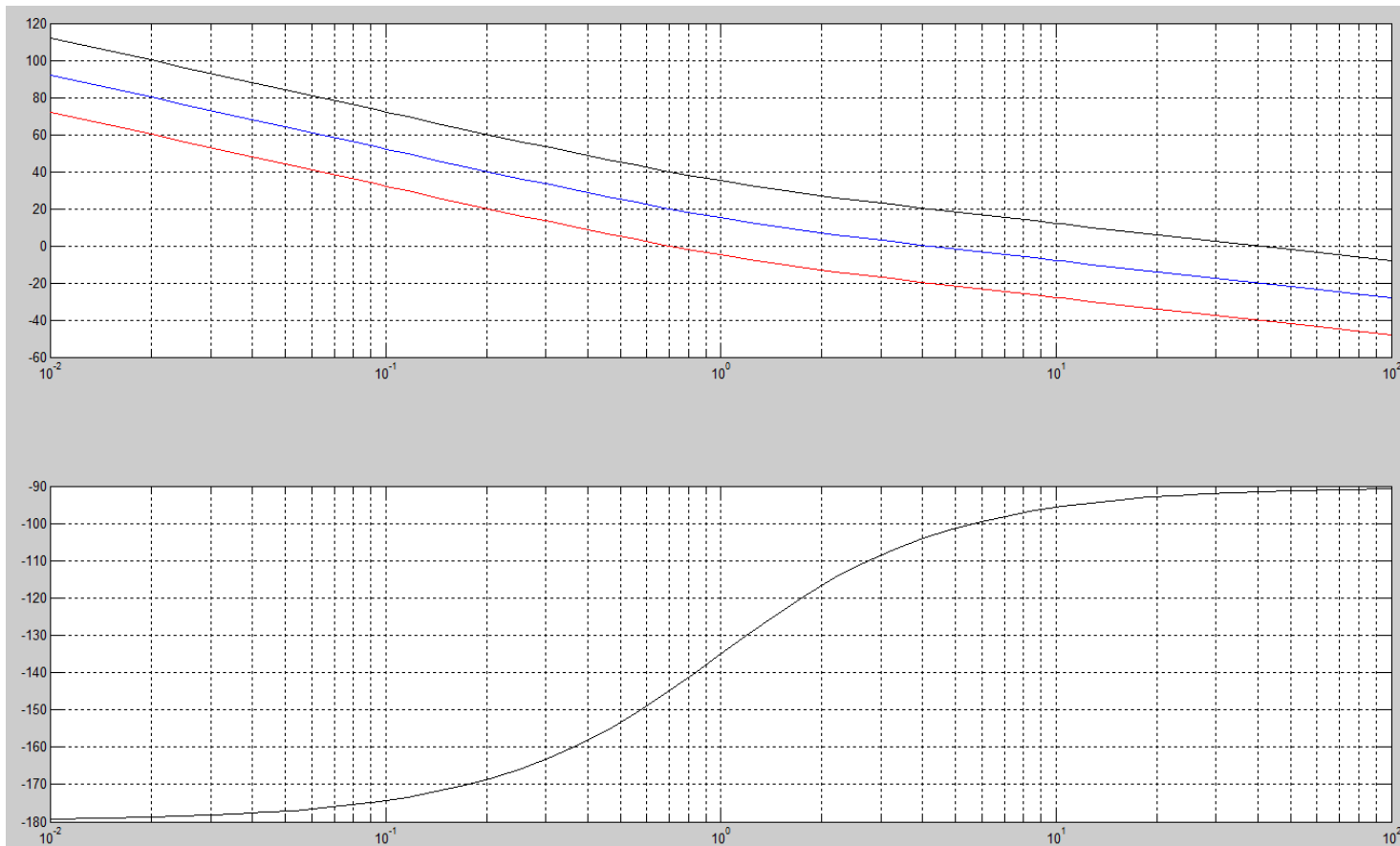
$$R=1, C_1=1, C_2=0.1$$



*A third-order system doesn't formally have a ζ value. Here we are using the same loop parameter values as the second-order type-2 PLL for a given ζ .

Second-Order Type-2 PLL w/ Passive Series-RC Lag-Lead Filter Stability

$20\log_{10}\left|\frac{G(j\omega)}{N}\right|$ (dB)



$$G(s) = \frac{NK\left(s + \frac{1}{RC}\right)}{s^2}$$

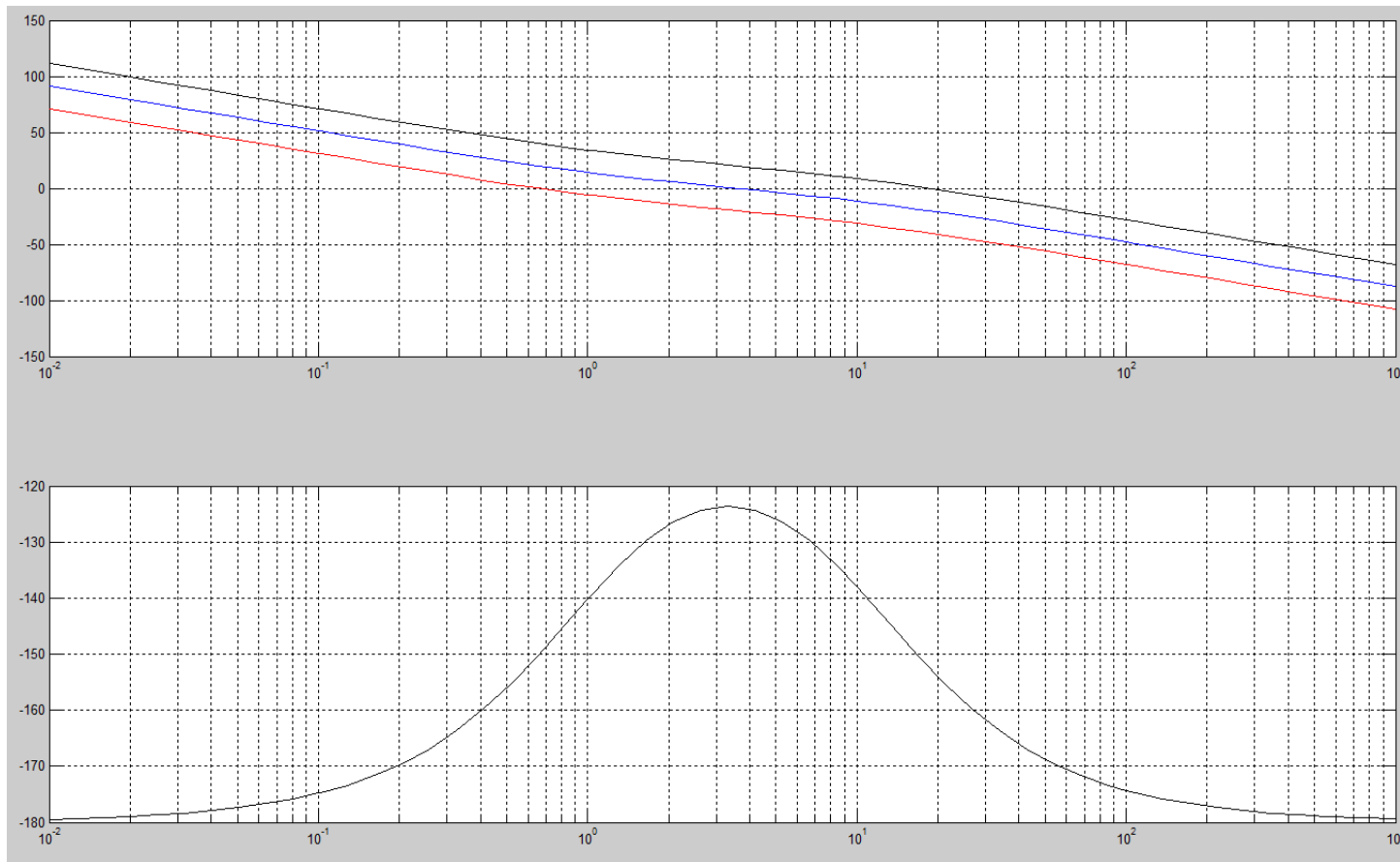
Normalizing K
for $\zeta=1$

Norm. K	Zeta	PM
0.1	0.38	35
1	1	76.2
10	3.09	88.6

- A larger K provide a more stable system

Third-Order Type-2 PLL w/ Passive Series-RC Lag-Lead Filter & Additional Pole Stability

$20\log_{10}\left|\frac{G(j\omega)}{N}\right|$ (dB)



$$G(s) = \frac{NK \left(s + \frac{1}{RC_1} \right)}{RC_2 s^2 \left(s + \frac{C_1 + C_2}{RC_1 C_2} \right)}$$

Normalizing K
for $\zeta=1$

Norm. K	Zeta*	PM
0.1	0.38	30
1	1	55
10	3.09	27

*A third-order system doesn't formally have a ζ value. Here we are using the same loop parameter values as the second-order type-2 PLL for a given ζ .

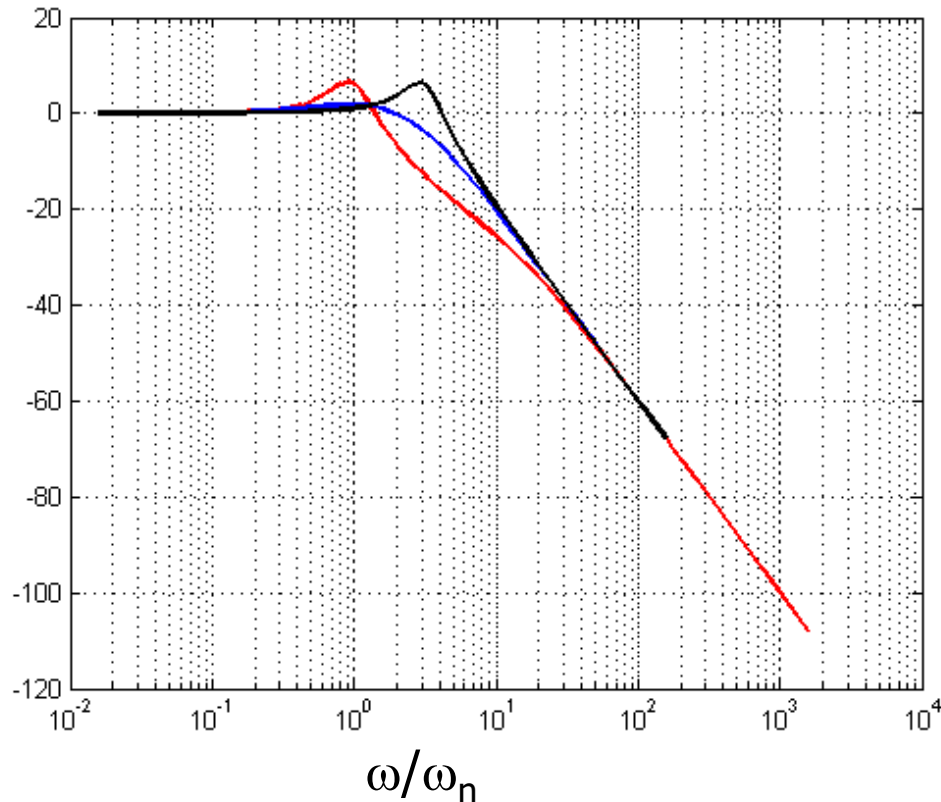
- A larger K may not provide a more stable system

Third-Order Type-2 PLL Closed-Loop Response

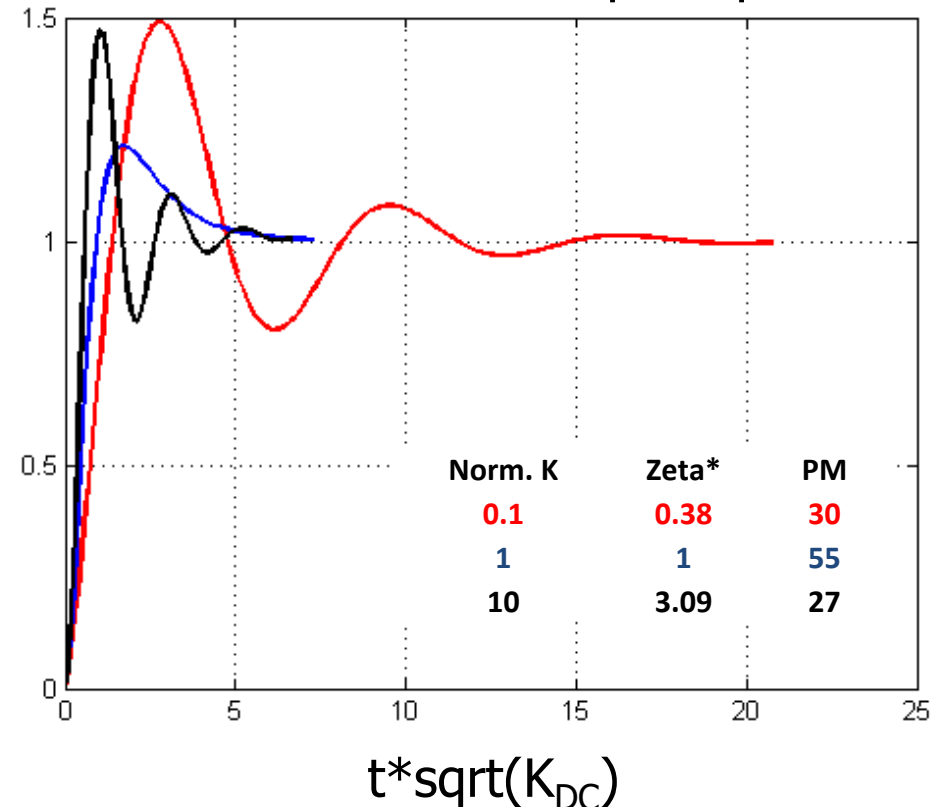
$$\text{Open-Loop: } \frac{G(s)}{N} = \frac{K \left(s + \frac{1}{RC_1} \right)}{RC_2 s^2 \left(s + \frac{C_1 + C_2}{RC_1 C_2} \right)}$$

$$\text{Closed-Loop: } H(s) = \frac{NK \left(s + \frac{1}{RC_1} \right)}{RC_2 s^3 + \left(\frac{C_1 + C_2}{C_1} \right) s^2 + Ks + \frac{K}{RC_1}}$$

$20 \cdot \log_{10} |H(j\omega)|$



Normalized Phase Step Response



- If K is increased too high frequency peaking and transient ringing occurs!

Instability and the Nyquist Criterion

[Karsilayan]

Transfer function of a 3-pole amplifier:

$$a(s) = \frac{a_o}{\left(1 - \frac{s}{p_1}\right) \left(1 - \frac{s}{p_2}\right) \left(1 - \frac{s}{p_3}\right)}$$

Nyquist criterion for stability of the amplifier:

Consider a feedback amplifier with a stable $\mathbf{T}(s)$. If the Nyquist plot of $\mathbf{T}(j\omega)$ encircles the point $(-1,0)$, the feedback amplifier is unstable.

For a PLL $T(s)$ is the forward gain $G(s)$ multiplied by the feedback factor $\frac{1}{N}$

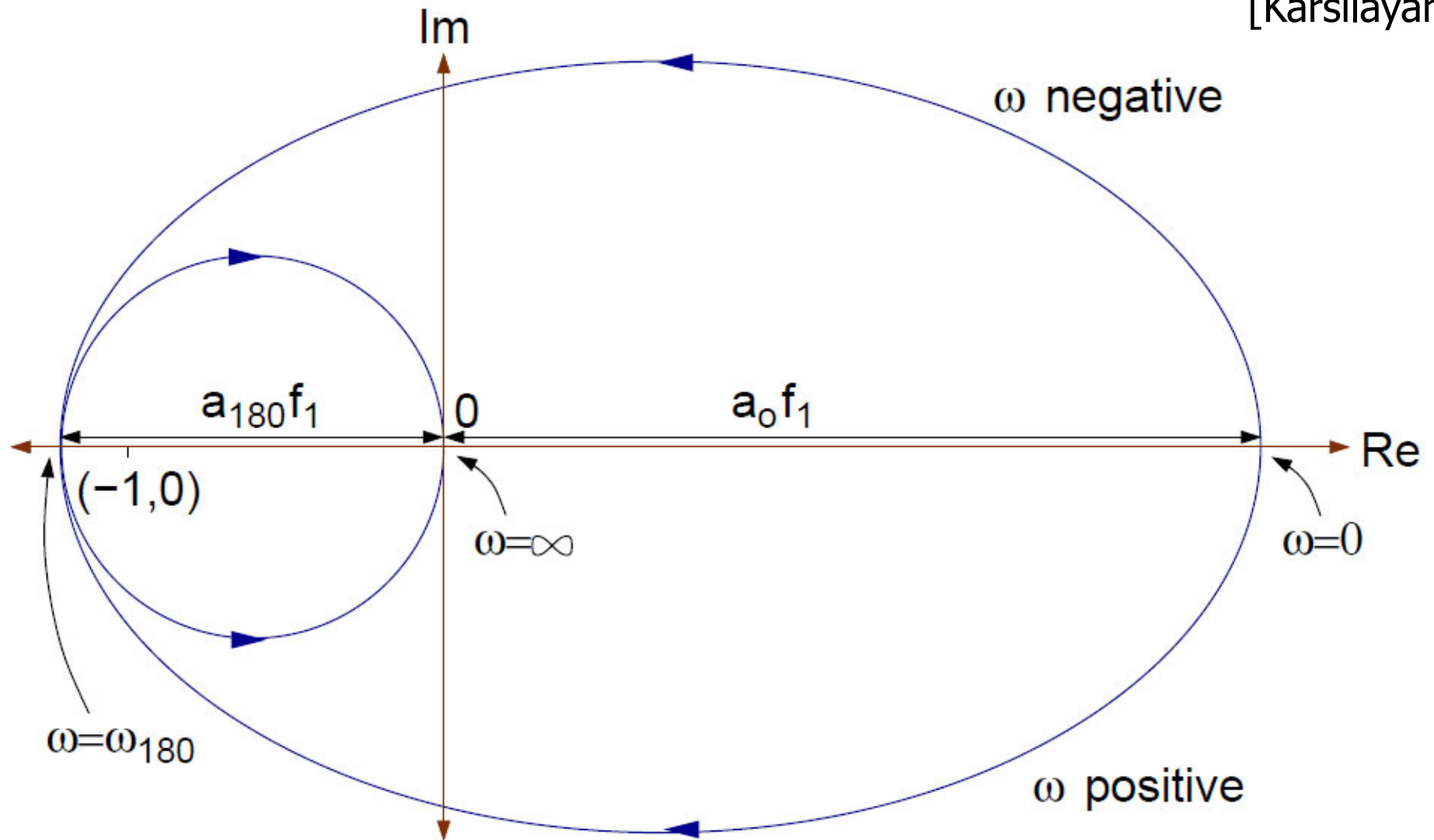
$$T(s) = \frac{G(s)}{N}$$

Nyquist Plot

For a PLL : $T(s) = \frac{G(s)}{N}$

Frequency Sweep of Loop Gain, $T(s)$

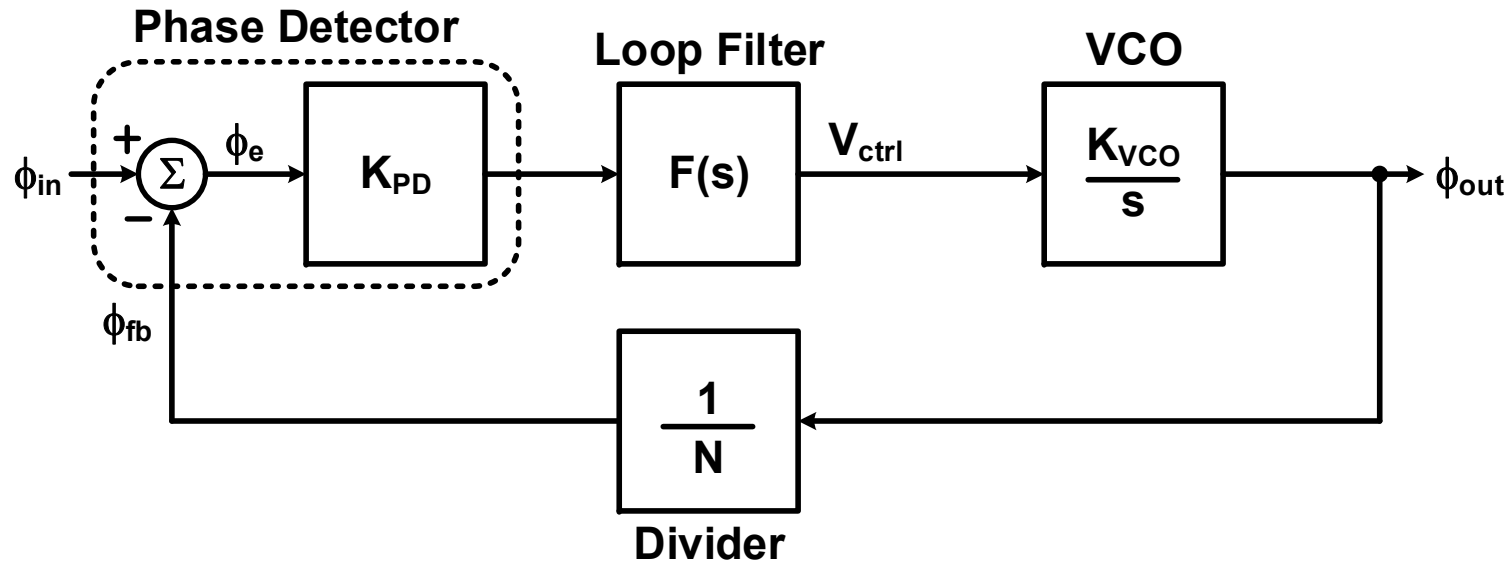
[Karsilayan]



Agenda

- PLL Overview
- PLL Linear Model
- PLL Stability
- Analog Charge Pump PLL Design Procedure
- PLL Noise Transfer Functions
- PLL Transient Behavior
- PLL Time Domain Modeling

Linear PLL Model



For Charge Pump PLL:

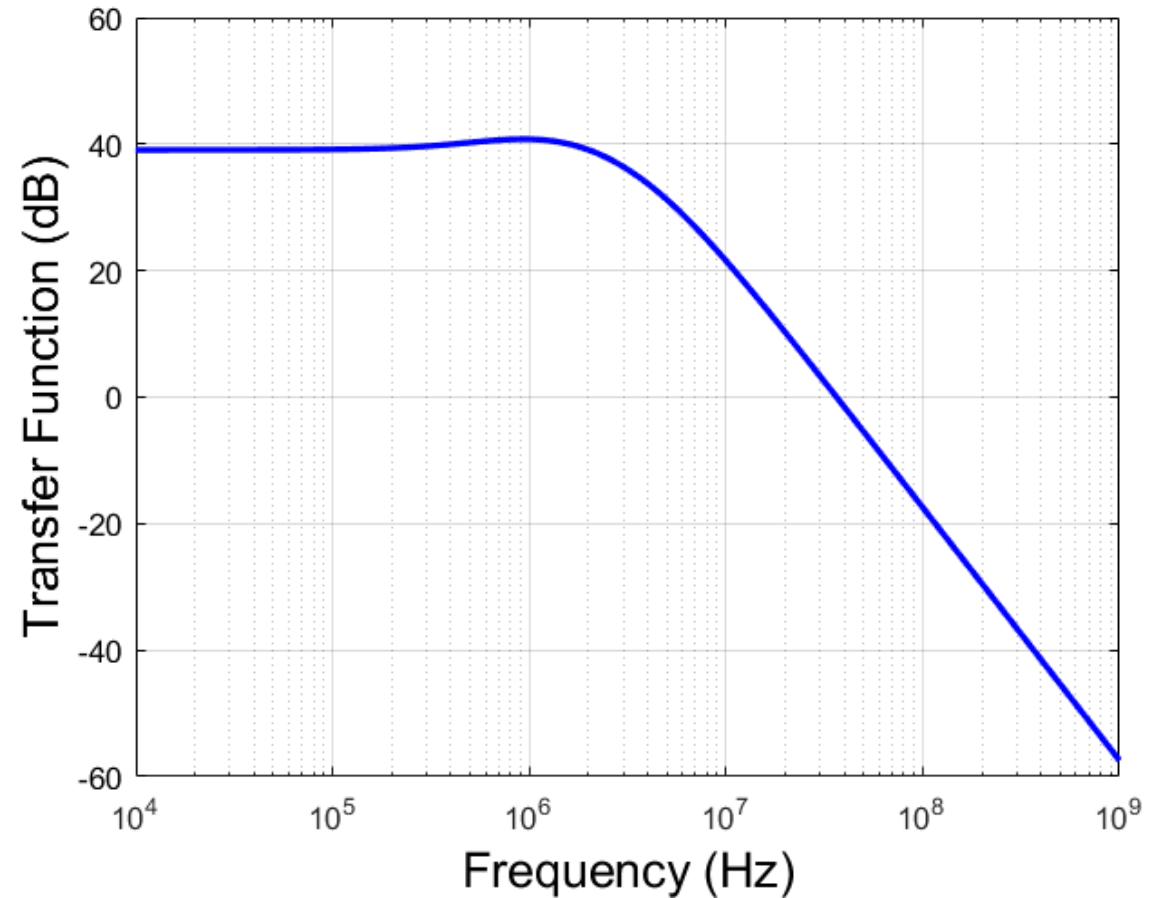
$$K_{PD} = \frac{I_{CP}}{2\pi}$$

$$F(s) = \frac{\left(\frac{1}{C_2}\right) \left(s + \frac{1}{RC_1}\right)}{s \left(s + \frac{C_1 + C_2}{RC_1 C_2}\right)}$$

$$H(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{\frac{K_{PD} K_{VCO}}{C_2} \left(s + \frac{1}{RC_1}\right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1 C_2}\right) s^2 + \left(\frac{K_{PD} K_{VCO}}{NC_2}\right) s + \frac{K_{PD} K_{VCO}}{NRC_1 C_2}}$$

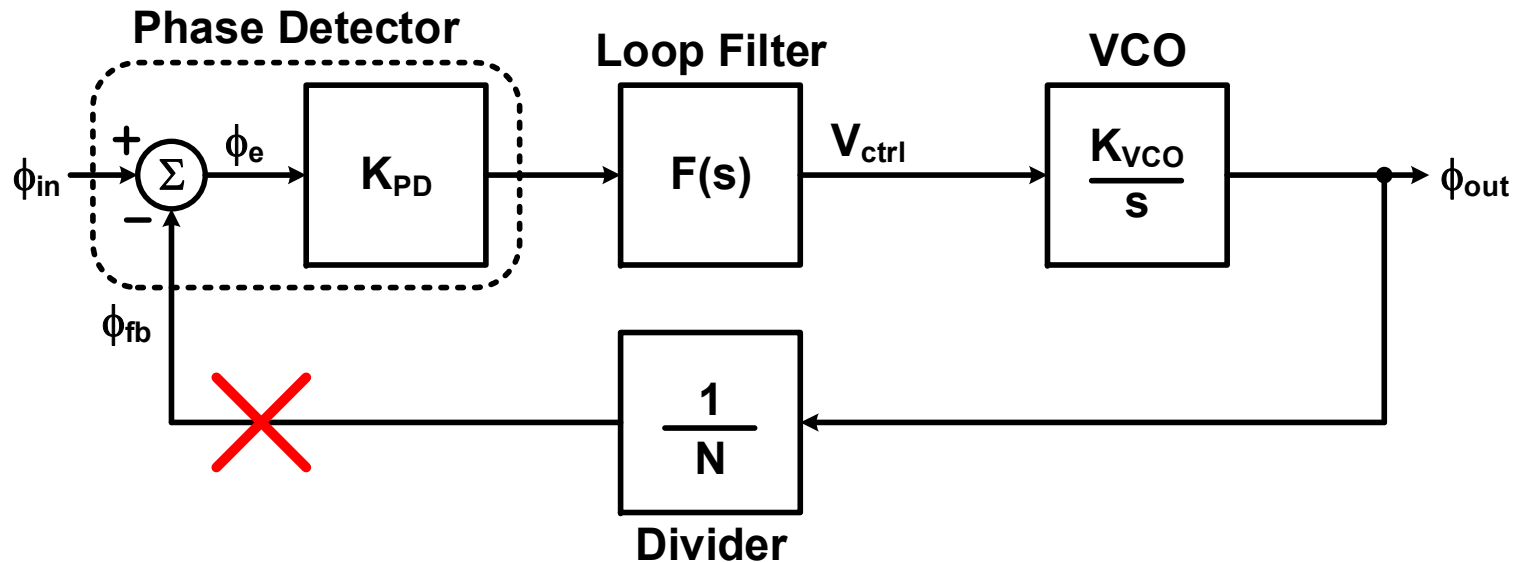
14GHz PLL Closed-Loop Transfer Function

Parameter	
Fref	156.25MHz
N	90
Fvco	14GHz
f _u	2MHz
Φ _m	60°
f _{3dB}	3.1MHz
Kvco	2π*1GHz/V
R	4kΩ
C ₁	74pF
C ₂	5.8pF
I _{cp}	310uA



$$H(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{\frac{K_{PD}K_{VCO}}{C_2} \left(s + \frac{1}{RC_1} \right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1C_2} \right) s^2 + \left(\frac{K_{PD}K_{VCO}}{NC_2} \right) s + \frac{K_{PD}K_{VCO}}{NRC_1C_2}}$$

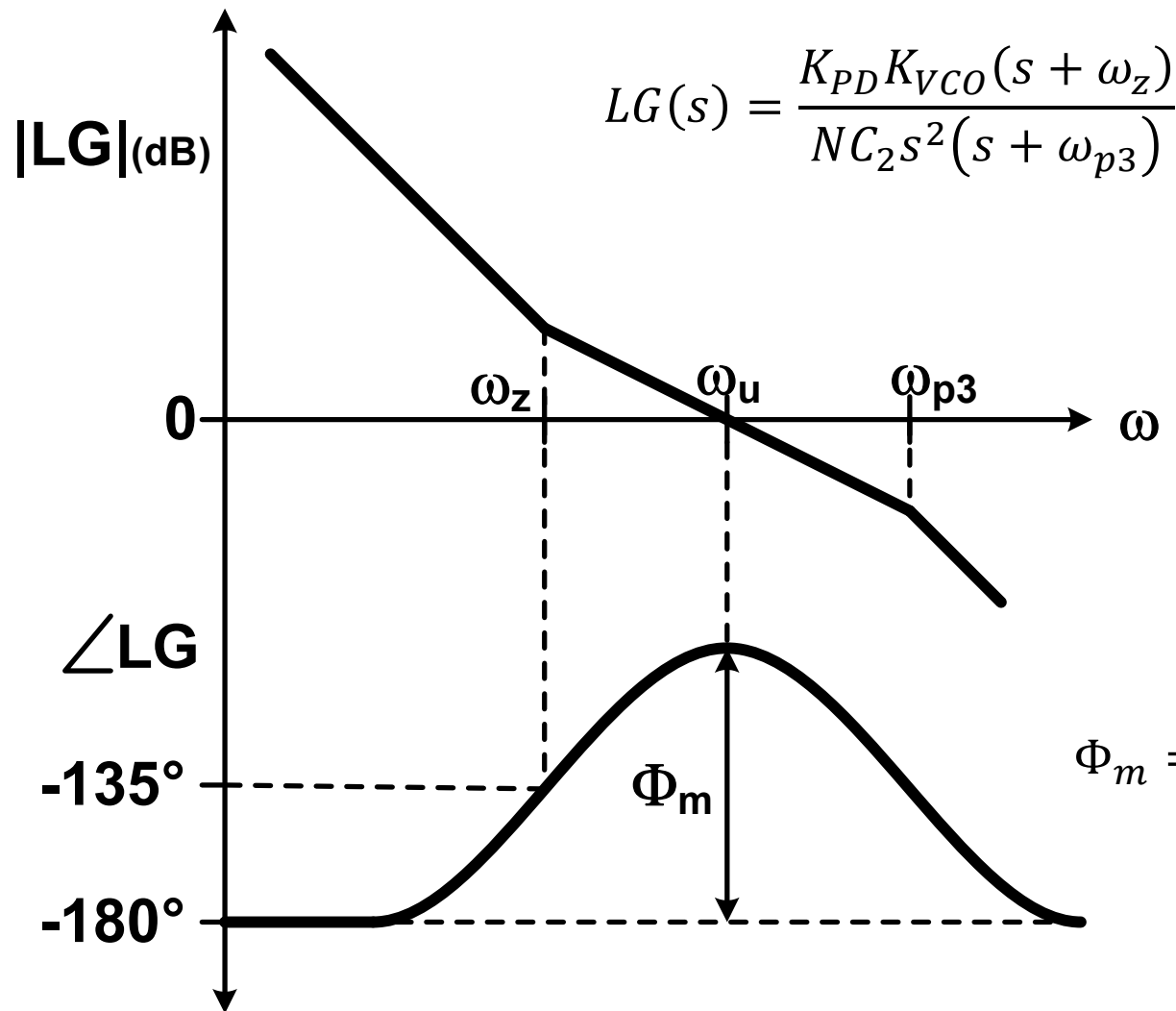
PLL Loop Gain



$$LG(s) = \frac{K_{PD}F(s)K_{VCO}}{Ns} = \frac{K_{PD}K_{VCO} \left(s + \frac{1}{R_1C_1} \right)}{NC_2s^2 \left(s + \frac{C_1 + C_2}{R_1C_1C_2} \right)}$$

$$\omega_z = \frac{1}{R_1C_1}, \quad \omega_{p1} = \omega_{p2} = 0, \quad \omega_{p3} = \frac{C_1 + C_2}{R_1C_1C_2}$$

Loop Gain Response



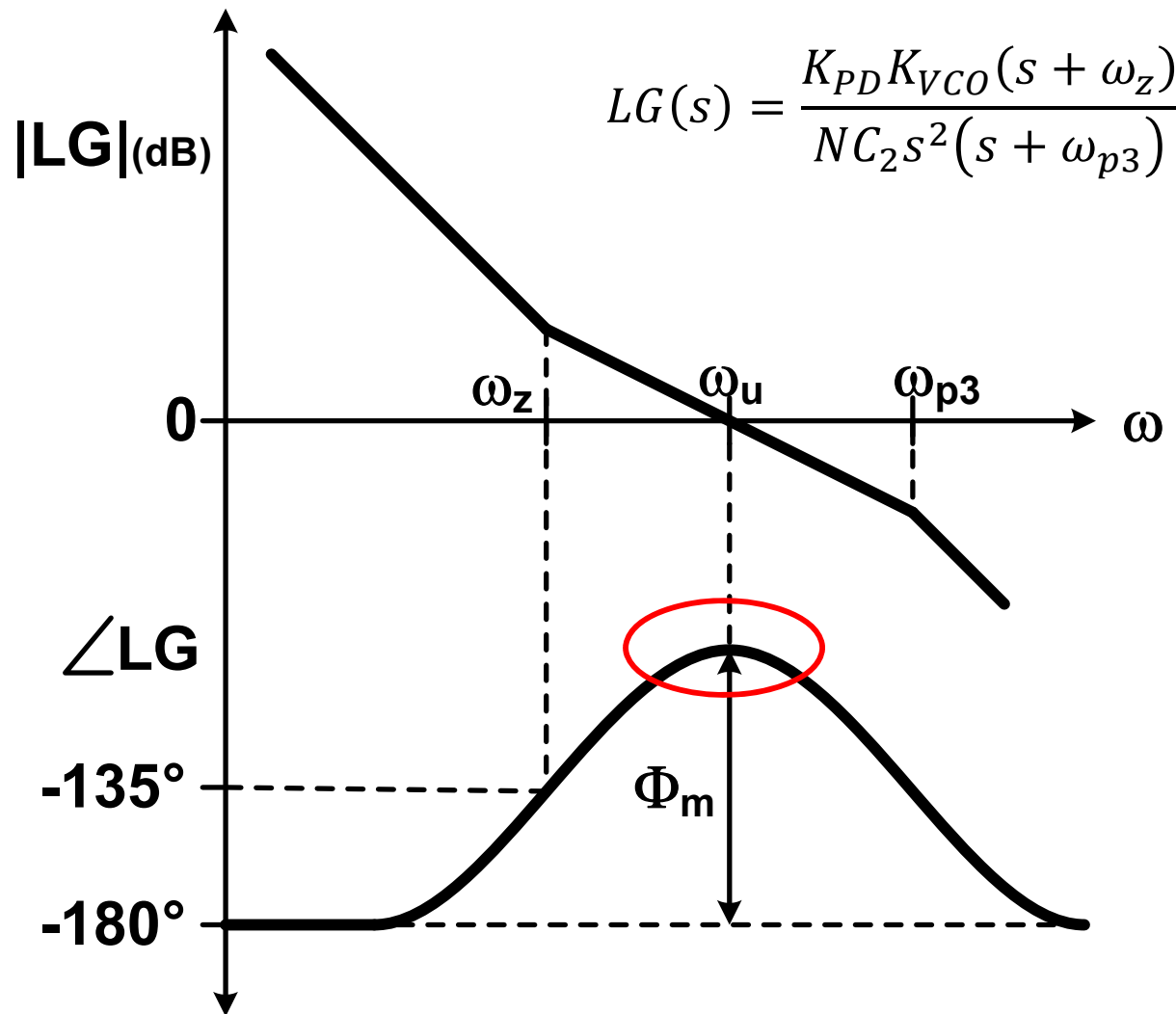
$$\omega_{p1} = \omega_{p2} = 0$$

$$\omega_z = \frac{1}{R_1 C_1}$$

$$\omega_{p3} = \frac{C_1 + C_2}{R_1 C_1 C_2}$$

$$\Phi_m = \tan^{-1} \left(\frac{\omega_u}{\omega_z} \right) - \tan^{-1} \left(\frac{\omega_u}{\omega_{p3}} \right)$$

Design Procedure for Max Φ_m



PLL Specs

Parameter	
Fref	156.25MHz
N	90
Fvco	14GHz
f_u	2MHz
Φ_m	60°
Kvco	2π*1GHz/V
R	??
C ₁	??
C ₂	??
I _{cp}	??

- Design procedure maximizes phase margin for a given f_u and Φ_m specification [Hanumolu TCAS1 2004]

Design Procedure for Max Φ_m

1. Set loop filter capacitor ratio based on Φ_m

$$K_C = \frac{C_1}{C_2} = 2 \left(\tan^2(\Phi_m) + \tan(\Phi_m) \sqrt{\tan^2(\Phi_m) + 1} \right)$$

$$\Phi_m = 60^\circ \rightarrow K_C = 12.9$$

2. Set loop filter values based on ω_u & with R set for low noise

$$\omega_z = \frac{\omega_u}{\sqrt{1 + K_C}}$$
$$C_1 = \frac{1}{\omega_z R}, \quad C_2 = \frac{C_1}{K_C}$$

$$\omega_u = 2\pi * 2MHz \rightarrow \omega_z = 2\pi * 536kHz$$

$$\text{Set } R = 4k\Omega \rightarrow C_1 = 74pF \quad \& \quad C_2 = 5.8pF$$

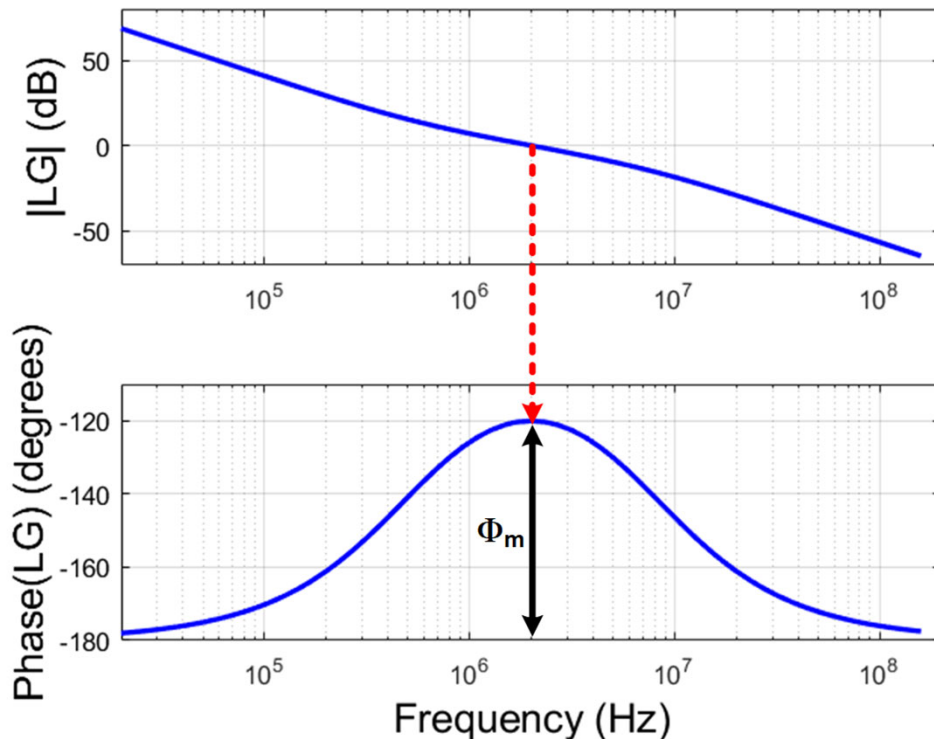
3. Set I_{cp} to achieve required loop gain

$$I_{cp} = \frac{NC_2\omega_u^2}{K_{VCO}} \sqrt{\frac{\omega_{p3}^2 + \omega_u^2}{\omega_z^2 + \omega_u^2}}$$

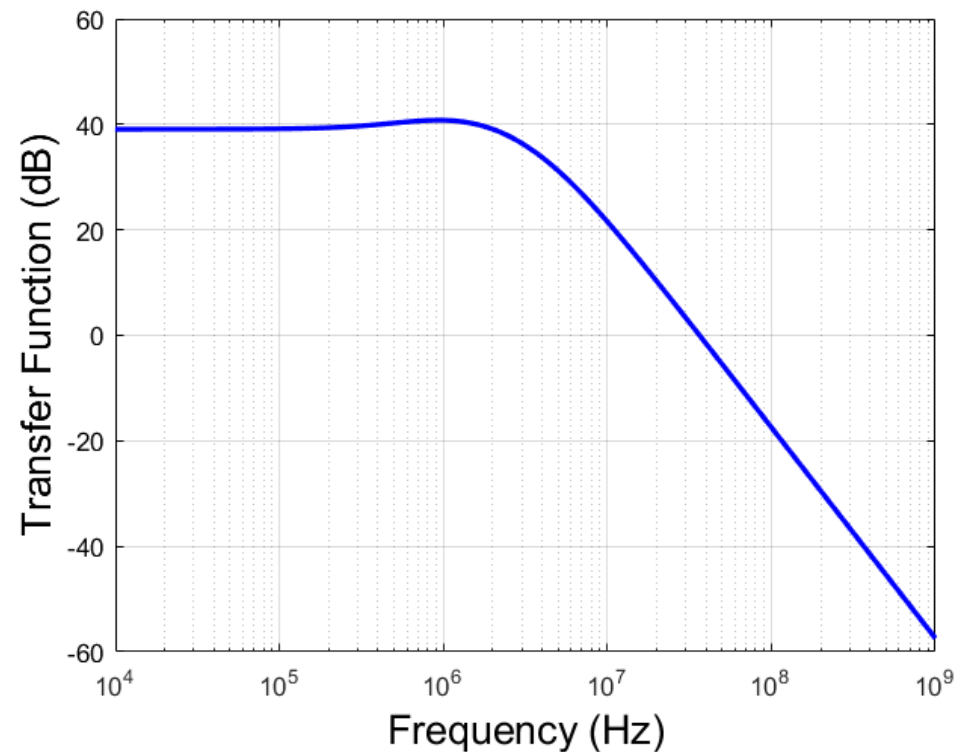
$$\omega_{p3} = 2\pi * 7.45MHz \rightarrow I_{cp} = 310\mu A$$

Simulated Responses

$$LG(s) = \frac{K_{PD}K_{VCO}(s + \omega_z)}{NC_2s^2(s + \omega_{p3})}$$



$$\frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{\frac{K_{PD}K_{VCO}}{C_2} \left(s + \frac{1}{RC_1} \right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1C_2} \right) s^2 + \left(\frac{K_{PD}K_{VCO}}{NC_2} \right) s + \frac{K_{PD}K_{VCO}}{NRC_1C_2}}$$

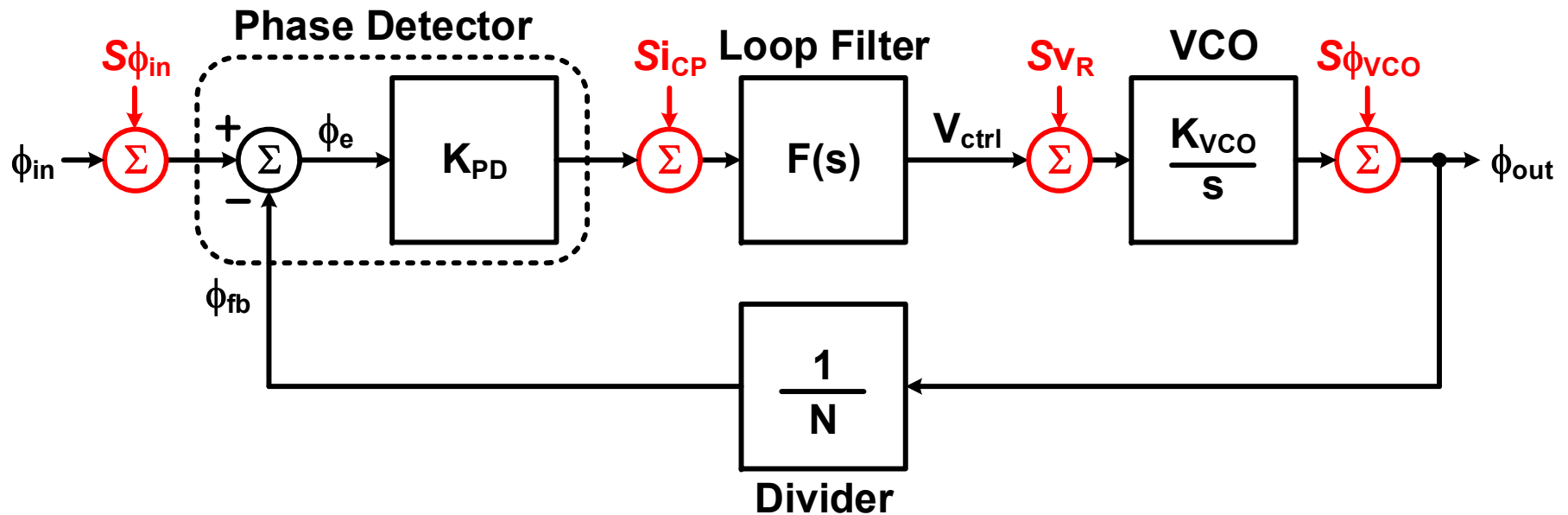


- Design achieves $f_u = 2\text{MHz}$ and $\Phi_m = 60^\circ$
- Closed loop response has $f_{3\text{dB}} = 3.1\text{MHz}$

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Common PLL Noise Sources



$$S_{\phi_{out}}^{\phi_{in}} = S_{\phi_{in}} |NTF_{IN}(s)|^2$$

$$S_{\phi_{out}}^{i_{CP}} = S_{i_{CP}} |NTF_{CP}(s)|^2$$

$$S_{\phi_{out}}^{v_R} = S_{v_R} |NTF_R(s)|^2$$

$$S_{\phi_{out}}^{\phi_{VCO}} = S_{\phi_{VCO}} |NTF_{VCO}(s)|^2$$

$$S_{\phi_{out}}^{Total} = S_{\phi_{out}}^{\phi_{in}} + S_{\phi_{out}}^{i_{CP}} + S_{\phi_{out}}^{v_R} + S_{\phi_{out}}^{\phi_{VCO}}$$

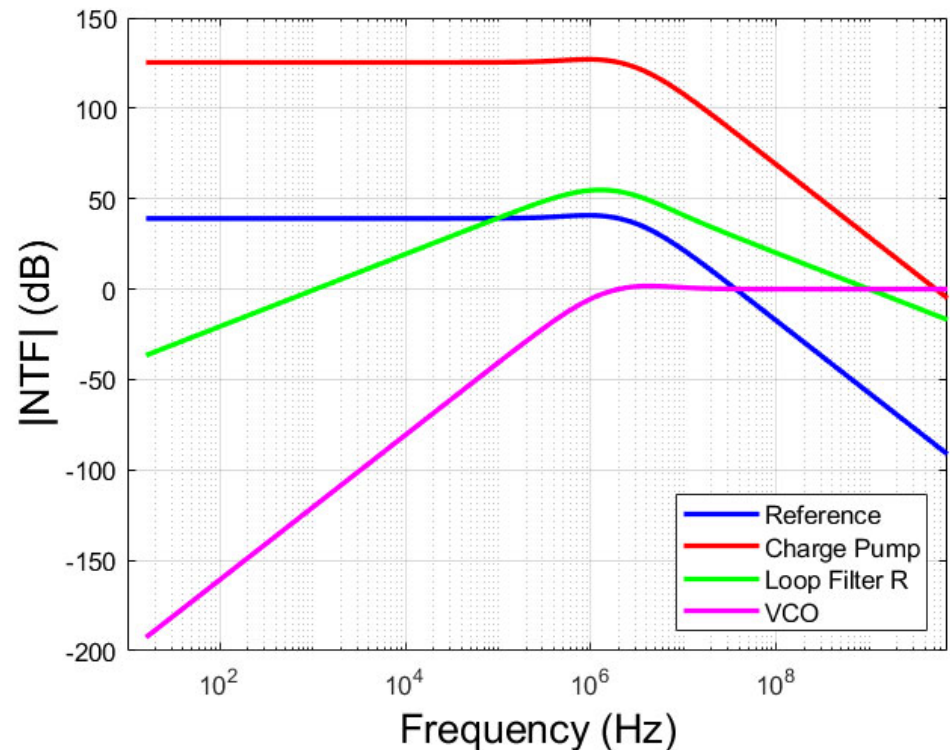
Noise Transfer Functions

$$NTF_{IN}(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{(N)LG(s)}{1 + LG(s)}$$

$$NTF_{CP}(s) = \frac{\phi_{out}(s)}{i_{CP}(s)} = \frac{\left(\frac{N}{K_{PD}}\right) LG(s)}{1 + LG(s)}$$

$$NTF_R(s) = \frac{\phi_{out}(s)}{v_R(s)} = \frac{\frac{K_{VCO}}{s}}{1 + LG(s)}$$

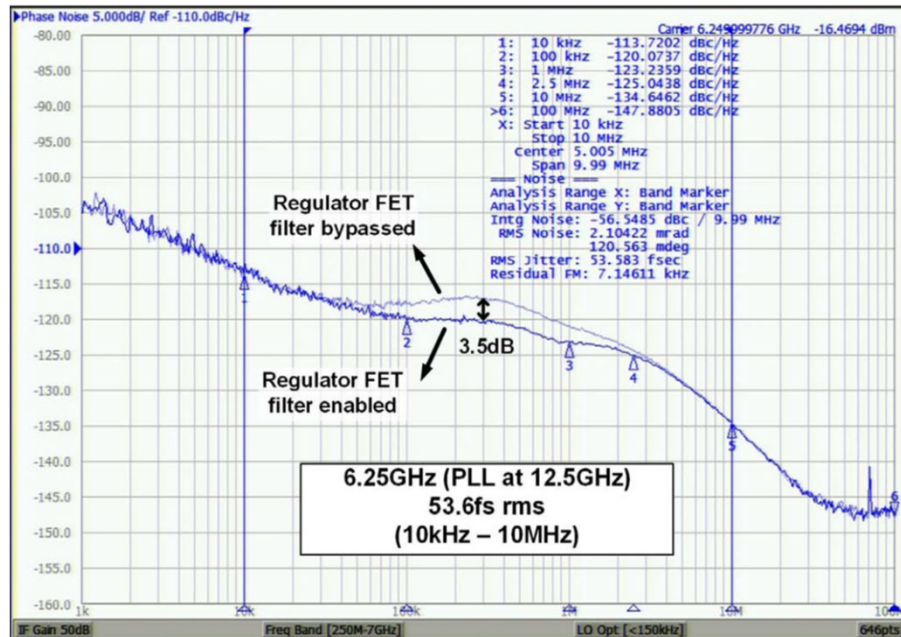
$$NTF_{VCO}(s) = \frac{\phi_{out}(s)}{\phi_{VCO}(s)} = \frac{1}{1 + LG(s)}$$



- Input reference and charge pump noise is low-pass filtered
- Loop filter noise (VCO input noise) is band-pass filtered
- VCO output phase noise is high-pass filtered

PLL Phase Noise & Jitter

[Turker ISSCC 2018]



	[3]	[4]	[5]	[6]	This Work
PLL Architecture	Integer N, SSPD based	FracN, SSPD DPLL	FracN, DPLL	Integer N, SPD based	Integer N, CP based
VCO	LC	LC	LC	LC	LC
Technology	180nm	28nm	14nm FinFET	16nm FinFET	16nm FinFET
Reference Freq (MHz)	55.25	40	26	450	500
Frequency Range (GHz)	2.21	2.7 - 4.3	5.38	9 - 18	7.4 - 14
Measurement Frequency (GHz)	2.21	5.82	2.69	18	6.25
Phase Noise @100kHz (dBc/Hz)	-125 (@200kHz)	-105.5	-113.6	-104.1 (@200kHz)	-120
Phase Noise @1MHz (dBc/Hz)	-125 (from figure)	-115.4	-122.45	-107.3	-123.2
Phase Noise @100kHz (normalized to 1GHz)	-131.9 (@200kHz)	-120.8	-122.2	-129.2 (@200kHz)	-135.9
Phase Noise @1MHz (normalized to 1GHz)	-131.9	-130.7	-131	-132.4	-139.1
RMS Jitter (fs)	160 (10k - 100M)	159 (10k - 40M)	137 (10k - 10M)	164 (1k - 100M)	53.6 (10k - 10M)
Reference Spur (dBc)	-56	-78	-87.6	N.A	-75.5 *
Power (mW)	2.5	8.2	13.4	29.2	45
Area (mm ²)	0.2	0.3	0.257	0.39	0.35
FOM _T (dB)	N.A	-243.4	N.A	-239.3	-246.8

* including DAC, measured at 1.052GHz DAC output

$$FOM_T = 10 \log \left(\left(\frac{\sigma_{rms}}{1s} \right)^2 \times \frac{P}{1mW} \times \frac{1}{TR} \right) \text{ where } TR = \left(\frac{f_{max} - f_{min}}{f_{mid}} \right)$$

- PLL time-domain jitter is obtained by integrating the output phase noise

$$\sigma_{j,Total}^2 = \frac{2}{\omega_0^2} \int_{f_{start}}^{f_{stop}} S_{\phi_{out}}^{Total}(f) df$$

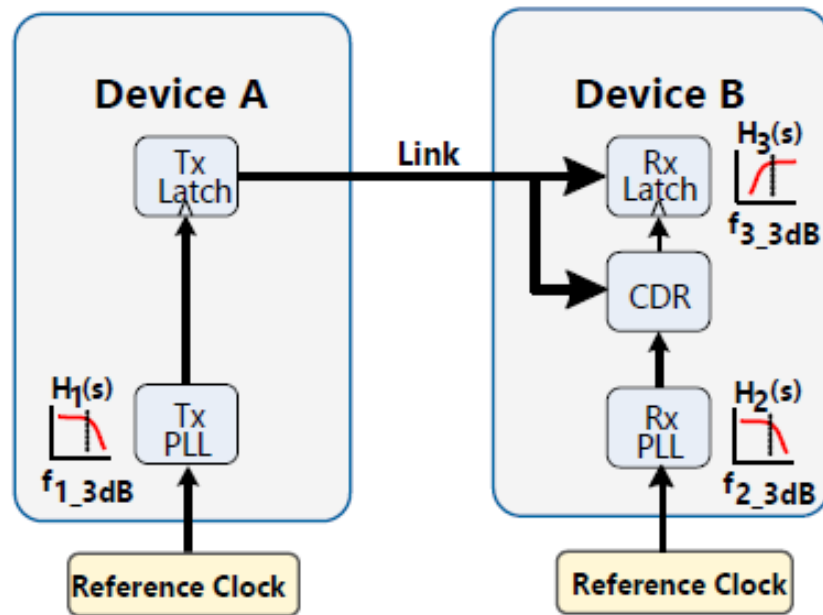
- We can model an individual noise source's contribution

$$\sigma_{j,i}^2 = \frac{2}{\omega_0^2} \int_{f_{start}}^{f_{stop}} S_i(f) |NTF_i(f)|^2 df$$

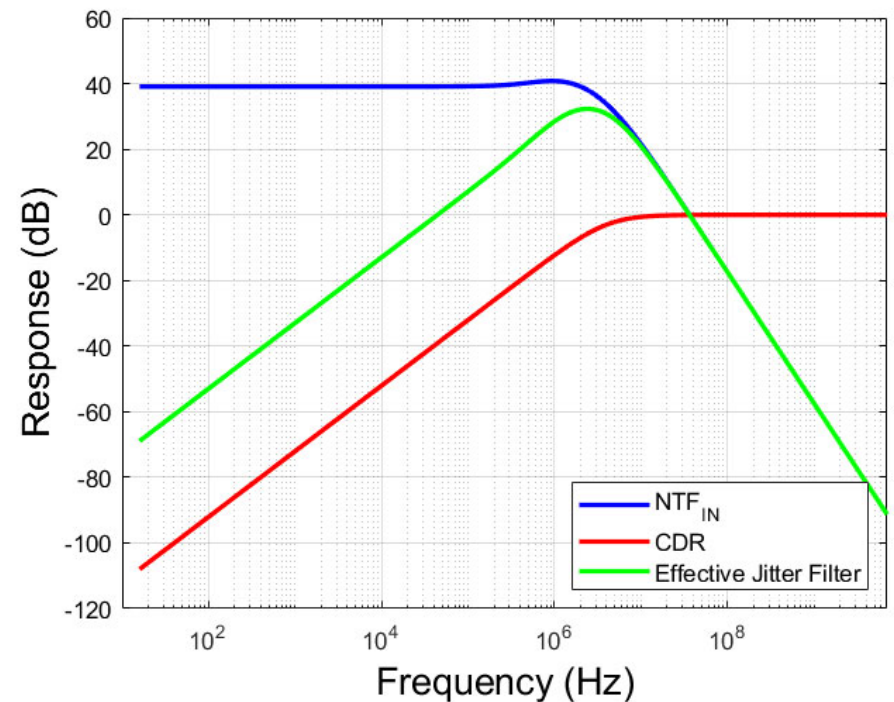
$$\sigma_{j,Total}^2 = \sum_i \sigma_{j,i}^2$$

$$\text{RMS Jitter } \sigma_j = \sqrt{\sigma_{j,Total}^2}$$

Wireline Transceiver Jitter Modeling



[Richmond SiLabs]



- Relative jitter (dynamic phase error) between the RX CDR-generated sampling clock and input data sets the system timing margin
- This CDR high-pass response provides additional filtering
- Modeled as a 4MHz 1st-order response (IEEE 802.3 & OIF-CEI)

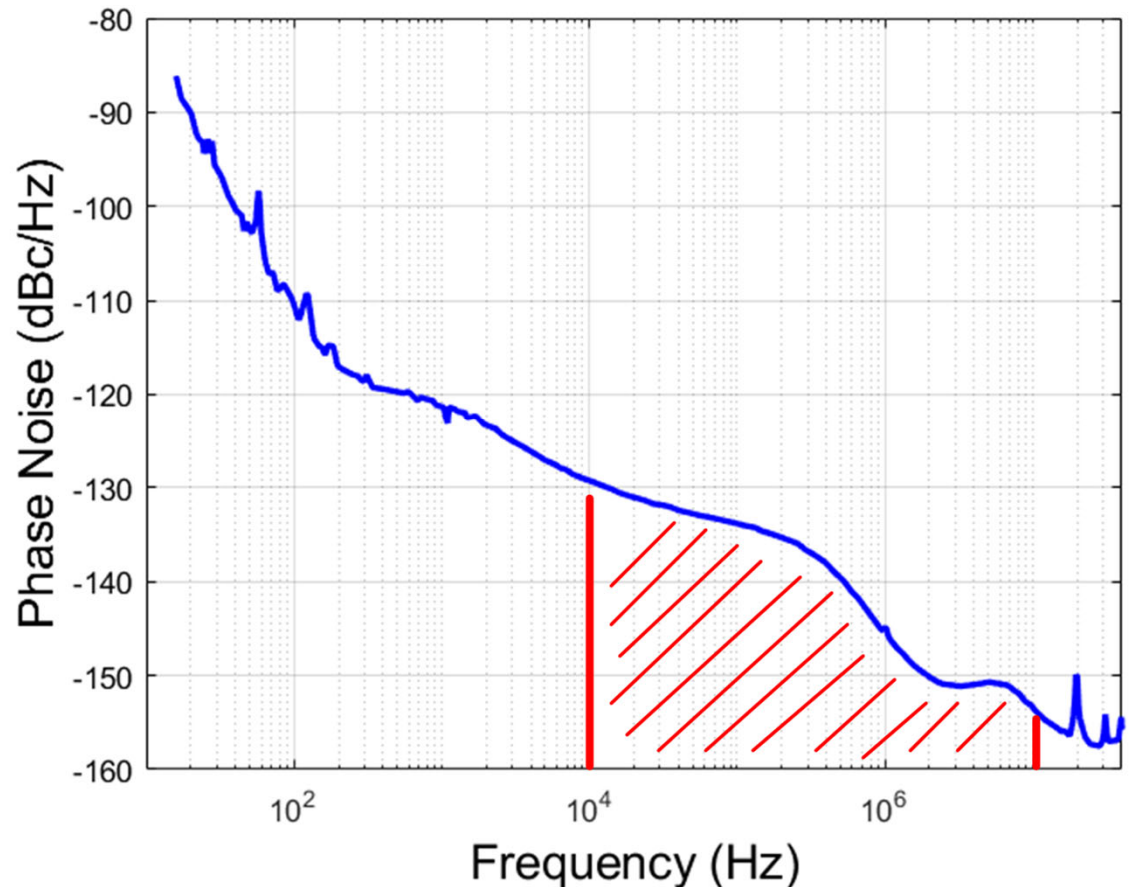
$$\sigma_{jSYS,i}^2 = \frac{2}{\omega_0^2} \int_0^{\frac{f_0}{2}} S_i(f) |NTF_i(f)|^2 |CDR(f)|^2 df$$

Input Reference Noise

Silicon Labs Ultra Low Jitter Crystal Oscillator



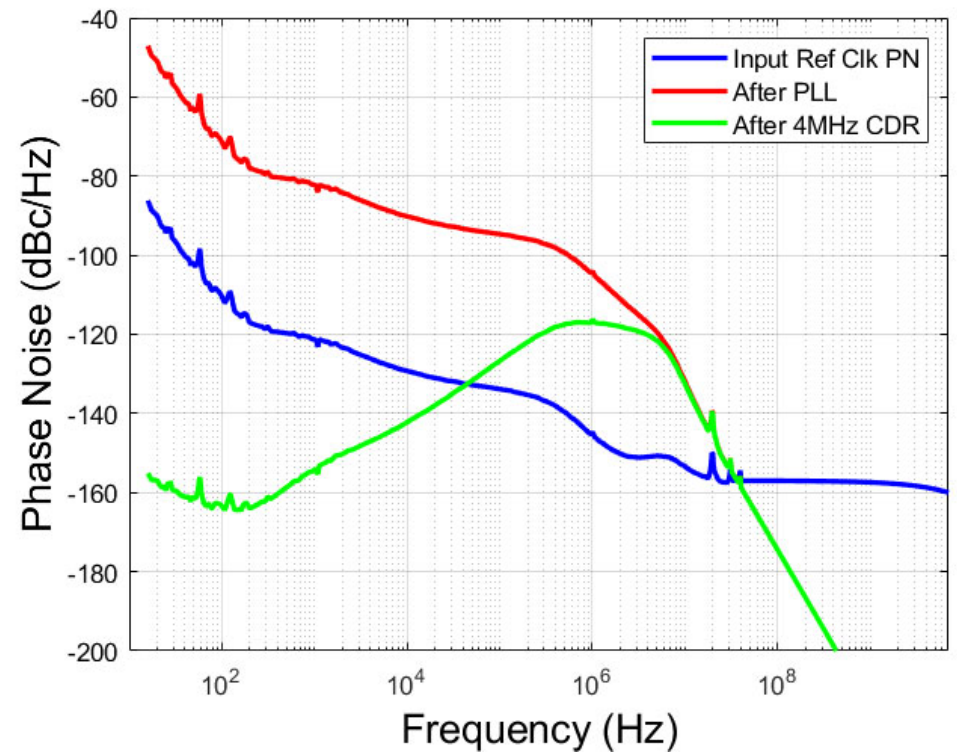
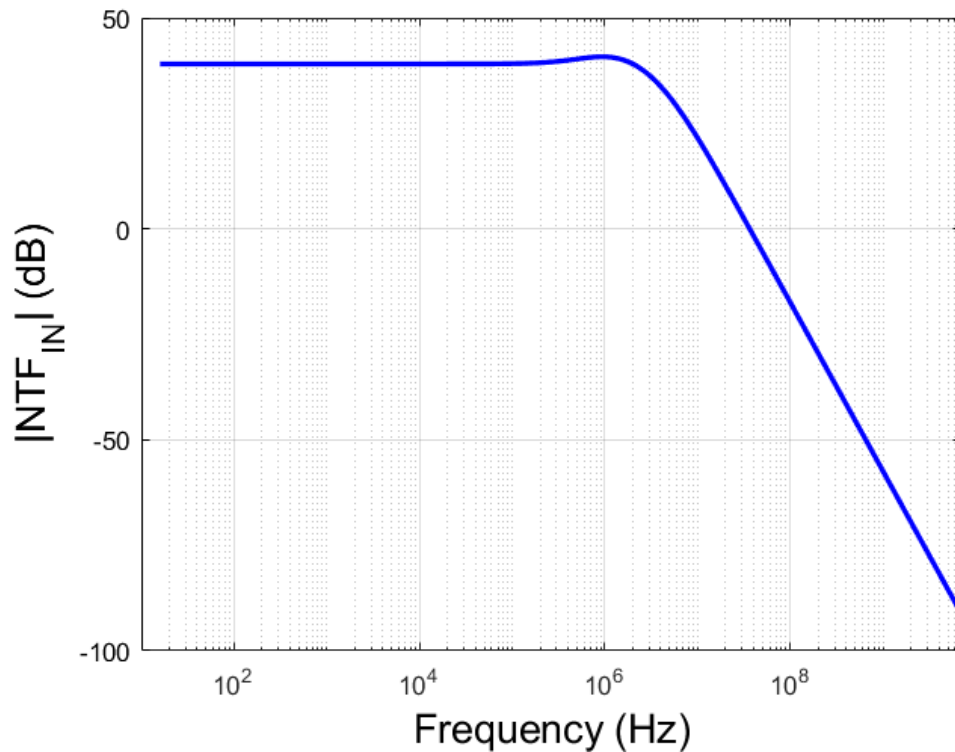
Phase Noise at 156.26MHz



- Reference jitter $\sigma_{j,in} = 226\text{fs}_{\text{rms}} (10\text{kHz} - 10\text{MHz})$

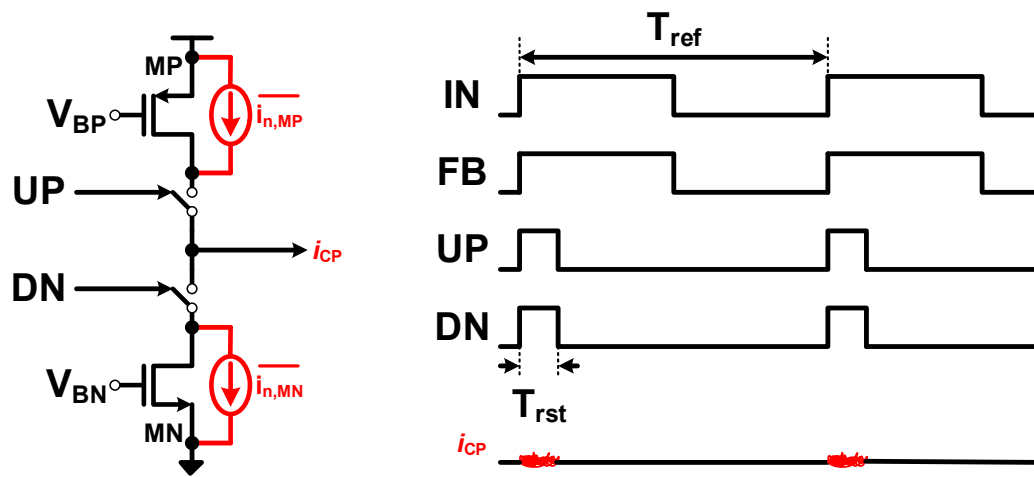
Input Reference Noise

$$NTF_{IN}(s) = \frac{\frac{K_{PD}K_{VCO}}{C_2} \left(s + \frac{1}{RC_1} \right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1C_2} \right) s^2 + \left(\frac{K_{PD}K_{VCO}}{NC_2} \right) s + \frac{K_{PD}K_{VCO}}{NRC_1C_2}}$$

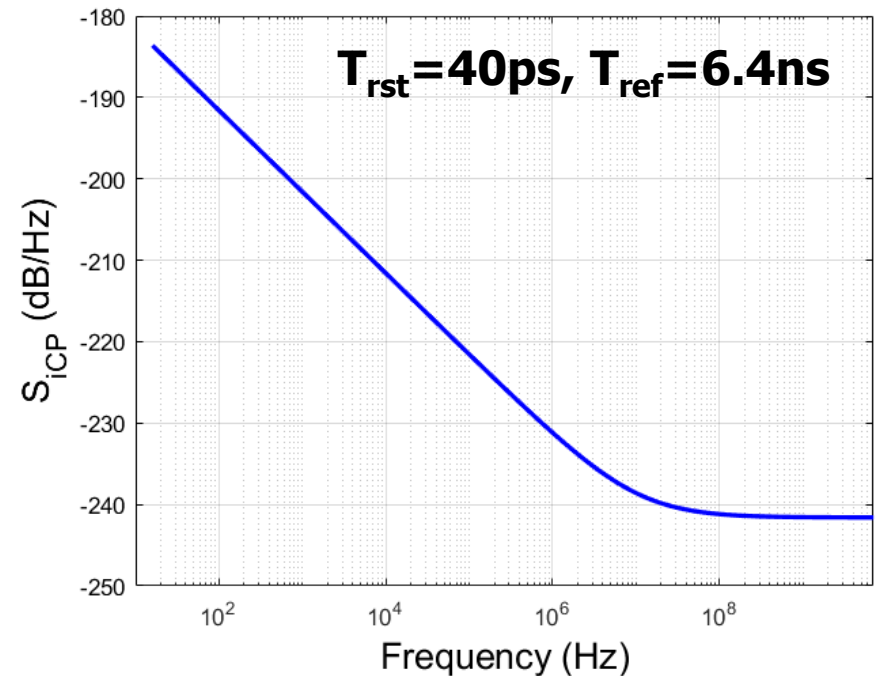


- After PLL: $\sigma_{j,in} = 217\text{fs}_{\text{rms}}$ (10kHz – 10MHz)
- Including CDR: $\sigma_{j,in} = 45\text{fs}_{\text{rms}}$ (100Hz – 7GHz)

Charge Pump Noise



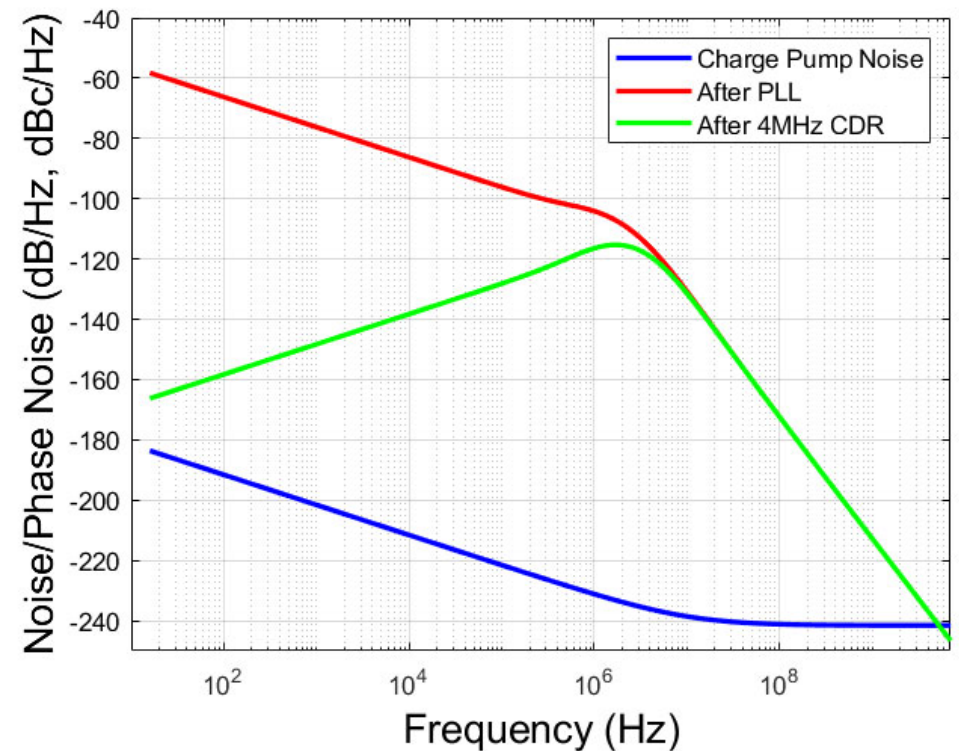
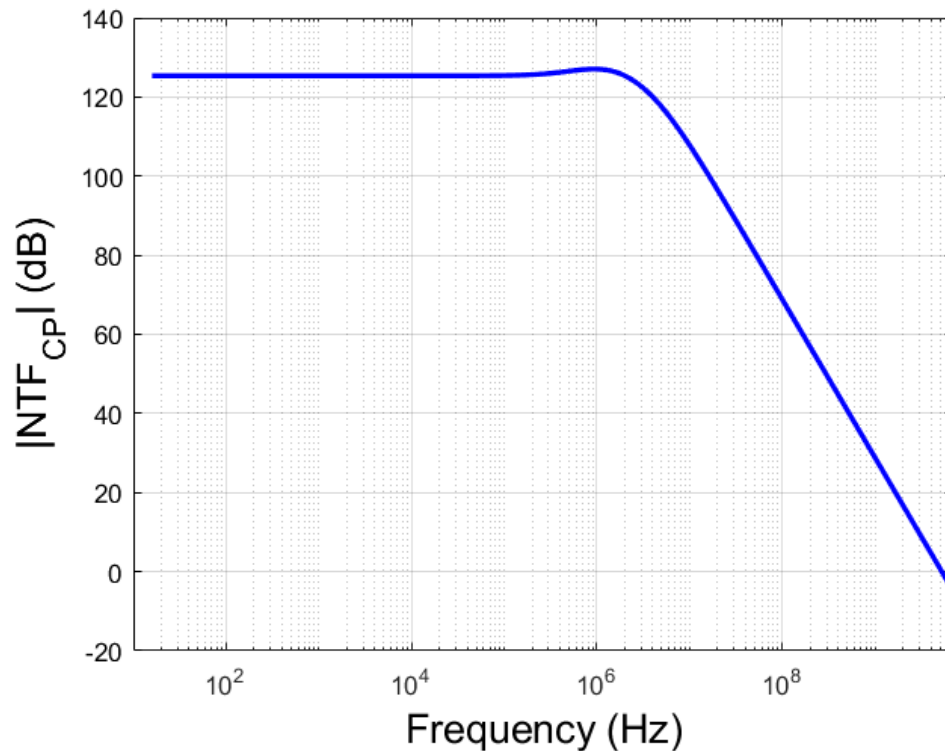
$$S_{i_{CP}} = \frac{T_{rst}}{T_{ref}} (S_{i_{n,MP}} + S_{i_{n,MN}})$$



- Charge pump noise current is injected into the loop filter during the PFD reset time
- Trade-off between charge pump noise contribution and deadzone robustness
- Transistor flicker noise can contribute significantly to PLL in-band phase noise

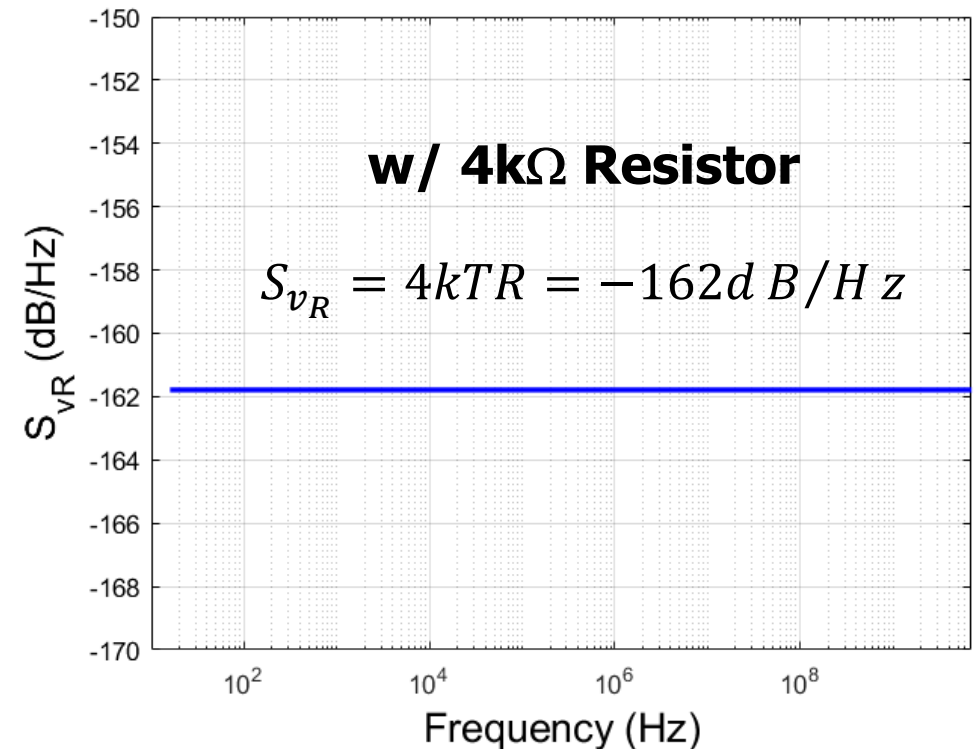
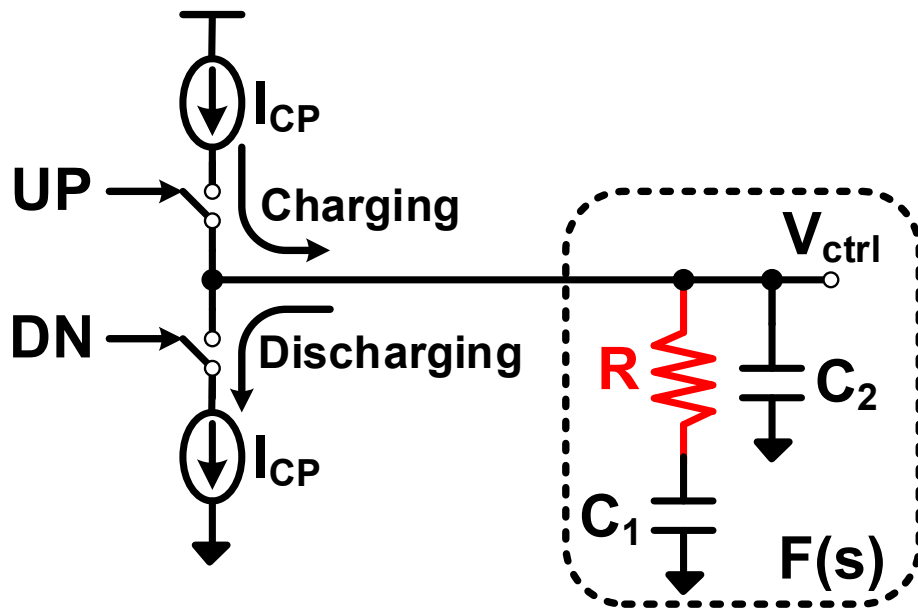
Charge Pump Noise

$$NTF_{CP}(s) = \frac{\frac{K_{VCO}}{C_2} \left(s + \frac{1}{RC_1} \right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1 C_2} \right) s^2 + \left(\frac{K_{PD} K_{VCO}}{NC_2} \right) s + \frac{K_{PD} K_{VCO}}{NRC_1 C_2}}$$



- After PLL: $\sigma_{j,CP} = 205\text{fs}_{\text{rms}}$ (10kHz – 10MHz)
- Including CDR: $\sigma_{j,CP} = 52\text{fs}_{\text{rms}}$ (100Hz – 7GHz)

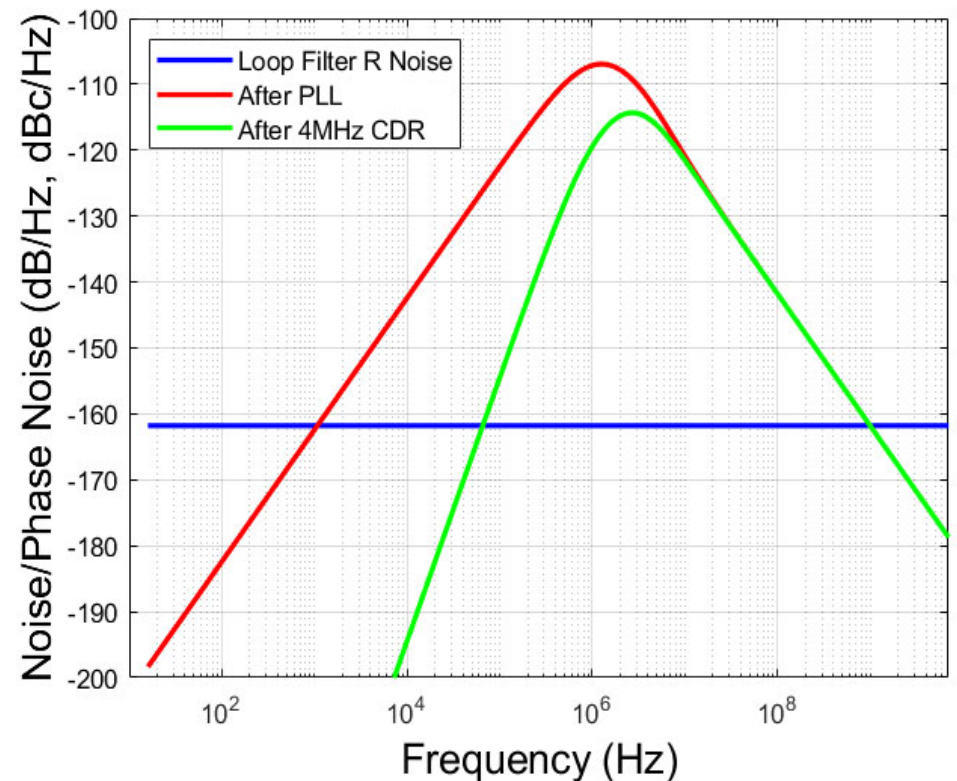
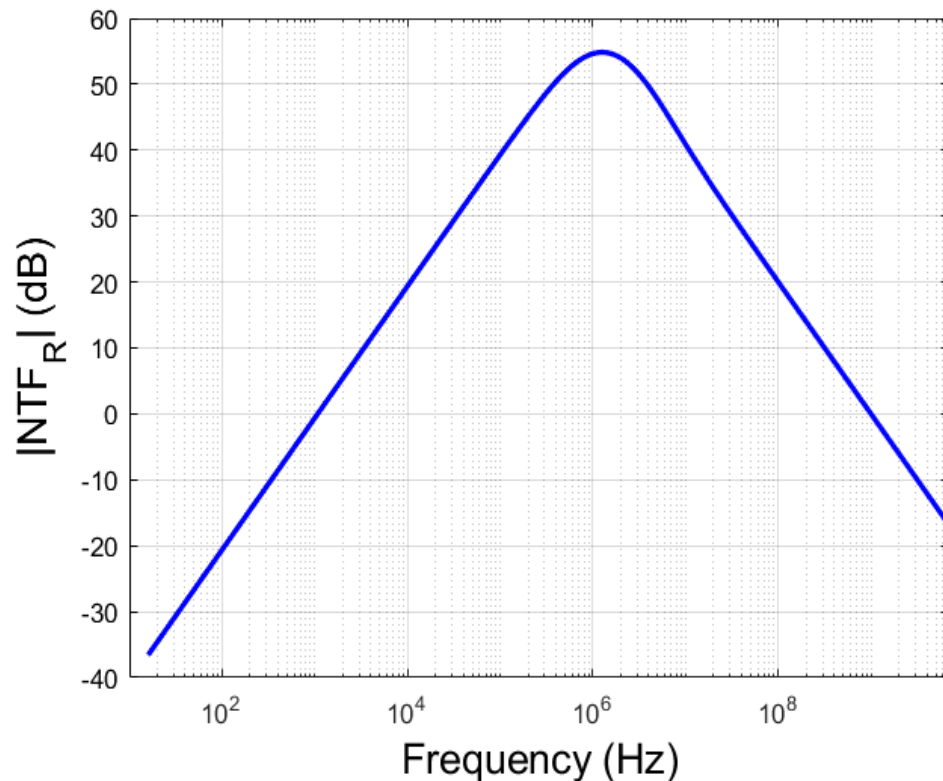
Loop Filter R Noise



- Trade-off between resistor noise, loop filter capacitor size, and charge pump noise
 - Smaller resistor results in larger capacitors (higher area) and larger charge pump current (higher S_{iCP})

Loop Filter R Noise

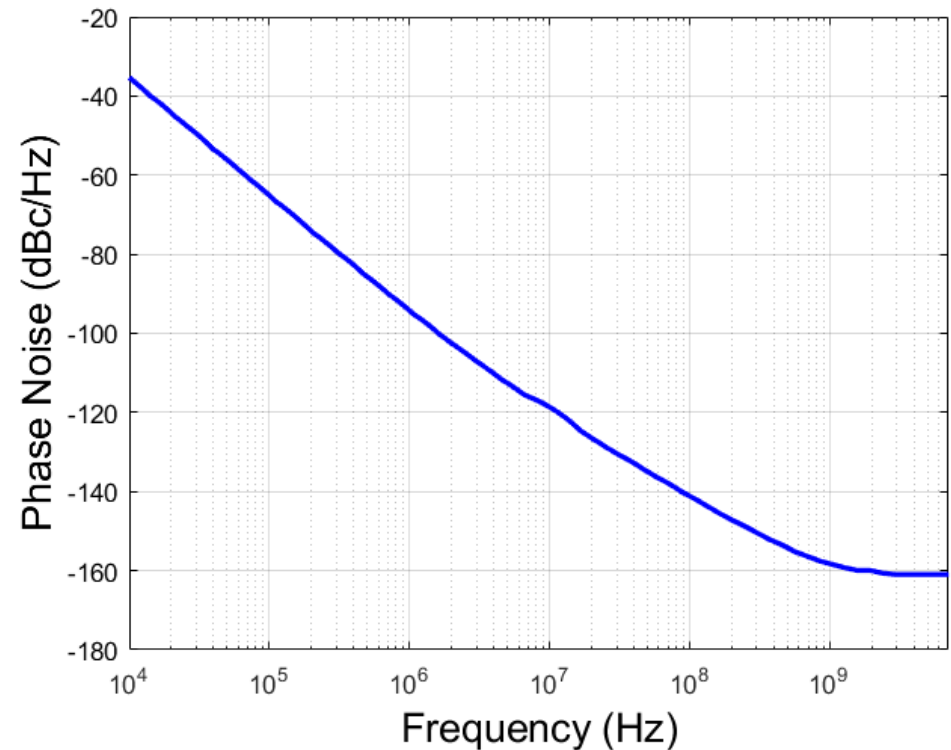
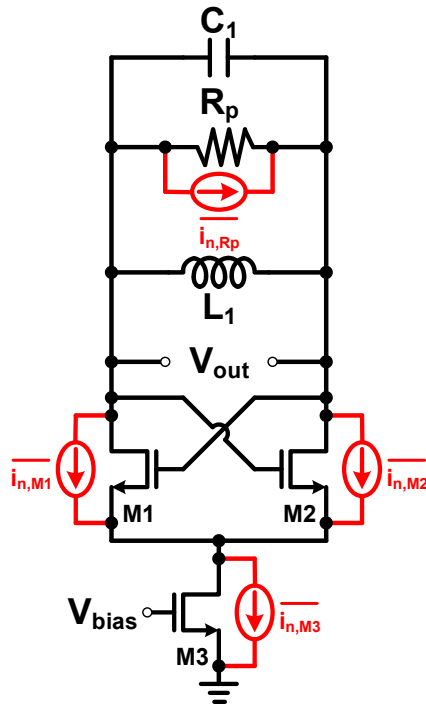
$$NTF_R(s) = \frac{K_{VCO}s \left(s + \frac{C_1 + C_2}{RC_1C_2} \right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1C_2} \right) s^2 + \left(\frac{K_{PD}K_{VCO}}{NC_2} \right) s + \frac{K_{PD}K_{VCO}}{NRC_1C_2}}$$



- After PLL: $\sigma_{j,R} = 128fs_{rms}$ (10kHz – 10MHz)
- Including CDR: $\sigma_{j,R} = 81fs_{rms}$ (100Hz – 7GHz)

VCO Noise

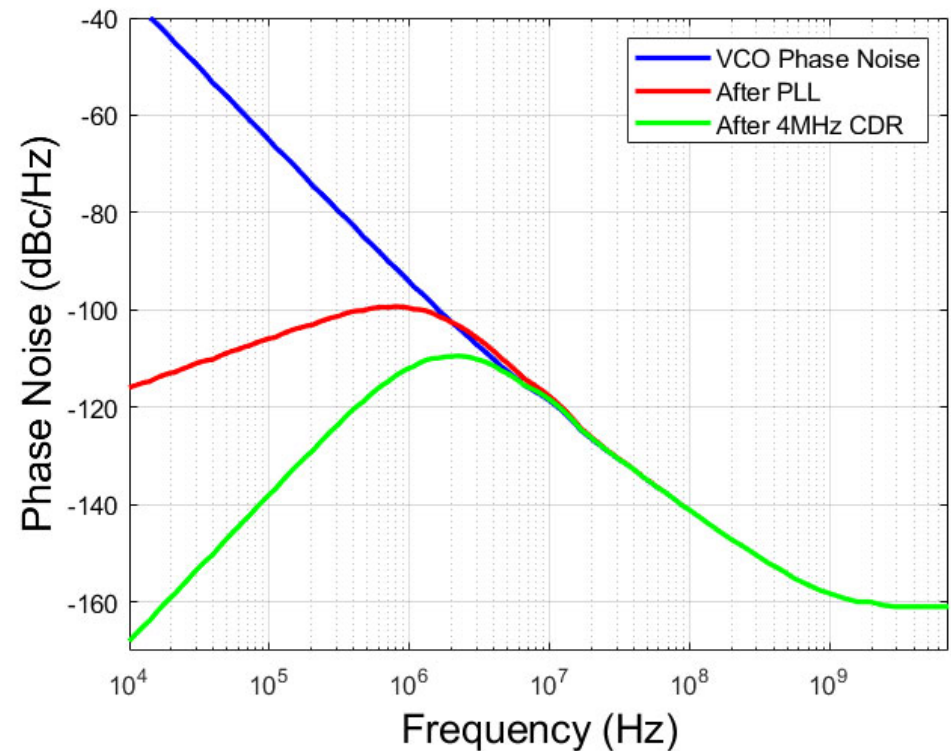
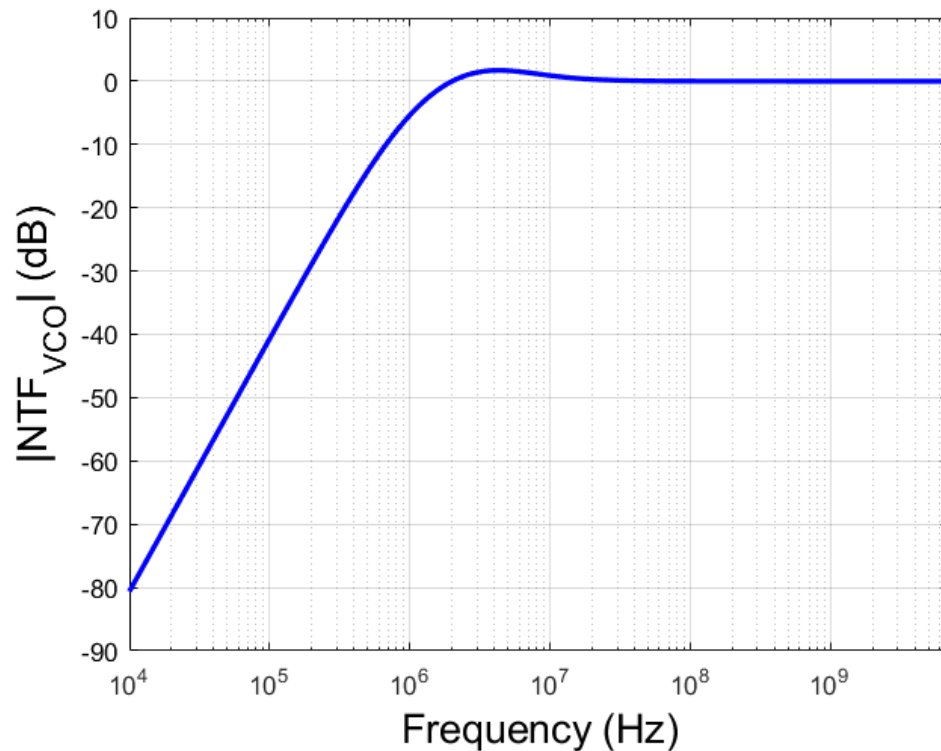
LC-Oscillator w/ Differential Tank & Noise Sources



- LC-VCO phase noise sources
 - Finite tank quality factor
 - Cross-coupled pair
 - Tail current source

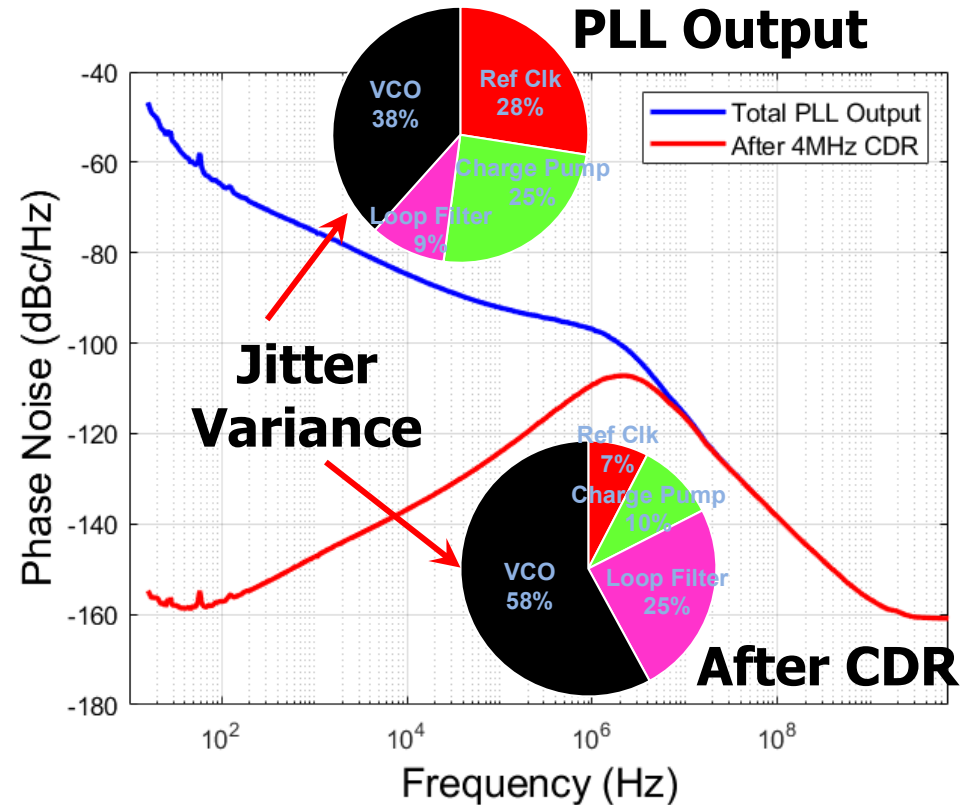
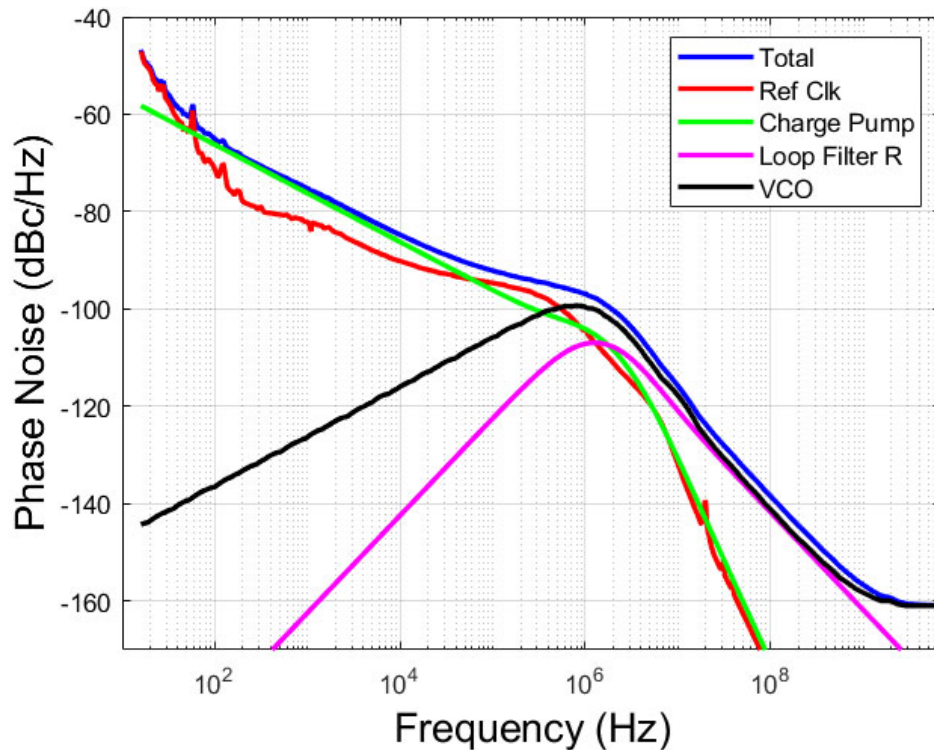
VCO Noise

$$NTF_{VCO}(s) = \frac{s^2 \left(s + \frac{C_1 + C_2}{RC_1C_2} \right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1C_2} \right) s^2 + \left(\frac{K_{PD}K_{VCO}}{NC_2} \right) s + \frac{K_{PD}K_{VCO}}{NRC_1C_2}}$$



- After PLL: $\sigma_{j,VCO} = 257\text{fs}_{\text{rms}}$ (10kHz – 10MHz)
- Including CDR: $\sigma_{j,R} = 125\text{fs}_{\text{rms}}$ (100Hz – 7GHz)

Total Noise



- After PLL: $\sigma_{j,Total} = 414f_{s_{rms}}$ (10kHz – 10MHz)
 - Reference clock and charge pump noise dominates at low frequency
 - VCO dominates near loop bandwidth and higher
- Including CDR: $\sigma_{j,Total} = 164f_{s_{rms}}$ (100Hz – 7GHz)
 - Now VCO noise clearly dominates total
 - Loop resistor noise is a larger percentage

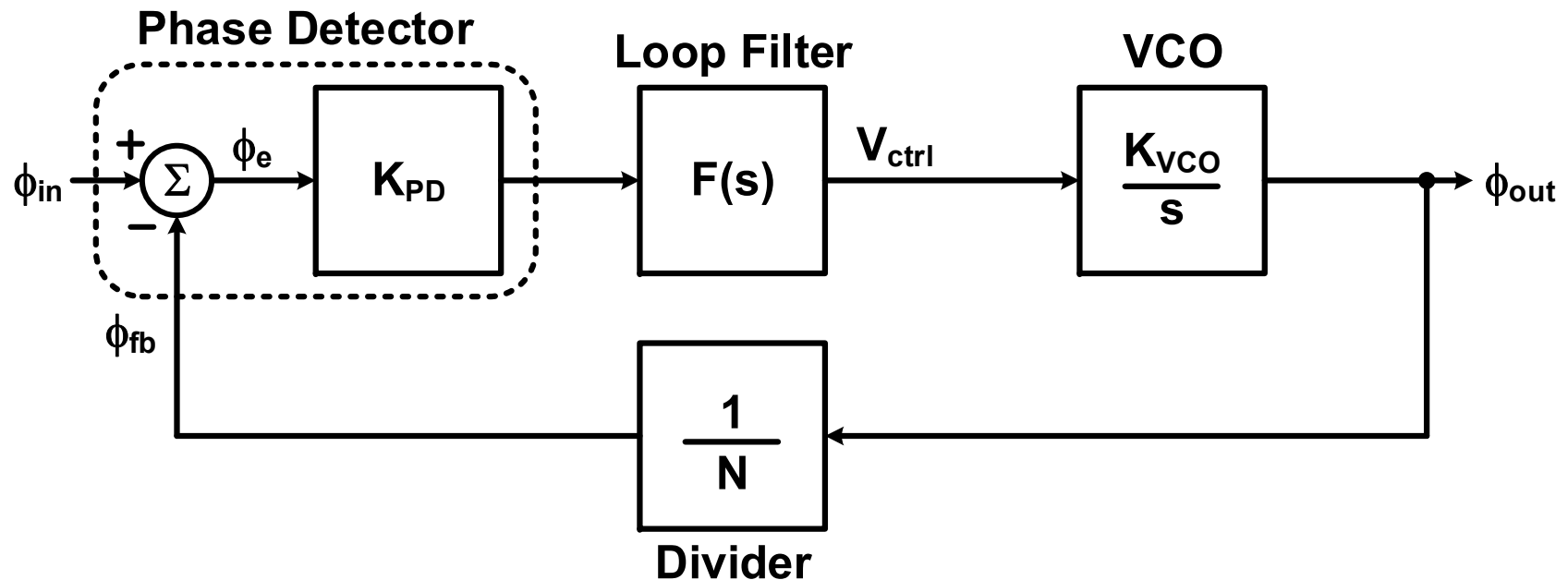
PLL Noise Transfer Function Take-Away Points

- The way a PLL shapes phase noise depends on where the noise is introduced in the loop
- Optimizing the loop bandwidth for one noise source may enhance other noise sources
- Generally, the PLL low-pass shapes input phase noise, band-pass shapes VCO input voltage noise, and high-pass shapes VCO/clock buffer output phase noise

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Linear PLL Model



- If the phase input amplitude is small, then the linear model can be used to predict the transient response

$$E(s) = \frac{\phi_e(s)}{\phi_{in}(s)} = \frac{1}{1 + \frac{G(s)}{N}} = \frac{s}{s + \frac{K_{PD}K_{VCO}F(s)}{N}}$$

- Ideally, we want this to be zero
- Phase error generally increases with frequency due to this high-pass response

First-Order PLL Tracking Response

$$F(s) = K_1, \quad E(s) = \frac{s}{s + \frac{K_{PD}K_{VCO}K_1}{N}} = \frac{s}{s + \omega_{3dB}}, \quad K_{DC} = \omega_{3dB} = \frac{K_{PD}K_{VCO}K_1}{N}$$

- Phase Step Response

Using the Final Value Theorem : $\lim_{s \rightarrow 0} \left(\frac{\Delta\Phi}{s} \right) (sE(s)) = \lim_{s \rightarrow 0} \frac{\Delta\Phi s^2}{s(s + K_{DC})} = 0$

Phase error should be zero with a phase step

Transient Response : $\mathcal{L}^{-1} \left\{ \left(\frac{\Delta\Phi}{s} \right) \left(\frac{s}{s + K_{DC}} \right) \right\} = \Delta\Phi e^{-K_{DC}t}$

Transient Response is an exponentially decaying step

First-Order PLL Tracking Response

$$F(s) = K_1, \quad E(s) = \frac{s}{s + \frac{K_{PD}K_{VCO}K_1}{N}} = \frac{s}{s + \omega_{3dB}}, \quad K_{DC} = \omega_{3dB} = \frac{K_{PD}K_{VCO}K_1}{N}$$

- Frequency Offset (Step) Response

Using the Final Value Theorem: $\lim_{s \rightarrow 0} \left(\frac{\Delta\omega}{s^2} \right) (sE(s)) = \lim_{s \rightarrow 0} \frac{\Delta\omega s^2}{s^2(s + K_{DC})} = \frac{\Delta\omega}{K_{DC}}$

The phase error is inversely proportional to the loop gain with a frequency offset

$$\text{Transient Response: } \mathcal{L}^{-1} \left\{ \left(\frac{\Delta\omega}{s^2} \right) \left(\frac{s}{s + K_{DC}} \right) \right\} = \frac{\Delta\omega}{K_{DC}} (1 - e^{-K_{DC}t})$$

Transient Response is an exponentially rising step

First-Order PLL Tracking Response

$$F(s) = K_1, \quad E(s) = \frac{s}{s + \frac{K_{PD}K_{VCO}K_1}{N}} = \frac{s}{s + \omega_{3dB}}, \quad K_{DC} = \omega_{3dB} = \frac{K_{PD}K_{VCO}K_1}{N}$$

- Frequency Ramp Response

Assume that the input frequency is changing linearly with time at a rate of Λ (rad/sec²)

$$\phi_{ref}(t) = \frac{\Lambda t^2}{2}$$

Using the Final Value Theorem : $\lim_{s \rightarrow 0} \left(\frac{\Lambda}{s^3} \right) (sE(s)) = \lim_{s \rightarrow 0} \frac{\Lambda s^2}{s^3(s + K_{DC})} \Rightarrow \infty$

The phase error will grow to infinity if K_{DC} is finite

$$\text{Transient Response : } \mathcal{L}^{-1} \left\{ \left(\frac{\Lambda}{s^3} \right) \left(\frac{s}{s + K_{DC}} \right) \right\} = \frac{\Lambda}{K_{DC}^2} (K_{DC}t + e^{-K_{DC}t} - 1)$$

Second-Order Type-1 PLL Tracking Response

$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)}, \quad E(s) = \frac{s \left(s + \frac{N\omega_n^2}{K_{PD}K_{VCO}} \right)}{s^2 + 2\zeta\omega_n s + \omega_n^2} = \frac{s \left(s + \frac{1}{\tau_1 + \tau_2} \right)}{s^2 + \left(\frac{1 + K_{DC}\tau_2}{\tau_1 + \tau_2} \right) s + \frac{K_{DC}}{\tau_1 + \tau_2}}, \quad K_{DC} = \frac{K_{PD}K_{VCO}}{N}$$

- Phase Step Response

Using the Final Value Theorem : $\lim_{s \rightarrow 0} \left(\frac{\Delta\Phi}{s} \right) (sE(s)) = \lim_{s \rightarrow 0} \frac{\Delta\Phi s^2 \left(s + \frac{1}{\tau_1 + \tau_2} \right)}{s \left(s^2 + \left(\frac{1 + K_{DC}\tau_2}{\tau_1 + \tau_2} \right) s + \frac{K_{DC}}{\tau_1 + \tau_2} \right)} = 0$

Phase error should be zero with a phase step

Transient Response : $\mathcal{L}^{-1} \left\{ \left(\frac{\Delta\Phi}{s} \right) \frac{s \left(s + \frac{1}{\tau_1 + \tau_2} \right)}{s^2 + \left(\frac{1 + K_{DC}\tau_2}{\tau_1 + \tau_2} \right) s + \frac{K_{DC}}{\tau_1 + \tau_2}} \right\}$

Try to compute this yourself

Second-Order Type-1 PLL Tracking Response

$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)}, \quad E(s) = \frac{s \left(s + \frac{N\omega_n^2}{K_{PD}K_{VCO}} \right)}{s^2 + 2\zeta\omega_n s + \omega_n^2} = \frac{s \left(s + \frac{1}{\tau_1 + \tau_2} \right)}{s^2 + \left(\frac{1 + K_{DC}\tau_2}{\tau_1 + \tau_2} \right) s + \frac{K_{DC}}{\tau_1 + \tau_2}}, \quad K_{DC} = \frac{K_{PD}K_{VCO}}{N}$$

- Frequency Offset (Step) Response

Using the Final Value Theorem : $\lim_{s \rightarrow 0} \left(\frac{\Delta\omega}{s^2} \right) (sE(s)) = \lim_{s \rightarrow 0} \frac{\Delta\omega s^2 \left(s + \frac{1}{\tau_1 + \tau_2} \right)}{s^2 \left(s^2 + \left(\frac{1 + K_{DC}\tau_2}{\tau_1 + \tau_2} \right) s + \frac{K_{DC}}{\tau_1 + \tau_2} \right)} = \frac{\Delta\omega}{K_{DC}}$

The phase error is inversely proportional to the loop gain with a frequency offset

Transient Response : $\mathcal{L}^{-1} \left\{ \left(\frac{\Delta\omega}{s^2} \right) \left(\frac{s \left(s + \frac{1}{\tau_1 + \tau_2} \right)}{s^2 + \left(\frac{1 + K_{DC}\tau_2}{\tau_1 + \tau_2} \right) s + \frac{K_{DC}}{\tau_1 + \tau_2}} \right) \right\}$

Try to compute this yourself

Second-Order Type-1 PLL Tracking Response

$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)}, \quad E(s) = \frac{s \left(s + \frac{N\omega_n^2}{K_{PD}K_{VCO}} \right)}{s^2 + 2\zeta\omega_n s + \omega_n^2} = \frac{s \left(s + \frac{1}{\tau_1 + \tau_2} \right)}{s^2 + \left(\frac{1 + K_{DC}\tau_2}{\tau_1 + \tau_2} \right) s + \frac{K_{DC}}{\tau_1 + \tau_2}}, \quad K_{DC} = \frac{K_{PD}K_{VCO}}{N}$$

- Frequency Ramp Response

Using the Final Value Theorem : $\lim_{s \rightarrow 0} \left(\frac{\Lambda}{s^3} \right) (sE(s)) = \lim_{s \rightarrow 0} \frac{\Lambda s^2 \left(s + \frac{1}{\tau_1 + \tau_2} \right)}{s^3 \left(s^2 + \left(\frac{1 + K_{DC}\tau_2}{\tau_1 + \tau_2} \right) s + \frac{K_{DC}}{\tau_1 + \tau_2} \right)} \Rightarrow \infty$

The phase error will grow to infinity if K_{DC} is finite

Transient Response : $\mathcal{L}^{-1} \left\{ \left(\frac{\Lambda}{s^3} \right) \left(\frac{s \left(s + \frac{1}{\tau_1 + \tau_2} \right)}{s^2 + \left(\frac{1 + K_{DC}\tau_2}{\tau_1 + \tau_2} \right) s + \frac{K_{DC}}{\tau_1 + \tau_2}} \right) \right\}$

Try to compute this yourself

Second-Order Type-2 PLL Tracking Response

$$F(s) = \frac{R\left(s + \frac{1}{RC}\right)}{s}, \quad E(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} = \frac{s^2}{s^2 + Ks + \frac{K}{RC}}, \quad K = \frac{K_{PD}K_{VCO}R}{N}$$

- Phase Step Response

Using the Final Value Theorem : $\lim_{s \rightarrow 0} \left(\frac{\Delta\Phi}{s} \right) (sE(s)) = \lim_{s \rightarrow 0} \frac{\Delta\Phi s^3}{s \left(s^2 + Ks + \frac{K}{RC} \right)} = 0$

Phase error should be zero with a phase step

Transient Response : $\mathcal{L}^{-1} \left\{ \left(\frac{\Delta\Phi}{s} \right) \left(\frac{s^2}{s^2 + Ks + \frac{K}{RC}} \right) \right\}$

Second-Order Type-2 PLL

Phase Step Response

$$\text{Transient Response: } \mathcal{L}^{-1} \left\{ \left(\frac{\Delta\Phi}{s} \right) \left(\frac{s^2}{s^2 + Ks + \frac{K}{RC}} \right) \right\}$$

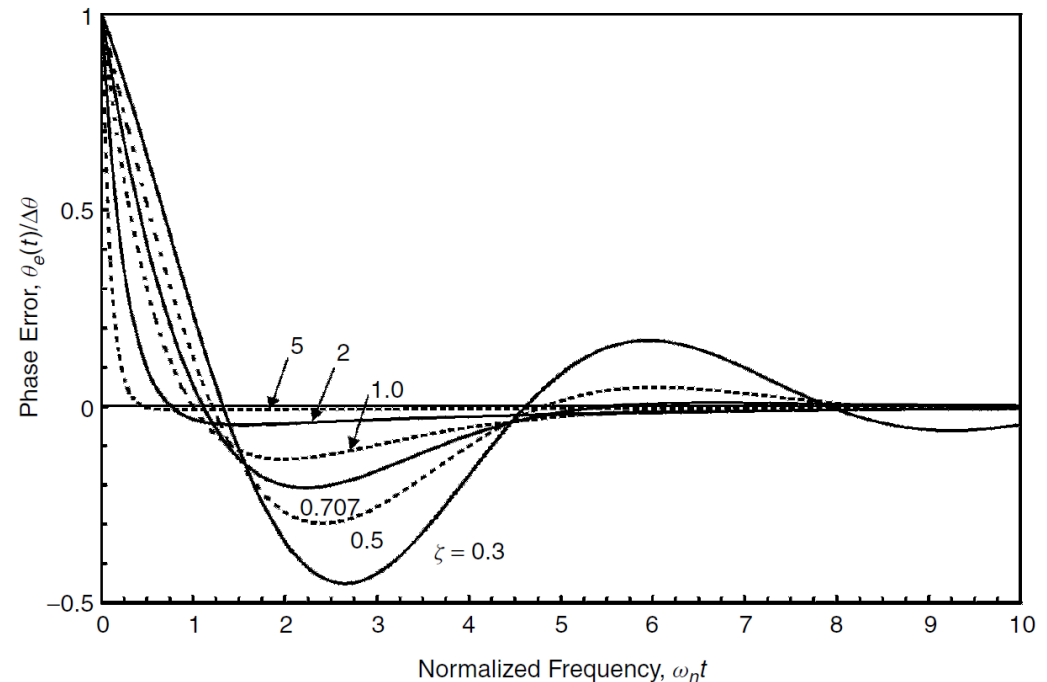
Phase Step, $\Delta\theta$ (rad)

$$\zeta < 1 \quad \Delta\theta \left(\cos \sqrt{1 - \zeta^2} \omega_n t - \frac{\zeta}{\sqrt{1 - \zeta^2}} \sin \sqrt{1 - \zeta^2} \omega_n t \right) e^{-\zeta \omega_n t}$$

$$\zeta = 1 \quad \Delta\theta (1 - \omega_n t) e^{-\omega_n t}$$

$$\zeta > 1 \quad \Delta\theta \left(\cosh \sqrt{\zeta^2 - 1} \omega_n t - \frac{\zeta}{\sqrt{\zeta^2 - 1}} \sinh \sqrt{\zeta^2 - 1} \omega_n t \right) e^{-\zeta \omega_n t}$$

$$\zeta = \frac{\omega_n}{2} RC = \frac{1}{2} \sqrt{KRC}$$



Second-Order Type-2 PLL Tracking Response

$$F(s) = \frac{R\left(s + \frac{1}{RC}\right)}{s}, \quad E(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} = \frac{s^2}{s^2 + Ks + \frac{K}{RC}}, \quad K = \frac{K_{PD}K_{VCO}R}{N}$$

- Frequency Offset (Step) Response

Using the Final Value Theorem : $\lim_{s \rightarrow 0} \left(\frac{\Delta\omega}{s^2} \right) (sE(s)) = \lim_{s \rightarrow 0} \frac{\Delta\omega s^3}{s^2 \left(s^2 + Ks + \frac{K}{RC} \right)} = 0$

The phase error goes to zero with a Type - 2 PLL

Transient Response : $\mathcal{L}^{-1} \left\{ \left(\frac{\Delta\omega}{s^2} \right) \left(\frac{s^2}{s^2 + Ks + \frac{K}{RC}} \right) \right\}$

Second-Order Type-2 PLL Frequency Step Response

Transient Response : $\mathcal{L}^{-1} \left\{ \left(\frac{\Delta\omega}{s^2} \right) \left(\frac{s^2}{s^2 + Ks + \frac{K}{RC}} \right) \right\}$

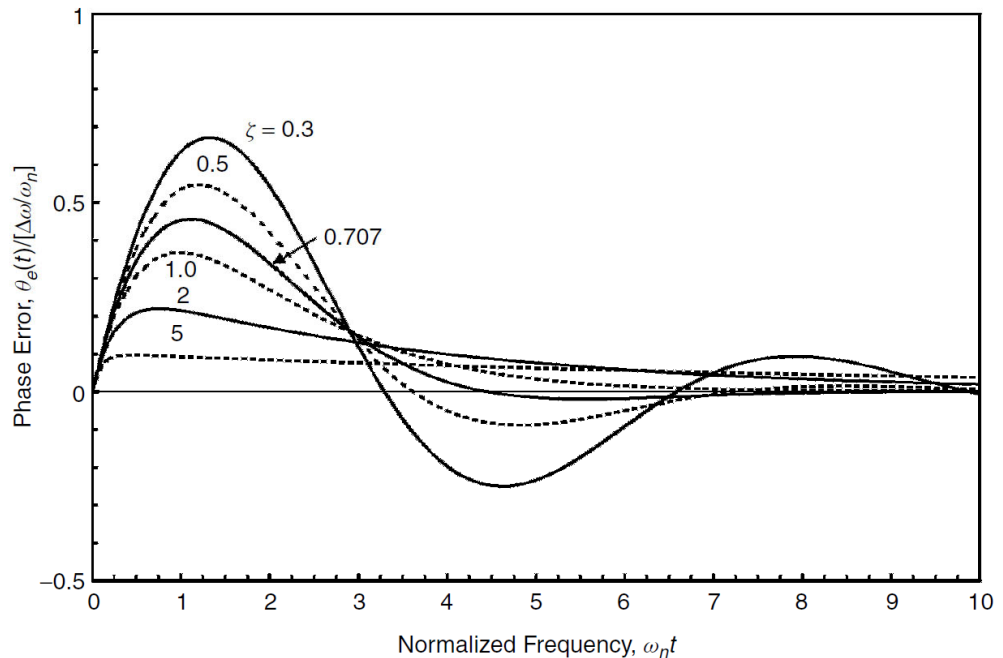
Frequency Step, $\Delta\omega$ (rad/sec)

$$\zeta < 1 \quad \frac{\Delta\omega}{\omega_n} \left(\frac{1}{\sqrt{1 - \zeta^2}} \sin \sqrt{1 - \zeta^2} \omega_n t \right) e^{-\zeta \omega_n t}$$

$$\zeta = 1 \quad \frac{\Delta\omega}{\omega_n} (\omega_n t) e^{-\omega_n t}$$

$$\zeta > 1 \quad \frac{\Delta\omega}{\omega_n} \left(\frac{1}{\sqrt{\zeta^2 - 1}} \sinh \sqrt{\zeta^2 - 1} \omega_n t \right) e^{-\zeta \omega_n t}$$

$$\zeta = \frac{\omega_n}{2} RC = \frac{1}{2} \sqrt{KRC}$$



Second-Order Type-2 PLL Tracking Response

$$F(s) = \frac{R\left(s + \frac{1}{RC}\right)}{s}, \quad E(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} = \frac{s^2}{s^2 + Ks + \frac{K}{RC}}, \quad K = \frac{K_{PD}K_{VCO}R}{N}$$

- Frequency Ramp Response

Using the Final Value Theorem : $\lim_{s \rightarrow 0} \left(\frac{\Lambda}{s^3} \right) (sE(s)) = \lim_{s \rightarrow 0} \frac{\Lambda s^3}{s^3 \left(s^2 + Ks + \frac{K}{RC} \right)} = \frac{\Lambda}{\omega_n^2}$

A second - order type - 2 PLL can track a frequency ramp with a dynamic phase lag

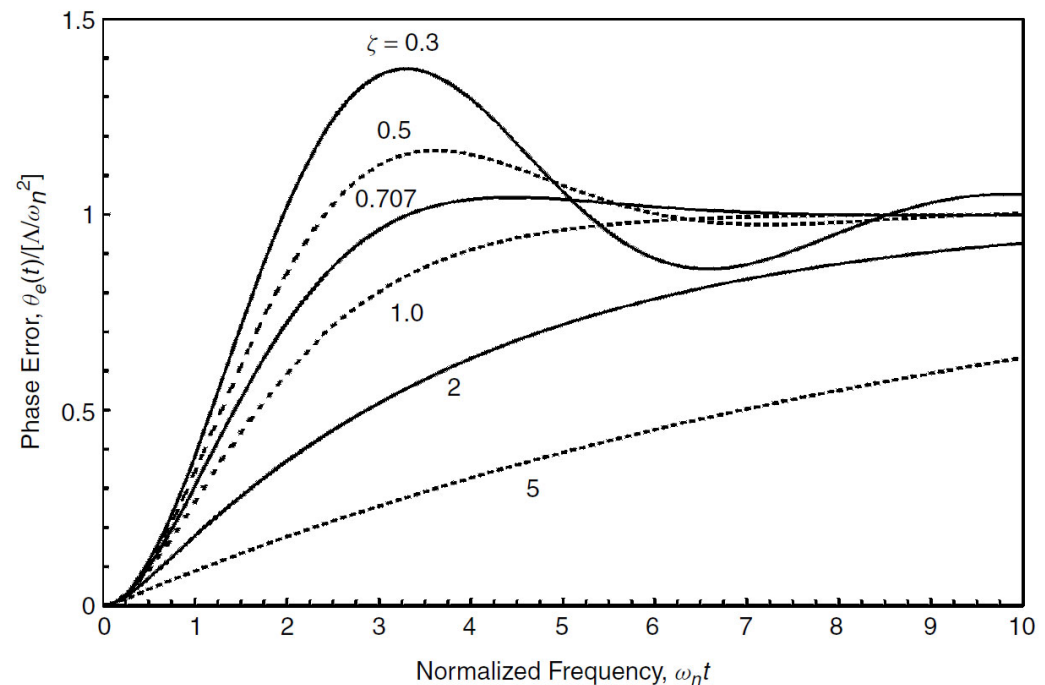
Transient Response : $\mathcal{L}^{-1} \left\{ \left(\frac{\Lambda}{s^3} \right) \left(\frac{s^2}{s^2 + Ks + \frac{K}{RC}} \right) \right\}$

Second-Order Type-2 PLL Frequency Ramp Response

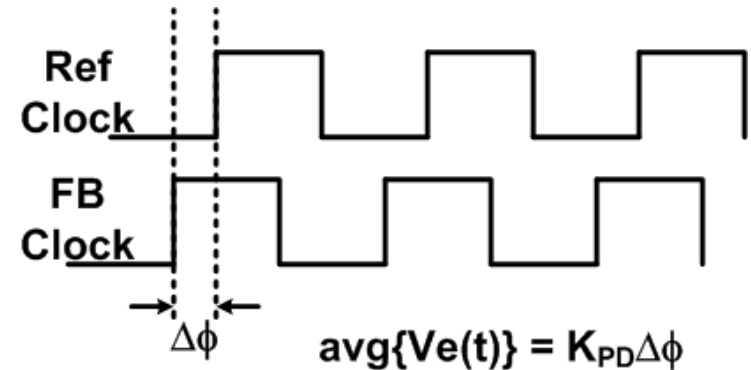
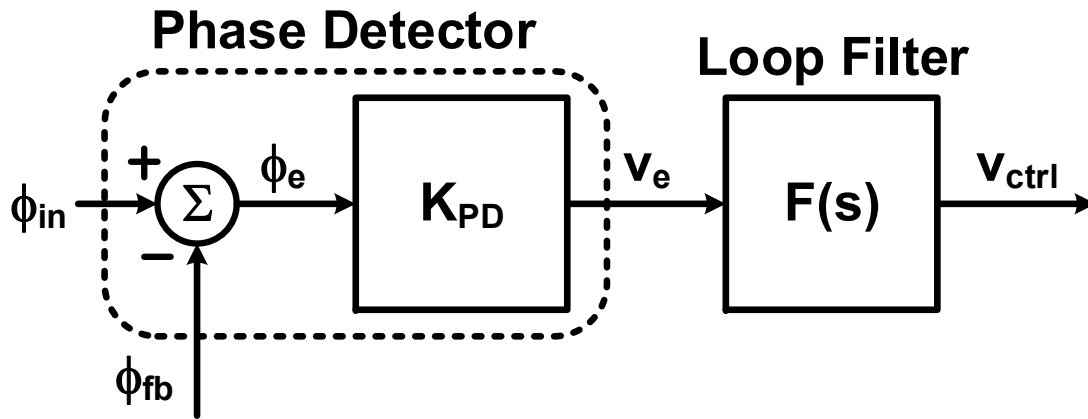
Transient Response : $\mathcal{L}^{-1} \left\{ \left(\frac{\Lambda}{s^3} \right) \left(\frac{s^2}{s^2 + Ks + \frac{K}{RC}} \right) \right\}$

$$\zeta = \frac{\omega_n}{2} RC = \frac{1}{2} \sqrt{KRC}$$

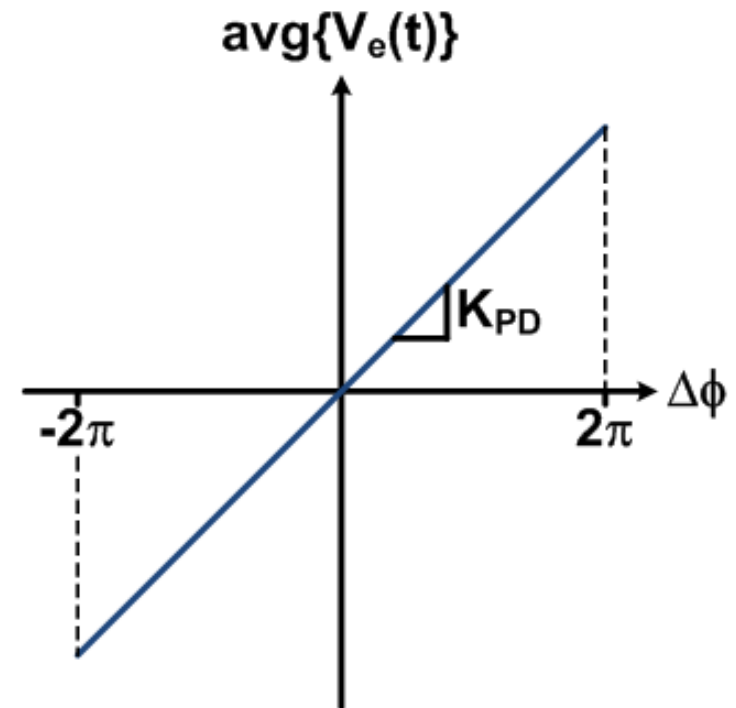
	Frequency Ramp, Λ (rad/sec ²)
$\zeta < 1$	$\frac{\Lambda}{\omega_n^2} - \frac{\Lambda}{\omega_n^2} \left(\cos \sqrt{1 - \zeta^2} \omega_n t + \frac{\zeta}{\sqrt{1 - \zeta^2}} \sin \sqrt{1 - \zeta^2} \omega_n t \right) e^{-\zeta \omega_n t}$
$\zeta = 1$	$\frac{\Lambda}{\omega_n^2} - \frac{\Lambda}{\omega_n^2} (1 + \omega_n t) e^{-\omega_n t}$
$\zeta > 1$	$\frac{\Lambda}{\omega_n^2} - \frac{\Lambda}{\omega_n^2} \left(\cosh \sqrt{\zeta^2 - 1} \omega_n t + \frac{\zeta}{\sqrt{\zeta^2 - 1}} \sinh \sqrt{\zeta^2 - 1} \omega_n t \right) e^{-\zeta \omega_n t}$



Ideal Phase Detector



- An ideal phase detector has the same gain (slope) over a $\pm 2\pi$ range
- This allows the linear PLL model to be used for all phase relationships



Real Phase Detectors

- Many phase detectors are nonlinear and do not display the same gain for a given phase relationship
- This implies that the PLL cannot be described by the linear model for large input phase deviations

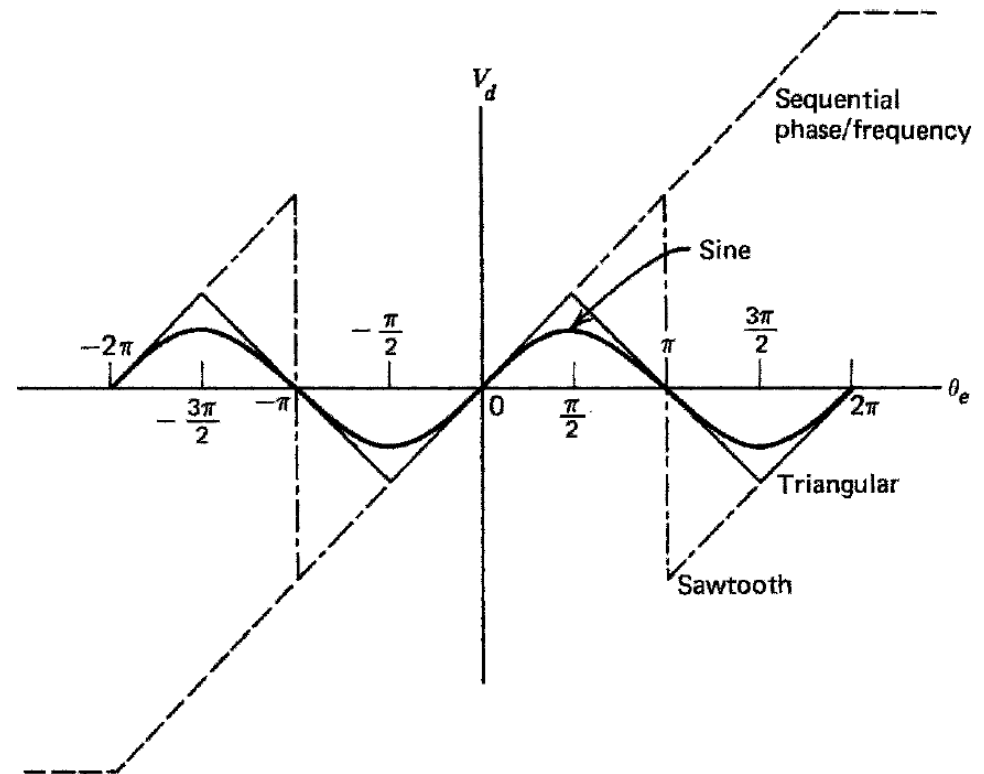
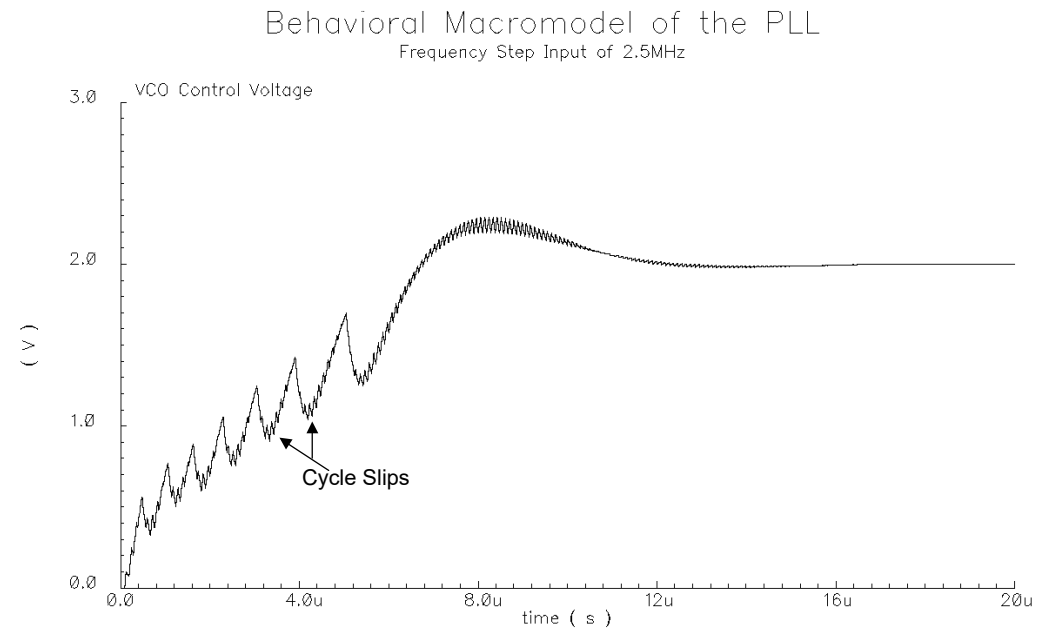
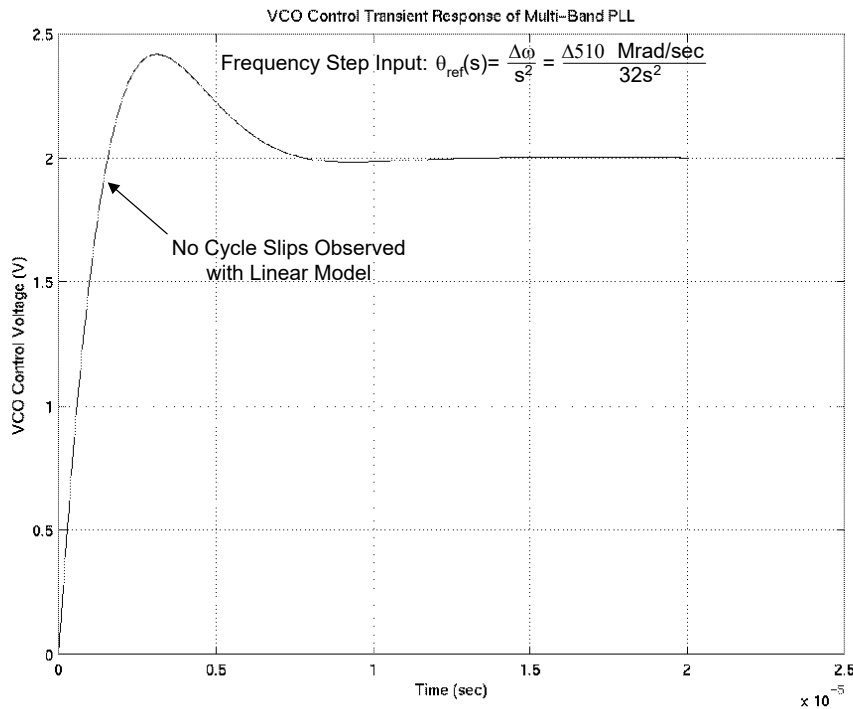


Figure 5.13 Phase detector s-curves.

PLL Frequency Step Response: Linear vs Behavioral Model



- Due to non-linearities in loop components (primarily the PD), a real PLL's response can vary significantly from the linear model

PLL Hold Range (Sinusoidal PD)

- A PLL **Hold Range** is the input frequency range over which the PLL can maintain static lock

w/ Linear Model the Steady - State Phase Error is $\phi_e = \frac{\Delta\omega}{K_{DC}}$

$$\text{First - Order : } K_{DC} = \frac{K_{PD}K_{VCO}K_1}{N}$$

$$\text{Second - Order Type - 1 : } K_{DC} = \frac{K_{PD}K_{VCO}}{N}$$

$$\text{Second - Order Type - 2 : } K_{DC} = \infty$$

With a sinusoidal phase detector, the phase error is

$$\sin\phi_e = \frac{\Delta\omega}{K_{DC}}$$

Since sine cannot exceed $|1|$, the lock frequency is constrained to $|\Delta\omega| \leq K_{DC}$

$$\text{Hold Range : } |\Delta\omega_H| = K_{DC} \text{ (rad/sec)}$$

- The hold range is finite for a type-1 PLL, and theoretically infinite for a type-2 PLL. However in practice it will be limited by another PLL block, such as the VCO tuning range.

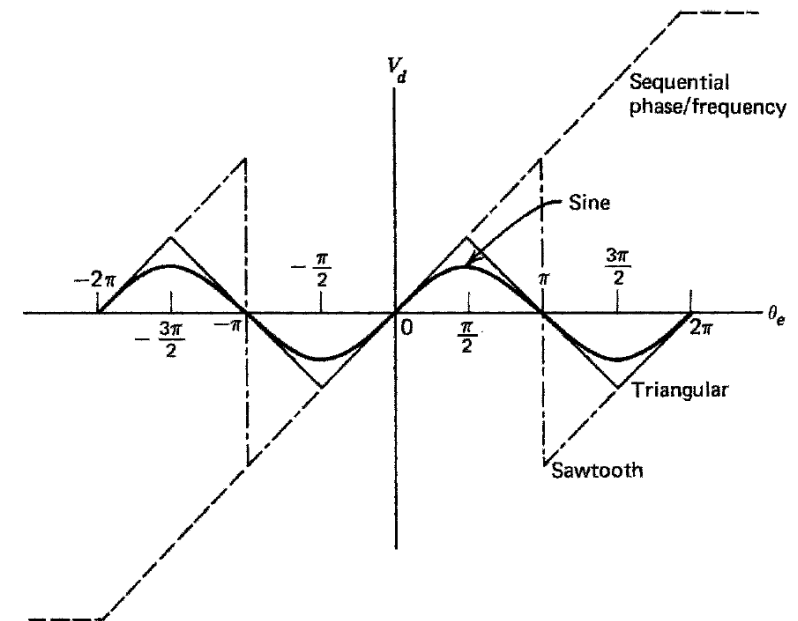
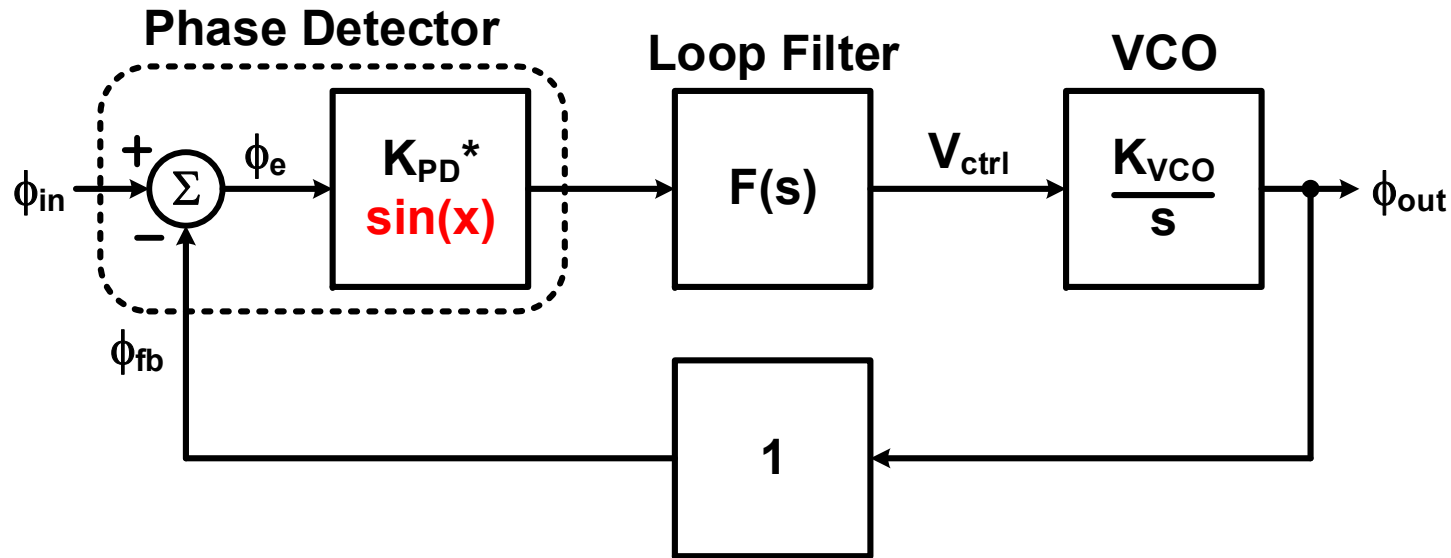


Figure 5.13 Phase detector s-curves.

First-Order PLL Phaselock Acquisition (Sinusoidal PD)



Assuming a simple first - order PLL with a sinusoidal PD

$$F(s) = K_1 = 1$$

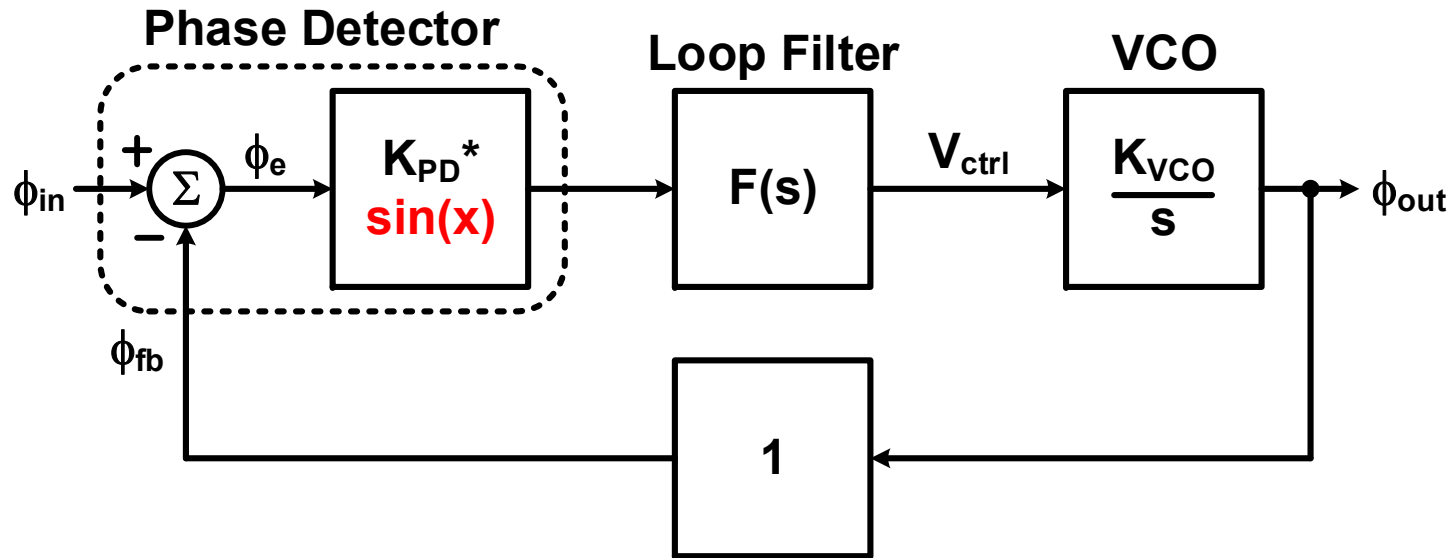
VCO Instantaneous Frequency : $\omega_o + K_{VCO} v_c(t)$

Sinusoidal Phase Detector Output : $K_{PD} \sin(\phi_e)$

Assume the input signal is at a frequency different from ω_o , such that the

input phase is $\omega_{ref} t$ and $\Delta\omega = \omega_{ref} - \omega_o$

First-Order PLL Phaselock Acquisition (Sinusoidal PD)



The PLL output phase is

$$\phi_{out}(t) = \omega_o t + \int_0^t K_{VCO} v_c(\tau) d\tau + \phi_{out}(0) = \omega_o t + \int_0^t K_{VCO} K_{PD} \sin(\phi_e(\tau)) d\tau + \phi_{out}(0)$$

The PLL phase error is

$$\phi_e = \phi_{ref} - \phi_{out} = (\omega_{ref} - \omega_o)t - \int_0^t K_{VCO} K_{PD} \sin(\phi_e(\tau)) d\tau - \phi_{out}(0)$$

Differentiating this w.r.t. time yields the following nonlinear differential equation

$$\frac{d\phi_e(t)}{dt} = \Delta\omega - K \sin(\phi_e(t)) \quad \text{where } K = K_{VCO} K_{PD}$$

First-Order PLL Hold Range (Sinusoidal PD)

If the PLL is locked,

$$\frac{d\phi_e(t)}{dt} = \Delta\omega - K \sin(\phi_e(\tau)) = 0$$

$$\sin(\phi_e) = \frac{\Delta\omega}{K}$$

Since sine cannot exceed $|1|$, the lock frequency is constrained to $\Delta\omega \leq K$

$$\boxed{\text{Hold Range : } |\Delta\omega_H| < K \text{ (rad/sec)}}$$

First-Order PLL Phaselock Acquisition (Sinusoidal PD)

Normalizing the first - order PLL differential equation by K

$$\frac{\dot{\phi}_e}{K} = \frac{\Delta\omega}{K} - \sin(\phi_e)$$

In the phase - plane plot, there are 2 nulls where $\frac{d\phi_e}{dt} = 0$

Negative - slope nulls are stable lock points,

while positive - slope nulls are unstable

Normalized Frequency Error, $\frac{\dot{\phi}_e}{K}$

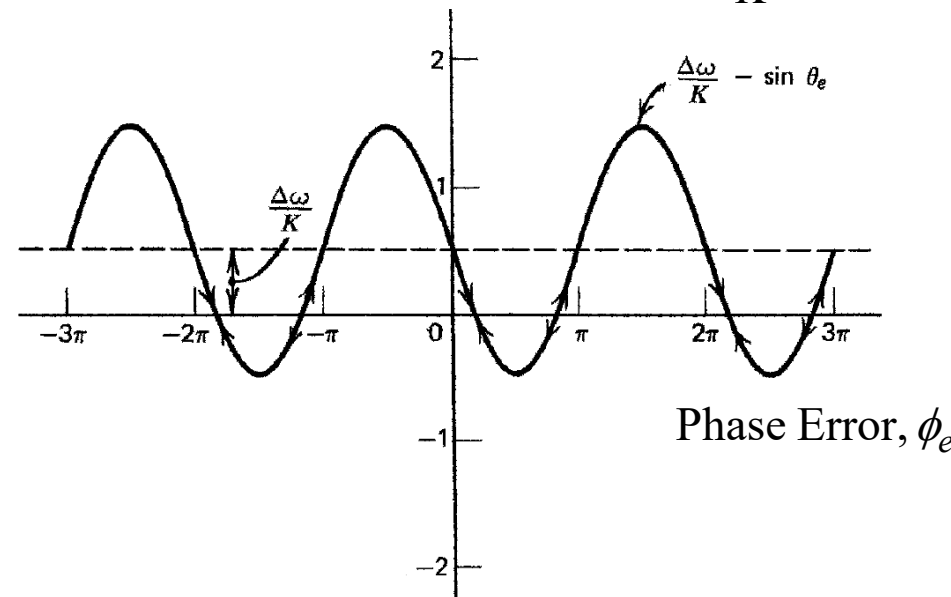


Figure 8.1 Phase-plane plot of a first-order PLL ($\Delta\omega/K = 0.5$).

- Every cycle (2π interval) contains a stable null, thus ϕ_e cannot change by more than one cycle before locking
- There is no cycle slipping in the locking process
- A cycle slip occurs when the phase error changes by more than 2π without locking

First-Order PLL Phaselock Acquisition Time (Sinusoidal PD)

In order to find the phaselock acquisition time, we need to formally solve

$$\phi_e(t) = \Delta\omega t - \int_0^t K_{VCO} K_{PD} \sin(\phi_e(\tau)) d\tau - \phi_{out}(0)$$

If $\Delta\omega$ is zero and $\phi_e(0)$ is small, such that $\sin(\phi_e) \approx \phi_e$,

the approximate solution is the linear model phase step response

$$\phi_e(t) = -\phi_{out}(0)e^{-Kt}$$

However, if $\phi_e(0)$ is large, the response will deviate

from this linear approximation and can increase significantly

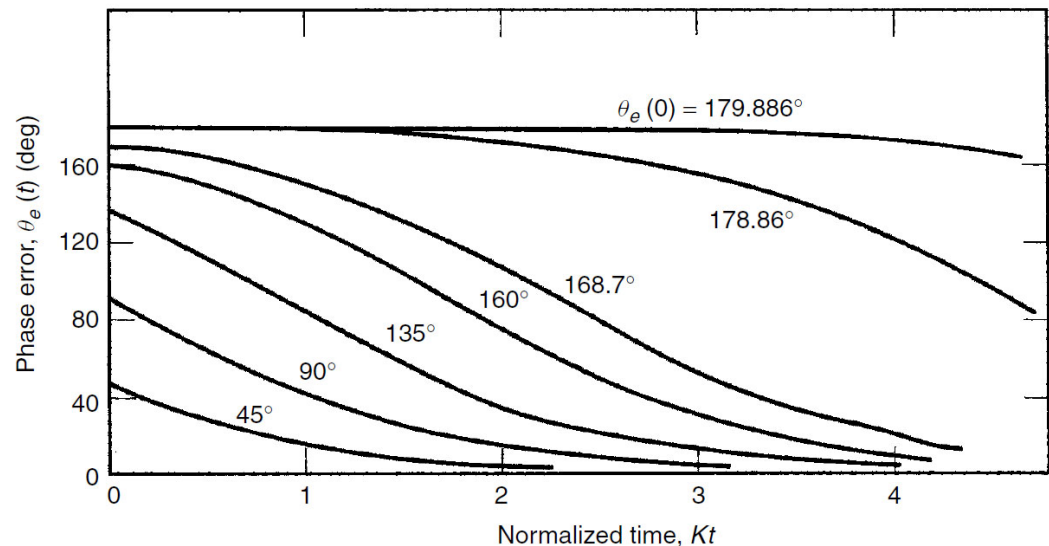
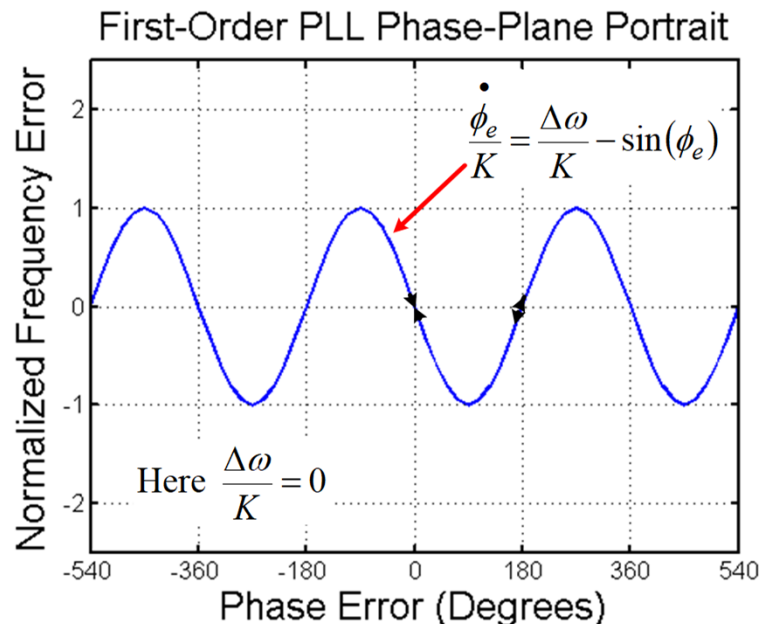
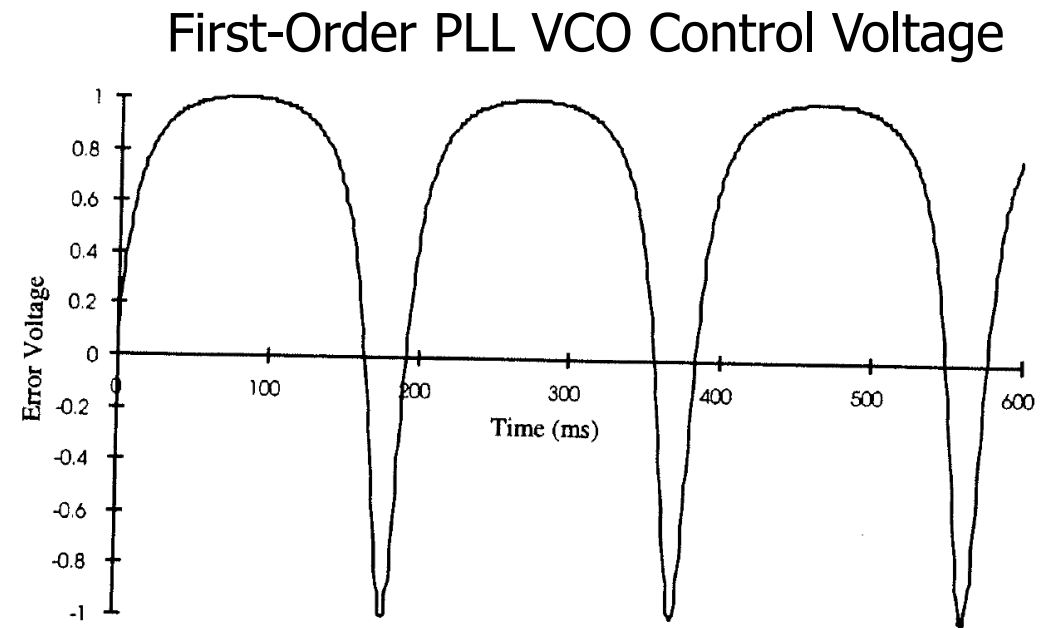
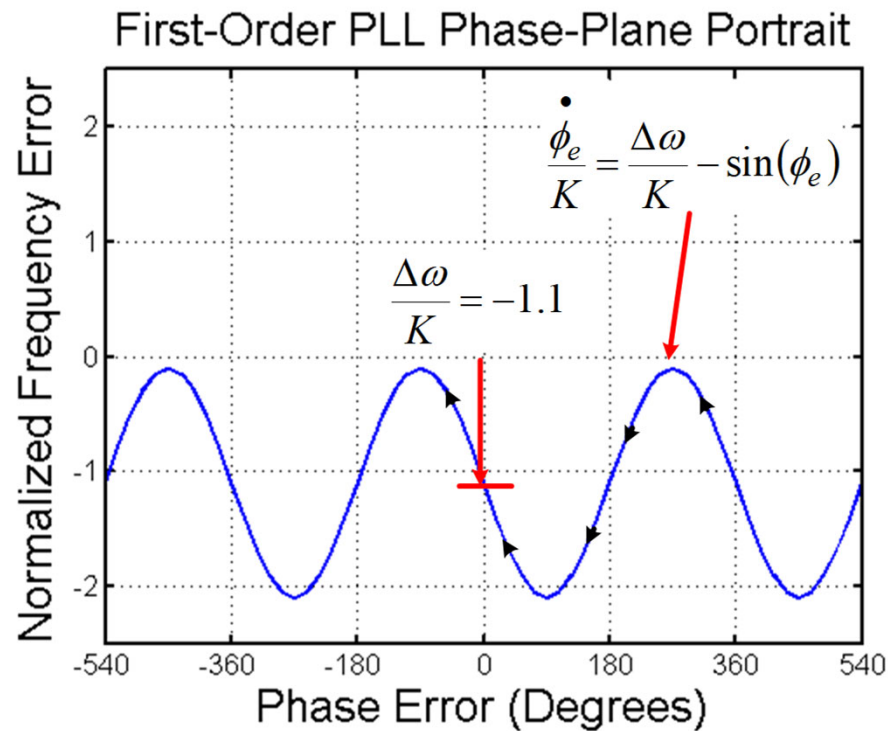


Figure 8.2 Transient phase errors in a first-order PLL, illustrating hang-up.

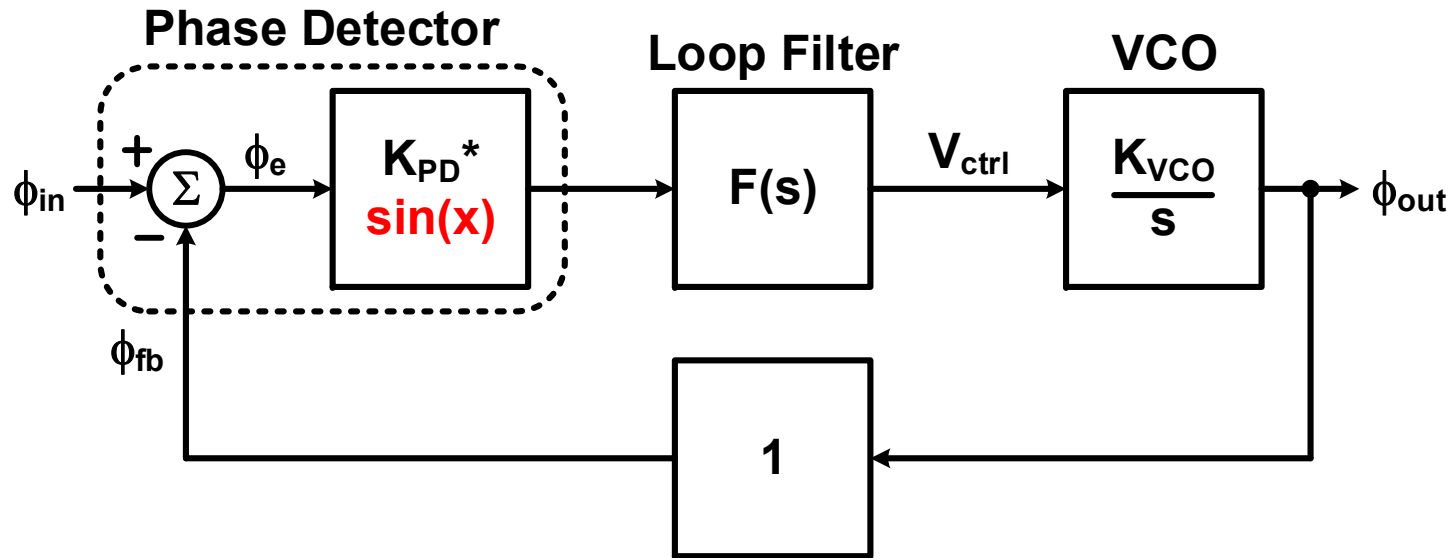
First-Order PLL Lock Failure (Sinusoidal PD)



$$\text{Hold Range : } |\Delta\omega_H| < K \text{ (rad/sec)}$$

- If the frequency offset exceeds the PLL hold range, the phase error will oscillate asymmetrically as the PLL undergoes cycle slips

Second-Order Type-2 PLL Phaselock Acquisition (Sinusoidal PD)



Assuming a second - order type - 2 PLL with a sinusoidal PD

$$F(s) = \frac{\tau_2 s + 1}{\tau_1 s} = \frac{\tau_2}{\tau_1} + \frac{1}{\tau_1 s}$$

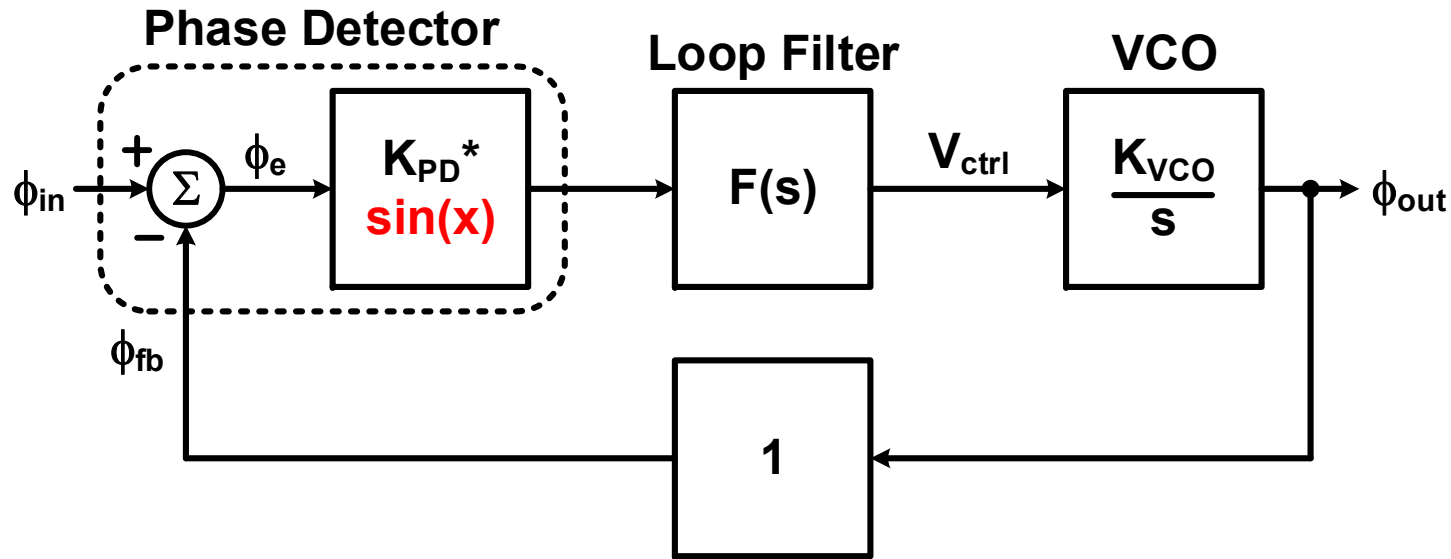
The filter response in the time - domain can be expressed as

$$v_c(t) = \frac{\tau_2}{\tau_1} v_e(t) + \frac{1}{\tau_1} \int_0^t v_e(\tau) d\tau = \frac{\tau_2}{\tau_1} K_{PD} \sin(\phi_e(\tau)) + \frac{1}{\tau_1} \int_0^t K_{PD} \sin(\phi_e(\tau)) d\tau$$

The PLL output phase is

$$\phi_{out}(t) = \omega_o t + \int_0^t K_{VCO} v_c(\tau) d\tau + \phi_{out}(0) = \omega_o t + K_{VCO} K_{PD} \left(\int_0^t \frac{\tau_2}{\tau_1} \sin(\phi_e(\tau)) d\tau + \int_0^t \left(\frac{1}{\tau_1} \int_0^\tau \sin(\phi_e(\tau)) d\tau \right) d\tau \right) + \phi_{out}(0)$$

Second-Order Type-2 PLL Phaselock Acquisition (Sinusoidal PD)



The PLL phase error is

$$\phi_e = \phi_{ref} - \phi_{out} = (\omega_{ref} - \omega_o)t - K_{VCO}K_{PD} \left(\int_0^t \frac{\tau_2}{\tau_1} \sin(\phi_e(\tau)) d\tau + \int_0^t \left(\frac{1}{\tau_1} \int_0^\tau \sin(\phi_e(\tau)) d\tau \right) d\tau \right) - \phi_{out}(0)$$

Differentiating this twice w.r.t. time yields the following nonlinear differential equation

$$\ddot{\phi}_e = -K_{VCO}K_{PD} \left(\frac{\tau_2}{\tau_1} \cos(\phi_e) \dot{\phi}_e + \frac{1}{\tau_1} \sin(\phi_e) \right)$$

Second-Order Type-2 PLL Phaselock Acquisition (Sinusoidal PD)

For this Second - Order Type - 2 PLL, the natural frequency and damping factor are

$$\omega_n^2 = \frac{K_{PD}K_{VCO}}{\tau_1}, \quad \zeta = \sqrt{\frac{\tau_2^2 K_{PD}K_{VCO}}{4\tau_1}}$$

Substituting this into the nonlinear differential equation yields the following

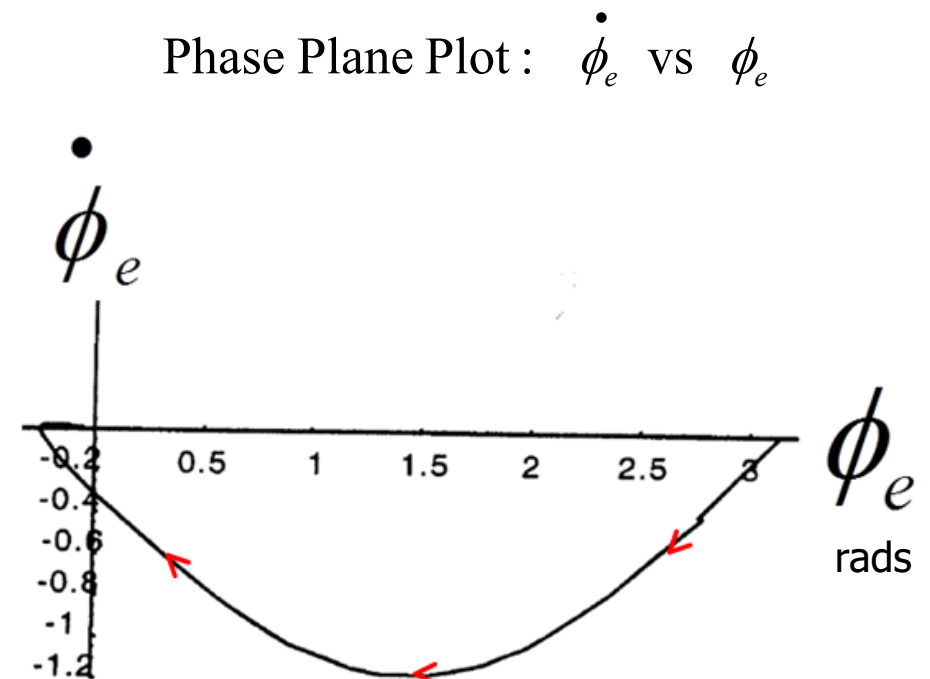
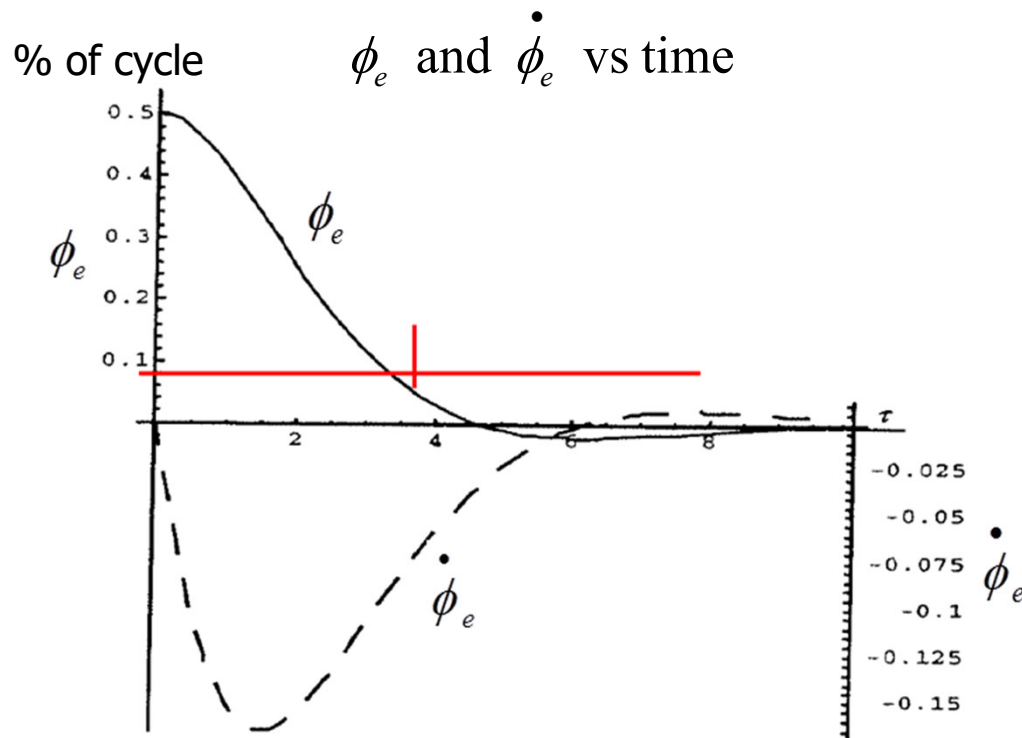
$$\ddot{\phi}_e + 2\zeta\omega_n \cos(\phi_e)\dot{\phi}_e + \omega_n^2 \sin(\phi_e) = 0$$

- No closed form solution exists, and numerical techniques are required to solve

Second-Order Type-2 PLL Phaselock Acquisition (Sinusoidal PD)

$$\ddot{\phi}_e + 2\zeta\omega_n \cos(\phi_e)\dot{\phi}_e + \omega_n^2 \sin(\phi_e) = 0$$

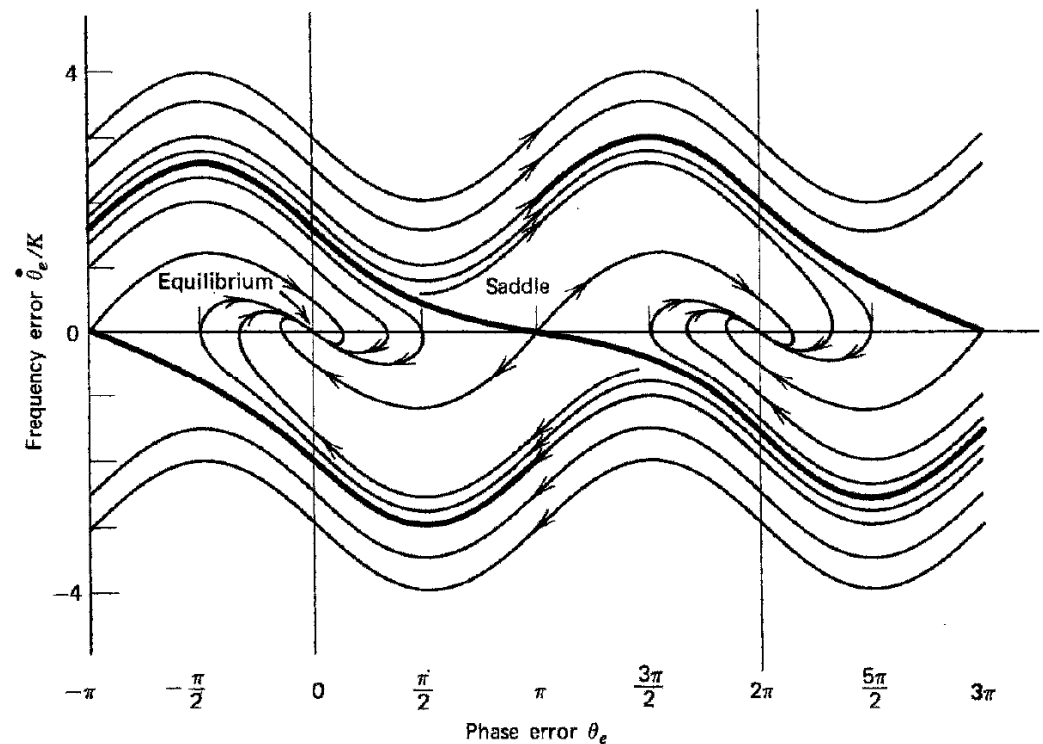
Acquisition with a phase error



Second-Order PLL Phase Plane Plots (Sinusoidal PD)

- An unstable singularity is called a Saddle Point
- A trajectory that terminates on a saddle point is called a "Separatrix"
- If a trajectory lies between the 2 separatrices, it will lock without cycle slipping
- If a trajectory lies outside the 2 separatrices, it will cycle slipping one or more times before locking (if at all)

$$\ddot{\phi}_e + 2\zeta\omega_n \cos(\phi_e)\dot{\phi}_e + \omega_n^2 \sin(\phi_e) = 0$$



Second-Order PLL Pull-Out Range and Lock Time (Sinusoidal PD)

- The **Pull-Out Range** is the maximum frequency step that can occur before the loop locks without cycle slipping

$$\Delta\omega_{PO} \approx 1.8\omega_n(\zeta + 1)$$

for ζ between 0.5 and 1.4

If a frequency step is less than the pull - out range, the PLL acquisition time can be approximated as

$$t_{acq} = t_{phase} + t_{freq} = \frac{4}{\omega_n} + \frac{4.2(\Delta f)^2}{B_L^3}$$

for phase error less than 10%

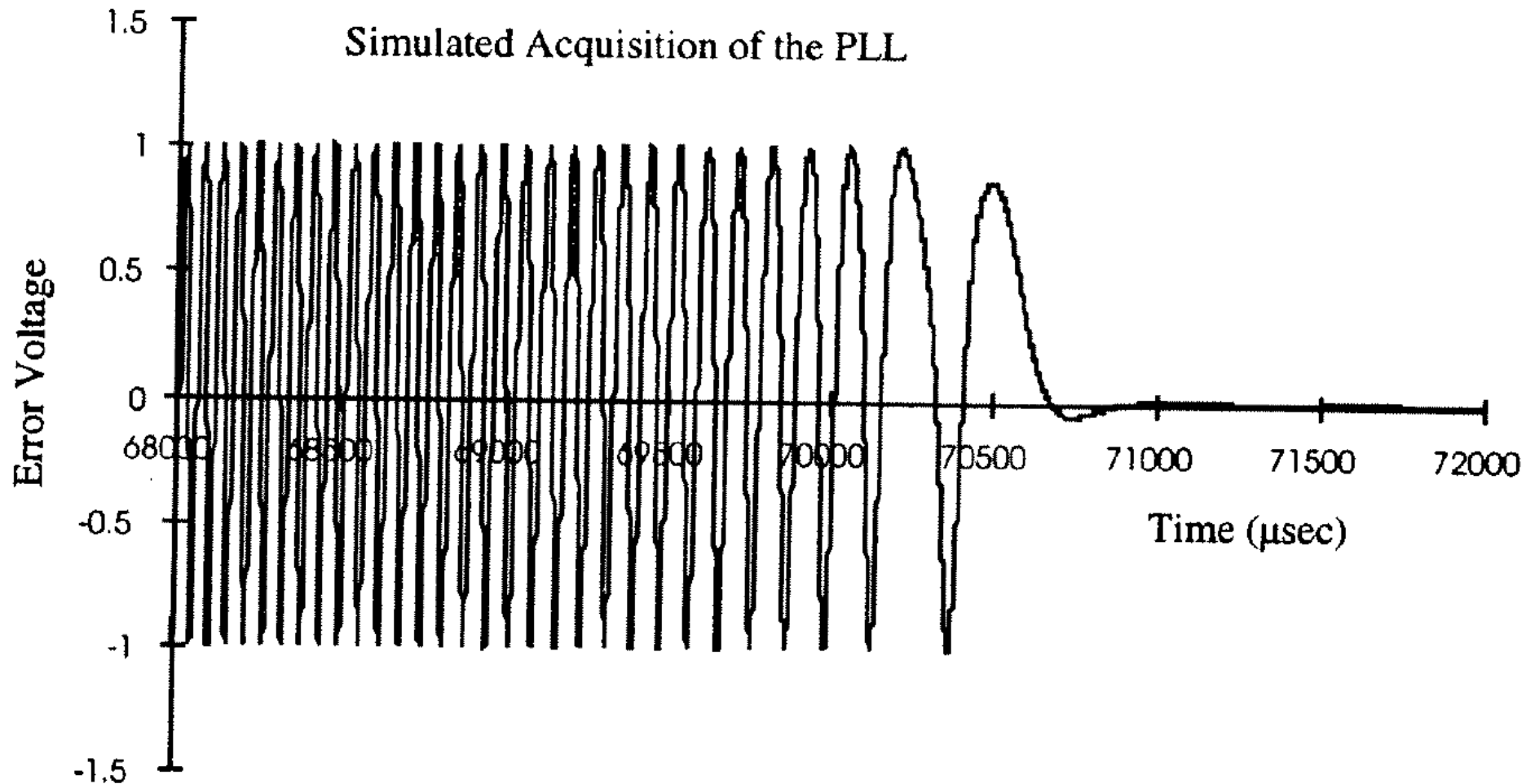
Here, B_L is the PLL noise bandwidth

$$B_L = \int_0^{\infty} |H(f)|^2 df \quad (\text{Hz})$$

$$\text{Assuming } F(s) = \frac{\tau_2 s + 1}{\tau_1 s} = \frac{\tau_2}{\tau_1} + \frac{1}{\tau_1 s},$$

$$B_L = \frac{\omega_n}{2} \left(\zeta + \frac{1}{4\zeta} \right) \quad (\text{Hz})$$

Second-Order PLL Locking Outside of the Pull-Out Range (Sinusoidal PD)



- Multiple cycle slips are observed before the loop locks

Agenda

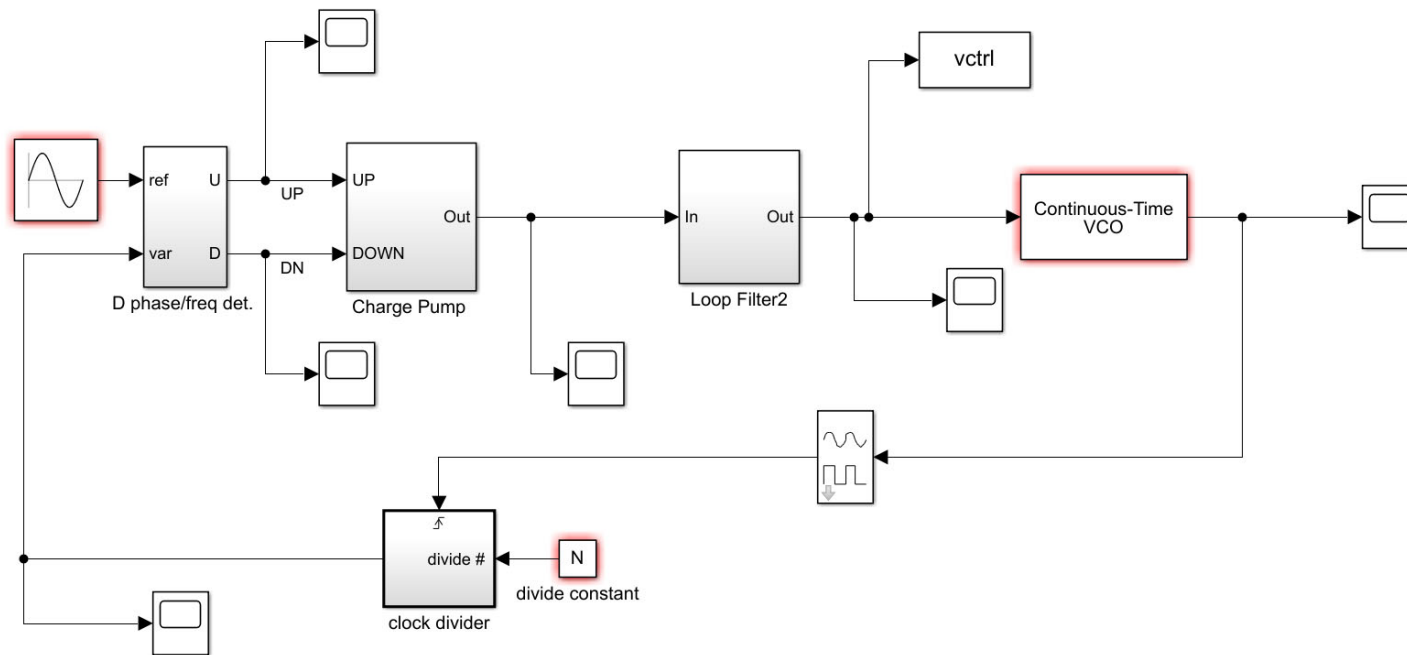
- PLL Overview
- PLL Linear Model
- PLL Stability
- Analog Charge Pump PLL Design Procedure
- PLL Noise Transfer Functions
- PLL Transient Behavior
- PLL Time Domain Modeling

Time Domain Model

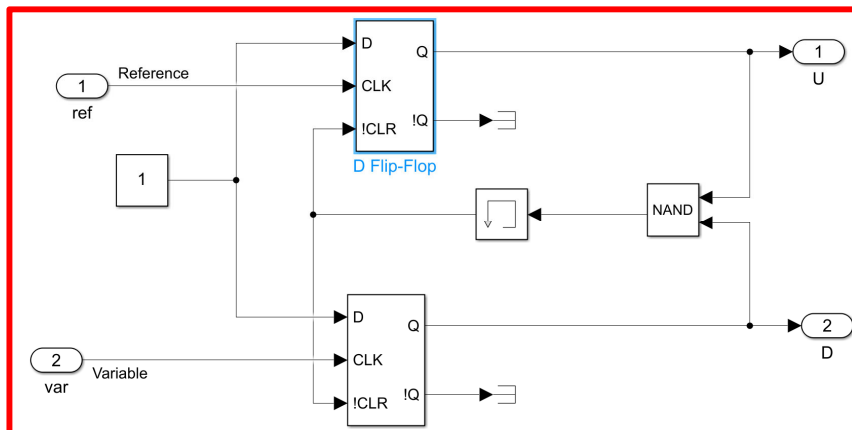
- Time domain models captures the discrete-time operation of the PLL architectures
 - Interaction between charge pump and loop filter
 - Cycle slipping behavior
- Allows modeling of non-linear control systems
 - Dynamic loop bandwidth control
 - Automatic frequency band selection
- Potential implementation tools
 - Matlab Simulink
 - CppSim
 - Cadence

Simulink Model

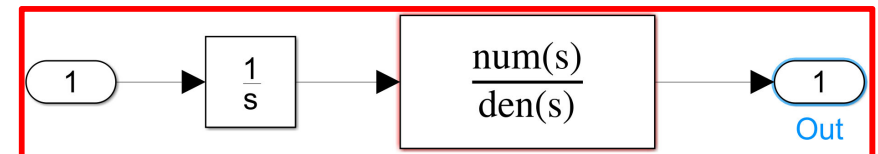
PLL FREQUENCY SYNTHESIZER MODEL



PFD

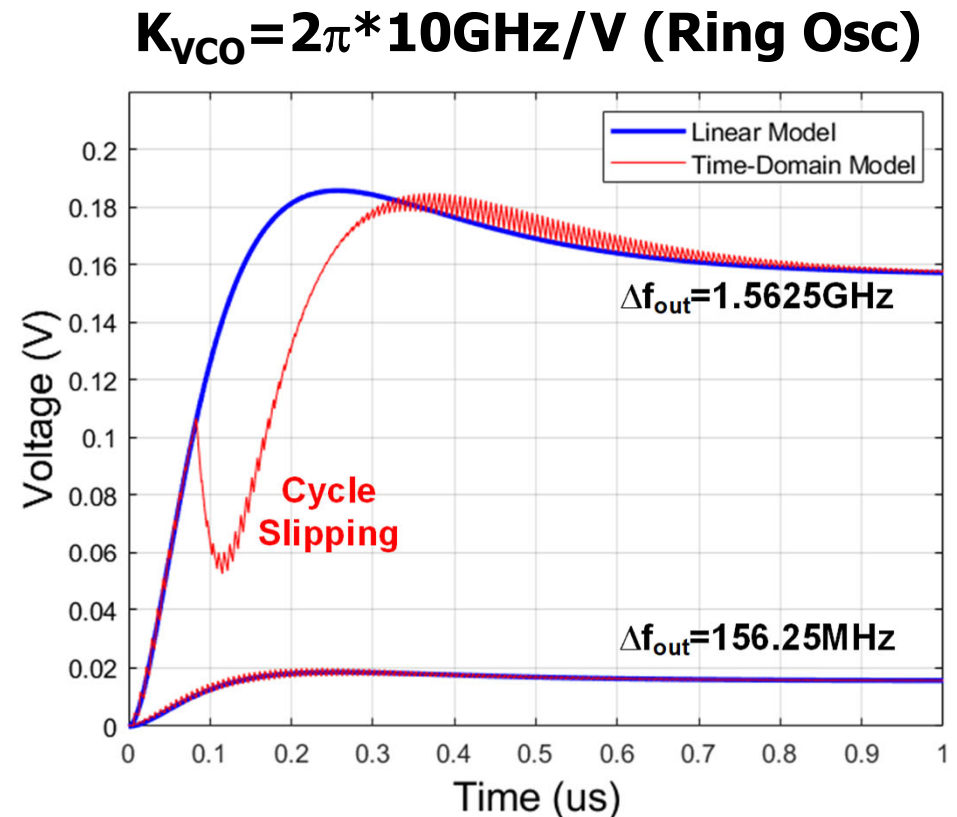
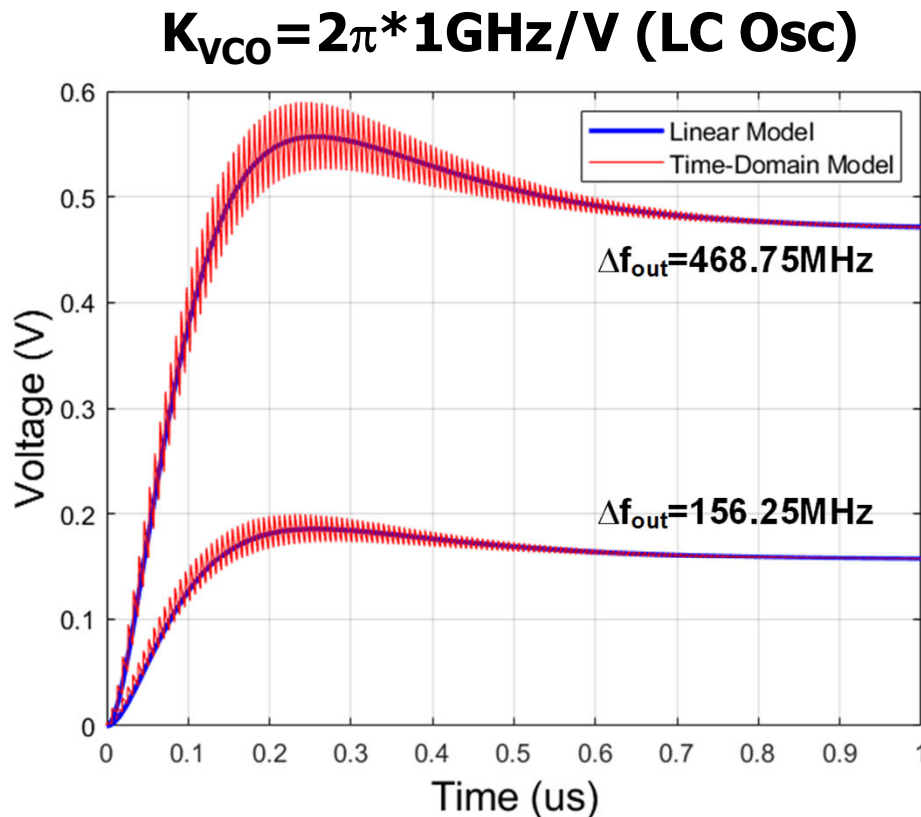


Loop Filter



Frequency Step w/ Simulink Model

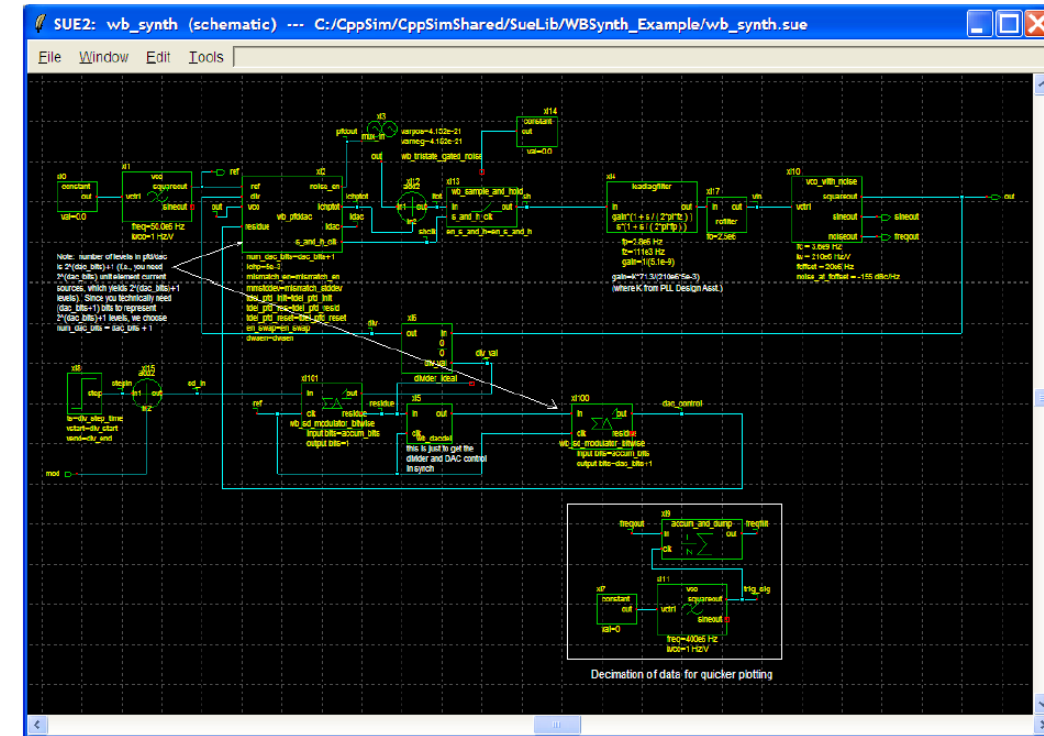
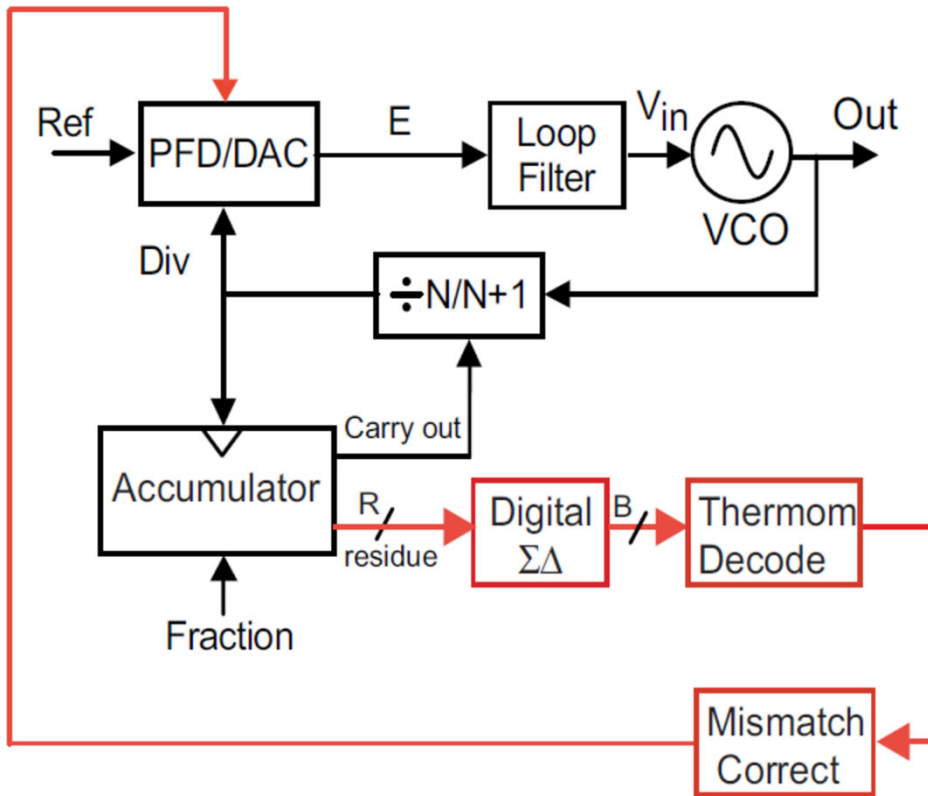
- VCO control voltage response to input frequency step



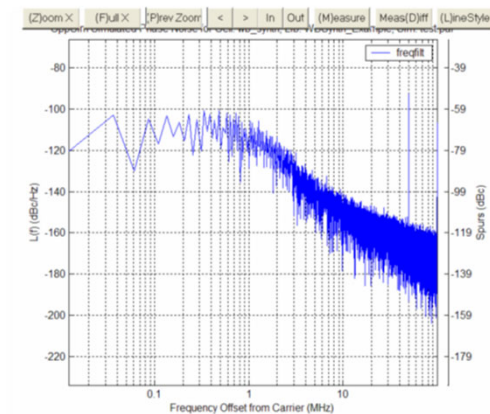
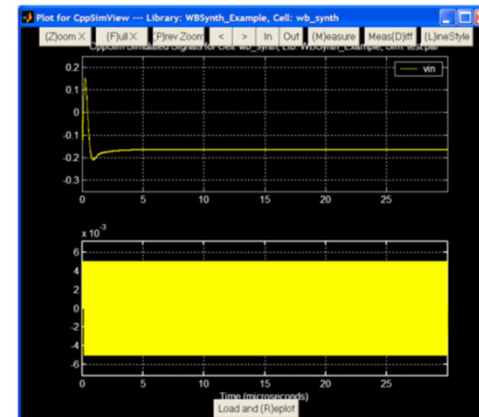
- Voltage spikes due to charge pump current driving loop filter resistor
- Cycle slipping occurs during lock acquisition due to large initial frequency difference

CppSim Model

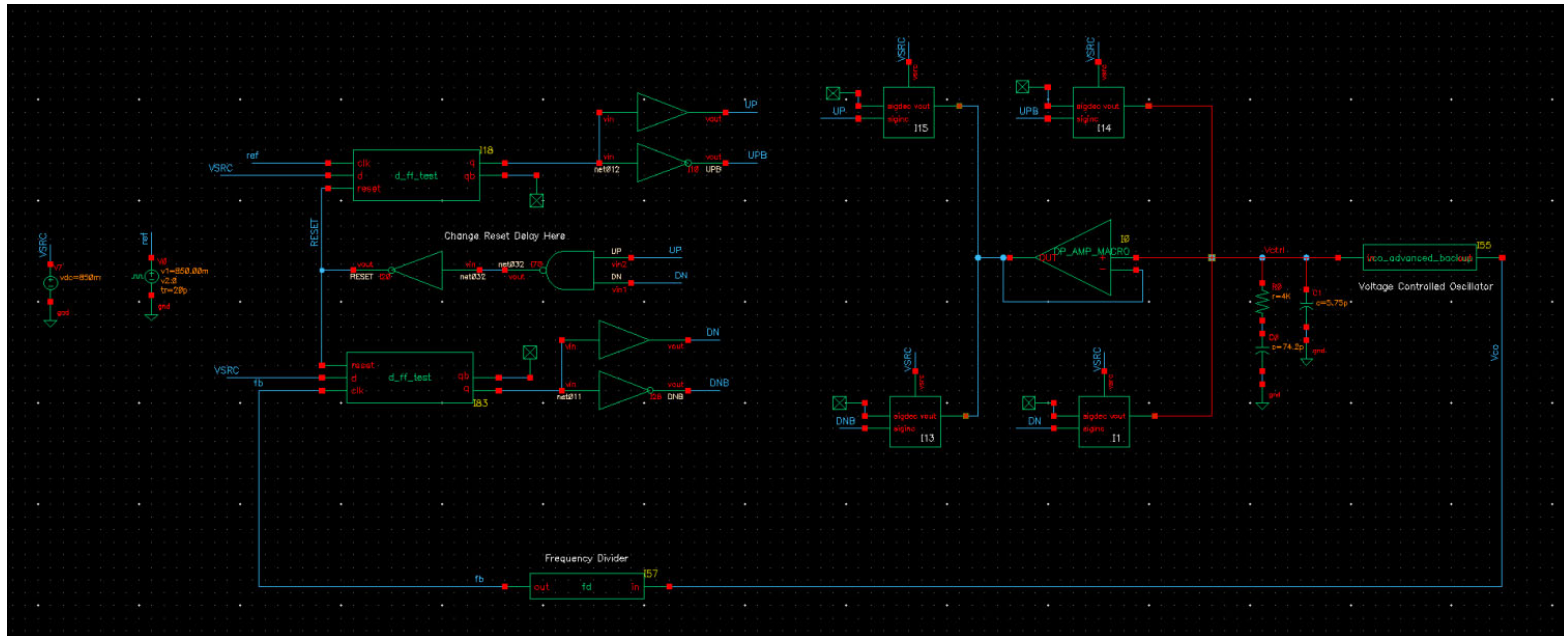
[Perrott/Meninger]



- <https://cppsim.com/>
- C++ based allows for rapid simulation of advanced architectures
- Many useful building blocks included

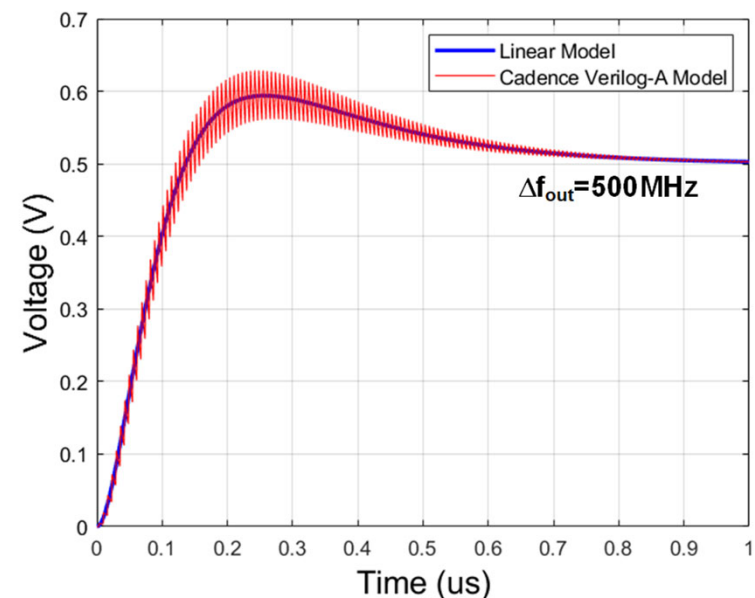


Cadence Verilog-A Model



VCO (Square Wave) Verilog-A Code Snippet

```
module vco_advanced_backup(in, out);
input in;
output out;
voltage in, out;
parameter real Vamp = 0.425;
parameter Fmax = 14.3125G;
parameter Fmin = 13.5625G;
//... (lines omitted)
real phase;
real ideal_phase;
real dPhase ;
//... (lines omitted)
analog begin
if(V(in)<Vmin) inst_freq = Fmin;
else if(V(in) > Vmax) inst_freq = Fmax;
else inst_freq = ((V(in)-Vmin)*(Fmax-Fmin)/(Vmax-Vmin)) + Fmin ;
ideal_phase = 2*PI*idtmod(inst_freq, 0.0, 1.0, -0.5);
phase = ideal_phase + dPhase;
//... (lines omitted)
n = (phase >= -PI/2)&&(phase < PI/2);
end
V(out) <+ transition(n?Vamp:0,0,tran_time);
end
endmodule
```



Conclusion

- The way a PLL shapes noise depends on where the noise is introduced in the loop
- Optimizing the loop bandwidth for one noise source may enhance other noise sources
- Time domain modeling captures loop nonlinearities and allows for verification of advanced control schemes

Next Time

- Phase Detector Circuits