ECEN720: High-Speed Links Circuits and Systems Spring 2021

Lecture 1: Introduction

Sam Palermo

Analog & Mixed-Signal Center

Texas A&M University

Class Topics

- System and design issues relevant to high-speed electrical (and optical) signaling
- Channel properties
  - Modeling, measurements, communication techniques
- High-Speed link circuits
  - Drivers, receivers, equalizers, timing systems
- Link system design
  - Modeling and performance metrics
- Link system examples

Administrative

- Instructor:
  - Sam Palermo
  - 315E WEB, 845-4114, spalermo@tamu.edu
  - Office hours: MF 9:00AM-10:30AM
- Lectures
  - MWF 1:35PM-2:25PM, Zoom
  - Videos posted on Canvas
- Lab: W 6:00pm-8:50pm, Zoom
  - Lab begins on January 27
- Class web page
  - https://people.engr.tamu.edu/spalermo/ecen720.html
  - Will use Canvas for turning in assignments

Class Material

- Textbook: Class Notes and Technical Papers
- Key References
  - *Digital Systems Engineering*, W. Dally and J. Poulton, Cambridge University Press, 1998.
  - *Advanced Signal Integrity for High-Speed Digital Designs,* S. H. Hall and H. L. Heck, John Wiley & Sons, 2009.
  - *High-Speed Digital Design: A Handbook of Black Magic*, H. Johnson & M. Graham, Prentice Hall, 1993.
  - *Design of Integrated Circuits for Optical Communications*, B. Razavi, McGraw-Hill, 2003.
- Class notes
  - Will post online before class

Grading

- Exams (50%)
  - Two midterm exams (25% each)
  - Posted online the day of exam around 8AM
  - You have until 5PM that day to upload your solution to Canvas
- Homework & Labs (25%)
  - Labs (Prelab + Report) and homeworks weighted equally
  - Collaboration is allowed, but independent simulations and write-ups
  - Need to setup CADENCE simulation environment
  - Turn in via Canvas
  - No late homework/labs will be graded
- Final Project (25%)
  - Groups of 1-3 students
  - Report and PowerPoint presentation required

Prerequisites

- This is a circuits AND systems class
- Circuits
  - ECEN474/704 or approval of instructor
  - Basic knowledge of CMOS gates, flops, etc…
  - Circuit simulation experience (HSPICE, Spectre)
- Systems
  - Basic knowledge of s- and z-transforms
  - Basic digital communication knowledge
  - MATLAB experience

Simulation Tools

- Matlab
- ADS (Statistical BER link analysis)
- Cadence
- 90nm CMOS device models
  - Can use other technology models if they are a 90nm or more advanced CMOS node
- Other tools, schematic, layout, etc… are optional

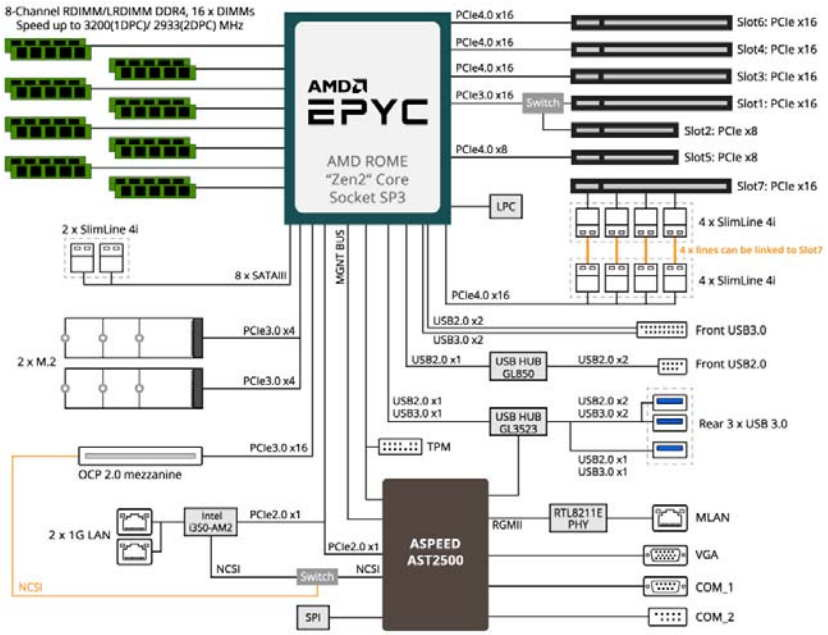
High-Speed Serial I/O

- Found in applications ranging from high-end computing systems to smart mobile devices

- Typical processor platform
  - Processor-to-memory: DDR4
  - Processor-to-peripheral: PCIe & USB
  - Storage: SATA
  - Network: LAN

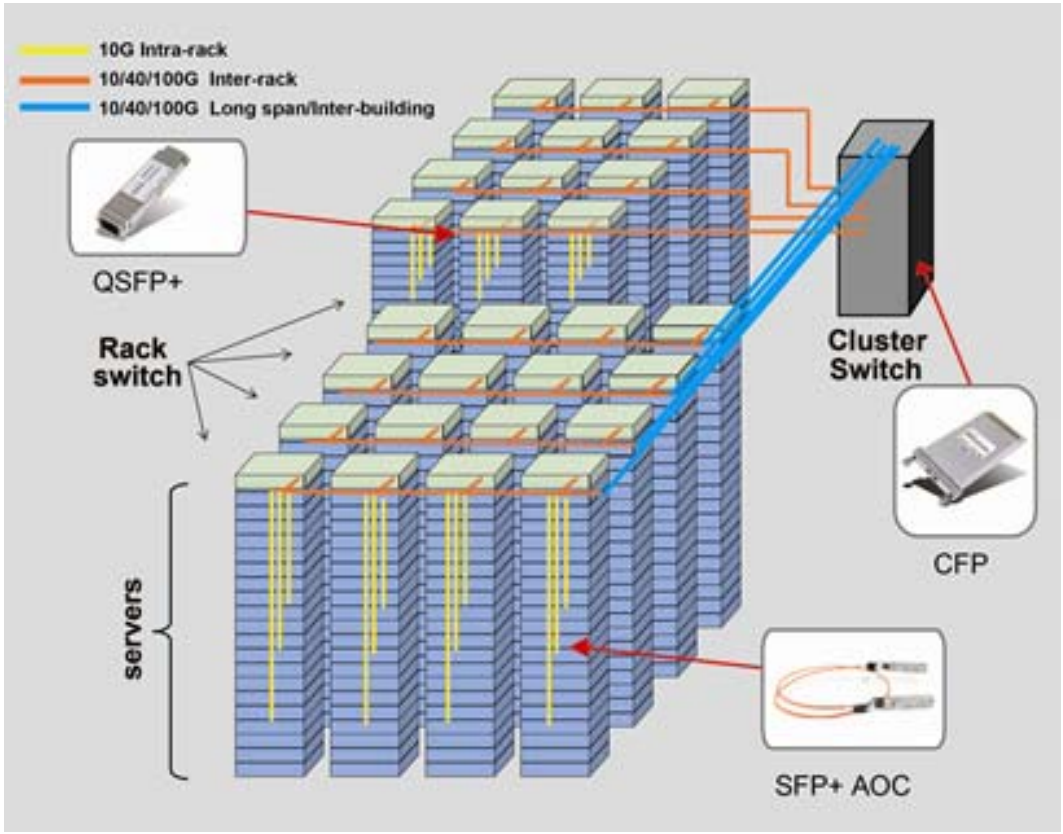
- Mobile systems
  - DSI : Display Serial Interface
  - CSI : Camera Serial Interface
  - UniPRO : MIPI Universal Protocol

AMD EPYC Rome Platform



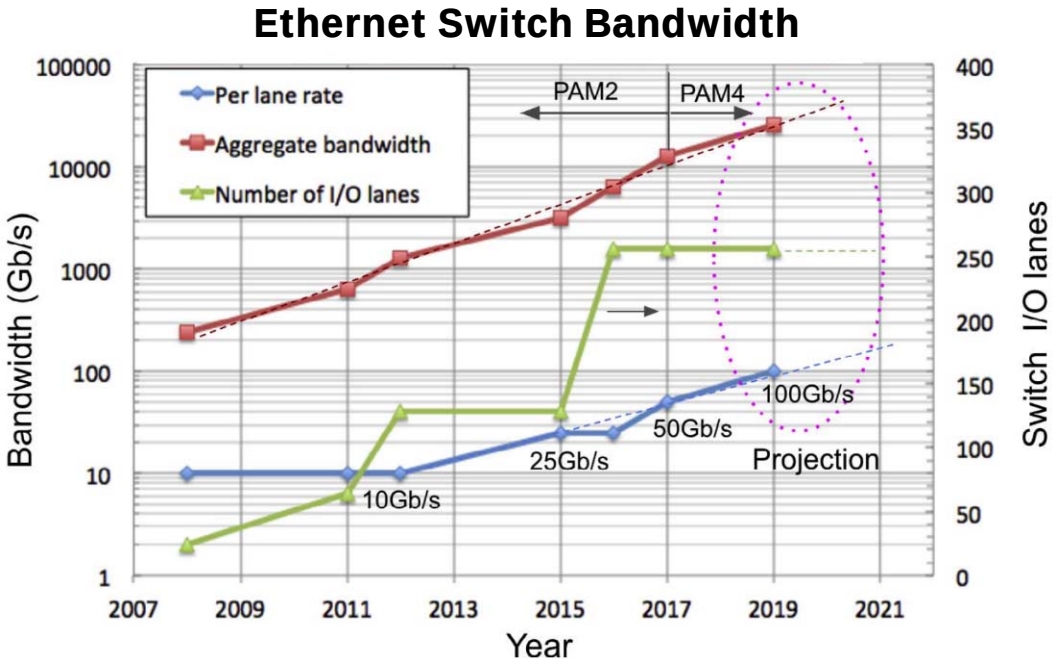
Data Center Links

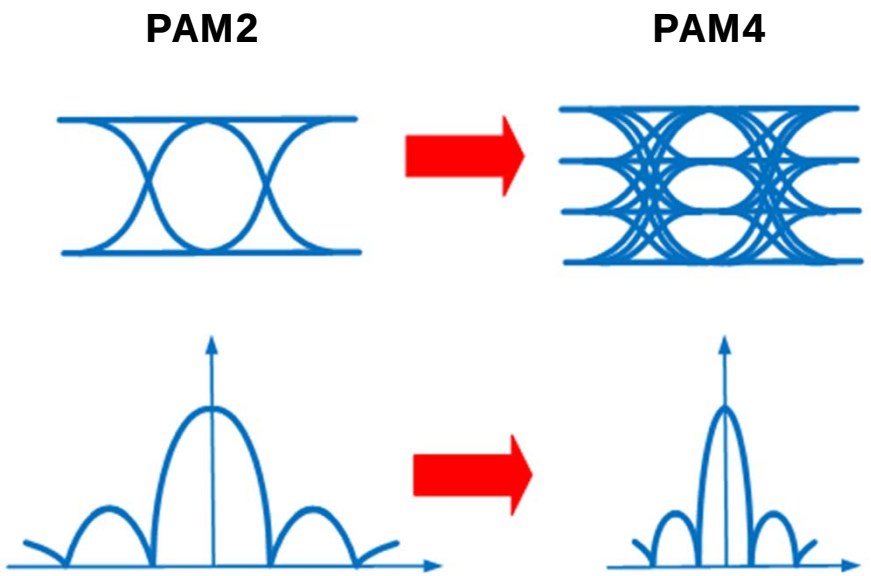
- Different interconnect technologies are used to span various distances
- Electrical I/O
  - Chip-to-module
  - Intra-rack
- Optical I/O
  - TOR switch to edge switch
  - Future intra-rack



[Gigalight]

Increasing I/O Bandwidth Demand

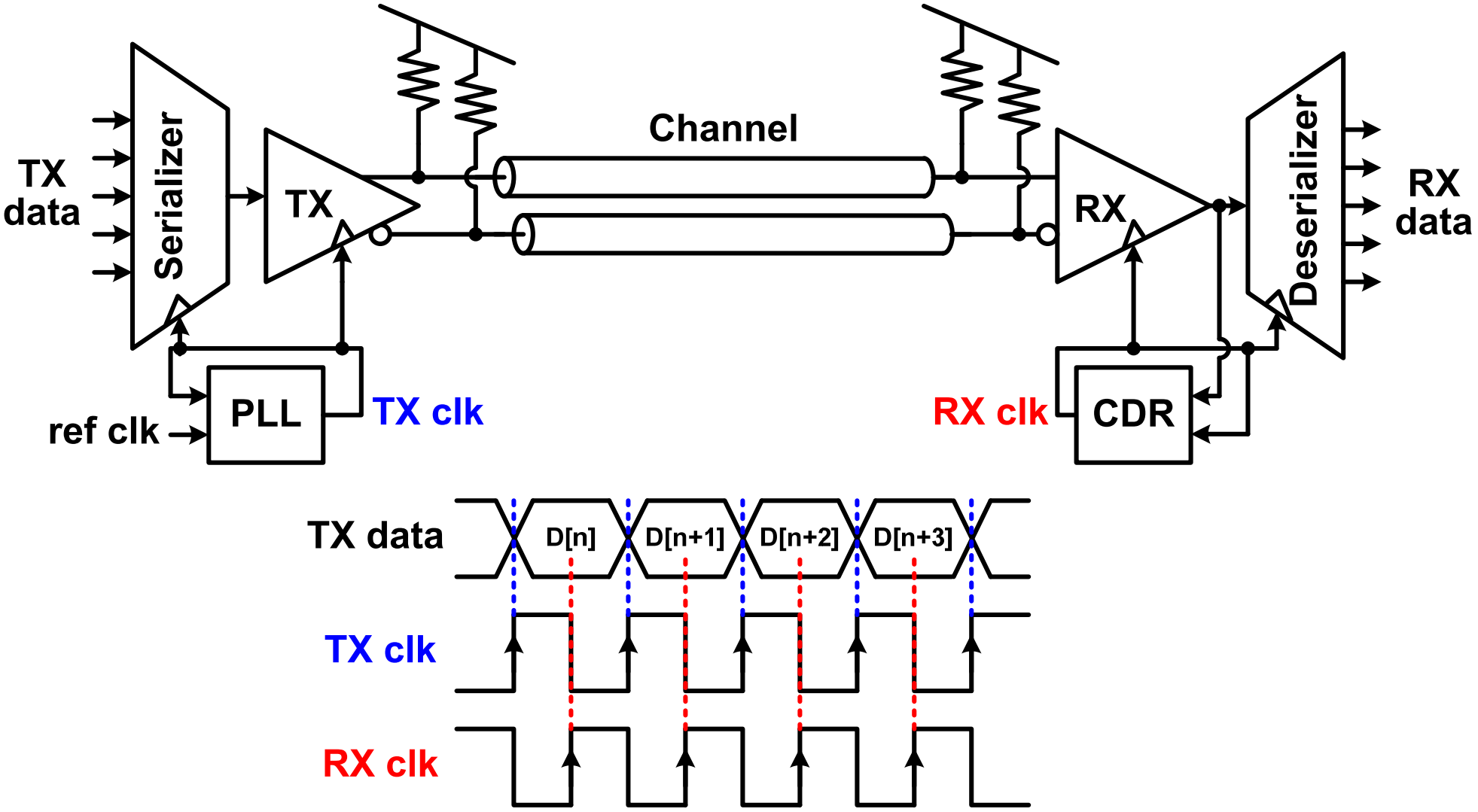




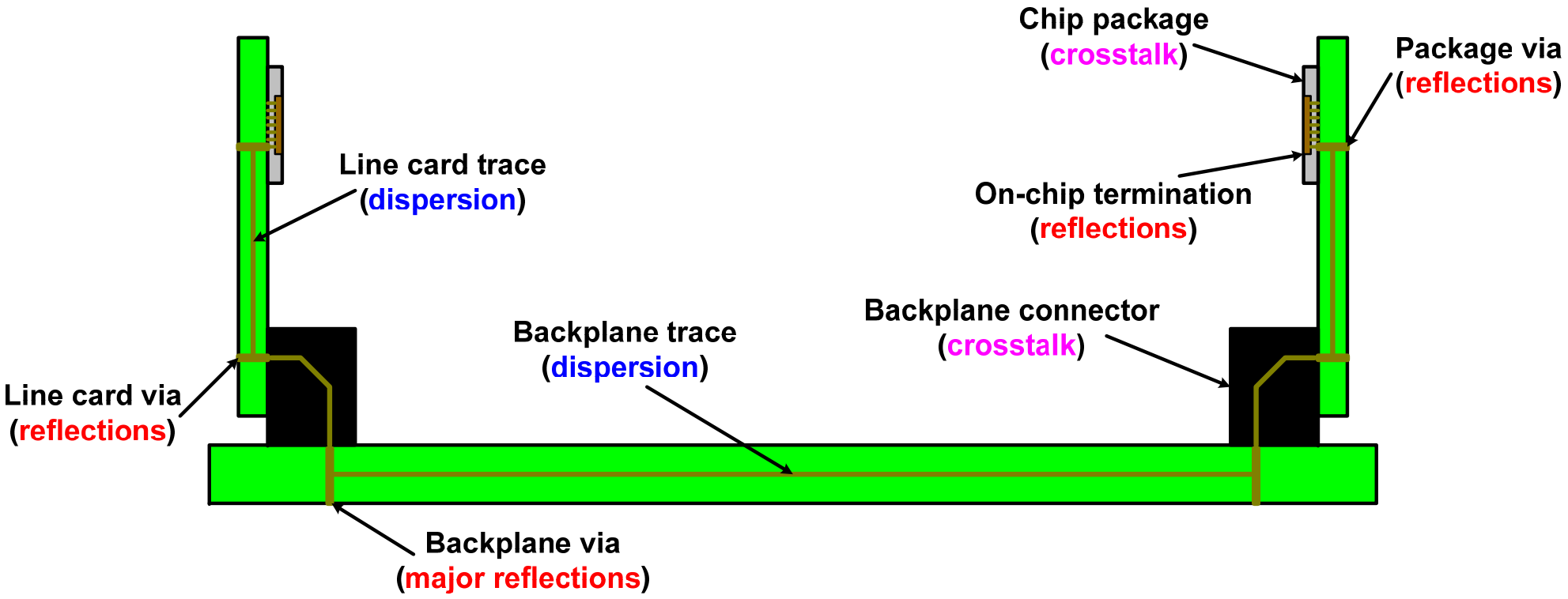
[Zhou Opt. Fiber Tech. 2017]

- Aggressive scaling of I/O data rates is required for data centers and HPC systems
- PAM4 modulation offers higher spectral efficiency and is commonly used in electrical I/Os operating above 50Gb/s

High-Speed Electrical Link System

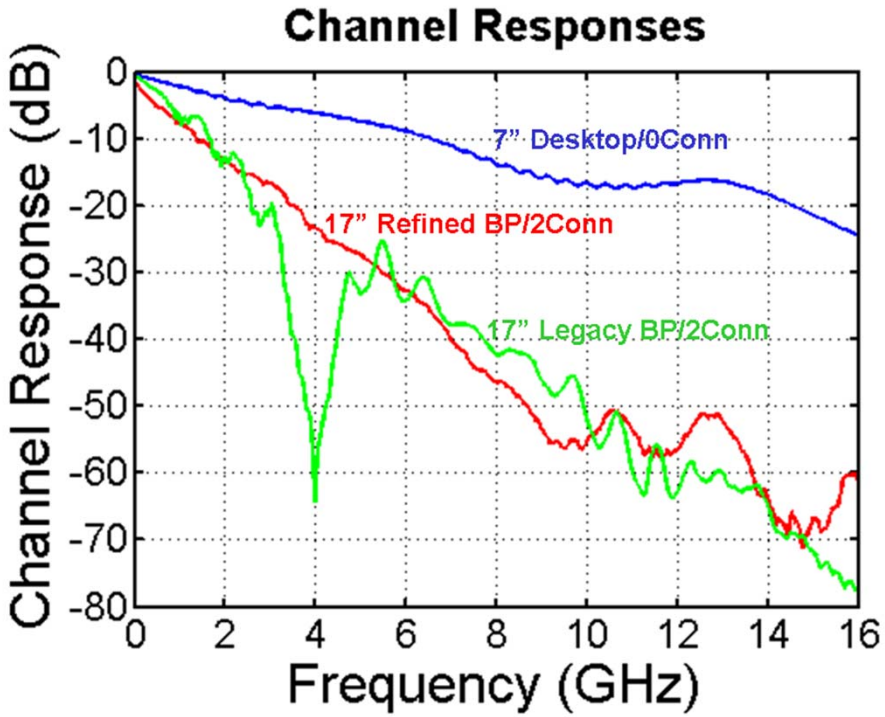


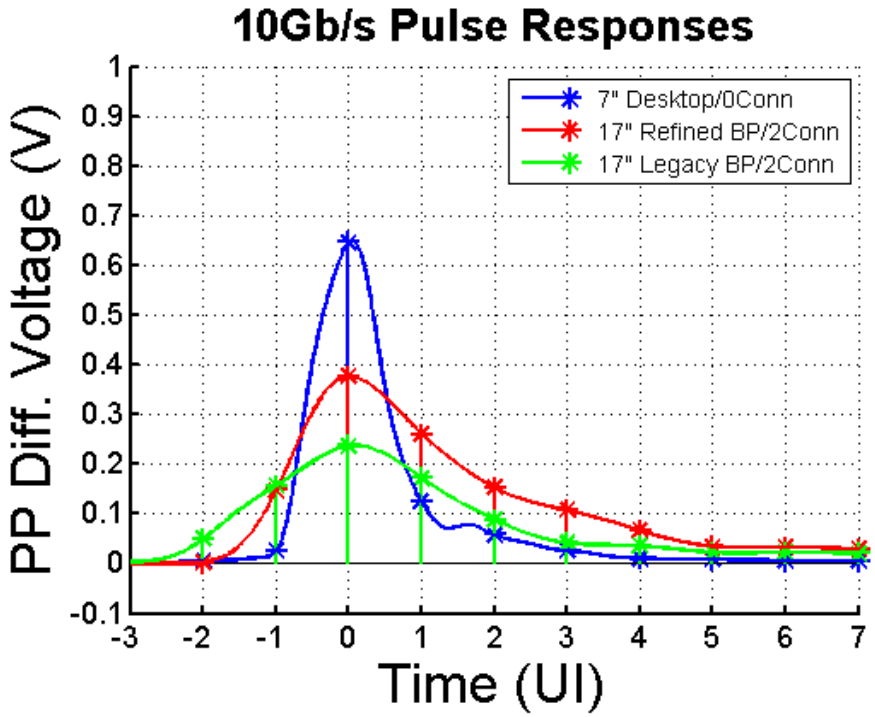
Electrical Backplane Channel

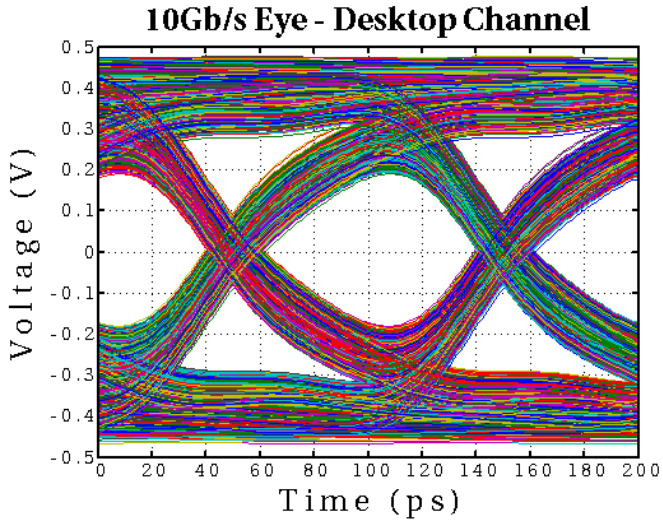


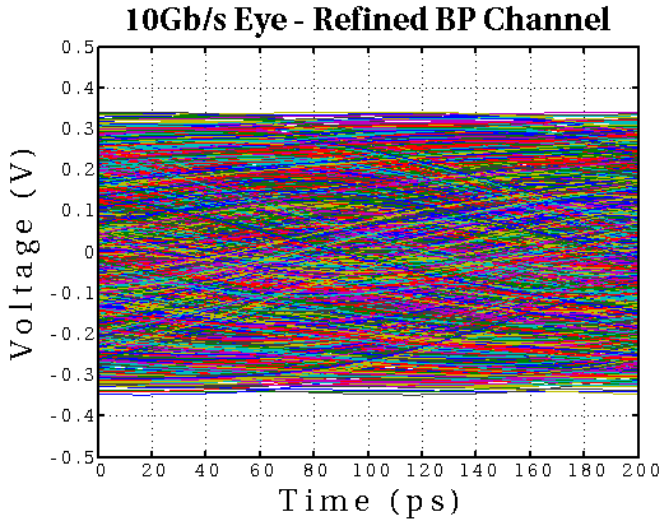
- Frequency dependent loss
  - Dispersion & reflections
- Co-channel interference
  - Far-end (FEXT) & near-end (NEXT) crosstalk

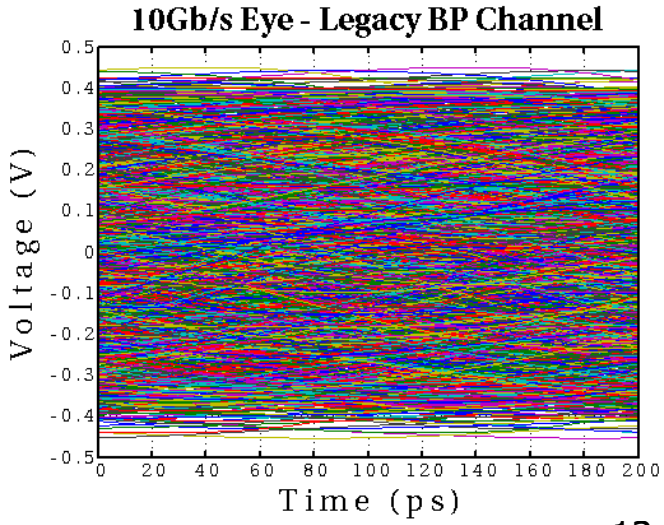
Channel Performance Impact



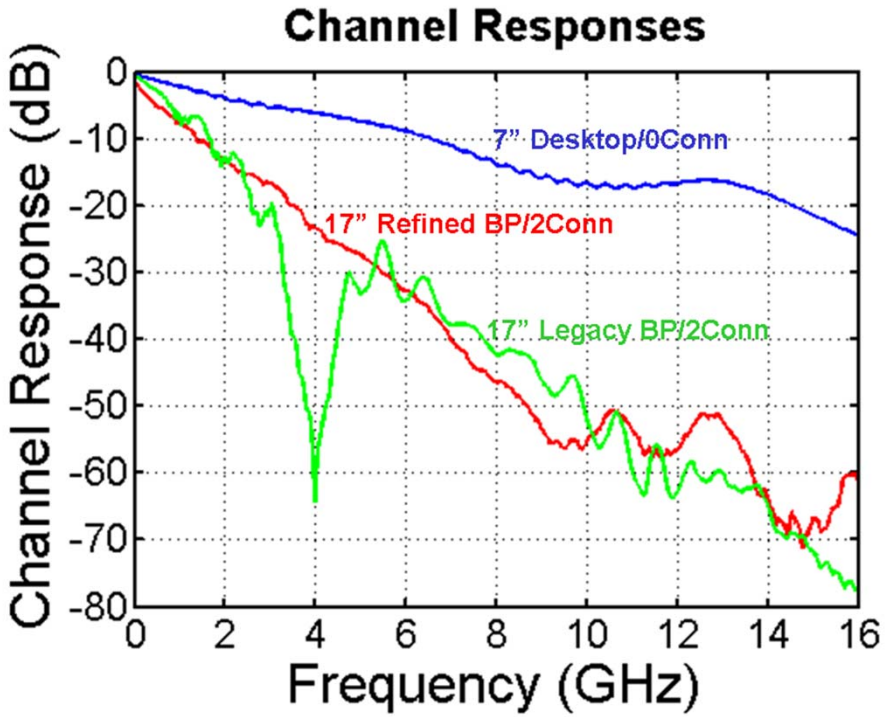


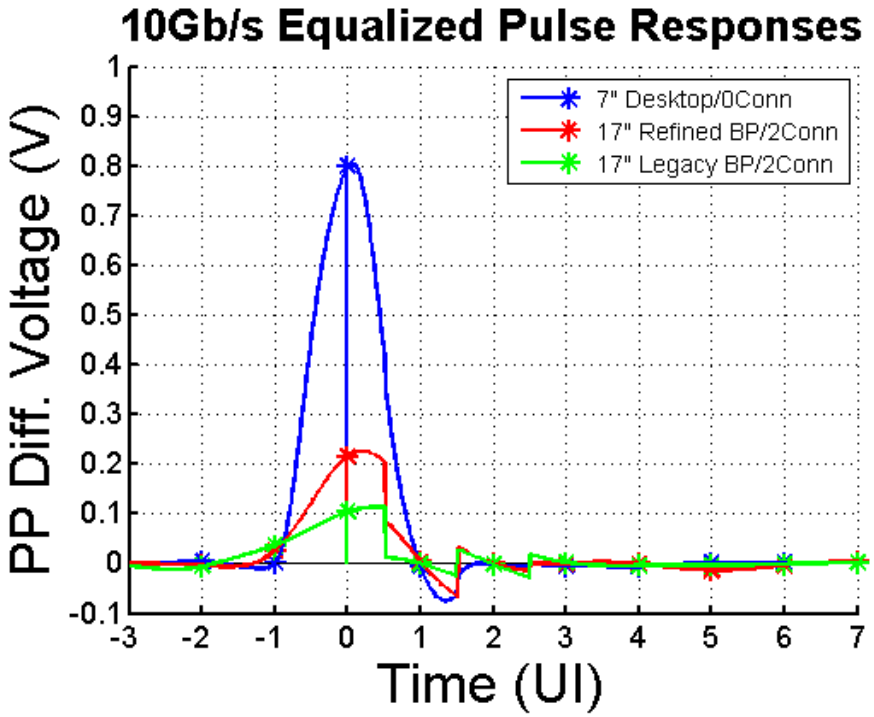


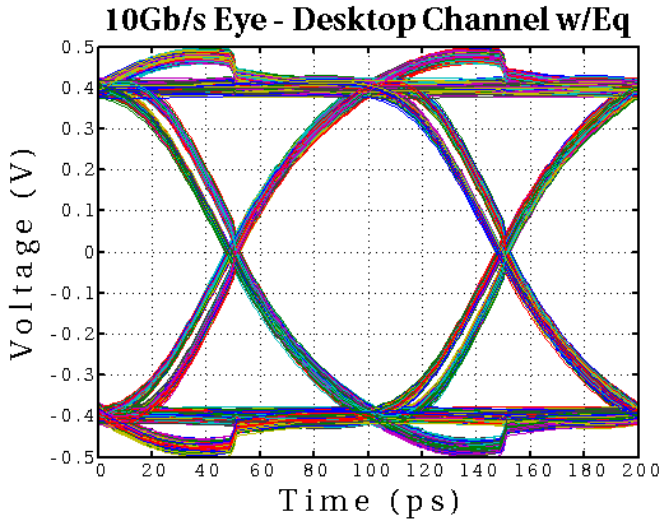


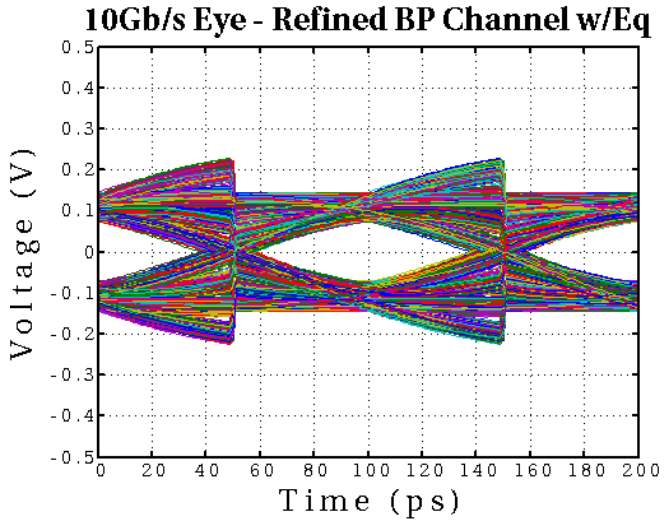


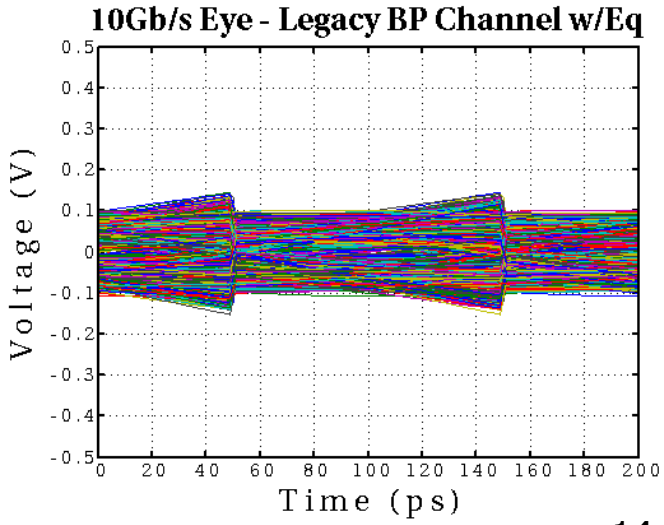
Channel Performance Impact











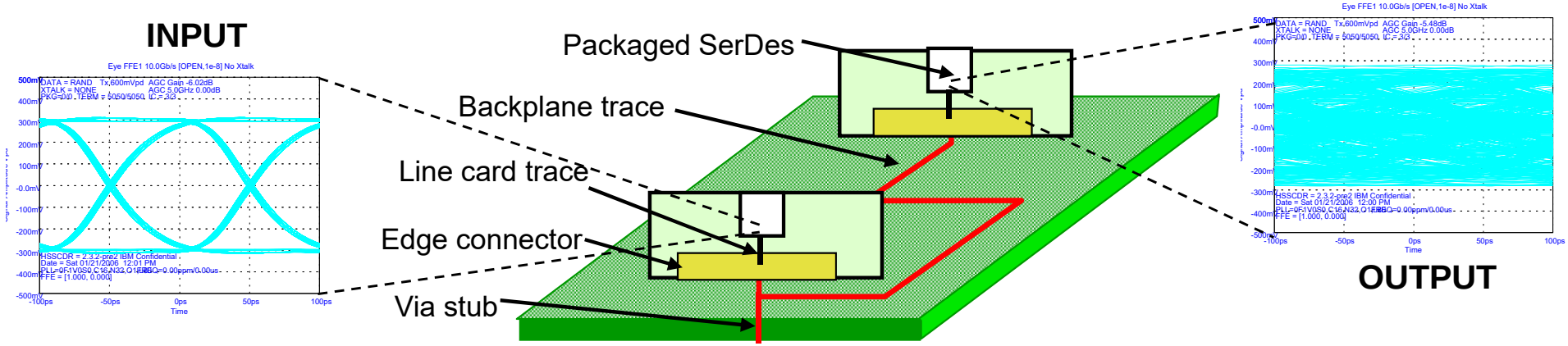
Backplane Link Example

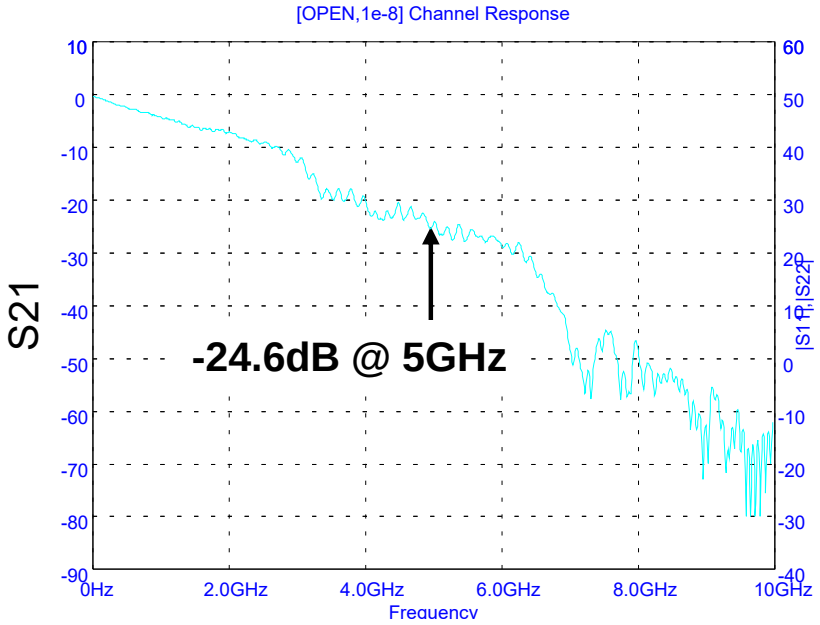
A 10Gb/s 5-tap DFE / 4-Tap FFE Transceiver in 90nm CMOS Technology

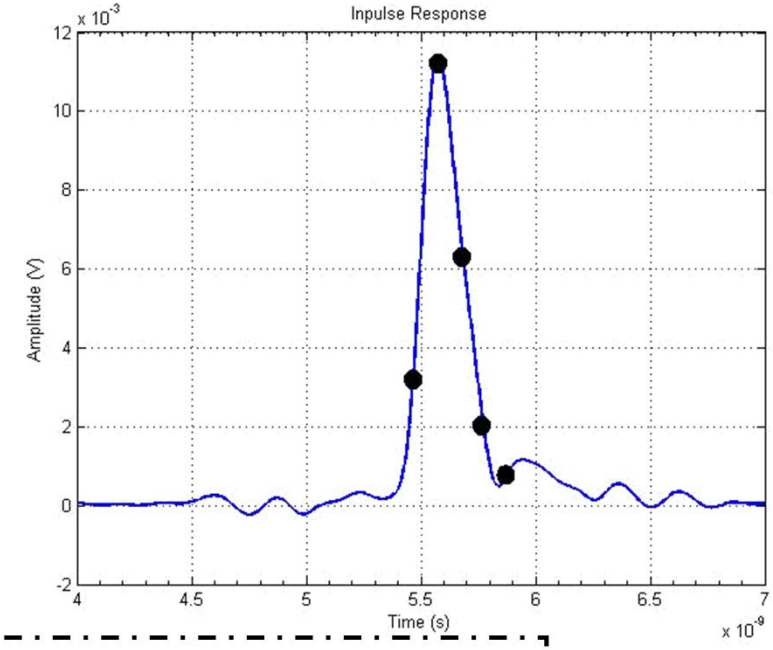
Mounir Meghelli, Sergey Rylov, John Bulzacchelli, Woogeun Rhee, Alexander Rylyakov, Herschel Ainspan, Ben Parker, Michael Beakes, Aichin Chung, Troy Beukema, Petar Pepeljugoski, Lei Shan, Young Kwark, Sudhir Gowda and Dan Friedman

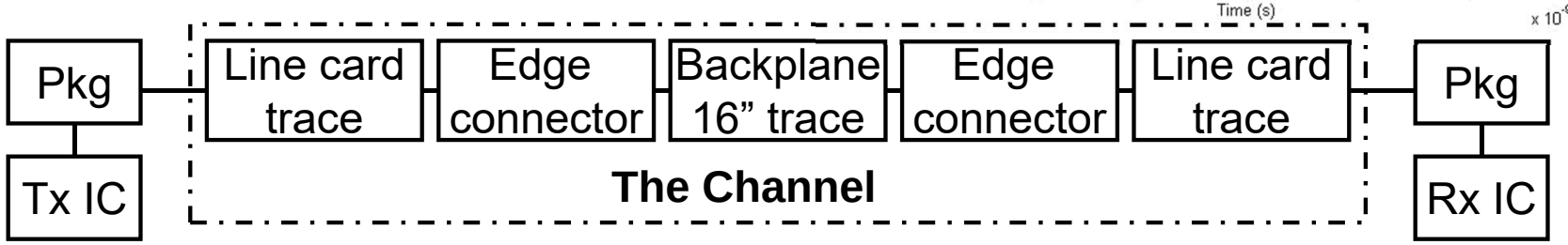
IBM T. J. Watson Research Center, Yorktown Heights, NY

Transmission Channel Impairments









[Meghelli (IBM) ISSCC 2006]

10Gb/s SerDes Main Features

- Tx with 1 baud-spaced 4-tap FFE
- Rx with 5-tap adaptive DFE and digital clock recovery
- LC-VCO based PLL for low noise clock generation
- 90nm CMOS technology

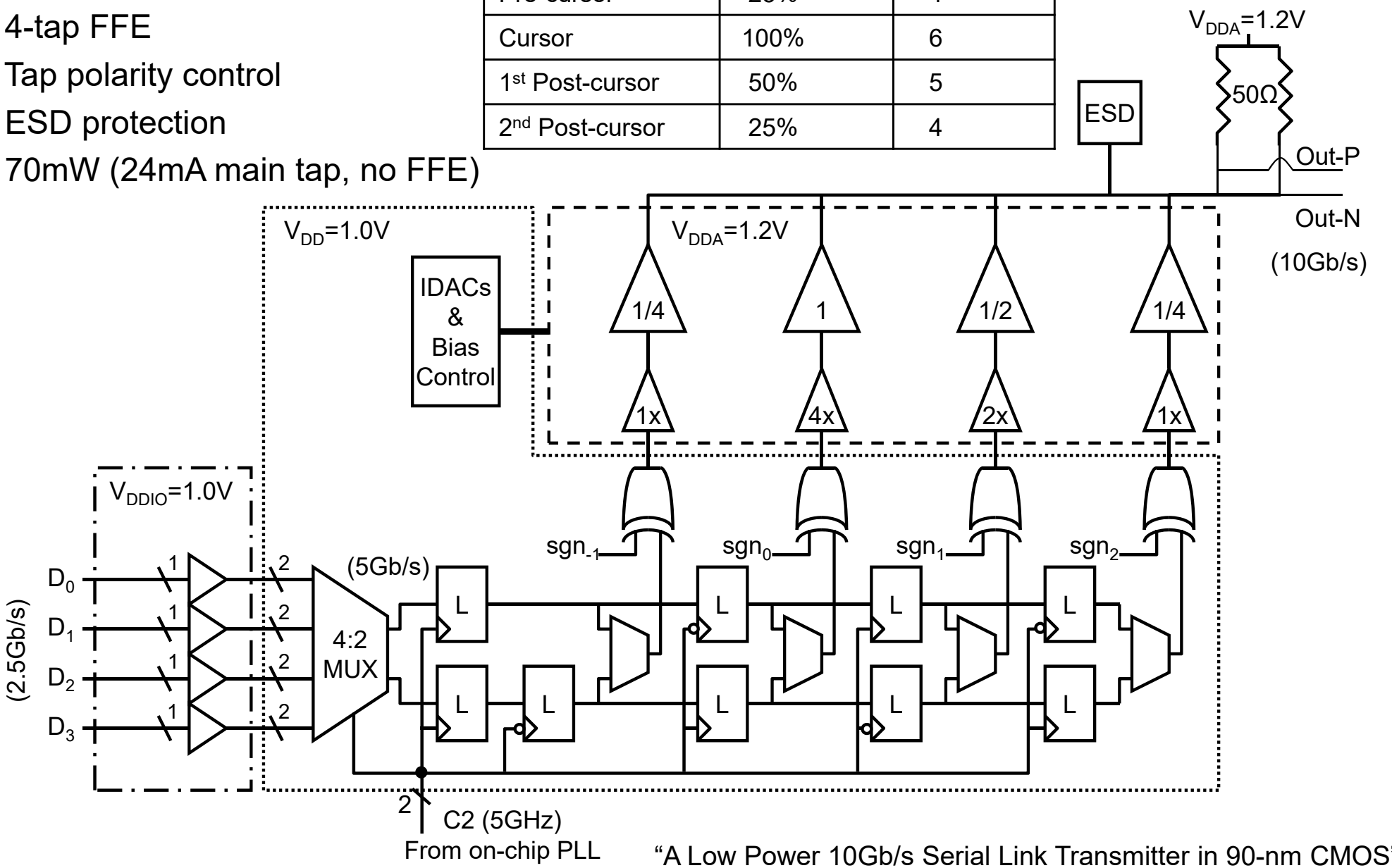
[Meghelli (IBM) ISSCC 2006]

Transmitter Architecture

Key Features:

- Half-rate CML design
- 4-tap FFE
- Tap polarity control
- ESD protection
- 70mW (24mA main tap, no FFE)

FFE Taps	Full Scale	DAC bits
Pre-cursor	25%	4
Cursor	100%	6
1st Post-cursor	50%	5
2nd Post-cursor	25%	4

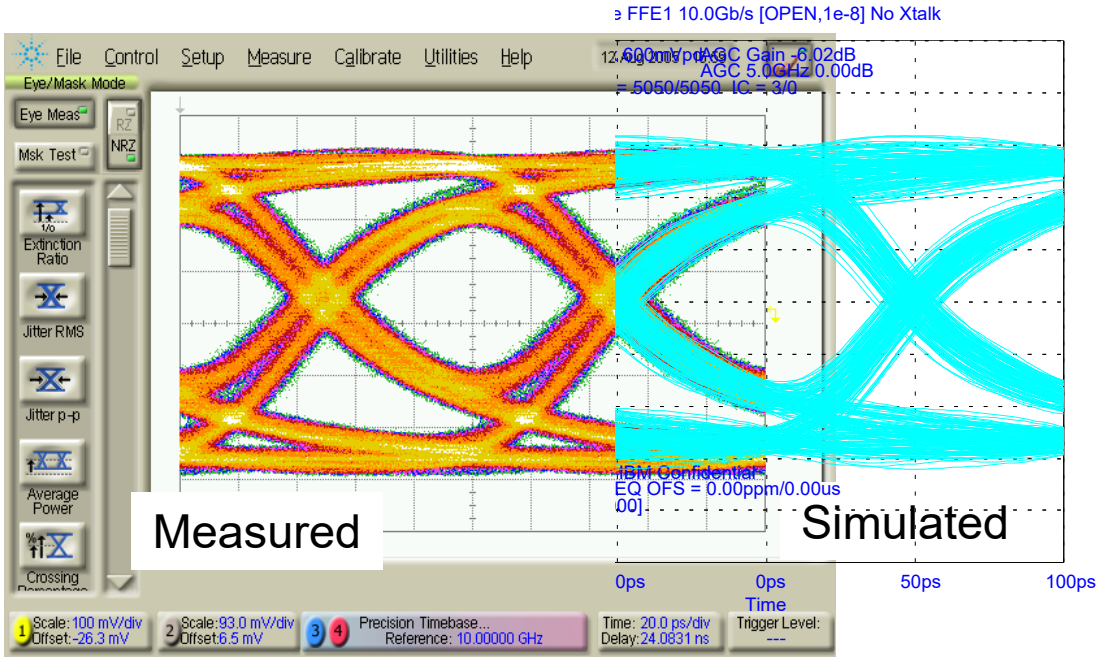


[Meghelli (IBM) ISSCC 2006]

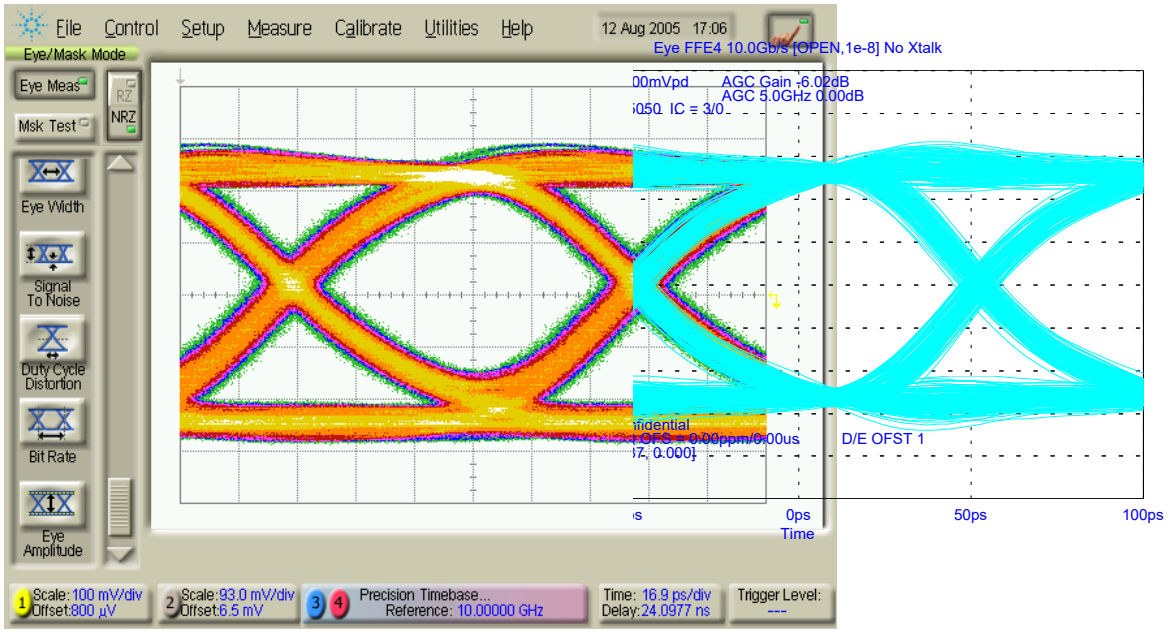
"A Low Power 10Gb/s Serial Link Transmitter in 90-nm CMOS"
A. Rylyakov et al., CSICS 2005

Tx Output Eye Diagram @ 10Gb/s

No FFE, 24mA on main tap

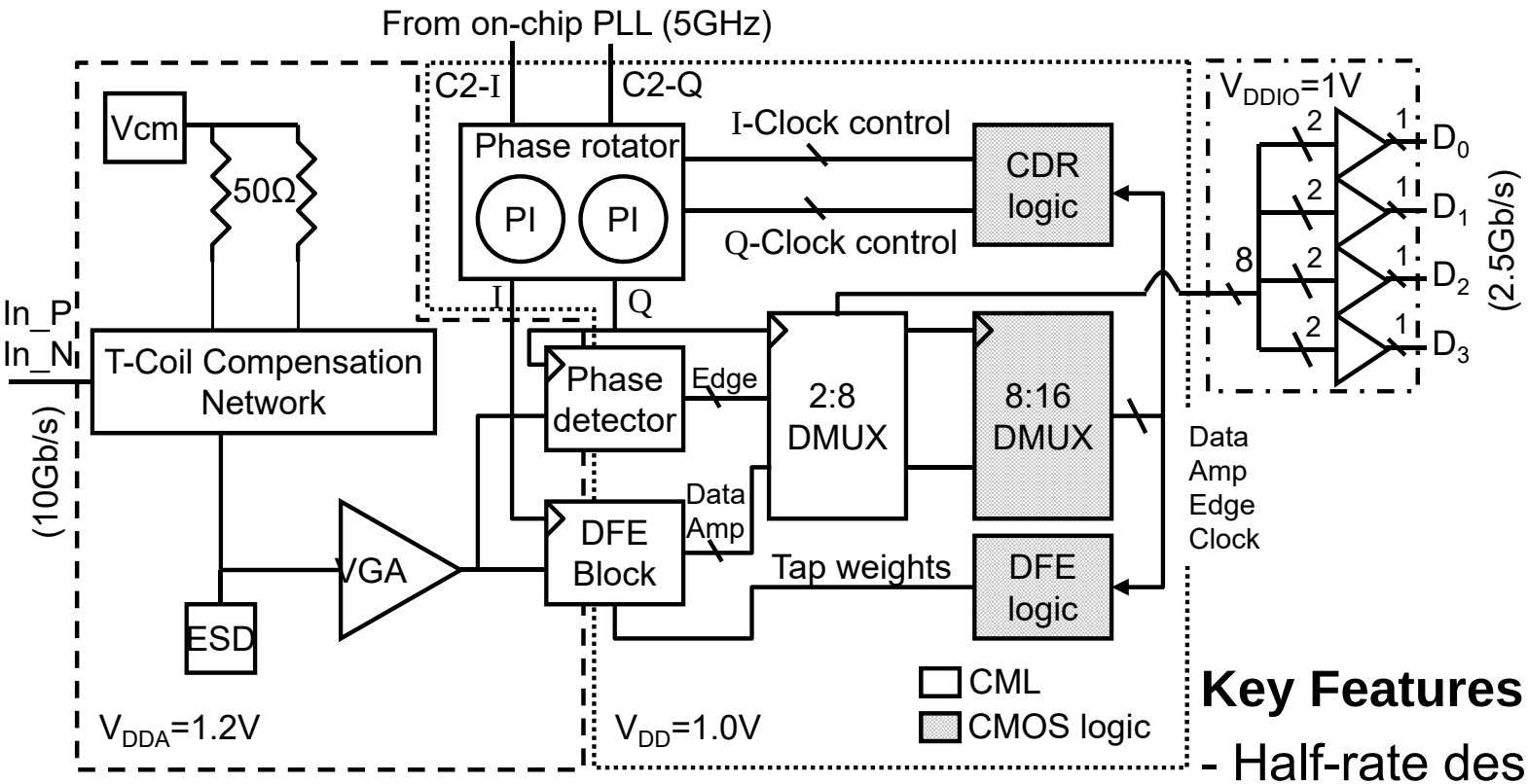


FFE 4=[0, 85%, -15%, 0, 0]



[Meghelli (IBM) ISSCC 2006]

Receiver Architecture

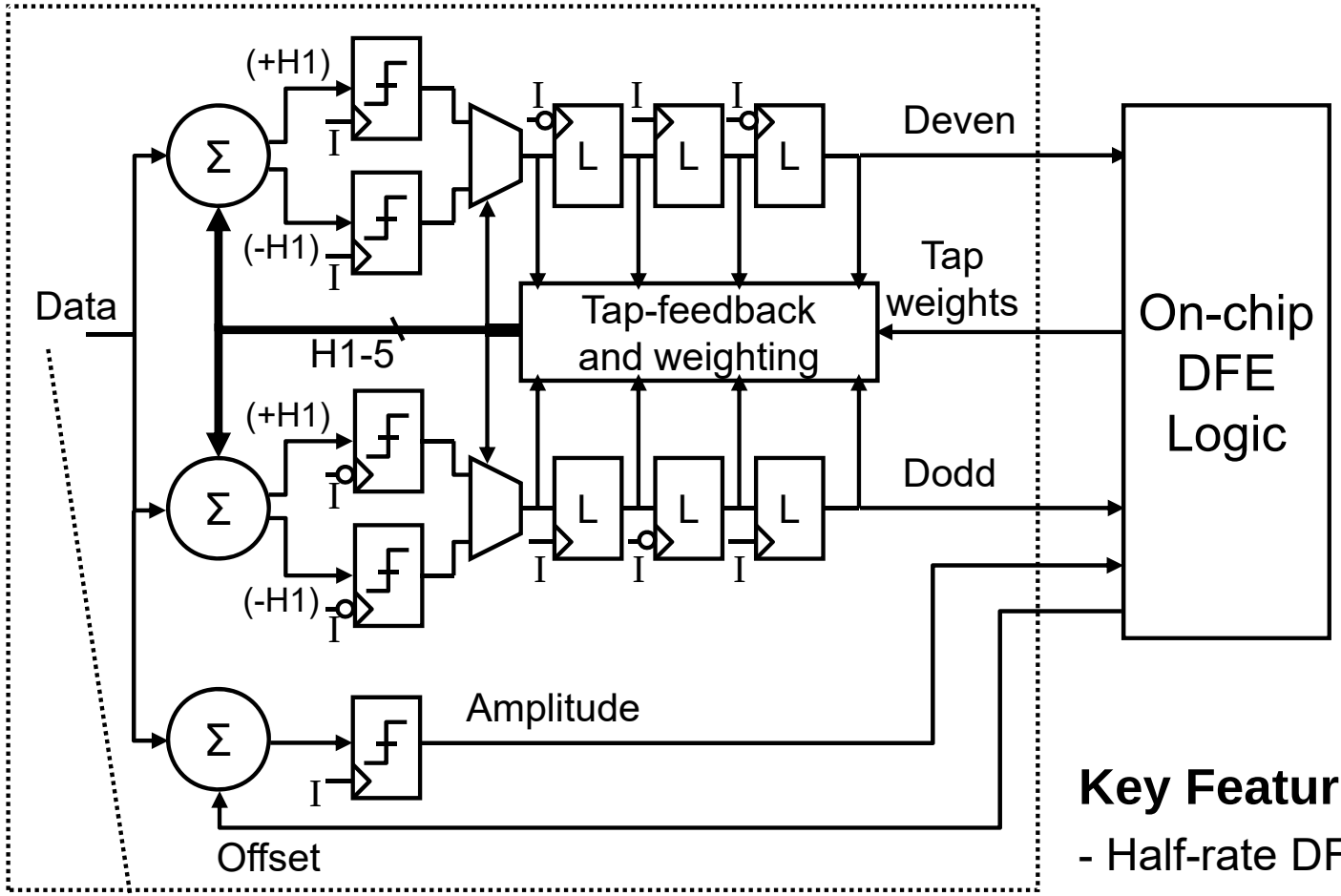


Key Features:

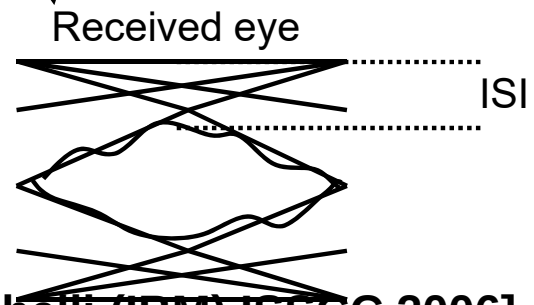
- Half-rate design
- 5-tap continuously adaptive DFE
- Variable gain amplifier
- Digital CDR
- ESD protection (HBM & CDM)
- 130mW (with DFE and CDR logic)

[Meghelli (IBM) ISSCC 2006]

DFE Approach



DFE Taps	Resolution
H1	6 bits
H2	5 bits
H3, H4, H5	4 bits

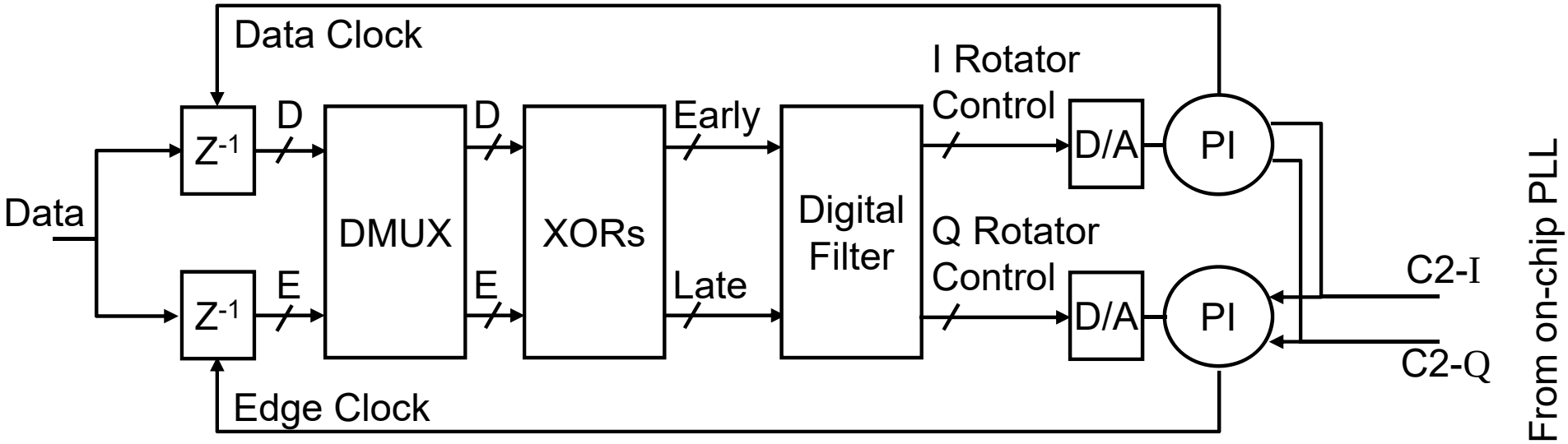


Key Features:

- Half-rate DFE with H1 speculation and dynamic H2-H5 feedback allows 2UI for settling
- DFE algorithm maximizes vertical eye opening at the data slicing instant
- Offset adjustment at all the slicer inputs

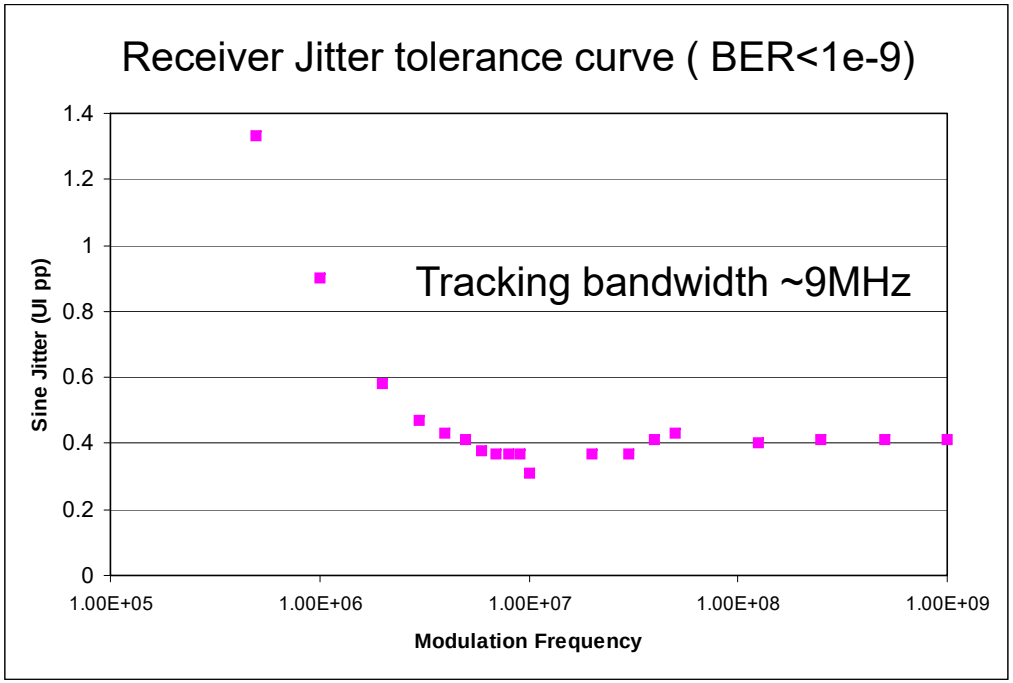
[Meghelli (IBM) ISSCC 2006]

CDR Loop



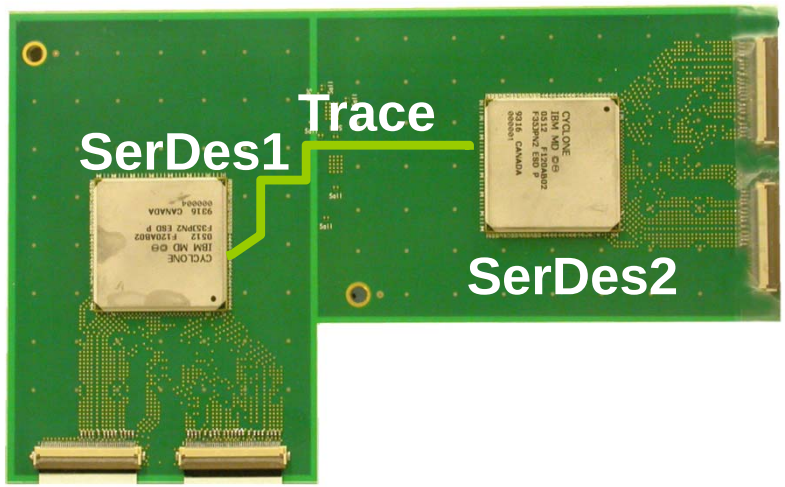
Key Features:

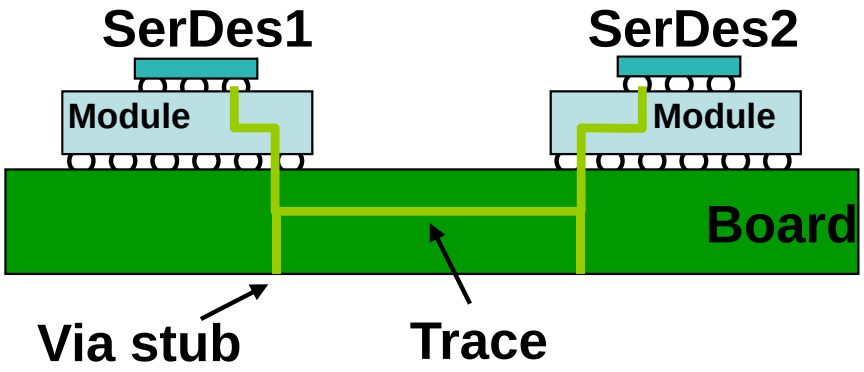
- Fully digital loop
- Can handle up to +/- 4000ppm frequency offset
- Independent I,Q control



[Meghelli (IBM) ISSCC 2006]

Chip-to-Chip Link Experiments





Trace Length	5GHz losses (Tx module + board trace + Rx module)	Number of vias 3.8mm via stub / 1.8mm via stub / 1.8mm via through
10” (#1)	12dB	2 / 0 / 0
10” (#2)	10dB	0 / 2 / 0
15”	25dB	4 / 2 / 0
20”	15dB	0 / 0 / 2

[Meghelli (IBM) ISSCC 2006]

Chip-to-Chip Measurement Results

Trace Length	5GHz losses (Tx module + board trace + Rx module)	Number of vias 3.8mm via stub / 1.8mm via stub / 1.8mm via through
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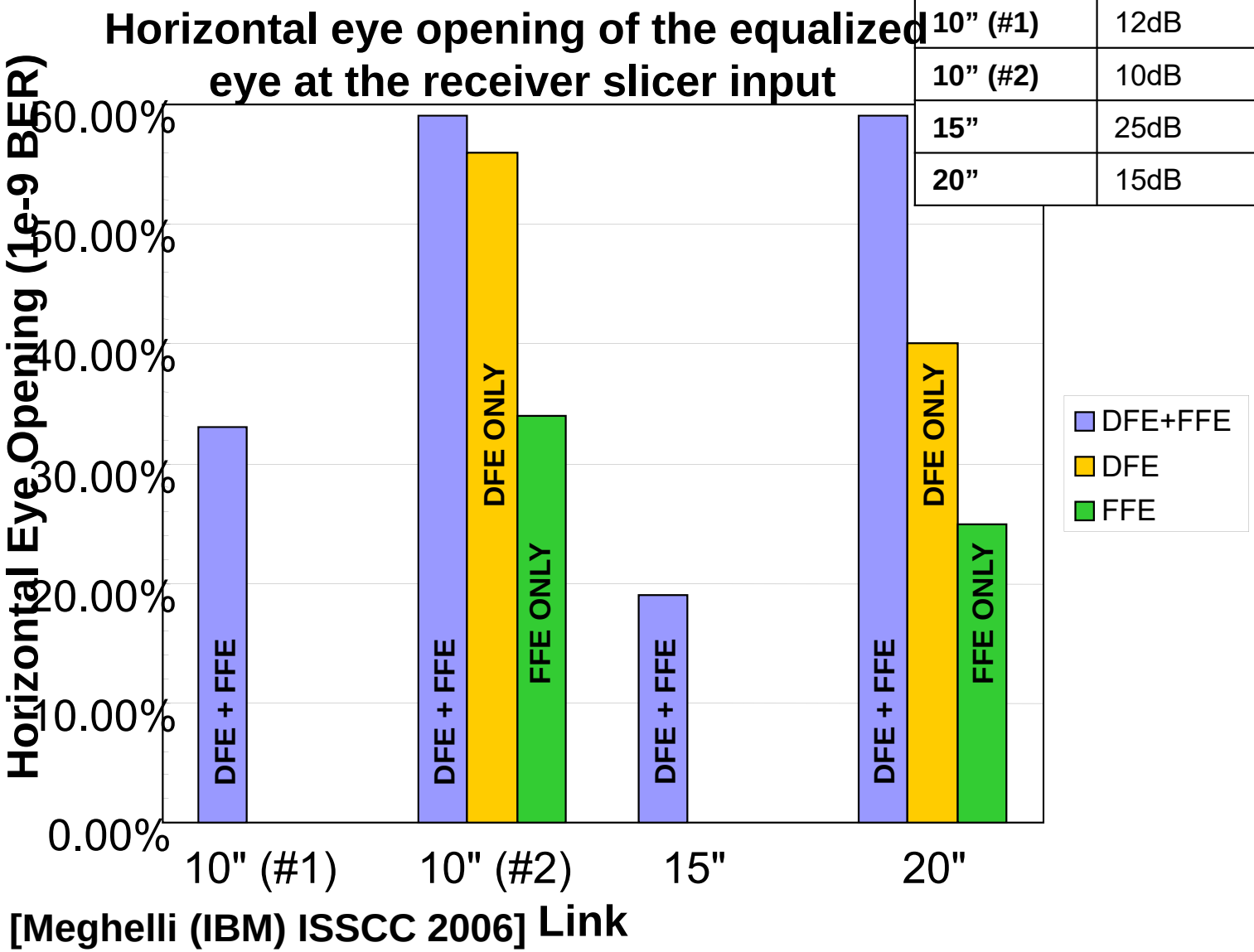

[Meghelli (IBM) ISSCC 2006]

Preliminary Schedule

Topic		Week
I.	Channels	Week 1-7
II.	Communication Techniques	
III.	Equalizers	
IV.	Transmitter/Receiver Circuits	
	First Exam	**March 15**
V.	Equalizer Circuits	Week 8-14
VI.	Clocking Circuits	
VII.	Clocking Systems	
VIII.	Link Modeling	
IX.	Link Examples	
	Second Exam	**April 23**
	Project Report Due	**April 29**
	Project Presentations	**May 4**

- Dates may change with reasonable notice

Next Time

- Channels
  - Components
    - Chip packages, PCBs, Wires, Connectors
  - Modeling
    - Wires, Transmission Lines