ASIC Tutorial

0.25u TSMC Technology

- Load and Initialize the design / libraries
- Pre-placement (of big blocks - mem, cpu, etc)
- Power routing
- Placement
- Clock tree insertion
- optFanout– Sizing and first route - Repeat
- Wroute
- Fill
- Final Checks - Timing

IO file for wirebond design

- Describes the location of each IO
- East, West, South, North specification
- Corners added to netlist without ports
- IO Fill not added to netlist, only IO file
- Bottom left as origin – each side starts low
- 2 corners, N IO and Fill on one side must equal the length of the side of the die
  - 6 85u IO, 2 315 corners = 510 + 630 = 1140u
  - IO Filler must make up the difference
  - IO Filler maintain continuity the 3 IO power rings

```
#########################################################
#  Silicon Perspective, A Cadence Company           #
#  FirstEncounter IO Assignment                     #
#########################################################
Version: 2
Pad: PCORNER_SE SE
Pad: PCORNER_SW SW
Pad: PCORNER_NW NW
Pad: PCORNER_NE NE

Pad: PFILLN01 n PFEED35
Pad: PFILLN02 n PFEED35
Pad: PFILLN03 n PFEED35
Pad: PFILLN04 n PFEED35
Pad: PFILLN05 n PFEED35
Pad: PFILLN06 n PFEED35
Pad: PFILLN07 n PFEED35
Pad: PFILLN08 n PFEED20
Pad: chip_io_adc_sclk_discharge N
Pad: PFILLN11 n PFEED35
Pad: PFILLN12 n PFEED35
Pad: PFILLN13 n PFEED35
Pad: PFILLN14 n PFEED35
Pad: PFILLN15 n PFEED35
Pad: PFILLN16 n PFEED35
Pad: PFILLN17 n PFEED35
Pad: PFILLN18 n PFEED20
Pad: chip_io_debug_clk_out N
Pad: PFILLN21 n PFEED35
Pad: PFILLN22 n PFEED35
.
.
.
```

Config file

- Describes basic config of libraries and design
- Basic Floorplanning – die size, etc

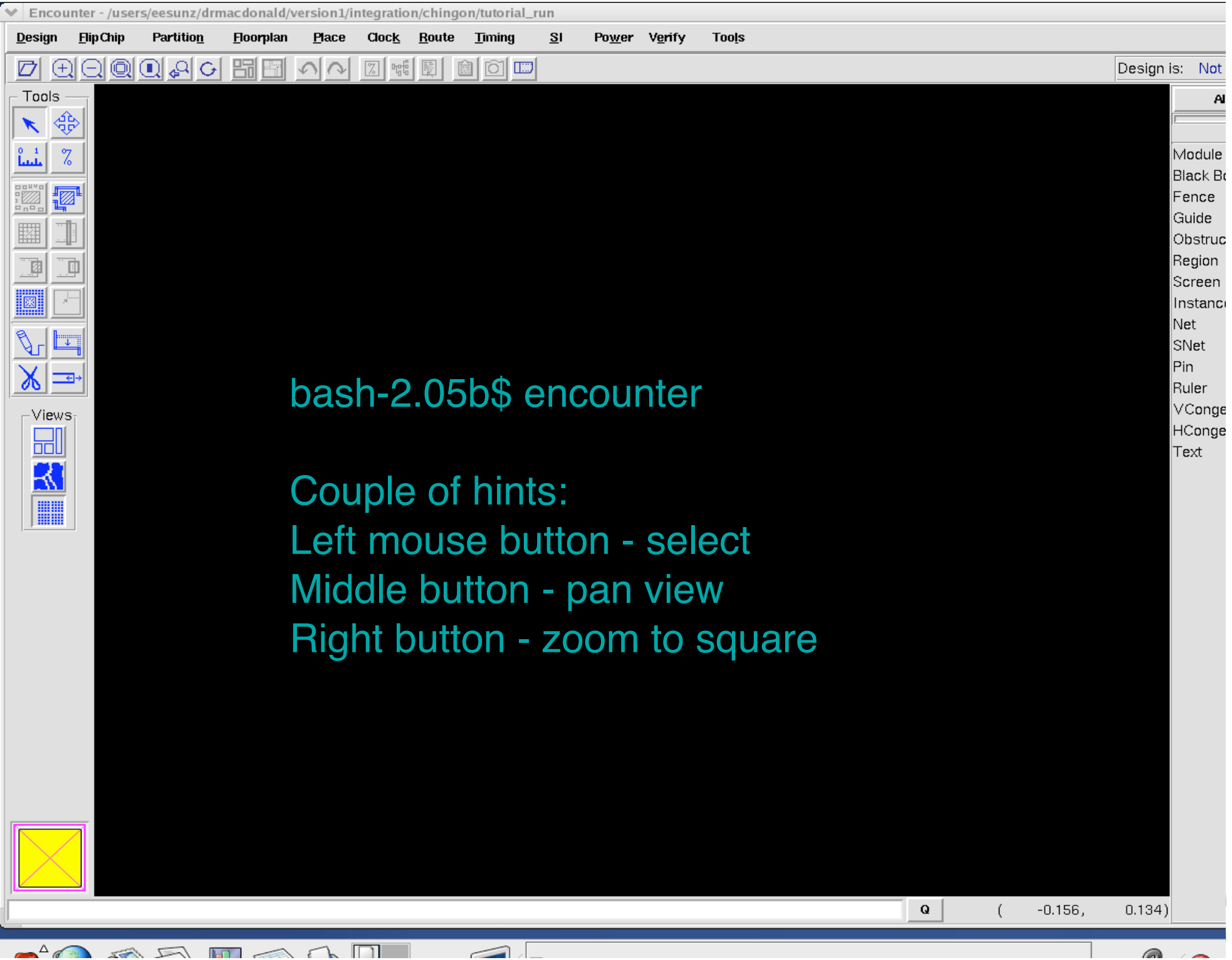
```
#################################################
#                                               #
#  FirstEncounter Input configuration file      #
#                                               #
#################################################
global rda_Input

set USER            /users/eesunz/faculty/cdsemac
set LIBRARY         $USER/xlsynergy/libraries_25TSMC
set TECH            $LIBRARY/aci/sc
set IO              $LIBRARY/new_fe_n/TSMCHOME/digital
set NETLIST         $USER/xlsynergy/integration/netlist
set MEMORIES        $USER/xlsynergy/memories_25TSMC
.
.
```

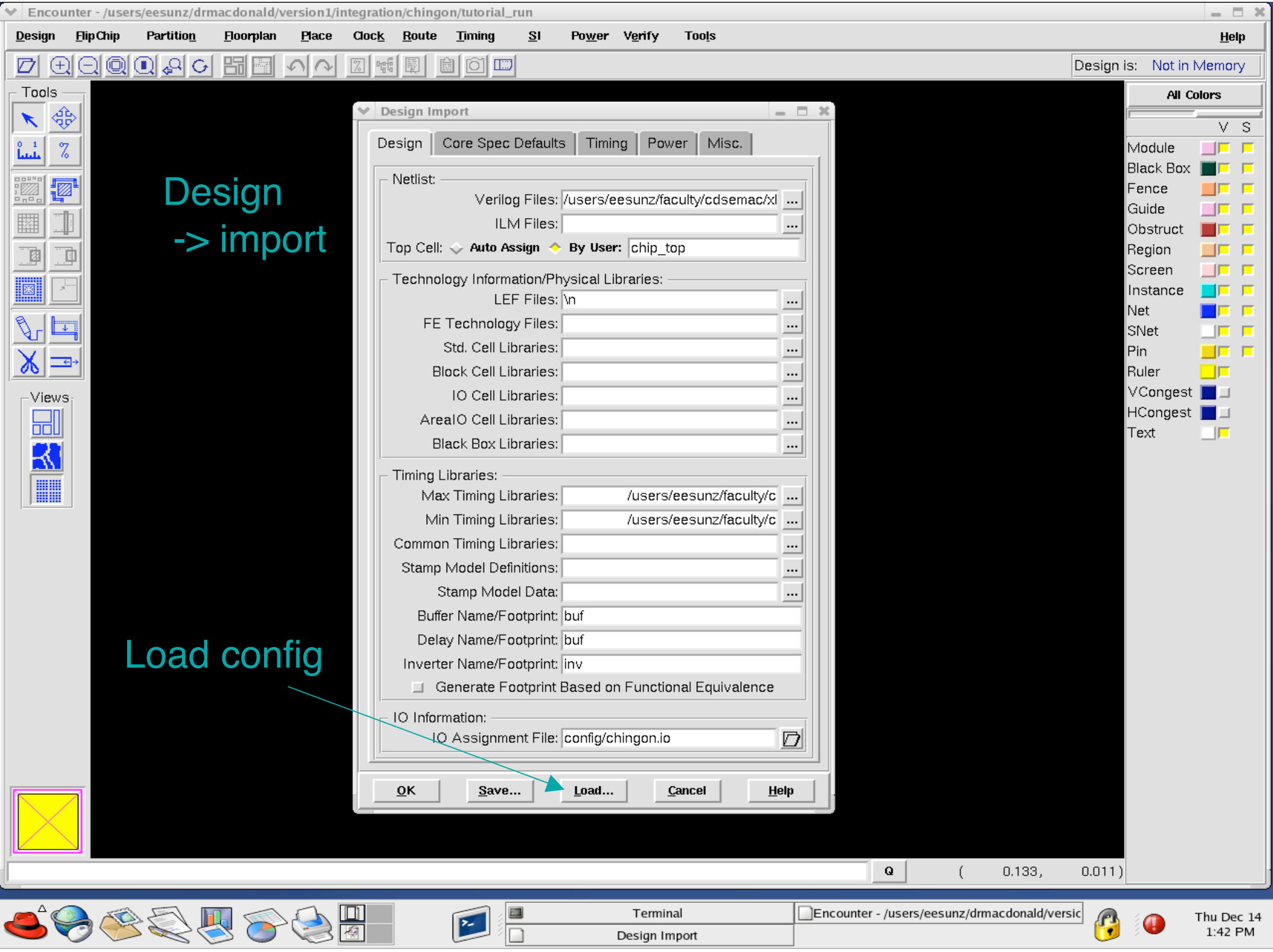
Timing File (const.sdc)

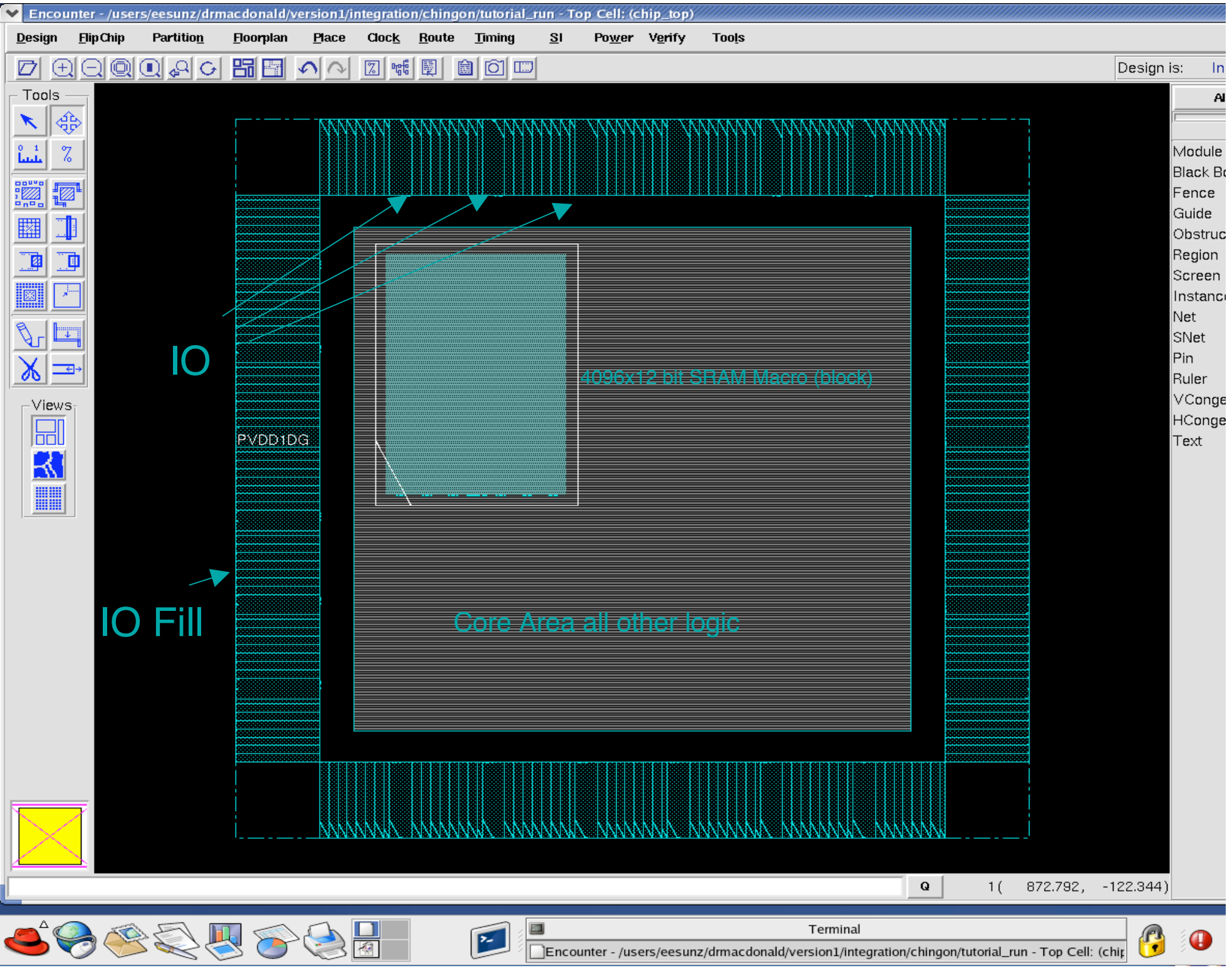
- Describes the timing of the design
- At minimum, needs to identify and provide frequency for all clocks
- Sets False Paths / multi-cycle paths
- Sets IO timing – arrival times

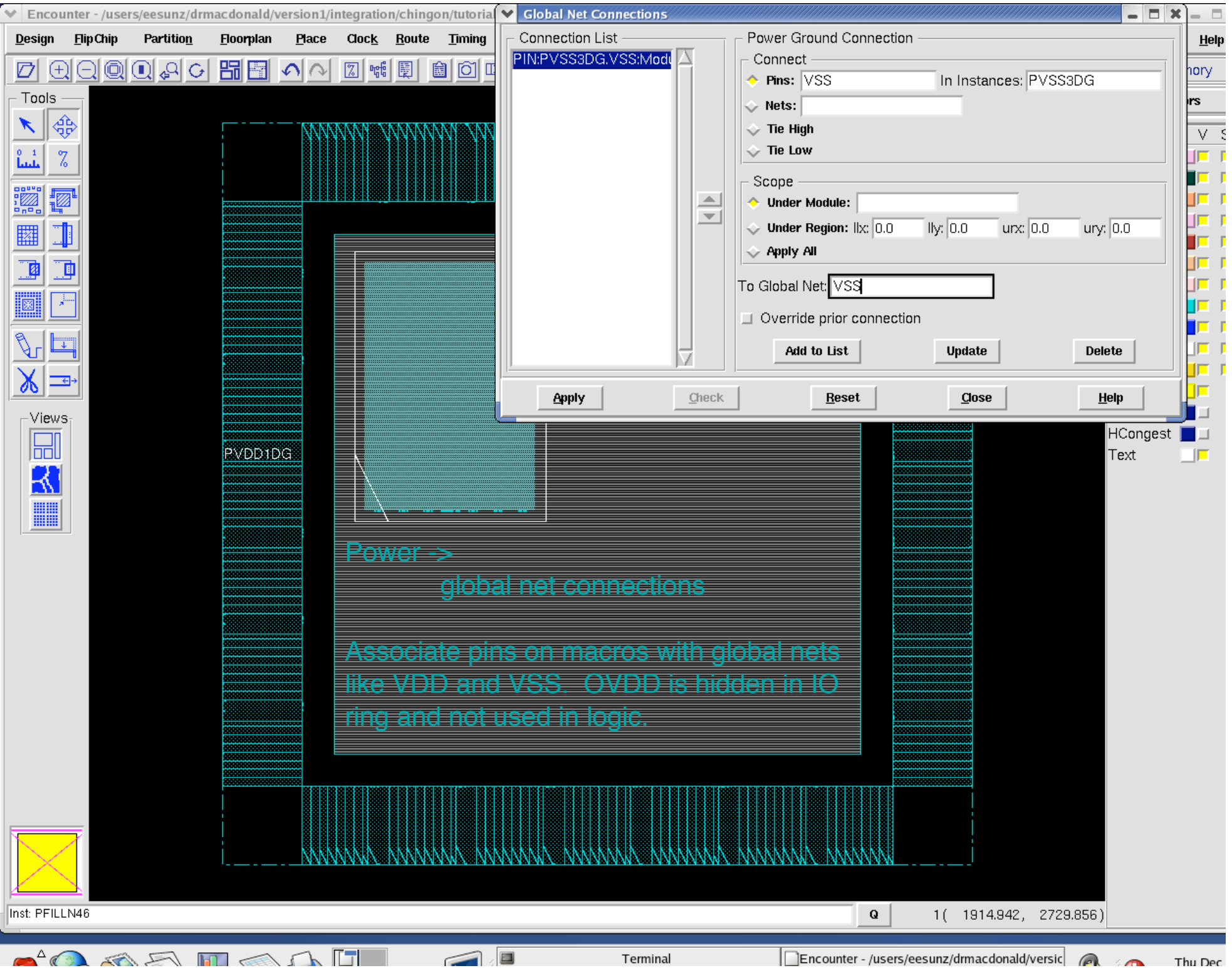
Timing File (const.sdc)

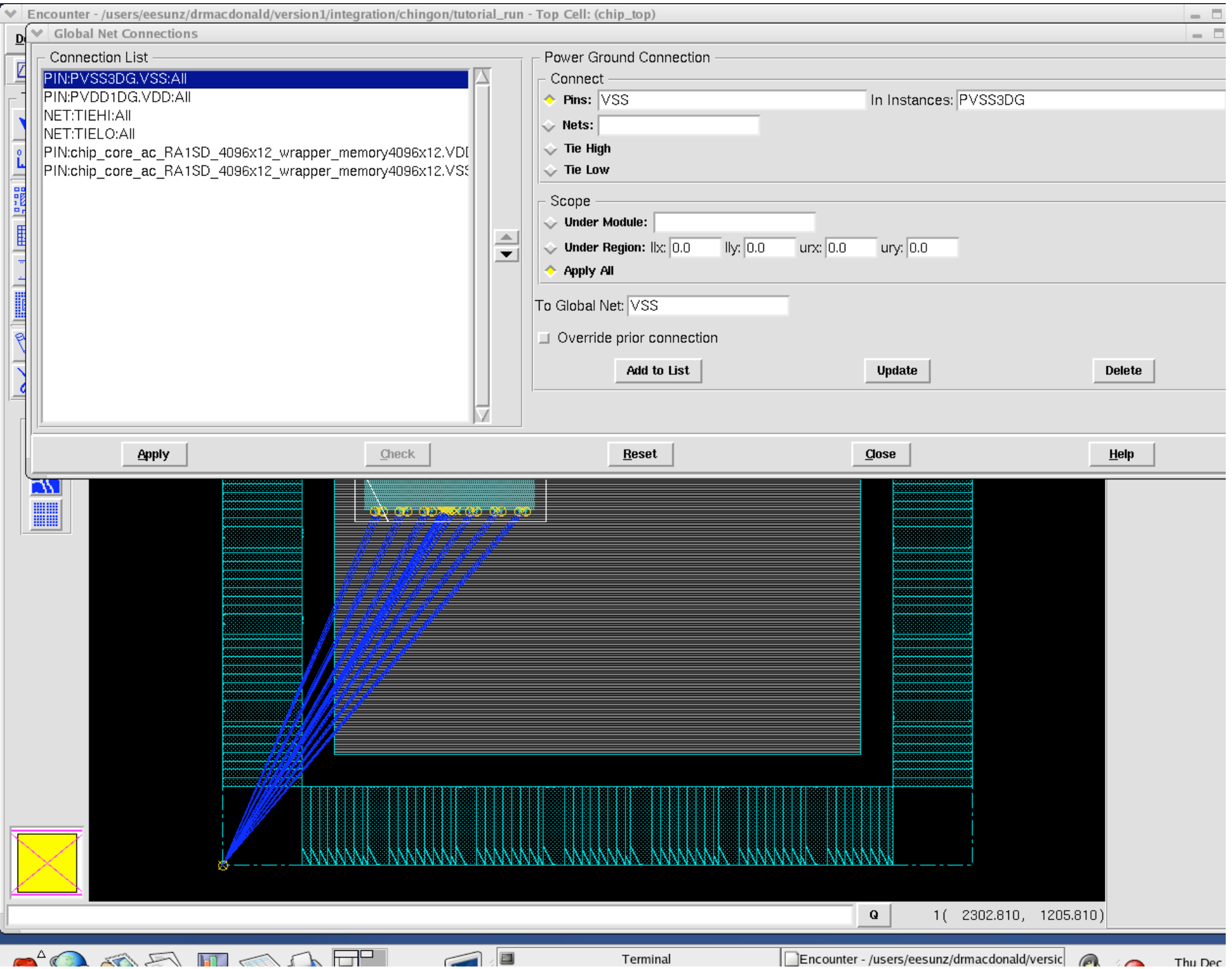
```
#/************************************************
# * Timing constraint file in SDC format
# ************************************************/
create_clock -name refclk -period 33.3000        -waveform { 0.0000 16.6500}      [get_pins {i_3297/Y}]
create_clock -name refclk_fast -period 5.0000    -waveform { 0.0000 2.5000}       [get_pins {i_3283/Y}]
create_clock -name refclk_jtag -period 100.0000              -waveform { 0.0000 50.0000}      [get_ports {jtag_tck_pad}]

set_false_path -from [get_ports {debug_mode_pad}]
set_false_path -from [get_ports {clk_select_pad}]
set_false_path -from [get_ports {adc_select_pad}]
set_false_path -from [get_clocks {refclk_jtag}]   -to [get_clocks {refclk}]
set_false_path -from [get_clocks {refclk}]        -to [get_clocks {refclk_jtag}]
set_false_path -from [get_clocks {refclk_fast}]   -to [get_clocks {refclk}]
set_false_path -from [get_clocks {refclk}]        -to [get_clocks {refclk_fast}]
set_false_path -from [get_clocks {refclk_fast}]   -to [get_clocks {refclk_jtag}]
set_false_path -from [get_clocks {refclk_jtag}]   -to [get_clocks {refclk_fast}]

set_input_delay -max -clock refclk 5.0000 {*}
set_input_delay -min -clock refclk 0.0000 {*}
set_drive 0.0000 [get_ports {*}]
set_load -pin_load 0.0000 [get_ports {*}]
set_output_delay -min -clock refclk 0.0000 {*}
set_output_delay -max -clock refclk 5.0000 {*}
```

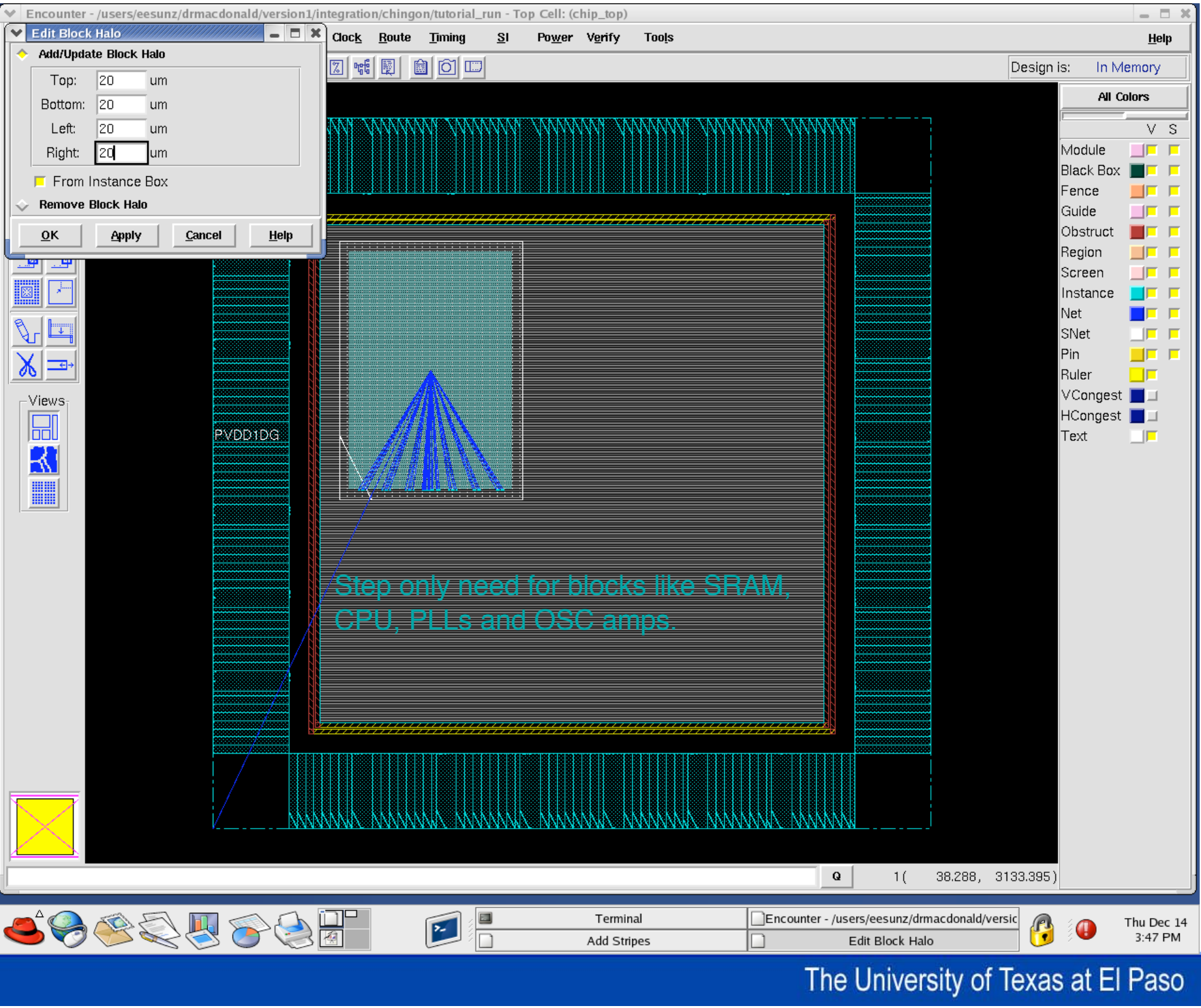

Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run
Design FlipChip Partition Floorplan Place Clock Route Timing SI Power Verify Tools
Design is: Not
Tools
Views
bash-2.05b$ encounter
Couple of hints:
Left mouse button - select
Middle button - pan view
Right button - zoom to square
Module
Fence
Guide
Region
Screen
Net
SNet
Pin
Ruler
Text
Q
(-0.156, 0.134)

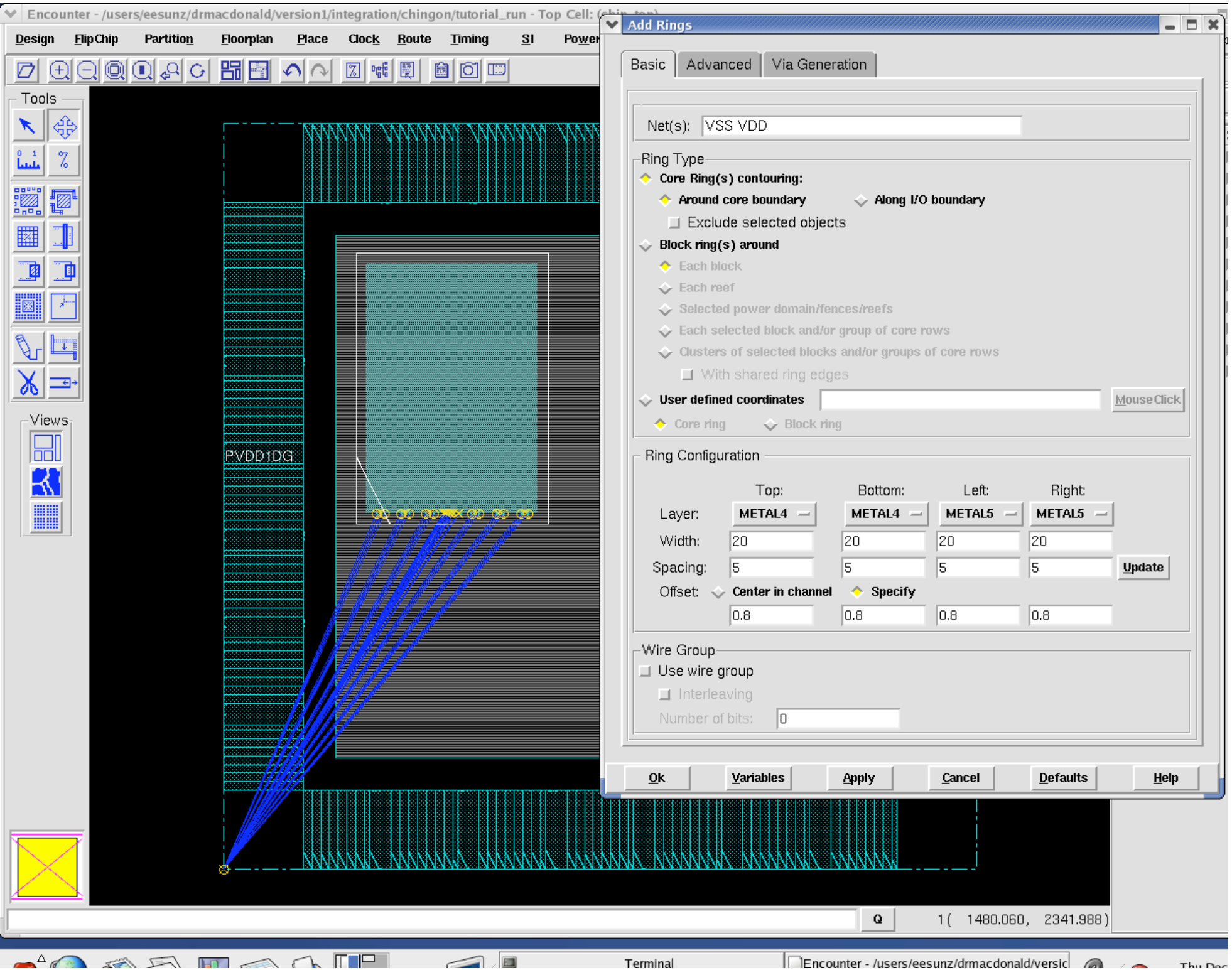

Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run
Design FlipChip Partition Floorplan Place Clock Route Timing SI Power Verify Tools Help
Design is: Not in Memory
Tools
Views
Design
-> import
Load config
Design Import
Design Core Spec Defaults Timing Power Misc.
Netlist:
Verilog Files: /users/eesunz/faculty/cdsemac/xl
ILM Files:
Top Cell: Auto Assign By User: chip_top
Technology Information/Physical Libraries:
LEF Files: \n
FE Technology Files:
Std. Cell Libraries:
Block Cell Libraries:
IO Cell Libraries:
AreaIO Cell Libraries:
Black Box Libraries:
Timing Libraries:
Max Timing Libraries: /users/eesunz/faculty/c
Min Timing Libraries: /users/eesunz/faculty/c
Common Timing Libraries:
Stamp Model Definitions:
Stamp Model Data:
Buffer Name/Footprint: buf
Delay Name/Footprint: buf
Inverter Name/Footprint: inv
Generate Footprint Based on Functional Equivalence
IO Information:
IO Assignment File: config/chingon.io
OK Save... Load... Cancel Help
All Colors
V S
Module
Black Box
Fence
Guide
Obstruct
Region
Screen
Instance
Net
SNet
Pin
Ruler
VCongest
HCongest
Text
Q (0.133, 0.011)
Terminal
Encounter - /users/eesunz/drmacdonald/versic
Design Import
Thu Dec 14
1:42 PM

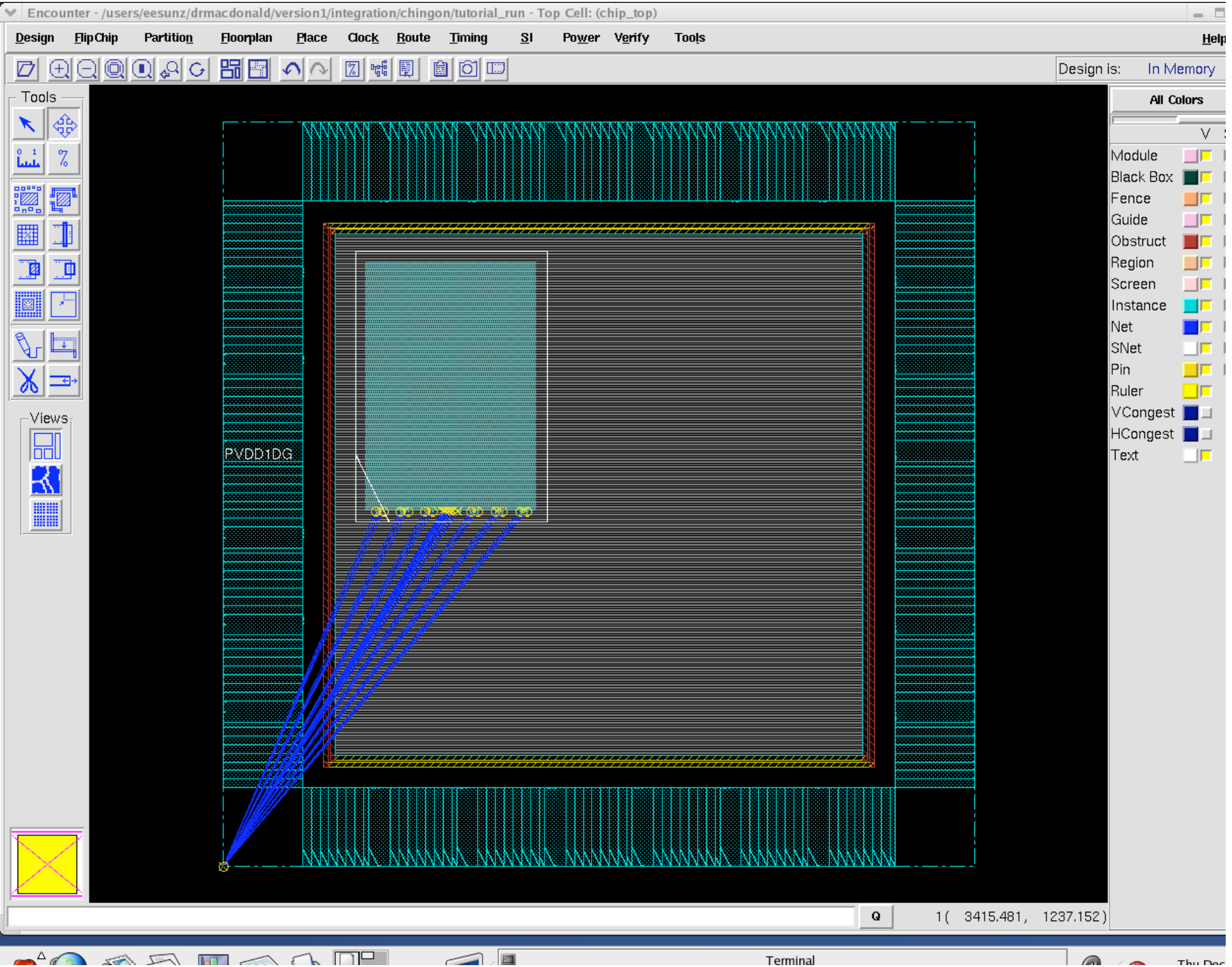

Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip_top)
Design
FlipChip
Partition
Floorplan
Place
Clock
Route
Timing
SI
Power
Verify
Tools
Design is:
Tools
Views
IO
IO Fill
PVDD1DG
4096x12 bit SRAM Macro (block)
Core Area all other logic
Module
Black Bo
Fence
Guide
Obstruc
Region
Screen
Instanc
Net
SNet
Pin
Ruler
VConge
HConge
Text
Q
1(872.792, -122.344)
Terminal
Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip

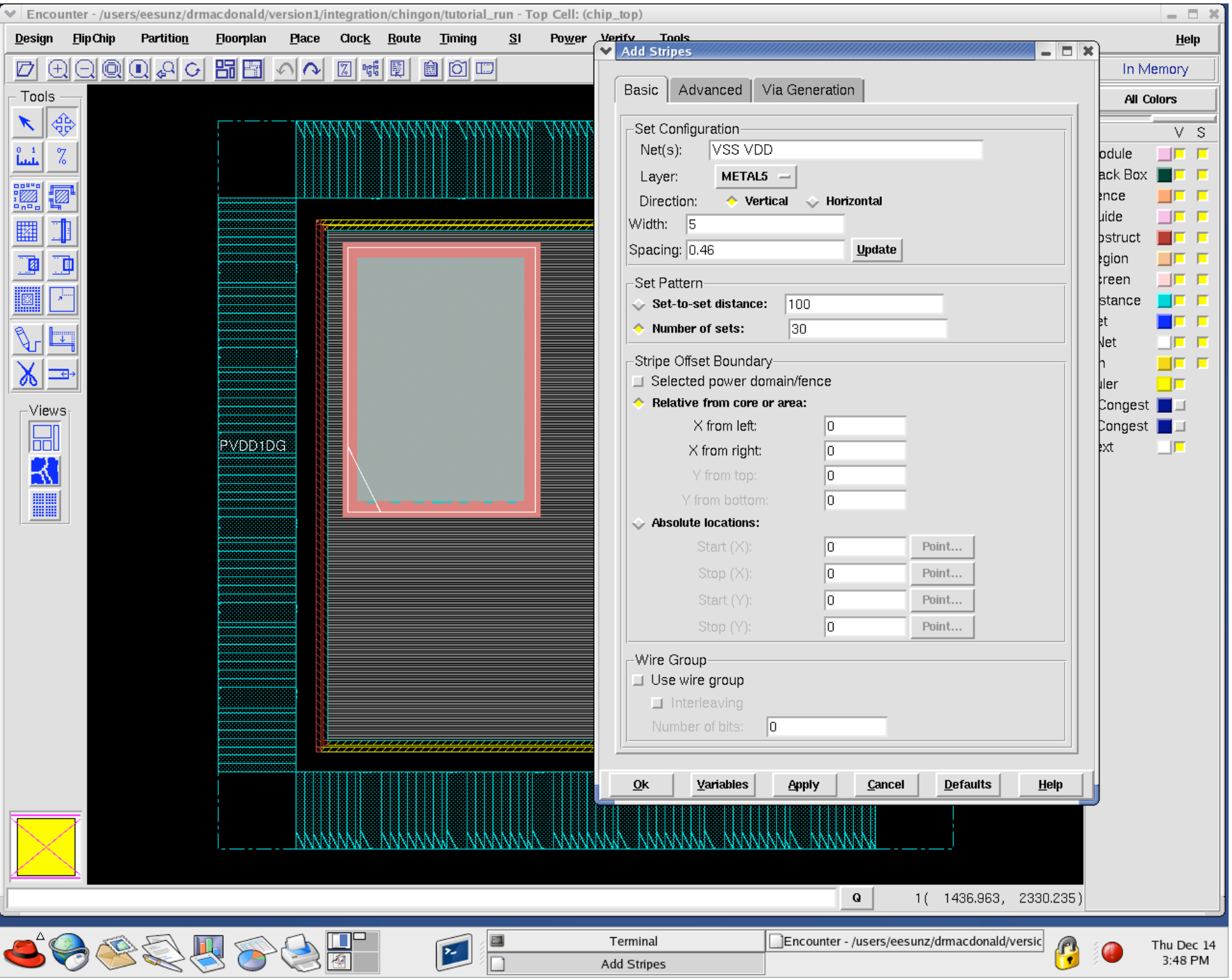

Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial
Design
FlipChip
Partition
Floorplan
Place
Clock
Route
Timing
Help
Tools
Views
Global Net Connections
Connection List
PIN:PVSS3DG.VSS:Modu
Power Ground Connection
Connect
Pins: VSS
In Instances: PVSS3DG
Nets:
Tie High
Tie Low
Scope
Under Module:
Under Region: llx: 0.0 lly: 0.0 urx: 0.0 ury: 0.0
Apply All
To Global Net: VSS
Override prior connection
Add to List
Update
Delete
Apply
Check
Reset
Close
Help
PVDD1DG
Power ->
global net connections
Associate pins on macros with global nets like VDD and VSS. OVDD is hidden in IO ring and not used in logic.
HCongest
Text
Inst: PFILLN46
Q
1(1914.942, 2729.856)
Terminal
Encounter - /users/eesunz/drmacdonald/versic
Thu Dec

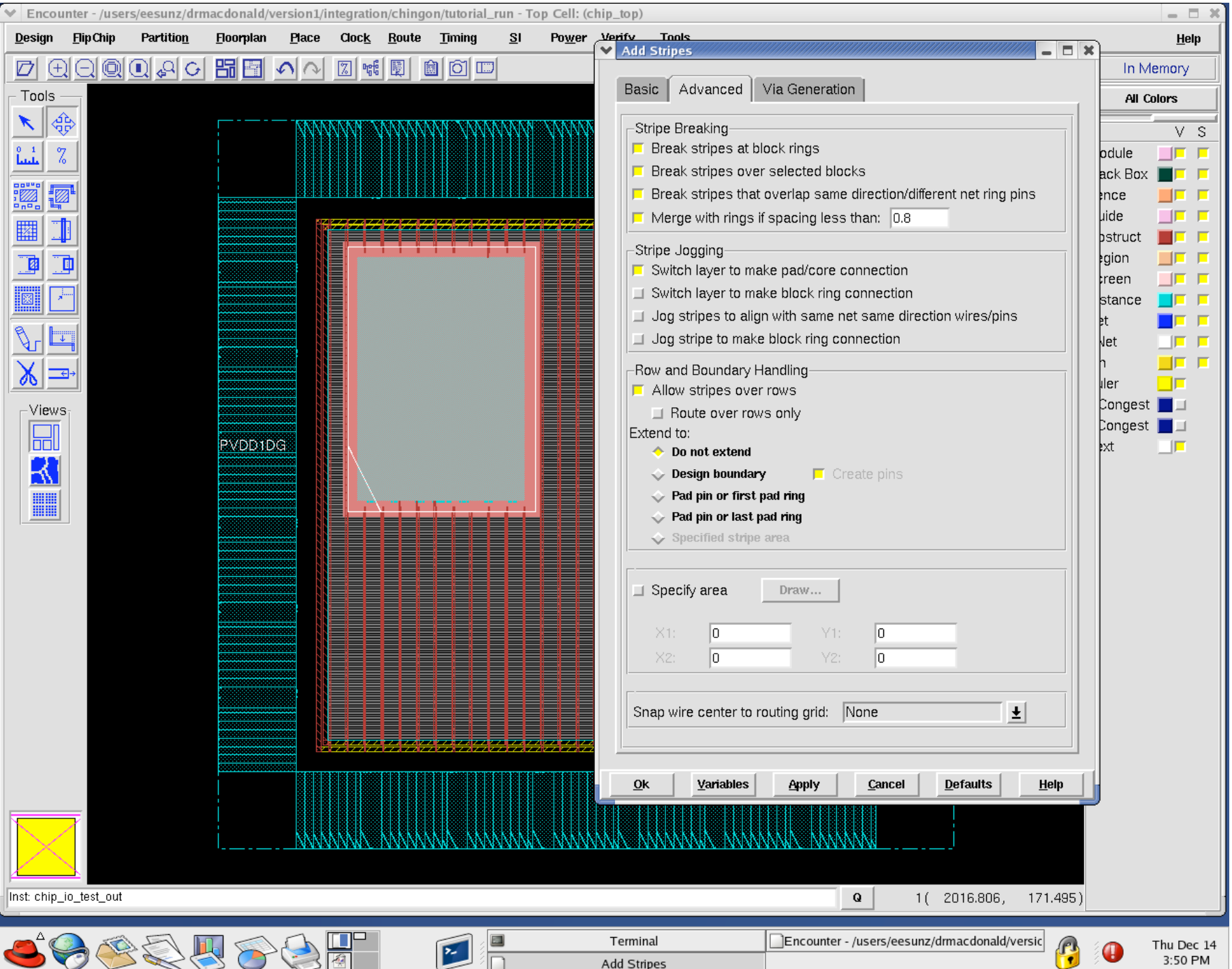

Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip_top)
Global Net Connections
Connection List
PIN:PVSS3DG.VSS:All
PIN:PVDD1DG.VDD:All
NET:TIEHI:All
NET:TIELO:All
PIN:chip_core_ac_RA1SD_4096x12_wrapper_memory4096x12.VDI
PIN:chip_core_ac_RA1SD_4096x12_wrapper_memory4096x12.VS
Power Ground Connection
Connect
Pins: VSS
In Instances: PVSS3DG
Nets:
Tie High
Tie Low
Scope
Under Module:
Under Region: llx: 0.0 lly: 0.0 urx: 0.0 ury: 0.0
Apply All
To Global Net: VSS
Override prior connection
Add to List
Update
Delete
Apply
Check
Reset
Close
Help
Q
1(2302.810, 1205.810)
Terminal
Encounter - /users/eesunz/drmacdonald/versic
Thu Dec

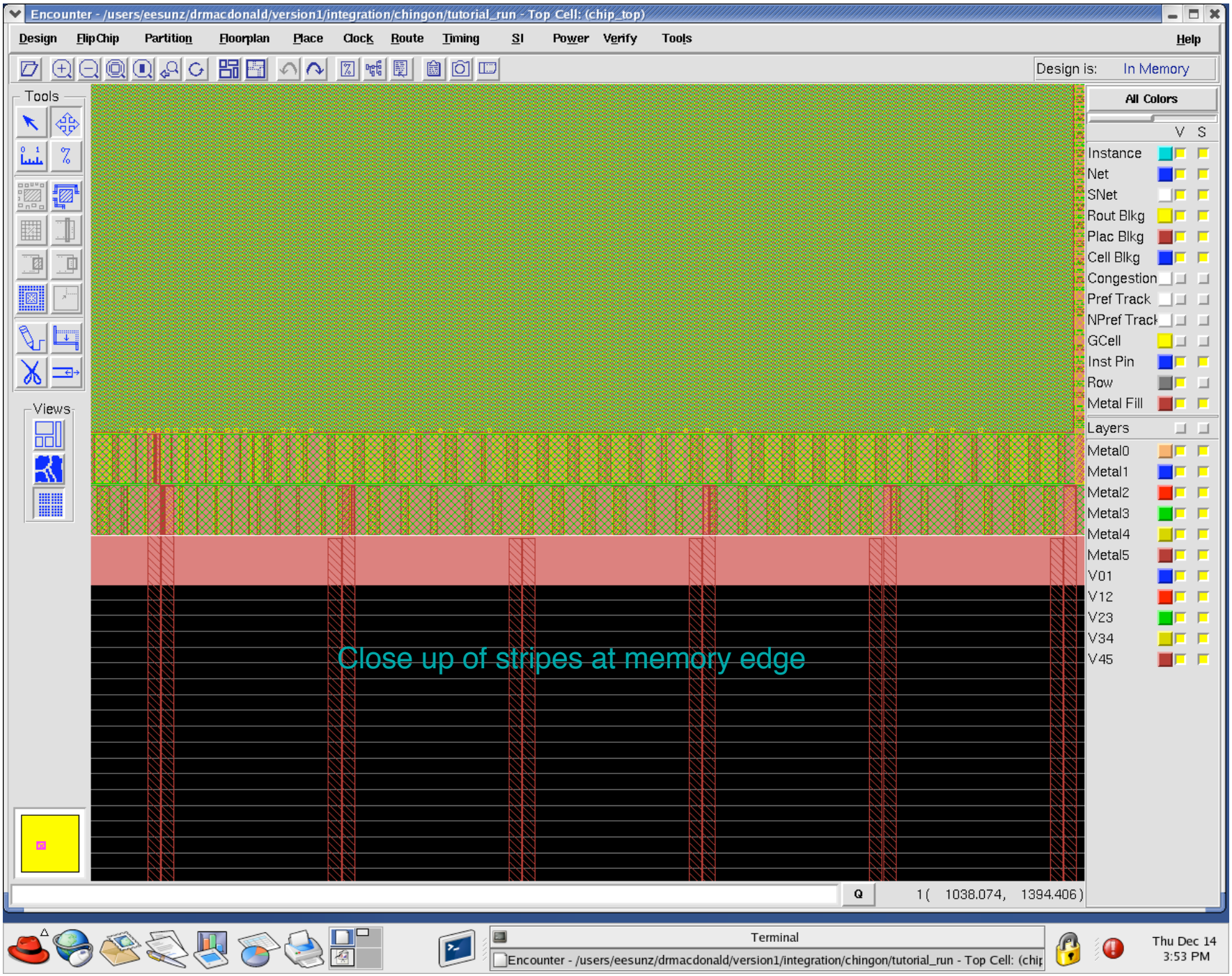

Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip_top)
Edit Block Halo
Add/Update Block Halo
Top: 20 um
Bottom: 20 um
Left: 20 um
Right: 20 um
From Instance Box
Remove Block Halo
OK
Apply
Cancel
Help
Clock
Route
Timing
SI
Power
Verify
Tools
Help
Design is: In Memory
All Colors
V S
Module
Black Box
Fence
Guide
Obstruct
Region
Screen
Instance
Net
SNet
Pin
Ruler
VCongest
HCongest
Text
Views
PVDD1DG
Step only need for blocks like SRAM, CPU, PLLs and OSC amps.
Q
1(38.288, 3133.395)
Terminal
Encounter - /users/eesunz/drmacdonald/versic
Add Stripes
Edit Block Halo
Thu Dec 14
3:47 PM

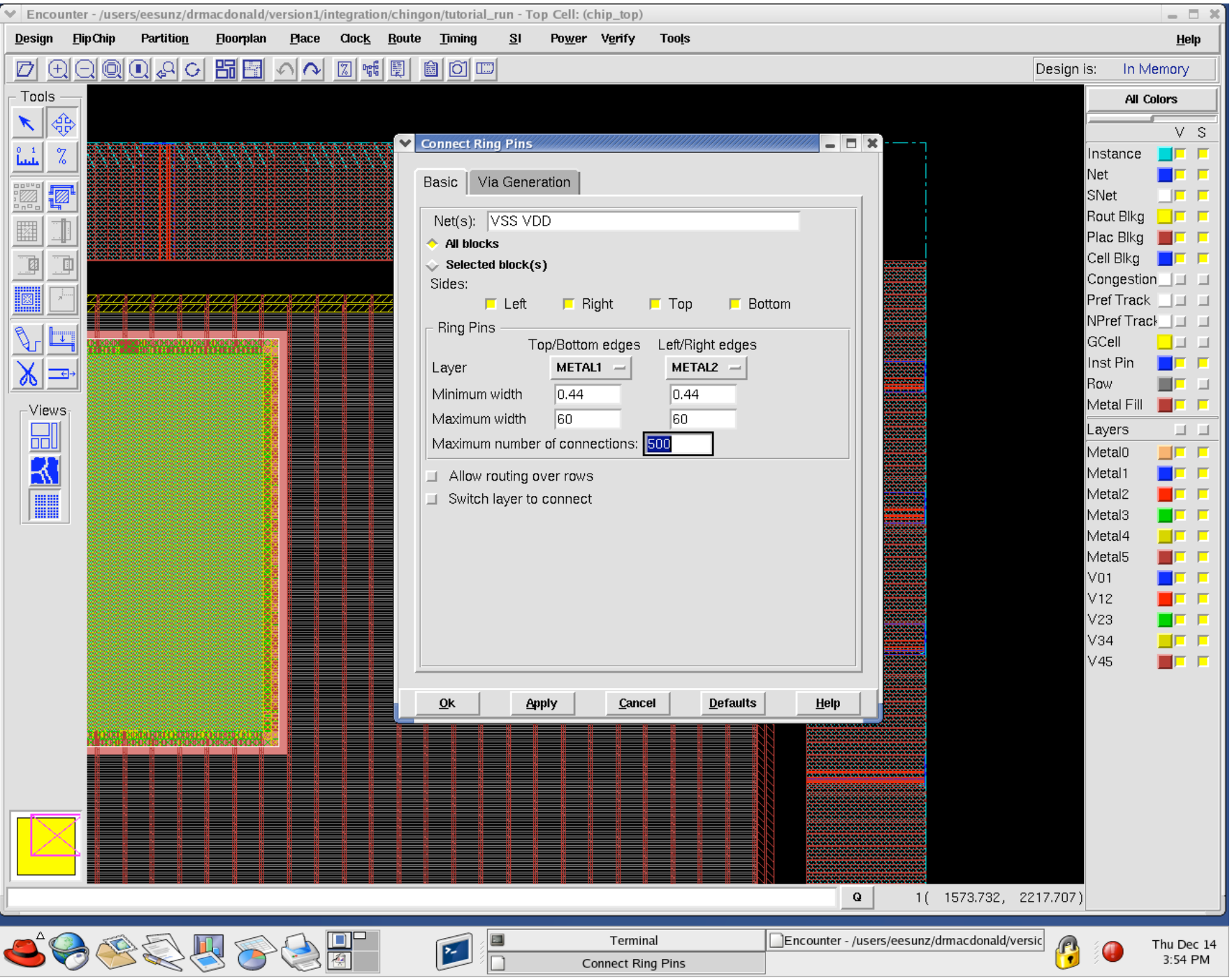

Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell:
Design
FlipChip
Partition
Floorplan
Place
Clock
Route
Timing
SI
Power
Tools
Views
PVDD1DG
Add Rings
Basic
Advanced
Via Generation
Net(s): VSS VDD
Ring Type
Core Ring(s) contouring:
Around core boundary
Along I/O boundary
Exclude selected objects
Block ring(s) around
Each block
Each reef
Selected power domain/fences/reefs
Each selected block and/or group of core rows
Clusters of selected blocks and/or groups of core rows
With shared ring edges
User defined coordinates
MouseClick
Core ring
Block ring
Ring Configuration
Top:
Bottom:
Left:
Right:
Layer:
METAL4
METAL4
METAL5
METAL5
Width:
20
20
20
20
Spacing:
5
5
5
5
Update
Offset:
Center in channel
Specify
0.8
0.8
0.8
0.8
Wire Group
Use wire group
Interleaving
Number of bits:
0
Ok
Variables
Apply
Cancel
Defaults
Help
Q
1(1480.060, 2341.988)
Terminal
Encounter - /users/eesunz/drmacdonald/versic

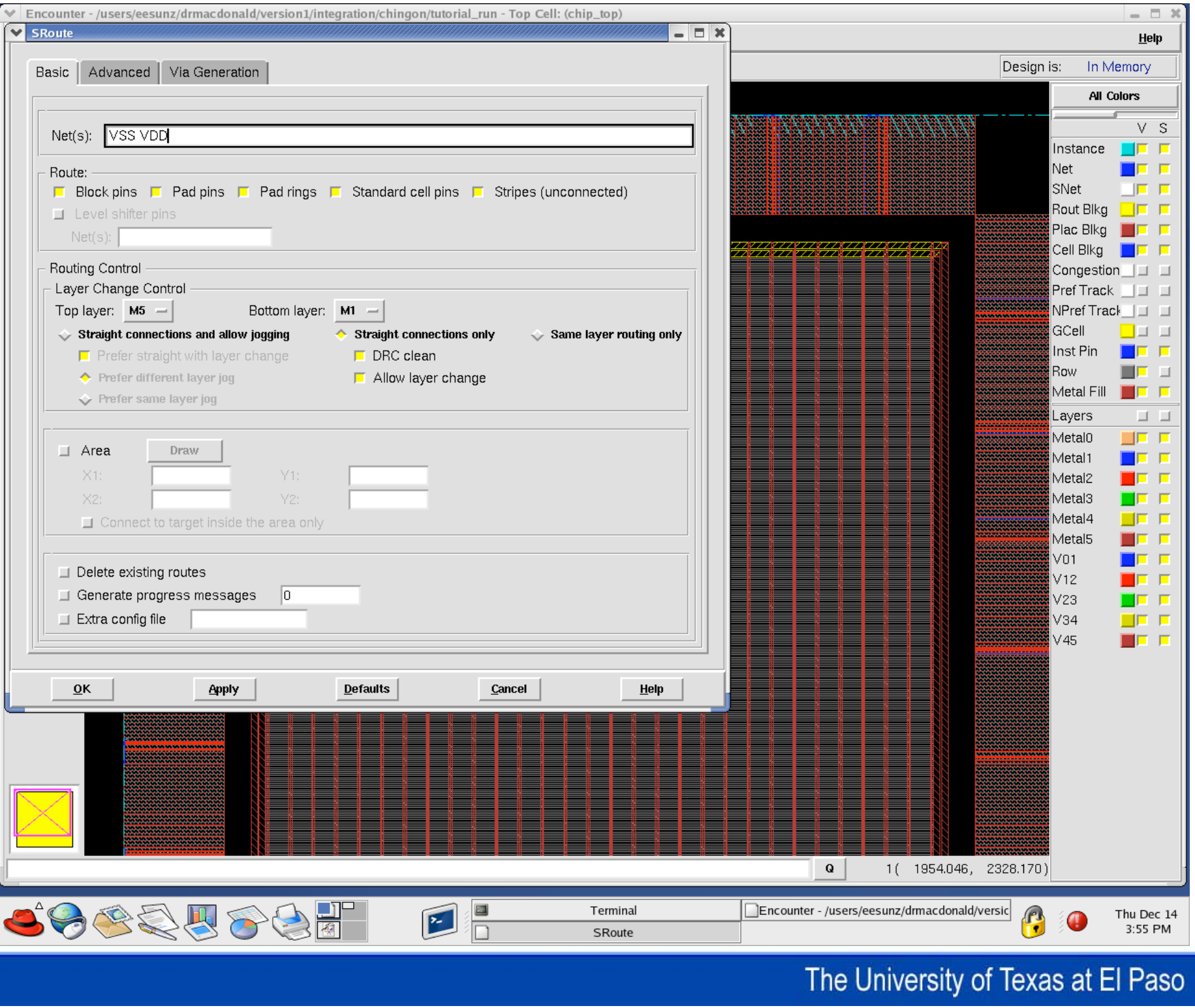

Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip_top)
Design
FlipChip
Partition
Floorplan
Place
Clock
Route
Timing
SI
Power
Verify
Tools
Help
Design is: In Memory
Tools
Views
All Colors
Module
Black Box
Fence
Guide
Obstruct
Region
Screen
Instance
Net
SNet
Pin
Ruler
VCongest
HCongest
Text
PVDD1DG
Q
1(3415.481, 1237.152)
Terminal

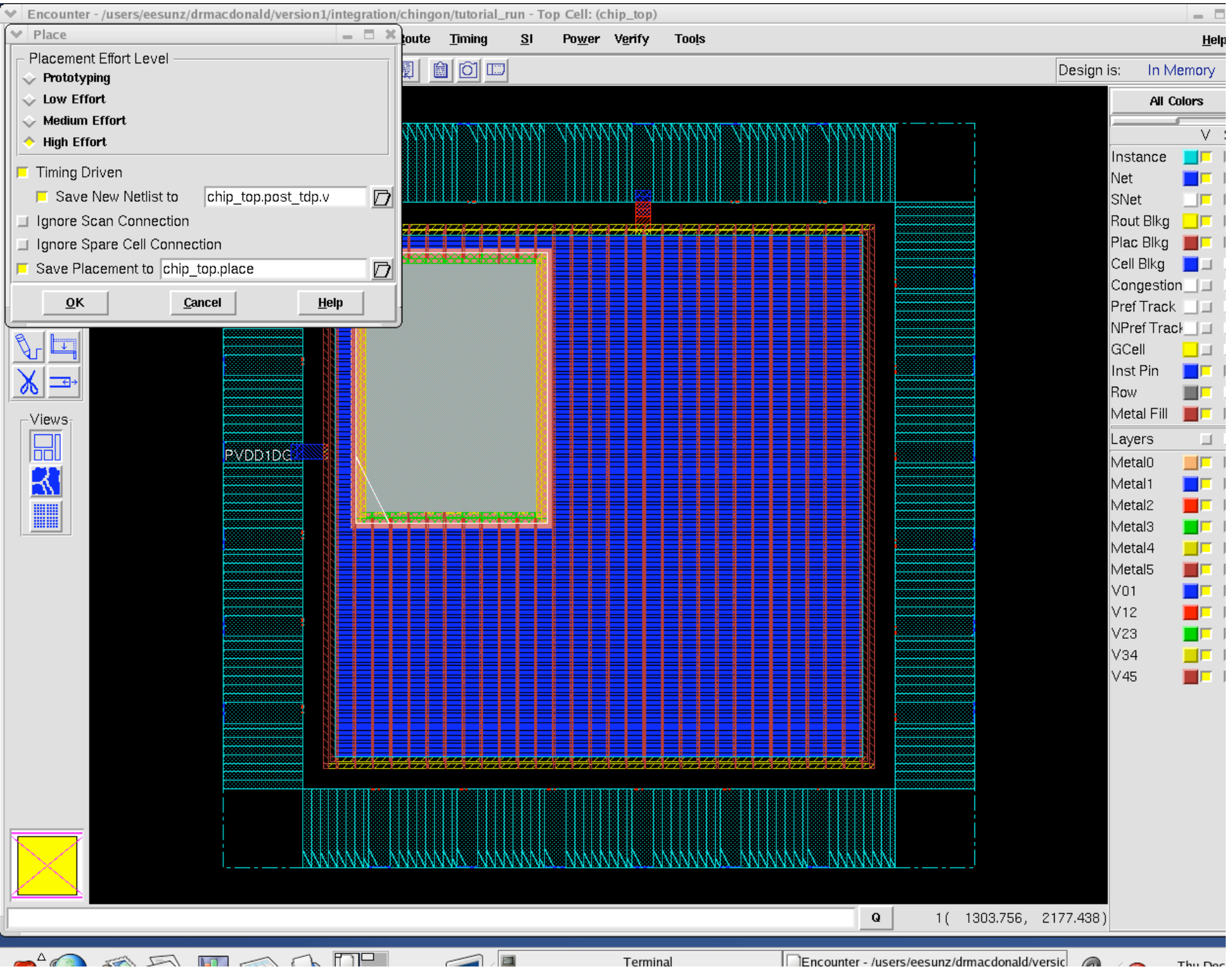

Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip_top)
Design FlipChip Partition Floorplan Place Clock Route Timing SI Power Verify Tools Help
Tools
Views
PVDD1DG
Add Stripes
Basic Advanced Via Generation
Set Configuration
Net(s): VSS VDD
Layer: METAL5
Direction: Vertical Horizontal
Width: 5
Spacing: 0.46 Update
Set Pattern
Set-to-set distance: 100
Number of sets: 30
Stripe Offset Boundary
Selected power domain/fence
Relative from core or area:
X from left: 0
X from right: 0
Y from top: 0
Y from bottom: 0
Absolute locations:
Start (X): 0 Point...
Stop (X): 0 Point...
Start (Y): 0 Point...
Stop (Y): 0 Point...
Wire Group
Use wire group
Interleaving
Number of bits: 0
Ok Variables Apply Cancel Defaults Help
In Memory
All Colors
1(1436.963, 2330.235)
Terminal
Add Stripes
Encounter - /users/eesunz/drmacdonald/versic
Thu Dec 14
3:48 PM

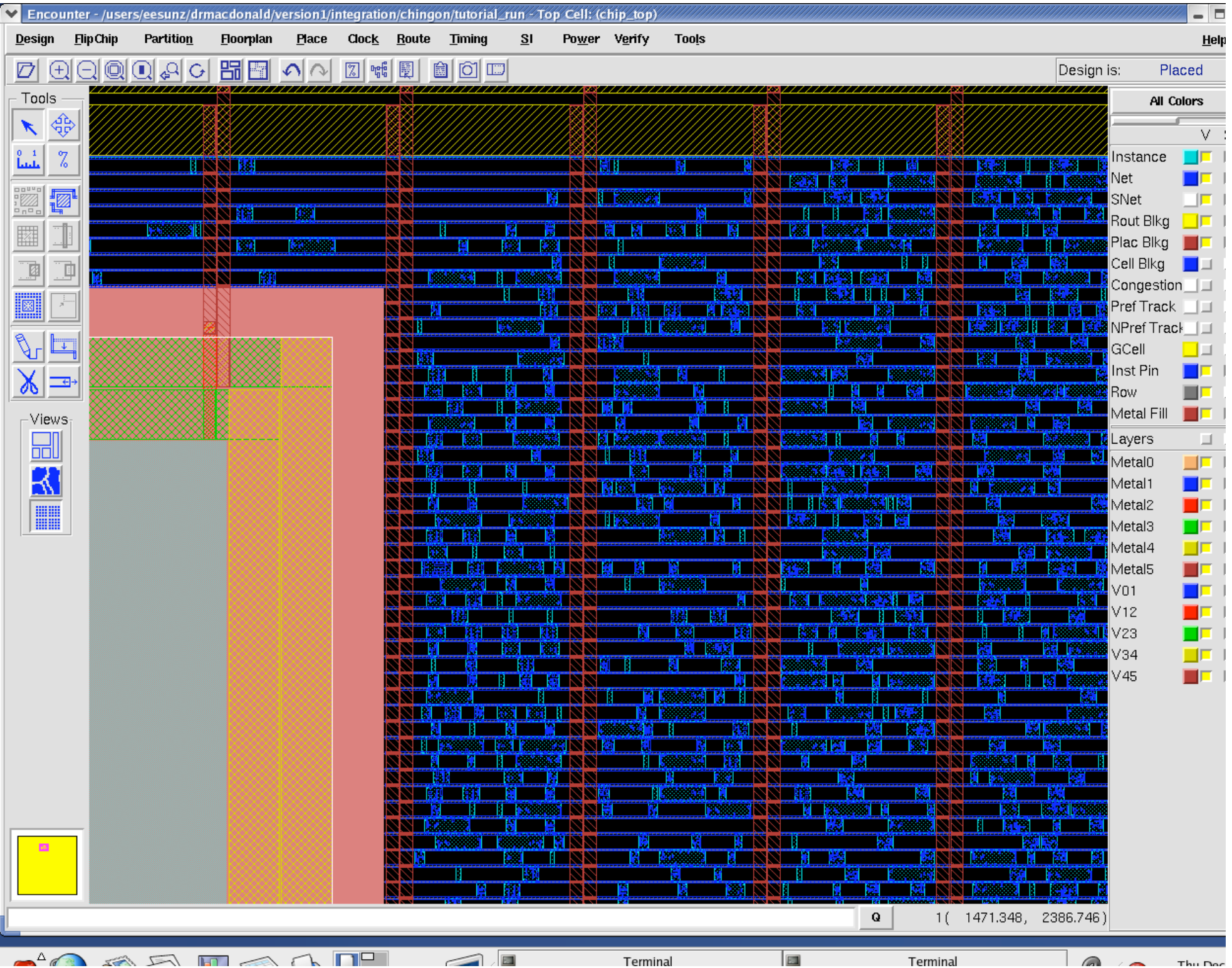

Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip_top)
Design FlipChip Partition Floorplan Place Clock Route Timing SI Power Verify Tools Help
Tools
Views
PVDD1DG
Add Stripes
Basic Advanced Via Generation
Stripe Breaking
Break stripes at block rings
Break stripes over selected blocks
Break stripes that overlap same direction/different net ring pins
Merge with rings if spacing less than: 0.8
Stripe Jogging
Switch layer to make pad/core connection
Switch layer to make block ring connection
Jog stripes to align with same net same direction wires/pins
Jog stripe to make block ring connection
Row and Boundary Handling
Allow stripes over rows
Route over rows only
Extend to:
Do not extend
Design boundary
Create pins
Pad pin or first pad ring
Pad pin or last pad ring
Specified stripe area
Specify area
Draw...
X1: 0
Y1: 0
X2: 0
Y2: 0
Snap wire center to routing grid: None
Ok Variables Apply Cancel Defaults Help
In Memory
All Colors
Inst: chip_io_test_out
Q
1(2016.806, 171.495)
Terminal
Add Stripes
Encounter - /users/eesunz/drmacdonald/versic
Thu Dec 14
3:50 PM

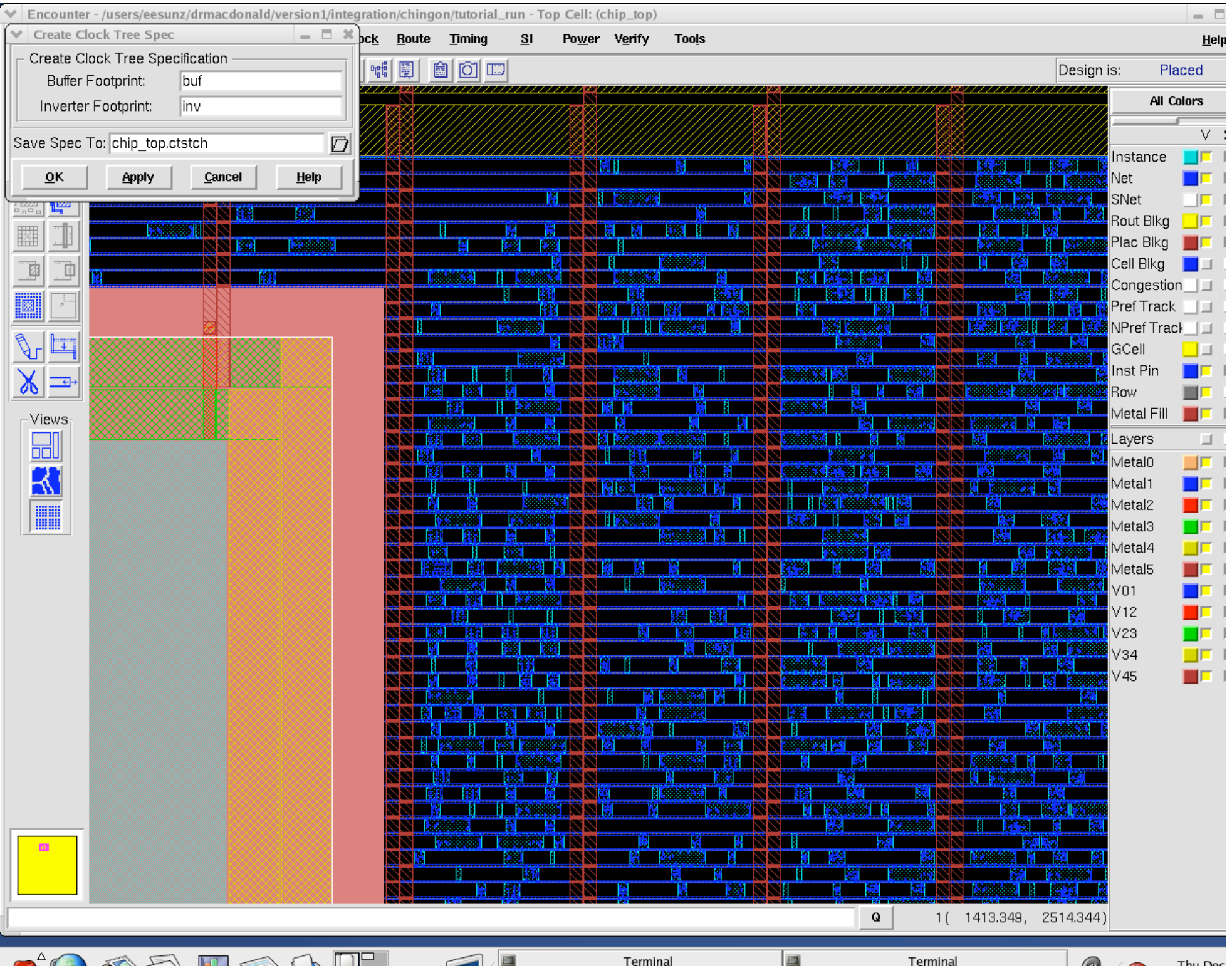

Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip_top)
Design FlipChip Partition Floorplan Place Clock Route Timing SI Power Verify Tools Help
Design is: In Memory
Tools
Views
All Colors
V S
Instance
Net
SNet
Rout Blkg
Plac Blkg
Cell Blkg
Congestion
Pref Track
NPref Track
GCell
Inst Pin
Row
Metal Fill
Layers
Metal0
Metal1
Metal2
Metal3
Metal4
Metal5
V01
V12
V23
V34
V45
Close up of stripes at memory edge
1(1038.074, 1394.406)
Terminal
Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip
Thu Dec 14
3:53 PM

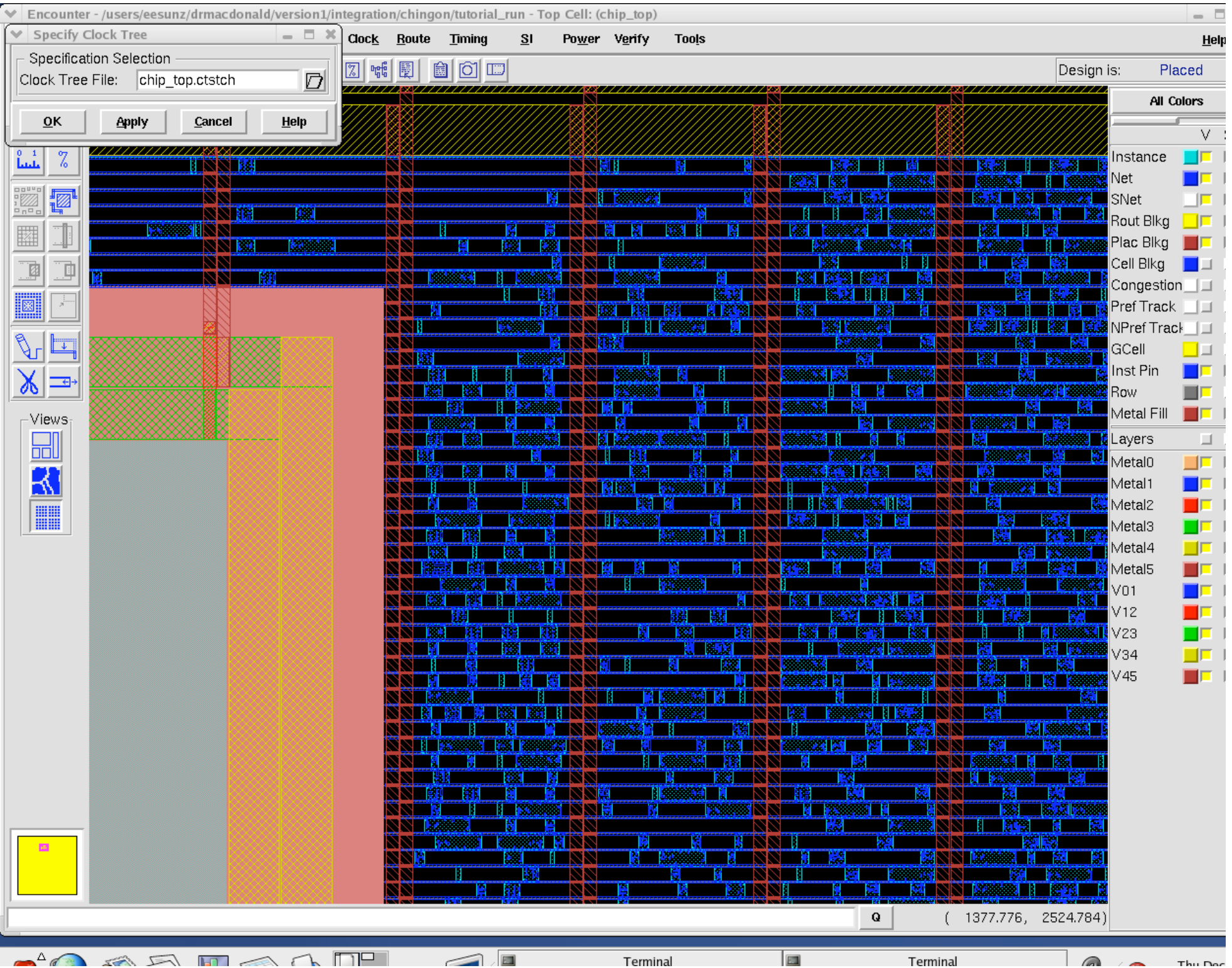

Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip_top)
Design FlipChip Partition Floorplan Place Clock Route Timing SI Power Verify Tools Help
Design is: In Memory
Tools
Views
Connect Ring Pins
Basic
Via Generation
Net(s): VSS VDD
All blocks
Selected block(s)
Sides:
Left
Right
Top
Bottom
Ring Pins
Top/Bottom edges
Left/Right edges
Layer
METAL1
METAL2
Minimum width
0.44
0.44
Maximum width
60
60
Maximum number of connections:
500
Allow routing over rows
Switch layer to connect
Ok
Apply
Cancel
Defaults
Help
All Colors
V S
Instance
Net
SNet
Rout Blkg
Plac Blkg
Cell Blkg
Congestion
Pref Track
NPref Track
GCell
Inst Pin
Row
Metal Fill
Layers
Metal0
Metal1
Metal2
Metal3
Metal4
Metal5
V01
V12
V23
V34
V45
Q
1(1573.732, 2217.707)
Terminal
Encounter - /users/eesunz/drmacdonald/versic
Connect Ring Pins
Thu Dec 14
3:54 PM

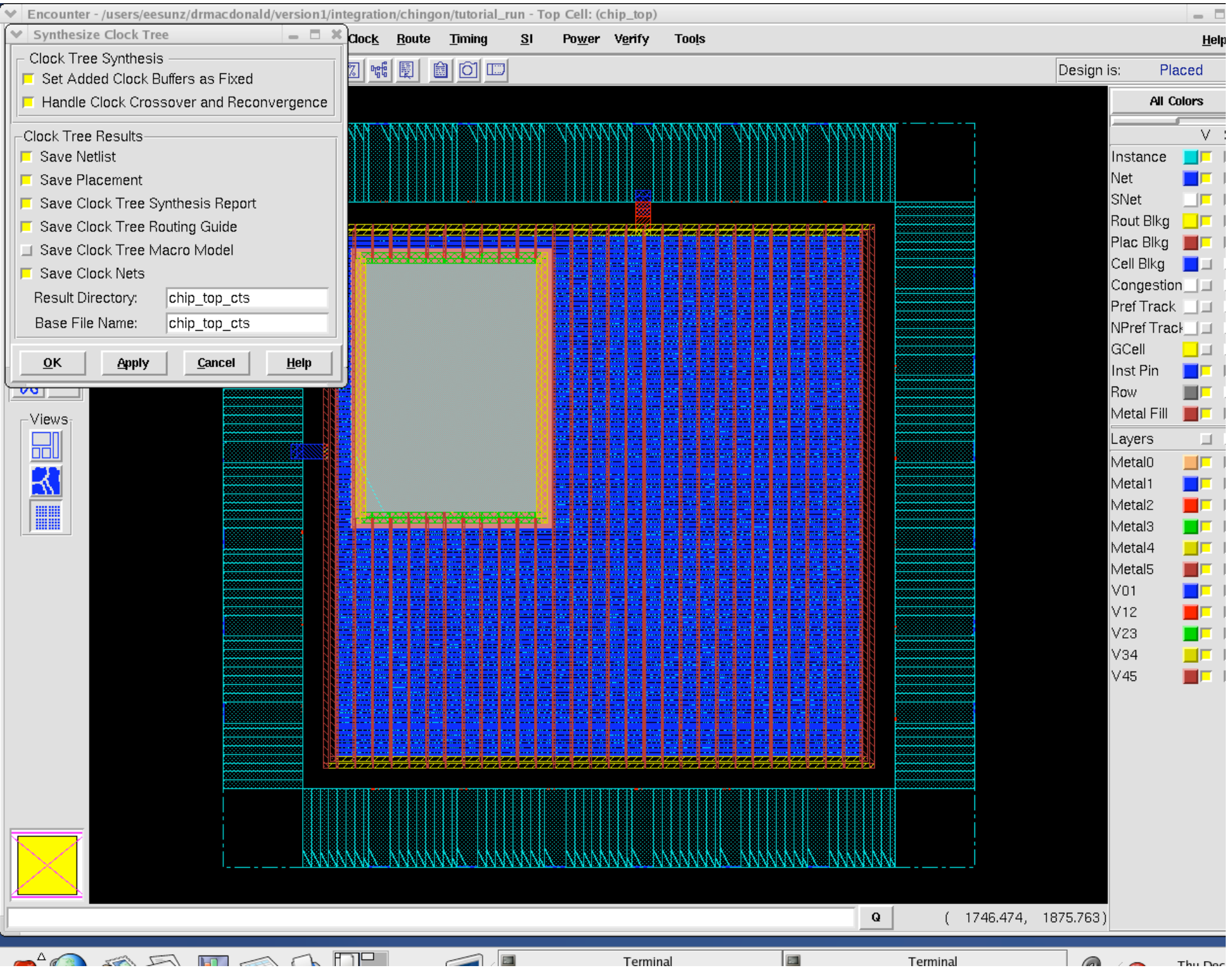

Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip_top)
SRoute
Basic
Advanced
Via Generation
Net(s): VSS VDD
Route:
Block pins
Pad pins
Pad rings
Standard cell pins
Stripes (unconnected)
Level shifter pins
Net(s):
Routing Control
Layer Change Control
Top layer: M5
Bottom layer: M1
Straight connections and allow jogging
Prefer straight with layer change
Prefer different layer jog
Prefer same layer jog
Straight connections only
DRC clean
Allow layer change
Same layer routing only
Area
Draw
X1:
Y1:
X2:
Y2:
Connect to target inside the area only
Delete existing routes
Generate progress messages
0
Extra config file
OK
Apply
Defaults
Cancel
Help
Design is: In Memory
All Colors
V S
Instance
Net
SNet
Rout Blkg
Plac Blkg
Cell Blkg
Congestion
Pref Track
NPref Track
GCell
Inst Pin
Row
Metal Fill
Layers
Metal0
Metal1
Metal2
Metal3
Metal4
Metal5
V01
V12
V23
V34
V45
Q
1(1954.046, 2328.170)
Terminal
SRoute
Encounter - /users/eesunz/drmacdonald/versic
Thu Dec 14
3:55 PM

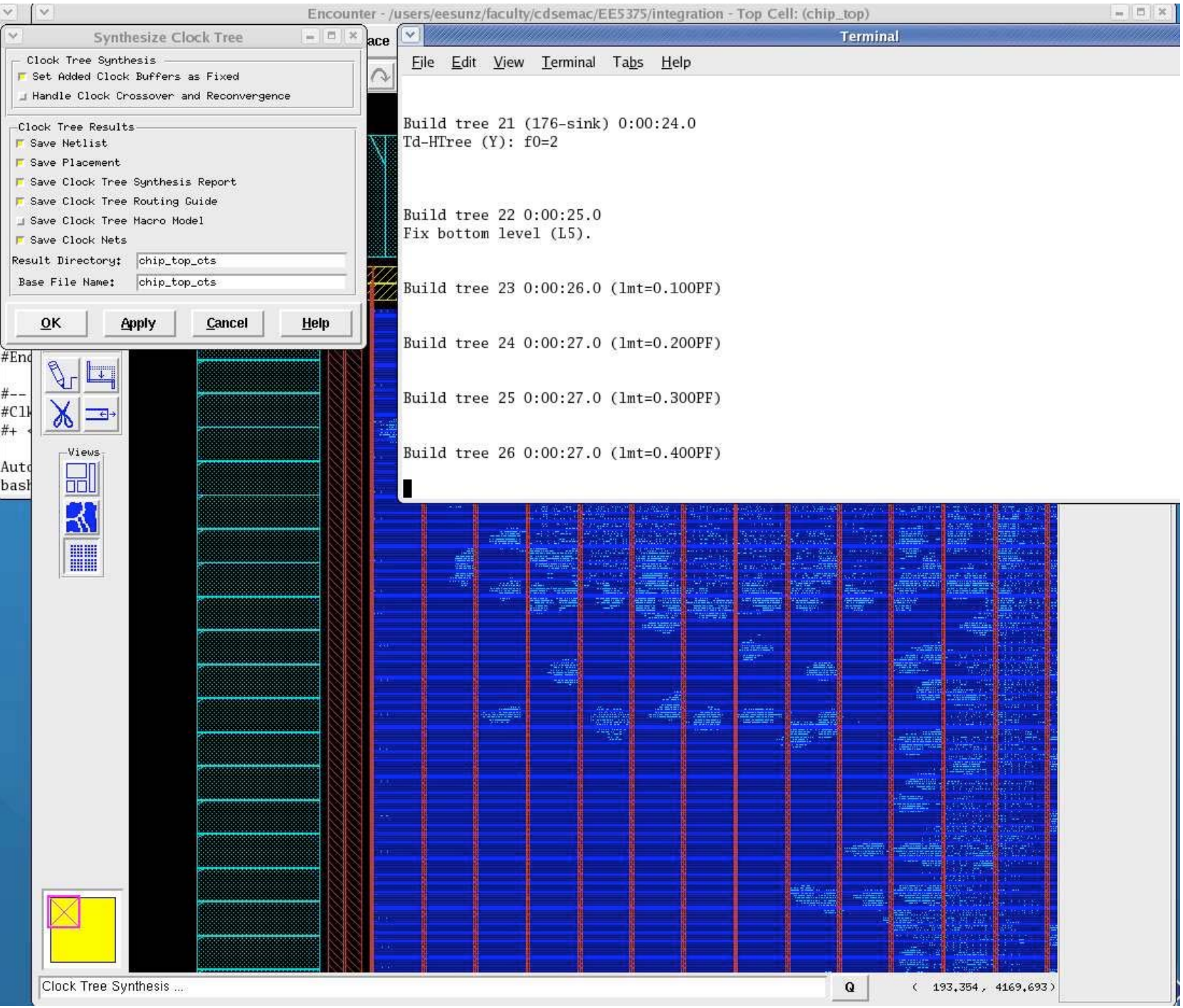

Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip_top)
Place
Placement Effort Level
Prototyping
Low Effort
Medium Effort
High Effort
Timing Driven
Save New Netlist to
chip_top.post_tdp.v
Ignore Scan Connection
Ignore Spare Cell Connection
Save Placement to
chip_top.place
OK
Cancel
Help
Route
Timing
SI
Power
Verify
Tools
Help
Design is:
In Memory
All Colors
Instance
Net
SNet
Rout Blkg
Plac Blkg
Cell Blkg
Congestion
Pref Track
NPref Track
GCell
Inst Pin
Row
Metal Fill
Layers
Metal0
Metal1
Metal2
Metal3
Metal4
Metal5
V01
V12
V23
V34
V45
Views
PVDD1DG
Q
1(1303.756, 2177.438)
Terminal
Encounter - /users/eesunz/drmacdonald/versic

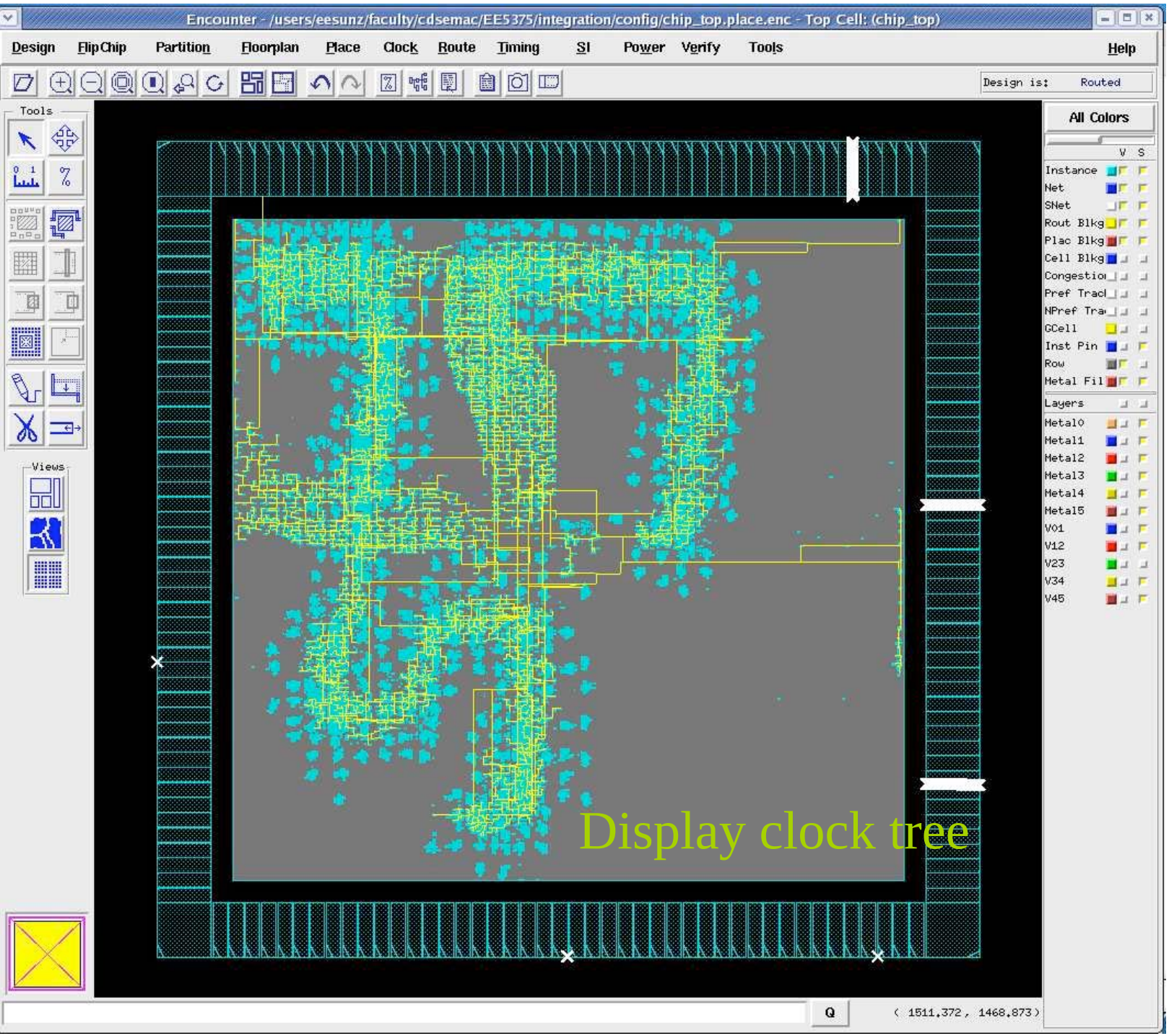

Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip_top)
Design FlipChip Partition Floorplan Place Clock Route Timing SI Power Verify Tools Help
Design is: Placed
Tools
Views
All Colors
Instance
Net
SNet
Rout Blkg
Plac Blkg
Cell Blkg
Congestion
Pref Track
NPref Track
GCell
Inst Pin
Row
Metal Fill
Layers
Metal0
Metal1
Metal2
Metal3
Metal4
Metal5
V01
V12
V23
V34
V45
Q
1(1471.348, 2386.746)
Terminal
Terminal

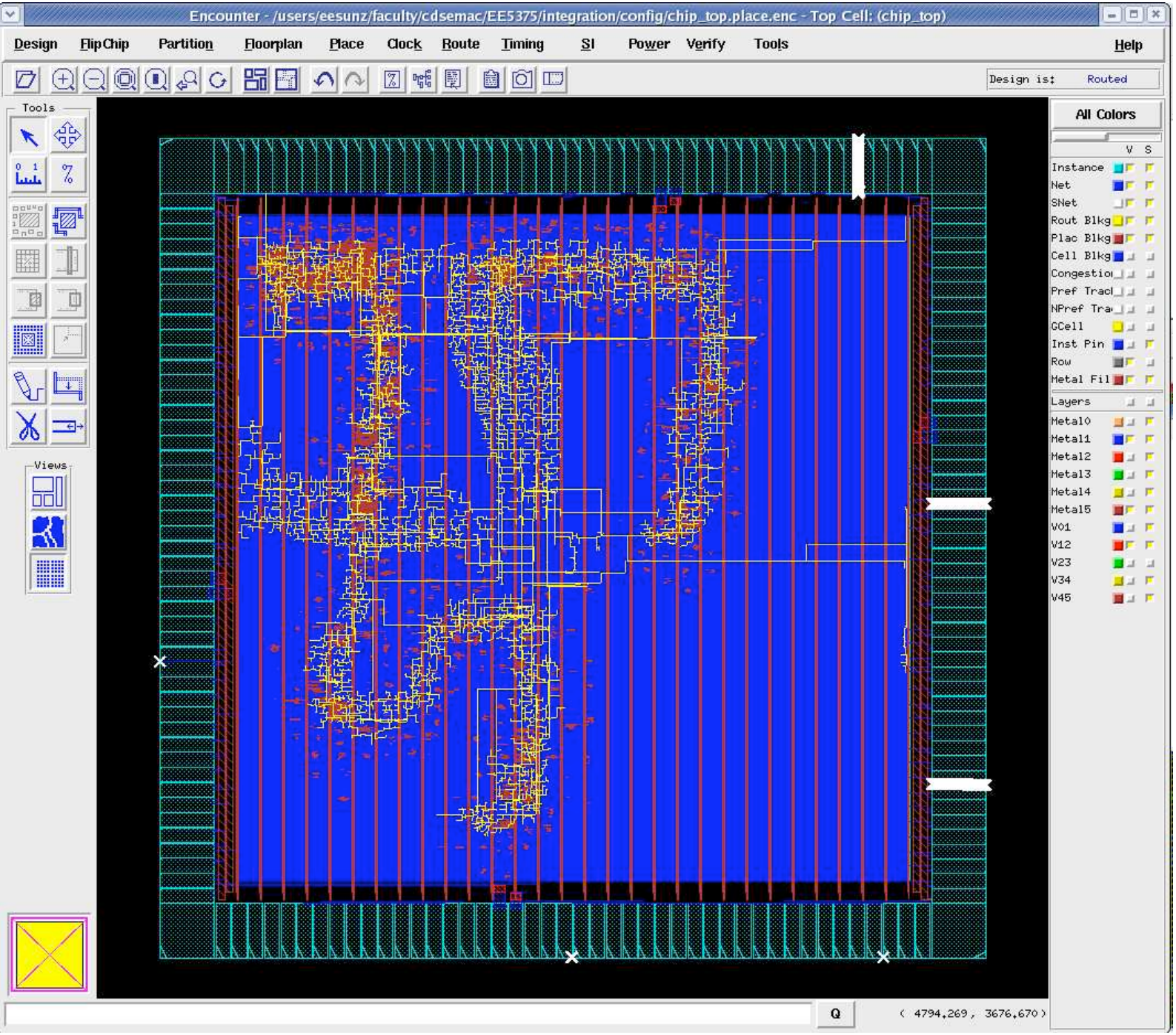

Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip_top)
Create Clock Tree Spec
Create Clock Tree Specification
Buffer Footprint:
buf
Inverter Footprint:
inv
Save Spec To:
chip_top.ctstch
OK
Apply
Cancel
Help
Route
Timing
SI
Power
Verify
Tools
Help
Design is:
Placed
All Colors
Instance
Net
SNet
Rout Blkg
Plac Blkg
Cell Blkg
Congestion
Pref Track
NPref Track
GCell
Inst Pin
Row
Metal Fill
Layers
Metal0
Metal1
Metal2
Metal3
Metal4
Metal5
V01
V12
V23
V34
V45
Views
Q
1(1413.349, 2514.344)
Terminal
Terminal

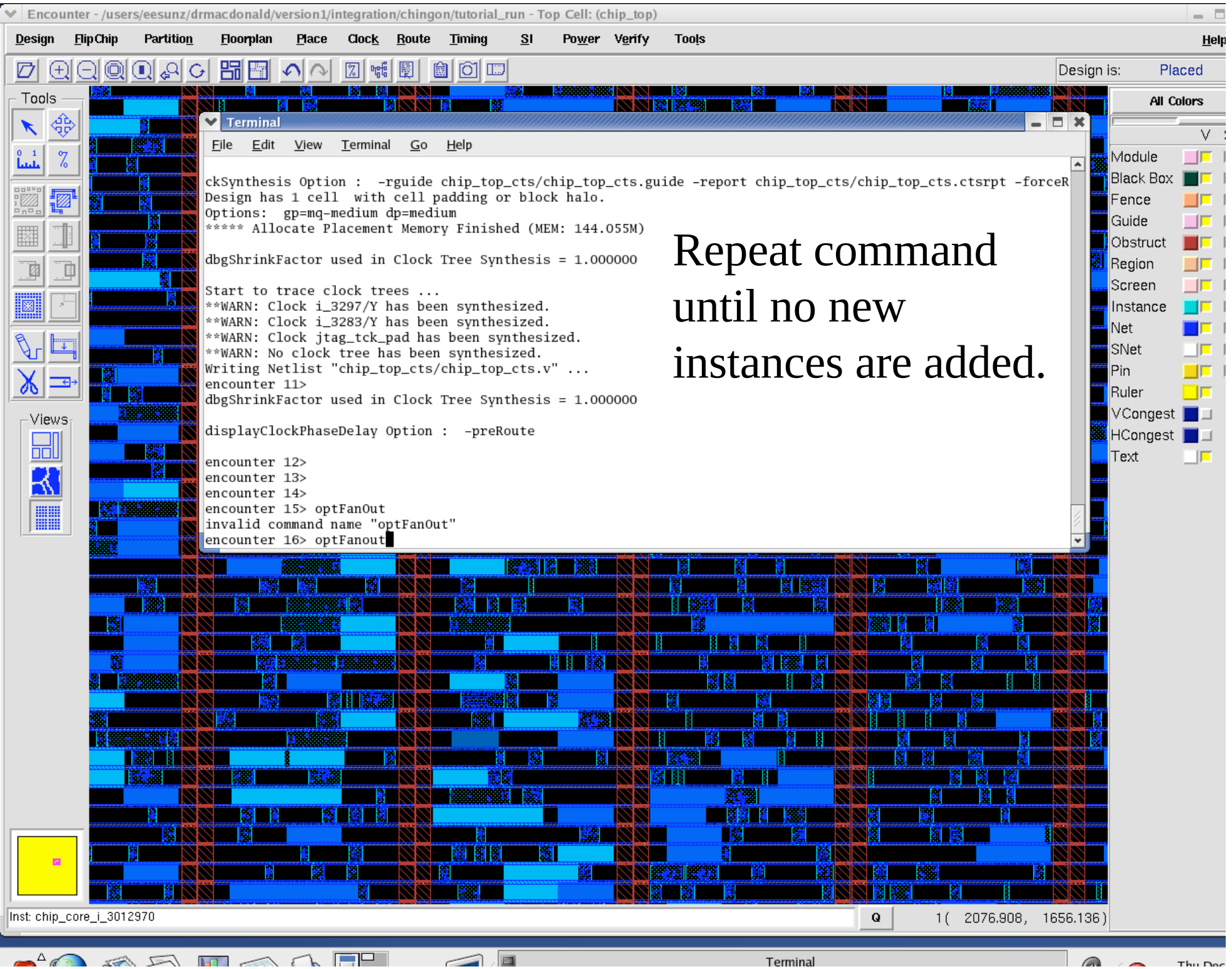

Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip_top)
Specify Clock Tree
Specification Selection
Clock Tree File:
chip_top.ctstch
OK
Apply
Cancel
Help
Clock
Route
Timing
SI
Power
Verify
Tools
Help
Design is:
Placed
All Colors
Instance
Net
SNet
Rout Blkg
Plac Blkg
Cell Blkg
Congestion
Pref Track
NPref Track
GCell
Inst Pin
Row
Metal Fill
Layers
Metal0
Metal1
Metal2
Metal3
Metal4
Metal5
V01
V12
V23
V34
V45
Views
Q
(1377.776, 2524.784)
Terminal
Terminal

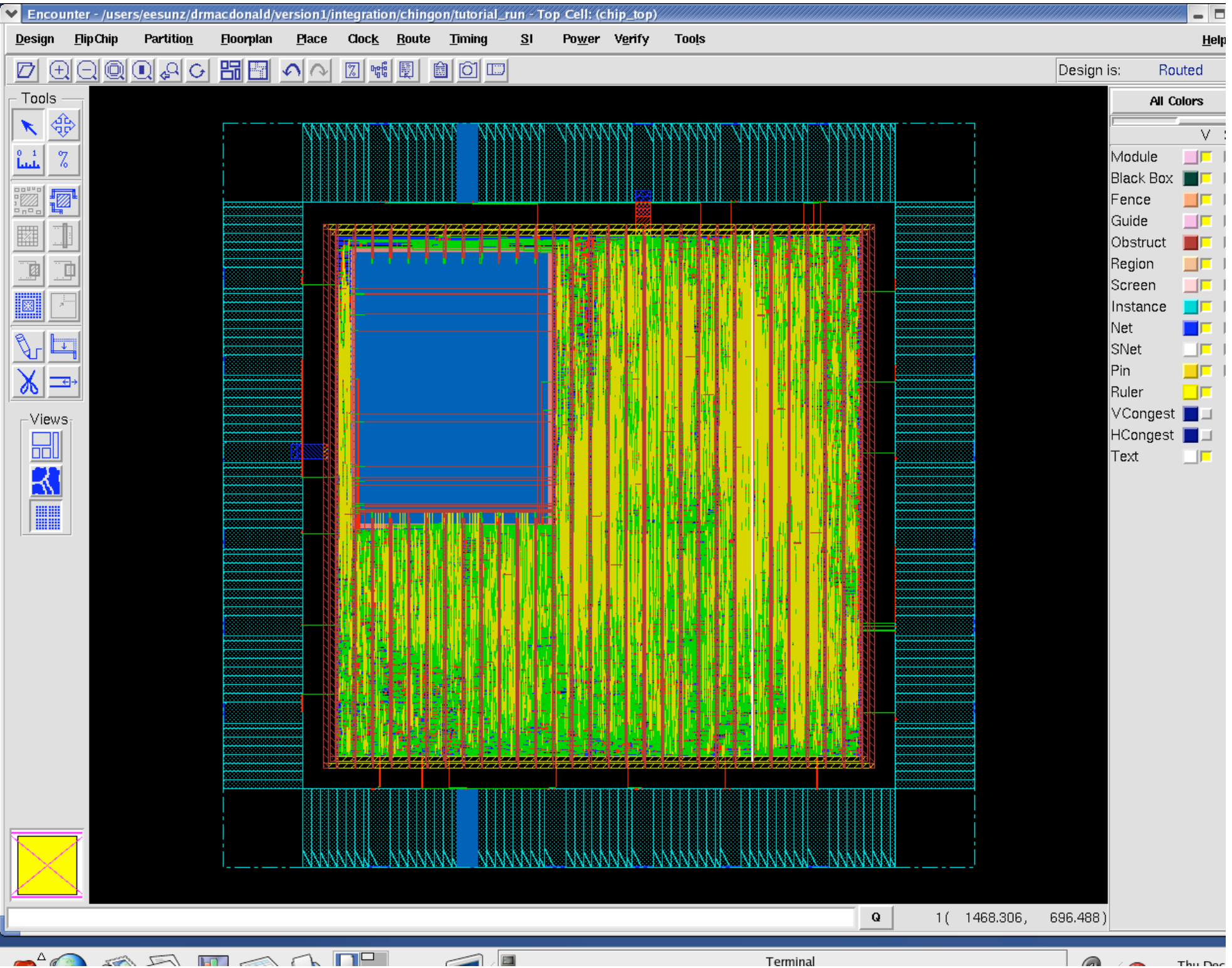

Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip_top)
Synthesize Clock Tree
Clock Tree Synthesis
Set Added Clock Buffers as Fixed
Handle Clock Crossover and Reconvergence
Clock Tree Results
Save Netlist
Save Placement
Save Clock Tree Synthesis Report
Save Clock Tree Routing Guide
Save Clock Tree Macro Model
Save Clock Nets
Result Directory: chip_top_cts
Base File Name: chip_top_cts
OK
Apply
Cancel
Help
Clock
Route
Timing
SI
Power
Verify
Tools
Help
Design is: Placed
All Colors
Instance
Net
SNet
Rout Blkg
Plac Blkg
Cell Blkg
Congestion
Pref Track
NPref Track
GCell
Inst Pin
Row
Metal Fill
Layers
Metal0
Metal1
Metal2
Metal3
Metal4
Metal5
V01
V12
V23
V34
V45
Views
Q
(1746.474, 1875.763)
Terminal
Terminal

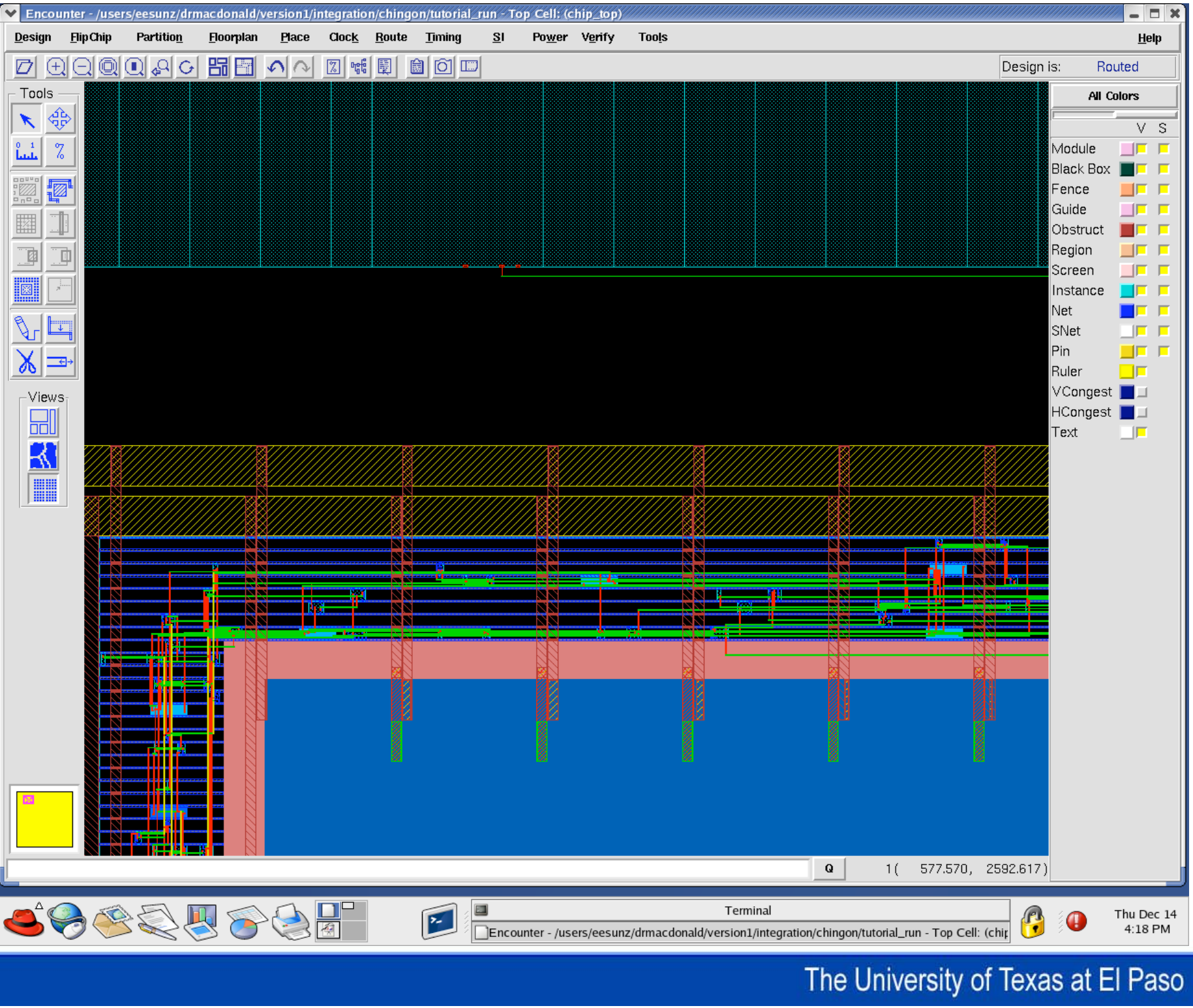

Encounter - /users/eesunz/faculty/cdsemac/EE5375/integration - Top Cell: (chip_top)
Synthesize Clock Tree
Clock Tree Synthesis
Set Added Clock Buffers as Fixed
Handle Clock Crossover and Reconvergence
Clock Tree Results
Save Netlist
Save Placement
Save Clock Tree Synthesis Report
Save Clock Tree Routing Guide
Save Clock Tree Macro Model
Save Clock Nets
Result Directory: chip_top_cts
Base File Name: chip_top_cts
OK
Apply
Cancel
Help
Terminal
File Edit View Terminal Tabs Help
Build tree 21 (176-sink) 0:00:24.0
Td-HTree (Y): f0=2
Build tree 22 0:00:25.0
Fix bottom level (L5).
Build tree 23 0:00:26.0 (lmt=0.100PF)
Build tree 24 0:00:27.0 (lmt=0.200PF)
Build tree 25 0:00:27.0 (lmt=0.300PF)
Build tree 26 0:00:27.0 (lmt=0.400PF)
Views
Clock Tree Synthesis ...
Q
(193.354 , 4169.693)

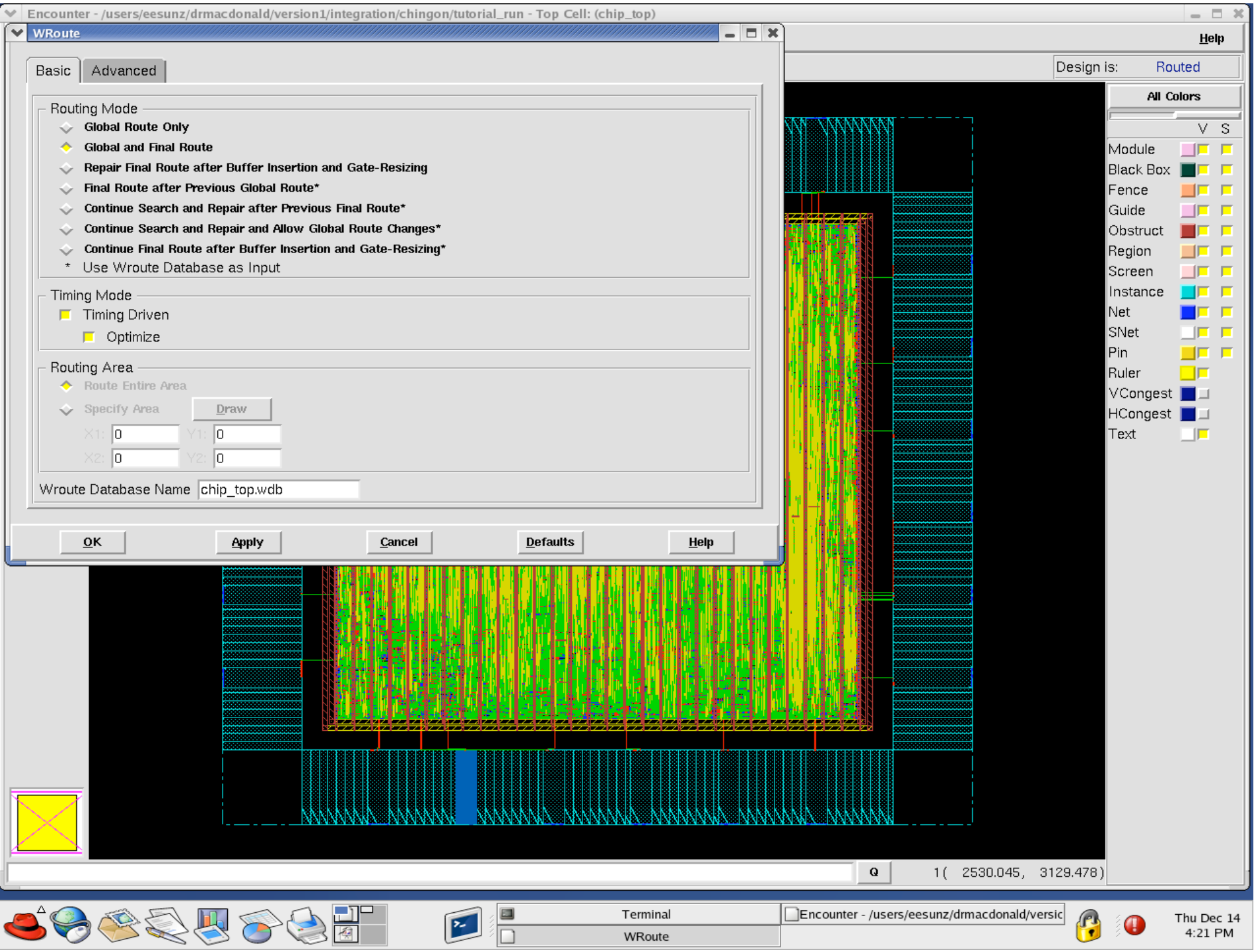

Encounter - /users/eesunz/faculty/cdsemac/EE5375/integration/config/chip_top.place.enc - Top Cell: (chip_top)
Design FlipChip Partition Floorplan Place Clock Route Timing SI Power Verify Tools Help
Design is: Routed
Tools
Views
All Colors
V S
Instance
Net
SNet
Rout Blkg
Plac Blkg
Cell Blkg
Congestio
Pref Tracl
NPref Tra
GCell
Inst Pin
Row
Metal Fil
Layers
Metal0
Metal1
Metal2
Metal3
Metal4
Metal5
V01
V12
V23
V34
V45
Display clock tree
Q
(1511.372, 1468.873)

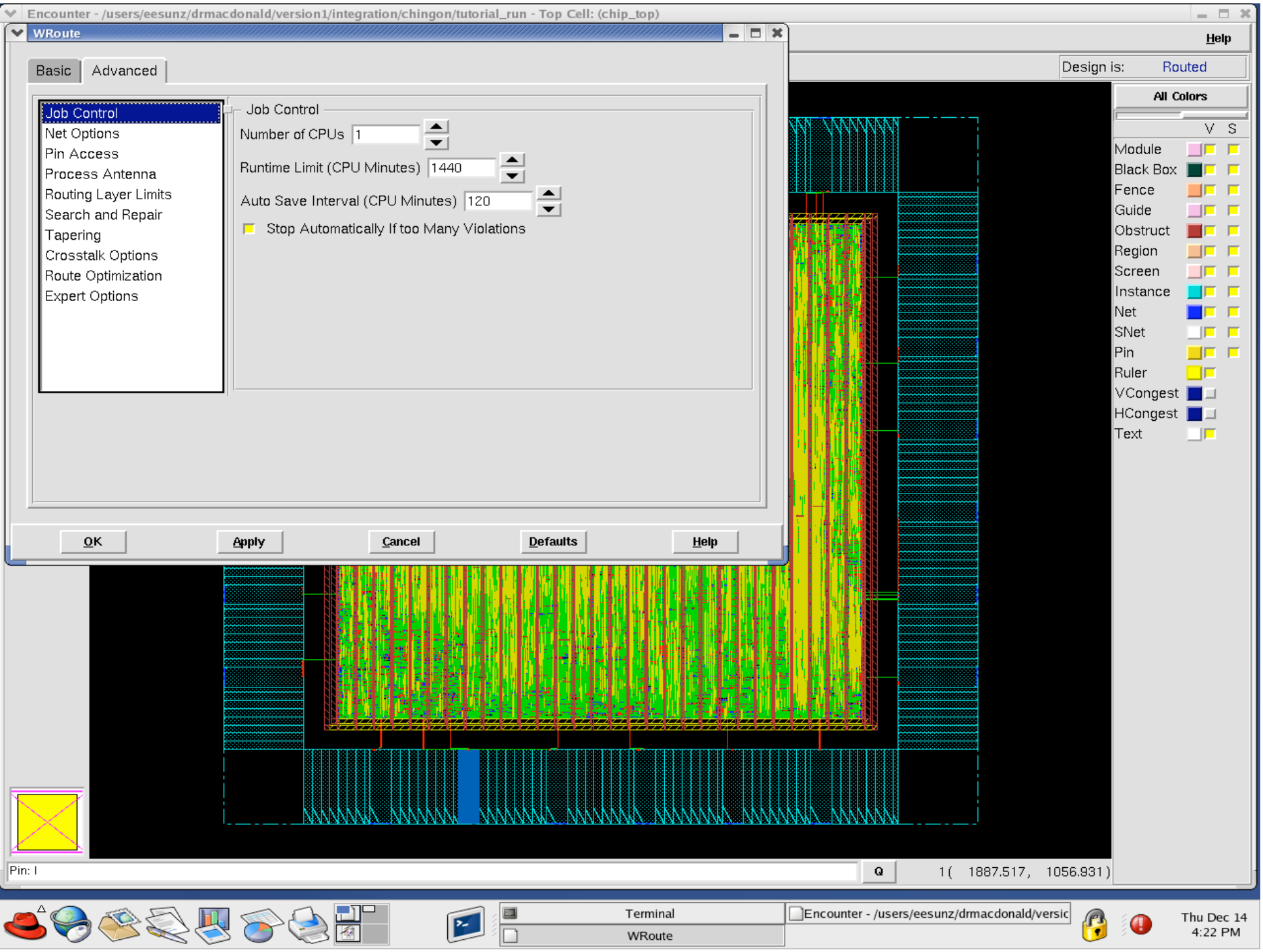

Encounter - /users/eesunz/faculty/cdsemac/EE5375/integration/config/chip_top.place.enc - Top Cell: (chip_top)
Design FlipChip Partition Floorplan Place Clock Route Timing SI Power Verify Tools Help
Design is: Routed
Tools
Views
All Colors
V S
Instance
Net
SNet
Rout Blkg
Plac Blkg
Cell Blkg
Congestio
Pref Trac
NPref Tra
GCell
Inst Pin
Row
Metal Fil
Layers
Metal0
Metal1
Metal2
Metal3
Metal4
Metal5
V01
V12
V23
V34
V45
Q
(4794,269 , 3676,670)

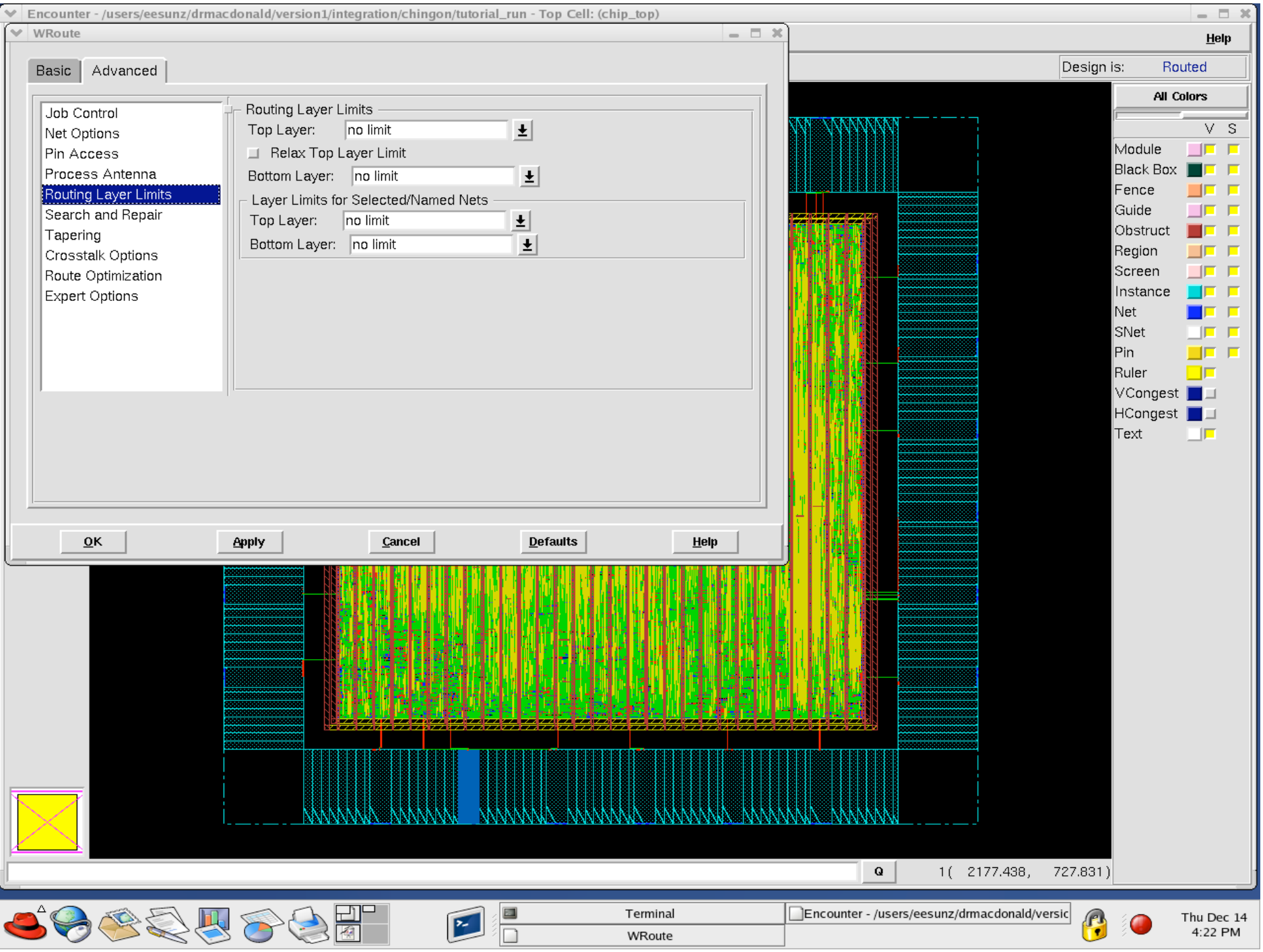

Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip_top)
Design FlipChip Partition Floorplan Place Clock Route Timing SI Power Verify Tools Help
Design is: Placed
Tools
Views
Terminal
File Edit View Terminal Go Help
ckSynthesis Option : -rguide chip_top_cts/chip_top_cts.guide -report chip_top_cts/chip_top_cts.ctsrpt -forceR
Design has 1 cell with cell padding or block halo.
Options: gp=mq-medium dp=medium
***** Allocate Placement Memory Finished (MEM: 144.055M)
dbgShrinkFactor used in Clock Tree Synthesis = 1.000000
Start to trace clock trees ...
**WARN: Clock i_3297/Y has been synthesized.
**WARN: Clock i_3283/Y has been synthesized.
**WARN: Clock jtag_tck_pad has been synthesized.
**WARN: No clock tree has been synthesized.
Writing Netlist "chip_top_cts/chip_top_cts.v" ...
encounter 11>
dbgShrinkFactor used in Clock Tree Synthesis = 1.000000
displayClockPhaseDelay Option : -preRoute
encounter 12>
encounter 13>
encounter 14>
encounter 15> optFanOut
invalid command name "optFanOut"
encounter 16> optFanout
Repeat command until no new instances are added.
All Colors
Module
Black Box
Fence
Guide
Obstruct
Region
Screen
Instance
Net
SNet
Pin
Ruler
VCongest
HCongest
Text
Inst: chip_core_i_3012970
Q
1(2076.908, 1656.136)
Terminal

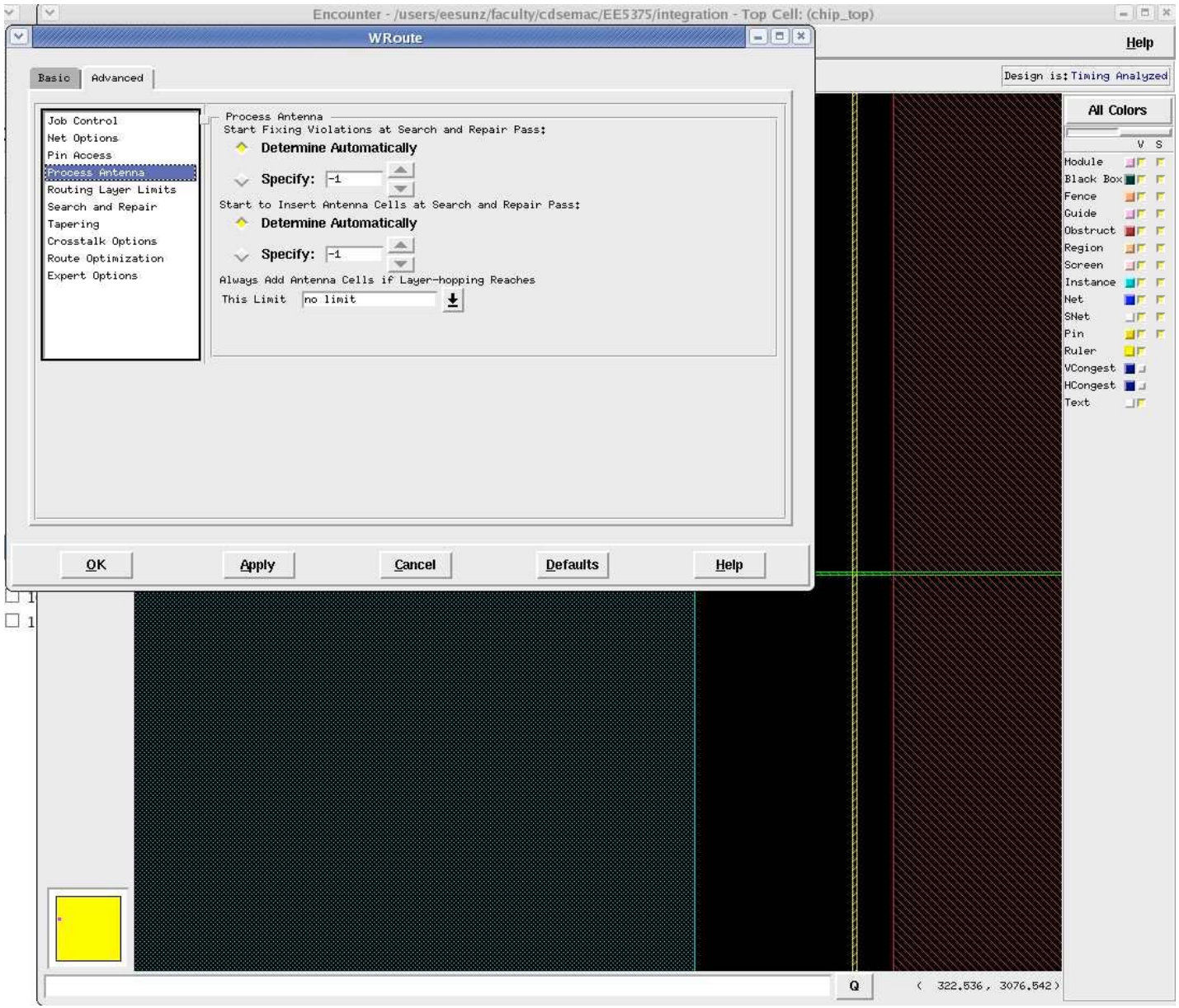

Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip_top)
Design FlipChip Partition Floorplan Place Clock Route Timing SI Power Verify Tools Help
Design is: Routed
Tools
Views
All Colors
Module
Black Box
Fence
Guide
Obstruct
Region
Screen
Instance
Net
SNet
Pin
Ruler
VCongest
HCongest
Text
Q
1(1468.306, 696.488)
Terminal


Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip_top)
Design FlipChip Partition Floorplan Place Clock Route Timing SI Power Verify Tools Help
Design is: Routed
Tools
Views
All Colors
V S
Module
Black Box
Fence
Guide
Obstruct
Region
Screen
Instance
Net
SNet
Pin
Ruler
VCongest
HCongest
Text
Q
1(577.570, 2592.617)
Terminal
Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip
Thu Dec 14
4:18 PM

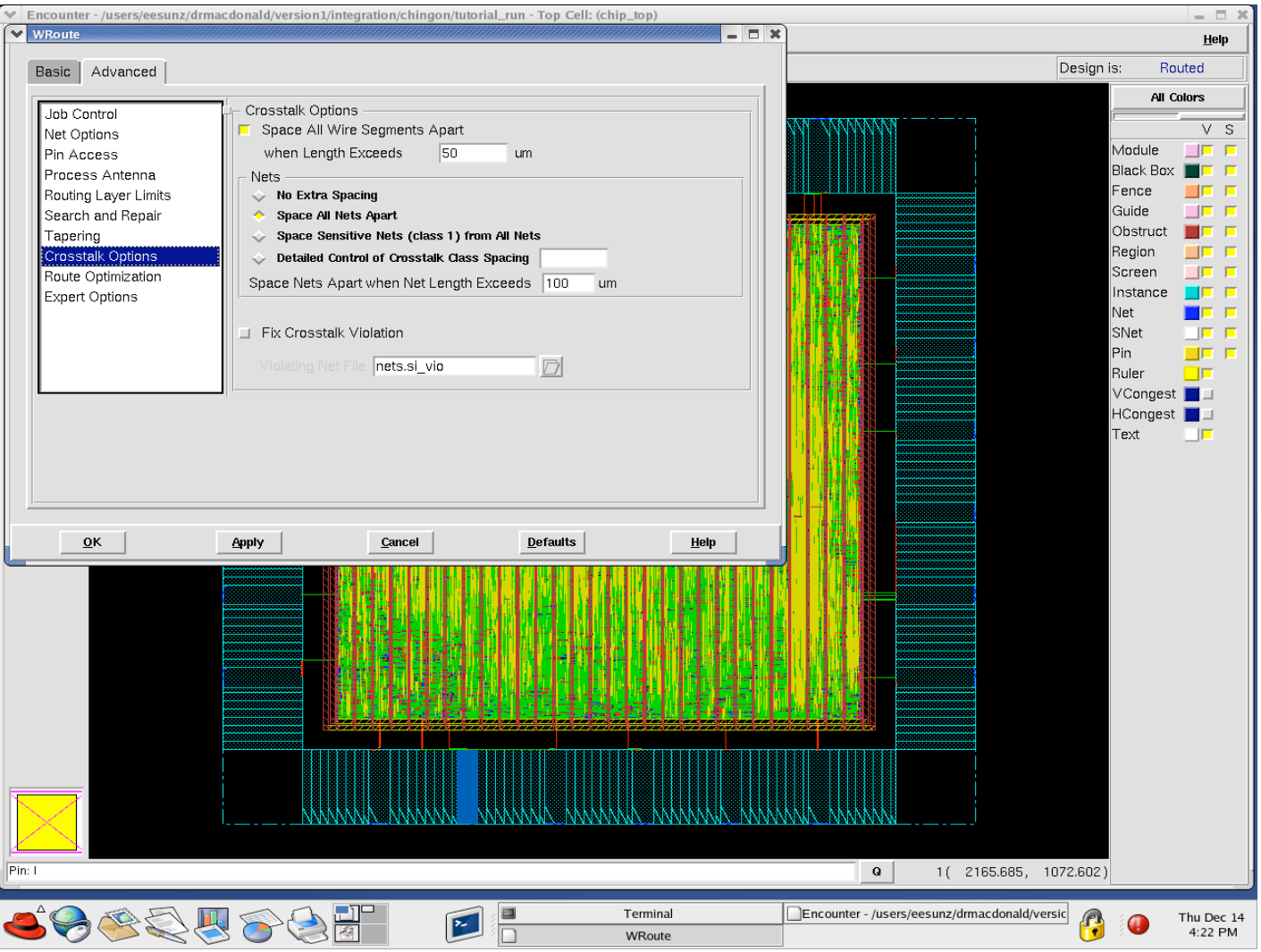

Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip_top)
WRoute
Basic
Advanced
Routing Mode
Global Route Only
Global and Final Route
Repair Final Route after Buffer Insertion and Gate-Resizing
Final Route after Previous Global Route*
Continue Search and Repair after Previous Final Route*
Continue Search and Repair and Allow Global Route Changes*
Continue Final Route after Buffer Insertion and Gate-Resizing*
* Use Wroute Database as Input
Timing Mode
Timing Driven
Optimize
Routing Area
Route Entire Area
Specify Area
Draw
X1: 0
Y1: 0
X2: 0
Y2: 0
Wroute Database Name chip_top.wdb
OK
Apply
Cancel
Defaults
Help
Help
Design is: Routed
All Colors
V S
Module
Black Box
Fence
Guide
Obstruct
Region
Screen
Instance
Net
SNet
Pin
Ruler
VCongest
HCongest
Text
Q
1(2530.045, 3129.478)
Terminal
WRoute
Encounter - /users/eesunz/drmacdonald/versic
Thu Dec 14
4:21 PM


Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip_top)
WRoute
Basic
Advanced
Job Control
Net Options
Pin Access
Process Antenna
Routing Layer Limits
Search and Repair
Tapering
Crosstalk Options
Route Optimization
Expert Options
Job Control
Number of CPUs 1
Runtime Limit (CPU Minutes) 1440
Auto Save Interval (CPU Minutes) 120
Stop Automatically If too Many Violations
OK
Apply
Cancel
Defaults
Help
Help
Design is: Routed
All Colors
V S
Module
Black Box
Fence
Guide
Obstruct
Region
Screen
Instance
Net
SNet
Pin
Ruler
VCongest
HCongest
Text
Pin: I
Q
1(1887.517, 1056.931)
Terminal
WRoute
Encounter - /users/eesunz/drmacdonald/versic
Thu Dec 14
4:22 PM


Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip_top)
WRoute
Basic
Advanced
Job Control
Net Options
Pin Access
Process Antenna
Routing Layer Limits
Search and Repair
Tapering
Crosstalk Options
Route Optimization
Expert Options
Routing Layer Limits
Top Layer: no limit
Relax Top Layer Limit
Bottom Layer: no limit
Layer Limits for Selected/Named Nets
Top Layer: no limit
Bottom Layer: no limit
OK
Apply
Cancel
Defaults
Help
Help
Design is: Routed
All Colors
V S
Module
Black Box
Fence
Guide
Obstruct
Region
Screen
Instance
Net
SNet
Pin
Ruler
VCongest
HCongest
Text
1(2177.438, 727.831)
Terminal
WRoute
Encounter - /users/eesunz/drmacdonald/versic
Thu Dec 14
4:22 PM

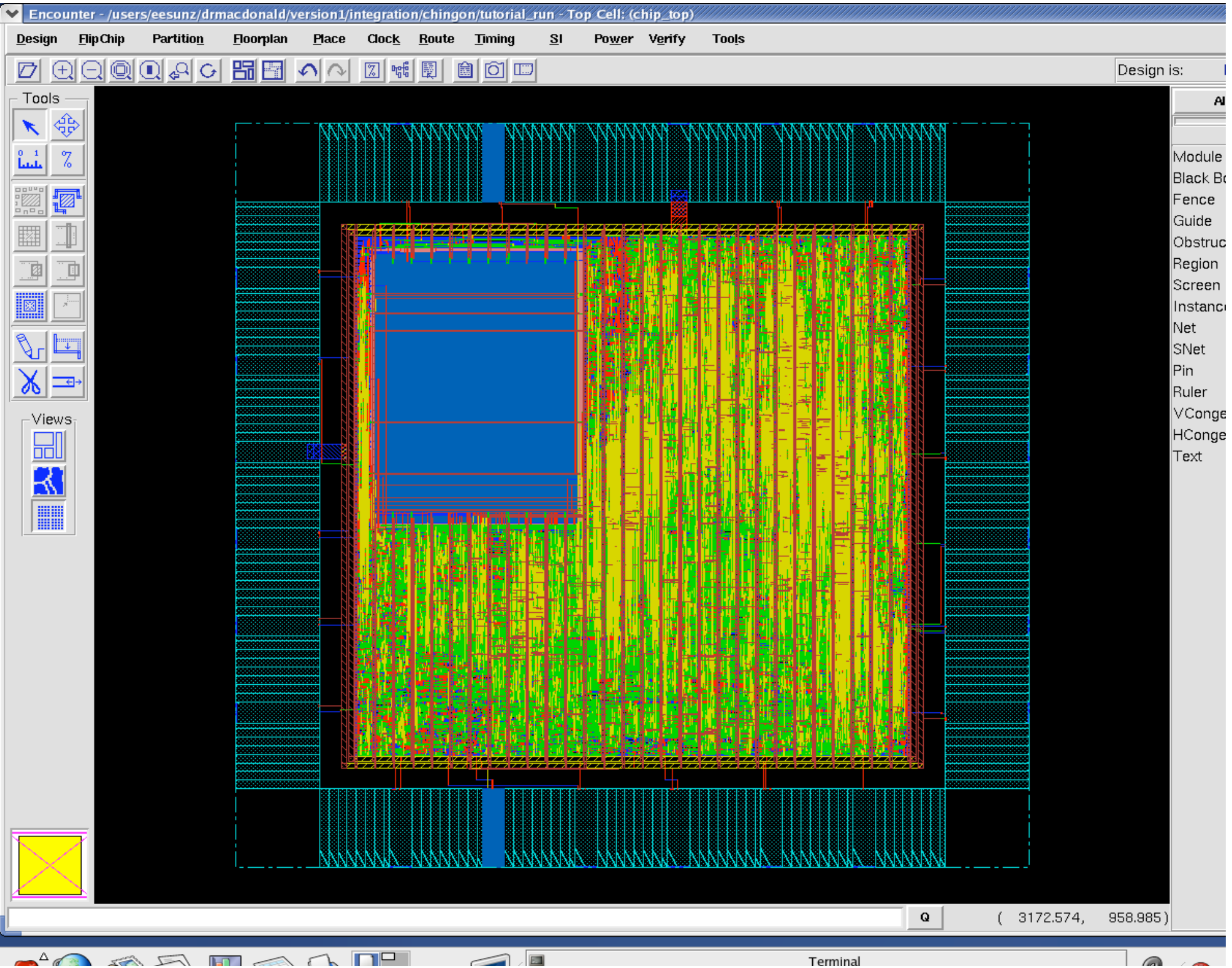


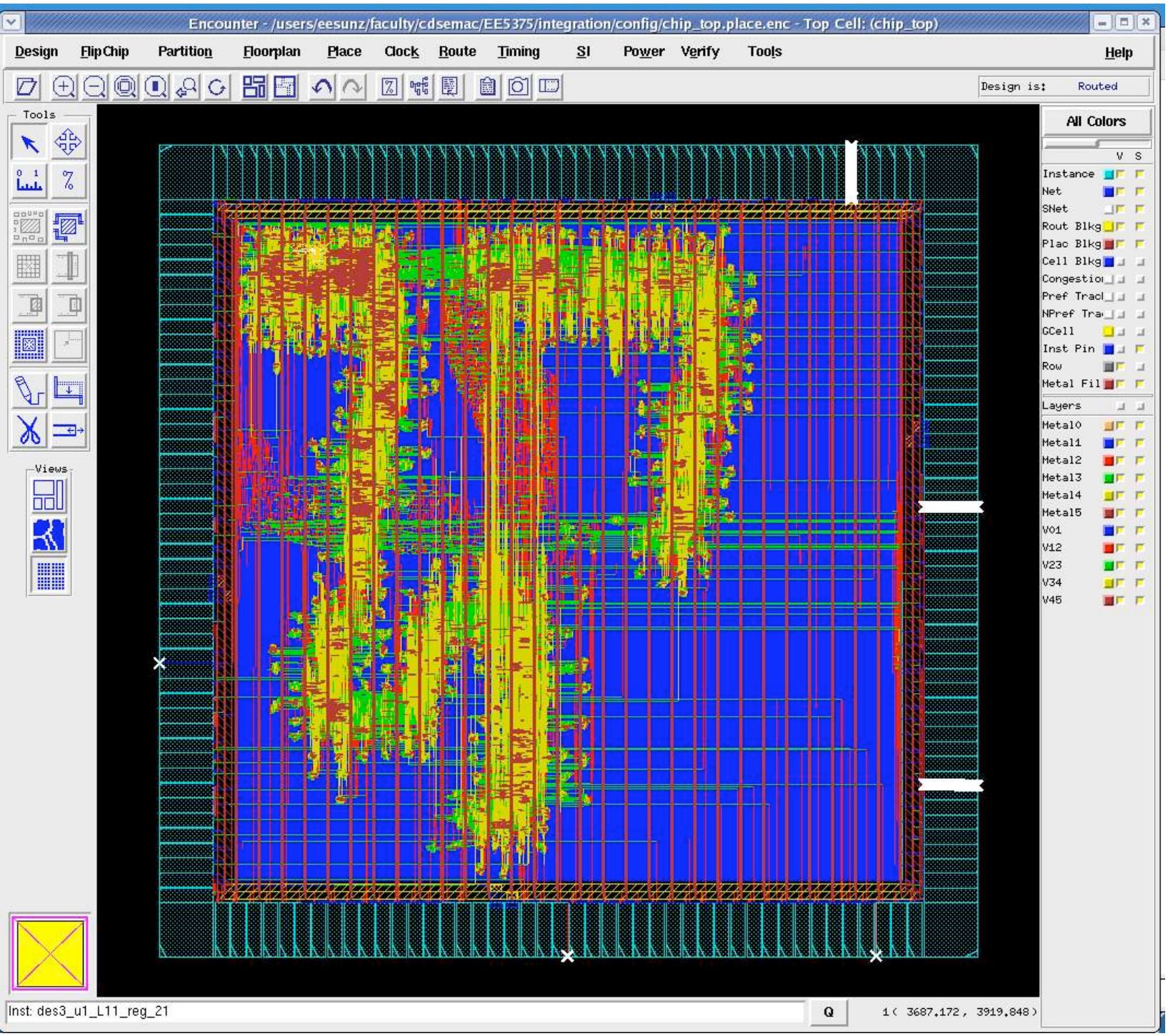
Antenna refers to a potential process problem. When plasma etching metal lines, long metal structures will build up charge. A metal line connected to a gate only will “pop” the oxide. Tying a metal line to a drain or antenna diode fixes the problem, but better solution is job line to break continuity.

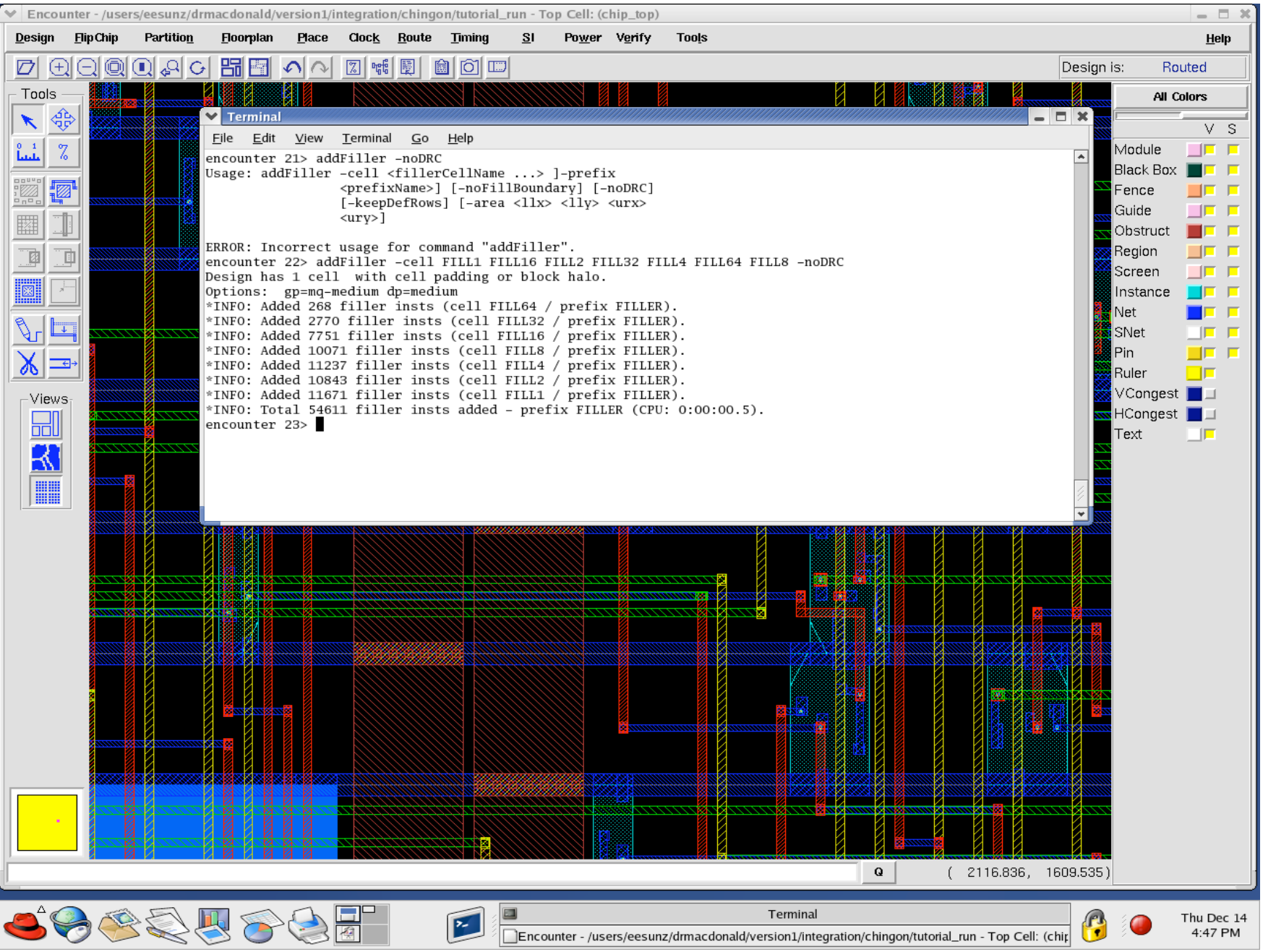


Two signals running in parallel for a long time, build a parasitic capacitance between them. If one (the aggressor) switches, the other (quiet net) can temporarily jump or if switching can be slowed down due to noise-induced delay.

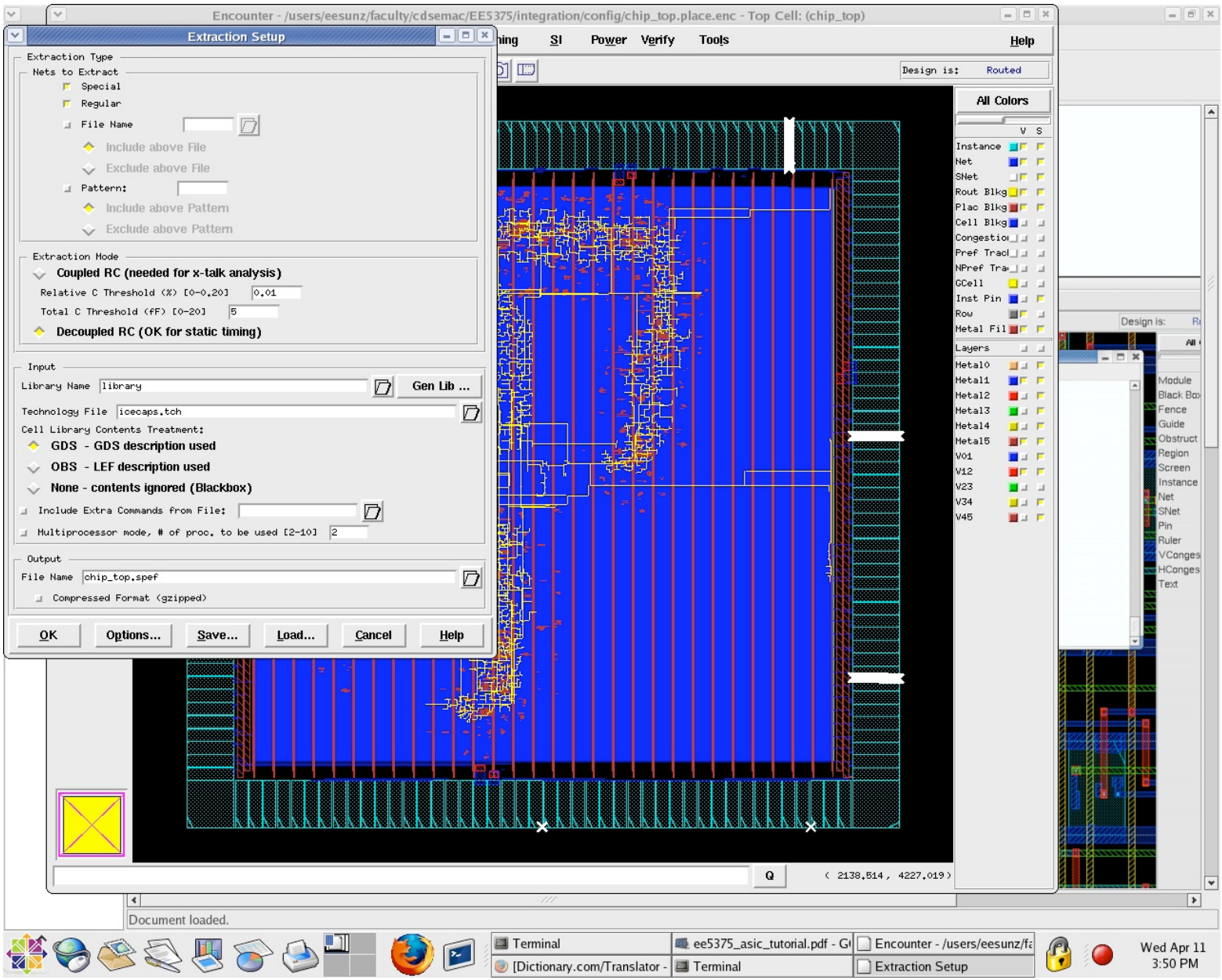
Solution? Spread wires when possible and shield important nets like clocks and asynchronous resets.


Encounter - /users/eesunz/drmacdonald/version1/integration/chingon/tutorial_run - Top Cell: (chip_top)
Design
FlipChip
Partition
Floorplan
Place
Clock
Route
Timing
SI
Power
Verify
Tools
Design is:
Tools
Views
Module
Fence
Guide
Region
Screen
Net
SNet
Pin
Ruler
Text
Q
(3172.574, 958.985)
Terminal


Encounter - /users/eesunz/faculty/cdsemac/EE5375/integration/config/chip_top.place.enc - Top Cell: (chip_top)
Design FlipChip Partition Floorplan Place Clock Route Timing SI Power Verify Tools Help
Design is: Routed
Tools
Views
All Colors
V S
Instance
Net
SNet
Rout Blkg
Plac Blkg
Cell Blkg
Congestio
Pref Trac
NPref Tra
GCell
Inst Pin
Row
Metal Fil
Layers
Metal0
Metal1
Metal2
Metal3
Metal4
Metal5
V01
V12
V23
V34
V45
Inst: des3_u1_L11_reg_21
Q
1(3687.172, 3919.848)



addFiller puts continuity blocks in the circuit rows.



Extract RCs and run timing with physical information.
Setup and holds / best case and worst case corners.