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 College of Engineering  
 Department of Electrical Engineering  
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6:30-8:00pm

## EECS 141: FALL 2010—MIDTERM 2

For all problems, you can assume that all transistors have a channel length of 100nm and the following parameters (unless otherwise mentioned):

**NMOS:**

$$V_{Tn} = 0.3V, \mu_n = 400 \text{ cm}^2/(V \cdot s), C_{oxn} = 1 \text{ } \mu\text{F}/\text{cm}^2, v_{sat} = 1e7 \text{ cm/s}, \lambda = 0$$

**PMOS:**

$$|V_{Tp}| = 0.3V, \mu_p = 200 \text{ cm}^2/(V \cdot s), C_{oxp} = 0.75 \text{ } \mu\text{F}/\text{cm}^2, v_{sat} = 1e7 \text{ cm/s}, \lambda = 0$$

<b>NAME</b>	Last <i>Solutions</i> First
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<b>GRAD/UNDERGRAD</b>	
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**Problem 1:** \_\_\_\_ / 24

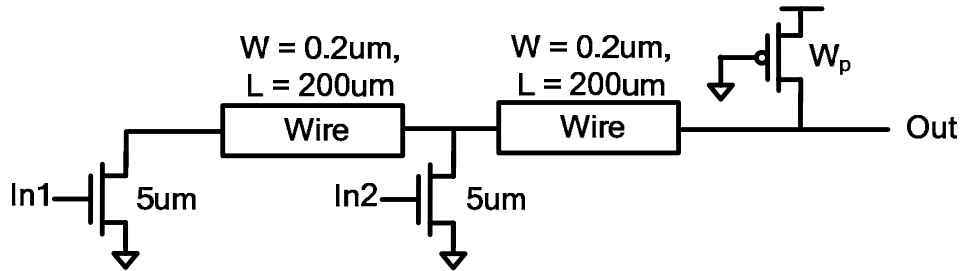
**Problem 2:** \_\_\_\_ / 18

**Problem 3:** \_\_\_\_ / 24

**Total:** \_\_\_\_ / 66

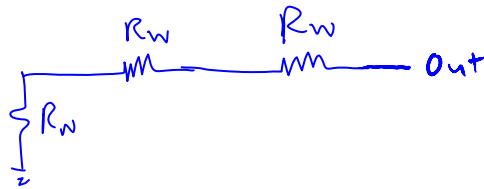
**PROBLEM 1. (24 pts) Wires, Delay, and Ratioed Logic**

For this problem, you should assume that all of the transistors are minimum channel length ( $L=0.1\mu\text{m}$ ) and have the following characteristics:  $C_G = C_D = 2\text{fF}/\mu\text{m}$  and  $R_{sqn} = R_{sqp}/2 = 10\text{k}\Omega/\square$ . For the wires, you should assume that  $C_{wpp} = 0.05\text{fF}/\mu\text{m}^2$ ,  $C_{wfringe} = 0.075\text{fF}/\mu\text{m}/\text{edge}$ , and  $R_{sqw} = 0.1\Omega/\square$



- a) (6 pts) For the circuit shown above, size the PMOS pull-up transistor (i.e., choose  $W_p$ ) so that the pull-up resistance of the gate is equal to 4 times the worst-case pull-down resistance.

Pull-down  $R$ :



$$R_w = R_{sqn} \cdot \frac{L}{W} = 10\text{k}\Omega/\square \cdot \frac{0.1\mu\text{m}}{5\mu\text{m}} = 200\Omega$$

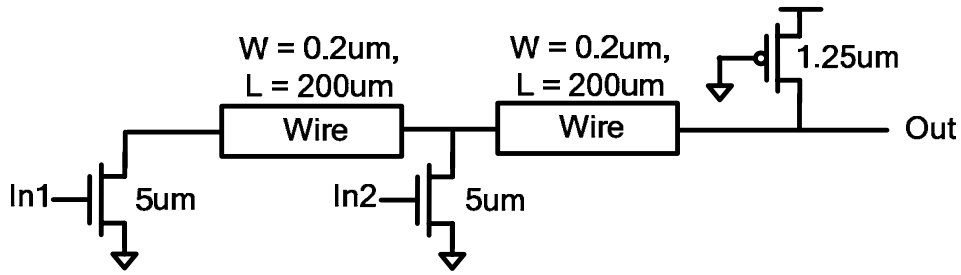
$$R_w = R_{sqw} \cdot \frac{L}{W} = 0.1\Omega/\square \cdot \frac{200\mu\text{m}}{0.2\mu\text{m}} = 100\Omega$$

$$R_{pd} = R_w + 2R_w = 400\Omega$$

$$R_{pu} = 4R_{pd} = 1.6\text{k}\Omega$$

$$\hookrightarrow 1.6\text{k}\Omega = R_{sqp} \cdot \frac{L}{W}$$

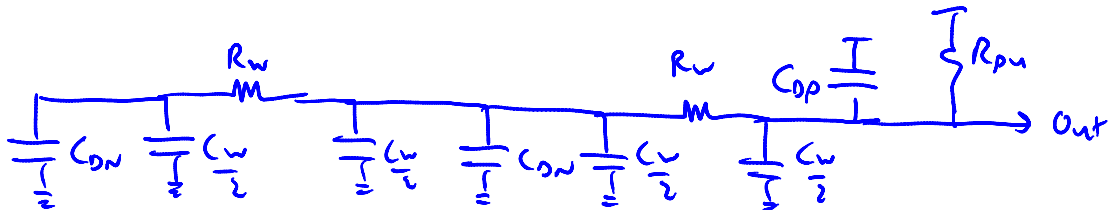
$$W = 1.25\mu\text{m}$$



- b) (10 pts) Assuming that you found that  $W_p = 1.25\mu\text{m}$  in order for the pull-up resistance to be 4 times larger than the worst-case pull-down resistance (as shown above – note that this may or may not be the right answer to part a) ), what is the worst-case ramp delay of the circuit?

Since we've sized  $R_{pu}$  to be  $4R_{pd}$ , worst case delay will actually be on output rising transition (even despite drive fight).

RC model:



$$R_{pu} = 1.6\text{k}\Omega$$

$$C_{op} = 2\text{fF}/\mu\text{m} \cdot 1.25\mu\text{m} = 2.5\text{fF}$$

$$C_{on} = 2\text{fF}/\mu\text{m} \cdot 5\mu\text{m} = 10\text{fF}$$

$$R_w = 100\Omega$$

$$C_w = W \cdot L \cdot C_{pp} + 2L \cdot C_{fr}$$

$$= 0.2\mu\text{m} \cdot 200\mu\text{m} \cdot 0.05\text{fF}/\mu\text{m}^2 +$$

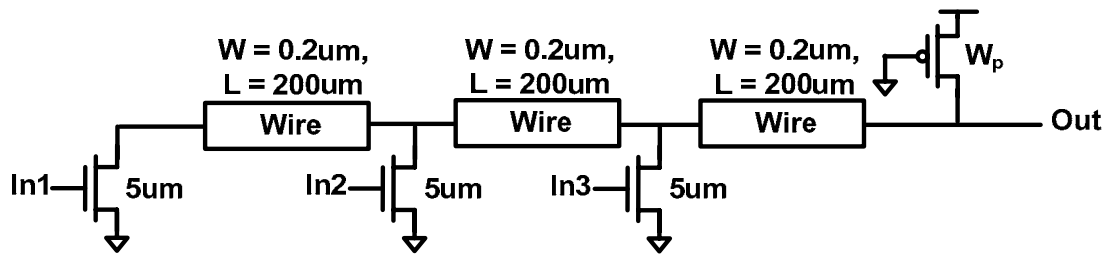
$$2 \cdot 200\mu\text{m} \cdot 0.075\text{fF}/\mu\text{m}$$

$$= 32\text{fF}$$

$$t_p = R_{pu} \cdot (C_{op} + 2C_{on} + 2C_w)$$

$$= 1.6\text{k}\Omega (2.5\text{fF} + 20\text{fF} + 64\text{fF})$$

$$t_p = 138.4\text{ps}$$



- c) (8 pts) Assuming that every time you add another input to the circuit an additional 200 μm of wire is added as well (as shown above for 3 inputs), and that the pull-up transistor is always resized to make its resistance 4 times that of the worst-case pull-down resistance, what is the worst-case ramp delay of the circuit as a function of the number of inputs ( $N_{in}$ )?

Based on previous result:  $t_p = R_{pu} \cdot C_{op} + R_{pu} \cdot N_{in} (C_{ov} + C_w)$

$R_{pu} \cdot C_{op}$  is fixed and equal to  $20k\Omega \cdot 0.1\mu m \cdot 2ff/\mu m = 4ps$

So we just need to work on the second term.

$$R_{pu} = 4 R_{pd}$$

$$R_{pd} = R_N + N_{in} \cdot R_w$$

$$= 200\Omega + N_{in} \cdot 100\Omega$$

$$\rightarrow R_{pu} = 400\Omega (2 + N_{in})$$

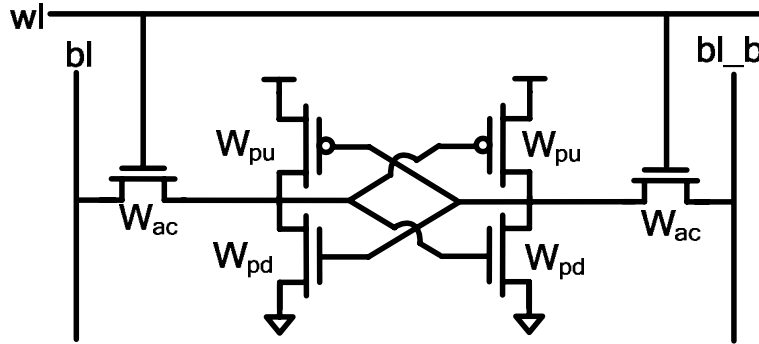
$$R_{pu} \cdot N_{in} (C_{ov} + C_w) = 400\Omega (2 + N_{in}) \cdot N_{in} \cdot (10ff + 32ff)$$

$$= 16.8ps (2 + N_{in}) \cdot N_{in}$$

$$t_p = 4ps + 16.8ps N_{in} (N_{in} + 2)$$

**PROBLEM 2. (18 pts) Scaling and SRAM Design**

Unless otherwise specified, you should assume that  $V_{DD} = 1.2V$  and use the velocity saturated model (with the parameters provided on the first page of the exam) throughout this problem.



- a) (6 pts) Assuming that the  $I_{DSAT}$  of the access transistor must be 1.5 times the  $I_{DSAT}$  of the pull-up transistor (i.e.,  $I_{DSAT\_ac} = 1.5 \cdot I_{DSAT\_pu}$ ) in order to ensure sufficient write margin, what should  $W_{pu}/W_{ac}$  be in our 100nm technology?

$$W_{ac} v_{sat,n} C_{oxn} \frac{(V_{DD} - V_{TN})^2}{V_{DD} - V_{TN} + E_{cn}L} = 1.5 W_{pu} v_{sat,p} C_{oxp} \frac{(V_{DD} - V_{TP})^2}{V_{DD} - V_{TP} + E_{cp}L}$$

$$v_{sat,n} = v_{sat,p}, V_{TN} = V_{TP}$$

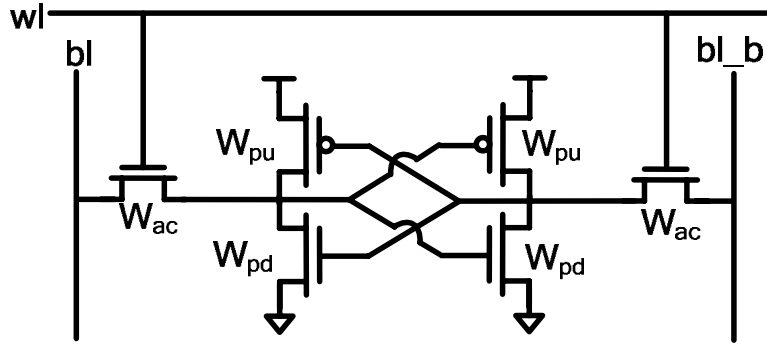
$$\frac{1}{1.5} \cdot \frac{C_{oxn}}{C_{oxp}} \cdot \frac{V_{DD} - V_T + E_{cp}L}{V_{DD} - V_T + E_{cn}L} = \frac{W_{pu}}{W_{ac}}$$

$$E_{cn}L = \frac{2v_{sat}}{\mu_n} \cdot L = 0.5V$$

$$E_{cp}L = E_{cn}L \cdot \frac{\mu_p}{\mu_n} \geq 1V$$

$$\frac{W_{pu}}{W_{ac}} = \frac{1}{1.5} \cdot \frac{1 \mu F/cm^2}{0.75 \mu F/cm^2} \cdot \frac{1.2V - 0.3V + 1V}{1.2V - 0.3V + 0.5V}$$

$$\boxed{\frac{W_{pu}}{W_{ac}} \approx 1.21}$$



- b) (8 pts) If we scale to a 50nm technology with fixed voltage scaling (i.e.,  $V_{DD}$  and  $V_{TH}$  fixed), recalculate the  $W_{ac}/W_{pu}$  required to maintain the same write margin as part a).

$V_{DD}, V_T$  fixed

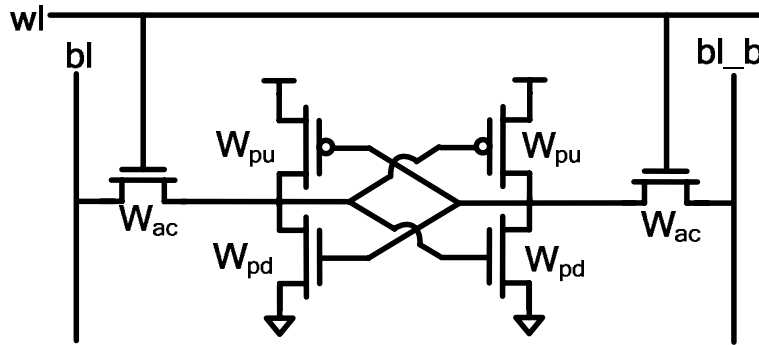
$\frac{C_{nw}}{C_{wp}}$  also fixed

$$\epsilon_{nw} L_{i,new} = \epsilon_{nw} L_{i,old} \cdot \frac{L_{new}}{L_{old}} = 0.25V$$

$$\epsilon_{wp} L_{i,new} = 0.5V$$

$$\frac{W_{pu}}{W_{ac}} = \frac{1}{1.5} \cdot \frac{1}{0.75} \cdot \frac{0.9V + 0.5V}{0.9V + 0.25V}$$

$$\frac{W_{pu}}{W_{ac}} \approx 1.08$$



- c) (4 pts) Given your answer to part b) and assuming that  $W_{pd}/W_{ac}$  is set to 1.5 independent of technology and that the area of the SRAM cell is set by  $W_{ac} \cdot L + W_{pu} \cdot L + W_{pd} \cdot L$ , how many times reduction in area is achieved by scaling the SRAM cell from the 100nm technology to the 50nm technology?

$$Area_{old} = (1 + 1.21 + 1.5) \cdot W_{ac,100nm} \cdot L_{100nm}$$

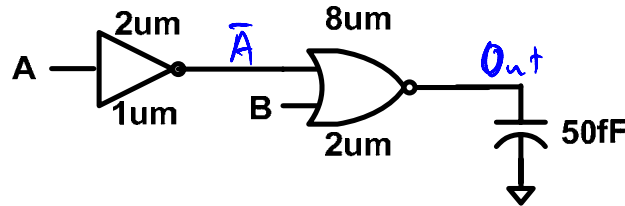
$$Area_{new} = (1 + 1.08 + 1.5) \cdot W_{ac,50nm} \cdot L_{50nm}$$

$$\frac{Area_{old}}{Area_{new}} = \frac{1 + 1.21 + 1.5}{1 + 1.08 + 1.5} \cdot \left(\frac{100nm}{50nm}\right)^2$$

$$\frac{Area_{old}}{Area_{new}} \approx 4.15$$

**PROBLEM 3. Power Consumption (24 points)**

This problem will deal with the circuit shown below. Unless otherwise specified, throughout this problem you can assume that  $V_{DD} = 1.2V$ ,  $V_{THN} = |V_{THP}| = 0.3V$ ,  $C_D = 0$ ,  $C_G = 2fF/\mu m$ , and  $R_{sqn} = 2 \cdot R_{sqp}$ . You can also assume that leakage current is modeled by  $(W/L)I_0 e^{(-V_{TH}/38mV)}$ , where  $I_{0,NMOS} = 10\mu A$  and  $I_{0,PMOS} = 5\mu A$ .



- a) (8 pts) Assuming that the A input is high half of the time, the B input is high 1/8 of the time, and that the circuit runs at a clock frequency of 400MHz, how dynamic much power is consumed by the circuit shown above? Don't forget to include the power consumed by driving the A and B inputs.

A input:  $P(A=1) = 1/2$ , so  $\alpha_{0 \rightarrow 1, A} = 1/4$

$C_{sw, A} = 1/4 \cdot 2fF/\mu m \cdot 3\mu m = 1.5fF$

Inverter doesn't modify activity factor, so  $\alpha_{0 \rightarrow 1, \bar{A}} = 1/4$

$C_{sw, \bar{A}} = 1/4 \cdot 2fF/\mu m \cdot 10\mu m = 5fF$

B input:  $P(B=1) = 1/8$ , so  $\alpha_{0 \rightarrow 1, B} = 1/8 \cdot 7/8 = 7/64$

$C_{sw, B} = 7/64 \cdot 2fF/\mu m \cdot 10\mu m = 2.1875fF$

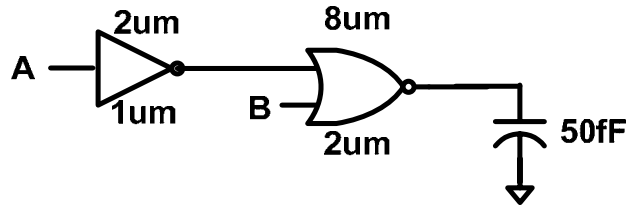
Out:  $P(out=1) = P(\bar{A}=0) \cdot P(B=0) = 1/2 \cdot 7/8 = 7/16$        $\alpha_{0 \rightarrow 1, out} = \frac{7}{16} \cdot \frac{9}{16} = \frac{63}{256}$

$C_{sw, out} = 63/256 \cdot 50fF \approx 12.305fF$

$P_{dynamic} \approx C_{sw, total} \cdot V_{DD}^2 \cdot f$

$P_{dynamic} \approx 12.1\mu W$





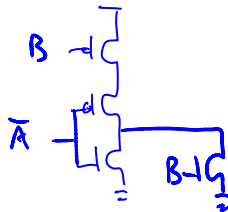
b) (8 pts) Under the same conditions as part a), how much leakage power does the circuit consume?

Inverter:  $\frac{I_{D,N}}{I_{D,P}} = \frac{W_P}{W_N}$ , so leakage independent of state

$$I_{lk,inv} = \frac{1\mu\text{m}}{0.1\mu\text{m}} \cdot 10\mu\text{A} \cdot e^{-300\text{mV}/38\text{mV}} = 37.27\text{ nA}$$

$$P_{lk,inv} = V_{DD} \cdot I_{lk,inv} \approx 44.72\text{ nW}$$

NOR gate:



$$\text{If } \bar{A}=0, B=0: (P(\bar{A}=0) \cdot P(B=0) = \frac{7}{16})$$

$$I_{lk,00} = 2 \cdot \frac{2\mu\text{m}}{0.1\mu\text{m}} \cdot 10\mu\text{A} \cdot e^{-300\text{mV}/38\text{mV}} \approx 149.1\text{ nA}$$

$$\text{If } \bar{A}=1, B=1 (P(\bar{A}=1) \cdot P(B=1) = \frac{1}{16})$$

$$I_{lk,11} = \frac{8\mu\text{m}}{2 \cdot 0.1\mu\text{m}} \cdot 5\mu\text{A} \cdot e^{-300\text{mV}/38\text{mV}} \approx 74.5\text{ nA}$$

$$\bar{A}=1, B=0 \text{ or } \bar{A}=0, B=1 (P = 1/2):$$

$$I_{lk,10} = \frac{8\mu\text{m}}{0.1\mu\text{m}} \cdot 5\mu\text{A} \cdot e^{-300\text{mV}/38\text{mV}} \approx 149.1\text{ nA}$$

$$P_{leak,nor} = V_{DD} \cdot \left( \frac{7}{16} I_{lk,00} + \frac{1}{16} I_{lk,11} + \frac{1}{2} I_{lk,10} \right)$$

$$P_{leak,nor} \approx 173.3\text{ nW}$$

$$P_{leak,tot} \approx 218\text{ nW}$$

- c) (8 pts) Given your answers to parts a) and b), if you could change both the  $V_{DD}$  and  $V_{TH}$  of the transistors in the circuit (but not any of the sizes), how would you change them in order to achieve lower total power consumption without increasing the delay? You do not need to provide any numerical answers – just an explanation of how you would change  $V_{DD}$  and  $V_{TH}$ , and why you would change them that particular way. However, the more specific your answer, the more credit you will receive. (Hint: You can use the  $V_T^*$  model to guide your answer when thinking about delay.)

Leakage is almost 100x smaller than dynamic power with current choice of  $V_{DD}$  and  $V_{TH}$ . This implies that if we were to reduce  $V_{TH}$  and  $V_{DD}$  at the same time so that  $t_{pd} \frac{V_{DD}}{I_{OSAT}} \propto \frac{V_{DD}}{V_{DD} - V_T^*}$  is constant, we can keep delay fixed and decrease total power because of the reduction in  $C V_{DD}^2 f$ .

For example, if we were to reduce  $V_{th}$  by 100mV (increasing the leakage power by a little bit more than 10x), we could reduce  $V_{DD}$  to: ( $V_T^* = V_{TH} + E_{CL}/4 = 425mV$ )

$$\frac{V_{DD,new}}{V_{DD,new} - 0.325V} = \frac{1.2V}{1.2V - 0.425V}$$

$$V_{DD,new} \approx 918mV$$

Therefore:

$$P_{dyn,new} = \left(\frac{0.918}{1.2}\right)^2 \cdot 12.1\mu W \approx 7.08\mu W$$

$$P_{lk,new} = \left(e^{-200mV/38mV} / e^{-300mV/38mV}\right) \cdot \left(\frac{0.918}{1.2}\right) \cdot 218\mu W \approx 2.32\mu W$$

$$P_{tot,new} \approx 9.4\mu W \quad (P_{tot,old} \approx 12.3\mu W)$$