EECS 247

Analog-Digital Interface Integrated Circuits

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Lecture 1: Introduction

Instructor's Technical Background

- Ph.D., EECS department -UC Berkeley 1985, advisor Prof. P.R. Gray
  - Thesis topic: Continuous-time CMOS high-frequency filters
- Industrial background
  - 11 years at ATT & Bell Laboratories, N.J., in the R&D area as a circuit designer
    - Circuits for wireline communications: CODECs, ISDN, and DSL including ADCs (nyquist rate & over-sampled), DACs, filters, VCOs
    - Circuits intended for wireless applications
    - Fiber-optics circuits
  - 3 years at Philips Semiconductors, Sunnyvale, CA
    - Managed a group in the RF IC department- developed ICs for CDMA & analog cell phones
  - 3 years @ Broadcom Corp. – Director of Analog/RF ICs in San Jose, CA.
    - Projects: Gigabit-Ethernet, TV tuners, and DSL circuitry
  - Currently consultant for IC design
- Teaching experience
  - Has taught/co-taught EE247 @ UCB since 2003
  - Instructor for short courses offered by MEAD Electronics
  - Adjunct Prof. @ Rutgers Univ., N.J. : Taught a graduate level IC course

Administrative Issues

- Course web page: http://inst.eecs.berkeley.edu/~EE247/fa09
  - Course notes will be uploaded on the course website prior to each class
  - Homeworks & due dates are posted on the course website
  - Announcements regarding the course will be posted on the home page, please visit course website often

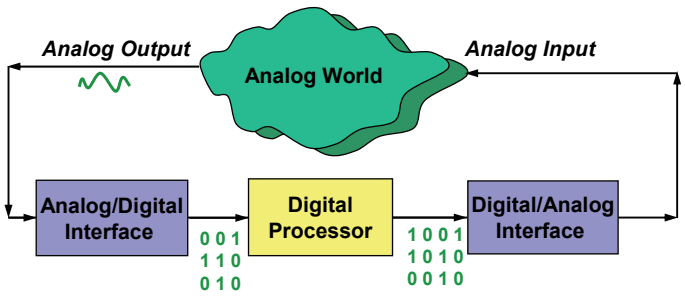
Office Hours & Grading

- Office hours:
  - Tues./Thurs. 4 to 5pm @ 567 Cory Hall (unless otherwise announced in the class)
  - Extra office hours by appointment
  - Feel free to discuss issues via email: haidehk@eecs.berkeley.edu
- Course grading:
  - Homework/project 50%
  - Midterm 20% (tentative date: Oct. 27)
  - Final 30%

Prerequisites & CAD Tools

- Prerequisites
  - Basic course in signal processing (Laplace and z-transform, discrete Fourier transform) i.e. EE120
  - Fundamental circuit concepts i.e. EE105 and EE140
- CAD Tools:
  - Hspice or Spectre
  - Matlab

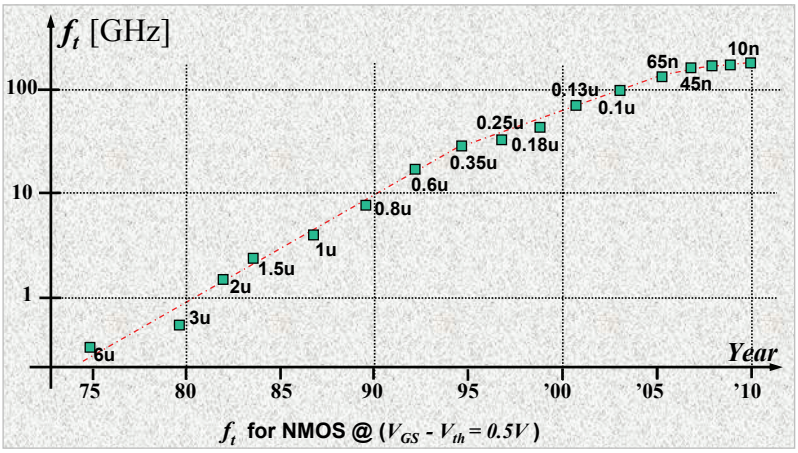
Analog-Digital Interface Circuitry



- Naturally occurring signals are analog
- To process signals in the digital domain
  ∴ Need Analog/Digital & Digital/Analog interface circuitry

Question: Why not perform the signal processing in the analog domain only & thus eliminate need for A/D & D/A?

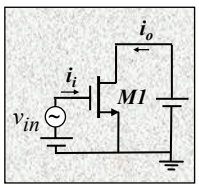
CMOS Technology Evolution versus Time

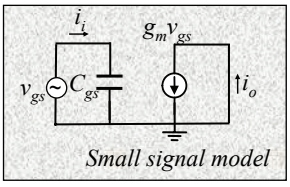


*Ref: Paul R. Gray UCB EE290 course '95
International Technology Roadmap for Semiconductors, http://public.itrs.net

What is f_t?

- f_t → transition frequency
- Freq. where short-circuit common-source current gain $A_I \sim 1$
- For a given technology single device f_t with minimum channel length is a measure of max. achievable ckt speed





$$\frac{i_o}{i_i} = \frac{g_m}{sC_{gs}}$$

$$\frac{i_o}{i_i} = 1 \rightarrow 2\pi f_t = \frac{g_m}{C_{gs}}$$

Substituting for g_m and C_{gs}:

$$f_t = 1.5\frac{\mu_n (V_{GS} - V_t)}{2\pi L^2}$$

where L is channel length

CMOS Device Evolution
Progression from 1975 to 2005

- Minimum feature sizes ~X1/100
- Cut-off frequency f_t ~X300
- Minimum size device area ~$1/L^2$
- Number of interconnect layers ~X8

❖Note: Moore's Law→ # of transistors per sq-inch increases x2 every 18months

Impact of CMOS Scaling on Digital Signal Processing

Direct beneficiary of VLSI technology down scaling

- Digital circuits deal with "0" & "1" signal levels only → Not sensitive to "analog" noise
- Si Area/function reduced drastically due to
  - Shrinking of feature sizes
  - Increase in # of metal levels for interconnections (currently >8 metal level v.s. only 1 in the 1970s)
- Enhanced functionality & flexibility
- Amenable to automated design & test
- "Arbitrary" precision
- Provides inexpensive storage capability

Analog Signal Processing Characteristics

- Sensitive to "analog" noise
- Has not fully benefited from technology down scaling:
  - Supply voltages scale down accordingly
    → Reduced voltage swings → more challenging analog design
  - Reduced voltage swings requires lowering of the circuit noise to keep a constant dynamic range
    → Higher power dissipation and chip area
- Not amenable to automated design
- Extra precision comes at a high price
- Rapid progress in DSP has imposed higher demands on analog/digital interface circuitry
  →Plenty of room for innovations!

Cost/Function Comparison DSP & Analog

- Digital circuitry: Fully benefited from CMOS device scaling
  - Cost/function decreases by ~29% each year
    - Cost/function X1/30 in 10 years*
- Analog circuitry: Not fully benefited from CMOS scaling
  - Device scaling mandates drop in supply voltages→ threaten analog feasibility
    - Cost/function for analog ckt almost constant or increase

➢ Rapid shift of function implementation from processing in analog domain to digital & hence increased need for A/D & D/A interface circuitry

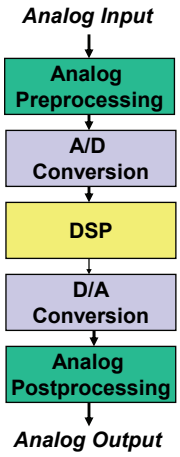
*Ref: International Technology Roadmap for Semiconductors, http://public.itrs.net

Digitally Assisted Analog Circuitry

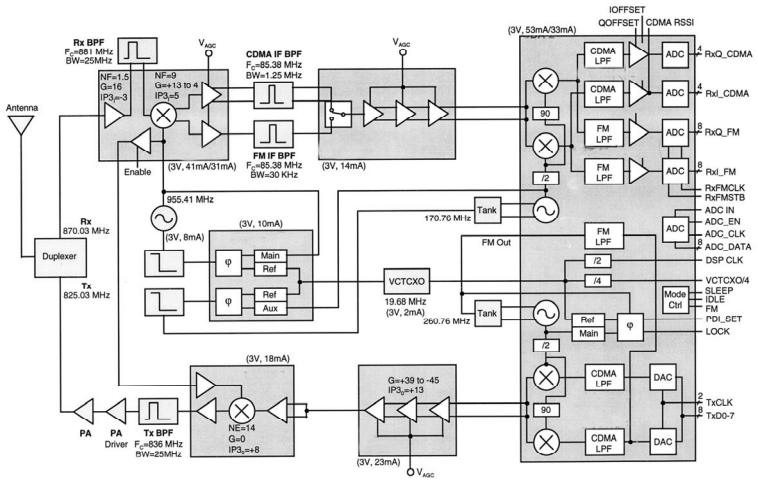
- Analog design has indeed benefited from the availability of inexpensive on-chip digital capabilities
- Examples:
  - Compensating/calibrating ADC & DAC inaccuracies
  - Automatic frequency tuning of filters & VCOs
  - DC offset compensation

Analog Digital Interface Circuitry Example: Digital Audio

- Goal-Lossless archival and transmission of audio signals
- Circuit functions:
  - Preprocessing
    - Amplification
    - Anti-alias filtering
  - A/D Conversion
    - Resolution→16Bits
  - DSP
    - Storage
    - Processing (e.g. recognition)
  - D/A Conversion
  - Postprocessing
    - Smoothing filter
    - Variable gain amplification



Example: Dual Mode CDMA (IS95)& Analog Cellular Phone RF & Baseband



Example: Typical Dual Mode Cell Phone

Contains in integrated form the following interface circuitry:

- 4 RX filters
- 3 or 4 TX filters
- 4 RX ADCs
- 2 TX DACs

Dual Standard, I/Q

- 3 Auxiliary ADCs
- 8 Auxiliary DACs

Audio, Tx/Rx power control, Battery charge control, display, ...

Total: Filters → 8

ADCs → 7

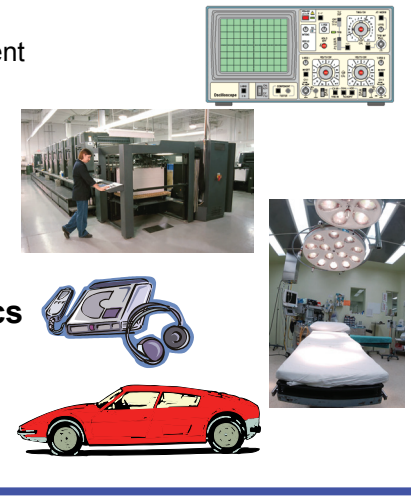
DACs → 12

Areas Utilizing Analog/Digital Interface Circuitry

- **Communications**
  - Wireline communications
    - Telephone related (DSL, ISDN, CODEC)
    - Television circuitry (Cable modems, TV tuners…)
    - Ethernet (Gigabit, 10/100BaseT…)
  - Wireless
    - Cellular telephone (CDMA, Analog, GSM….)
    - Wireless LAN (Blue tooth, 802.11a/b/g…..)
    - Radio (analog & digital), Television
    - Personal Data Assistants
- **Computing & Control**
  - Storage media (disk drives, digital tape)
  - Imagers & displays

Areas Utilizing Analog/Digital Interface Circuitry

- **Instrumentation**
  - Electronic test equipment & manufacturing environment ATEs
  - Semiconductor test equipment
  - Physical sensors & actuators
  - Medical equipment
- **Consumer Electronics**
  - Audio (CD, DAT, MP3)
  - Automotive control, appliances, toys



UCB Graduate Level Analog Courses
EECS 247 - 240 - 242

- EECS 240
  - Transistor level, building blocks such as opamps, buffers, comparator….
  - Device and circuit fundamentals
  - CAD Tools → SPICE
- EECS 247
  - Filters, ADCs, DACs, some system level
  - Signal processing fundamentals
  - Macro-models, large systems, some transistor level, constraints such as finite gain, supply voltage, noise, dynamic range considered
  - CAD Tools → Matlab, SPICE
- EECS 242
  - RF amplification, mixing
  - Oscillators
  - Exotic technology devices
  - Nonlinear circuits

Material Covered in EE247

- Filters
  - Continuous-time filters
    - Biquads & ladder type filters
    - Opamp-RC, Opamp-MOSFET-C, gm-C filters
    - Automatic frequency tuning techniques
  - Switched capacitor (SC) filters
- Data Converters
  - D/A converter architectures
  - A/D converter
    - Nyquist rate ADC- Flash, Pipeline ADCs,….
    - Self-calibration techniques
    - Oversampled converters
- Systems utilizing analog/digital interfaces
  - Wireline communication systems- ISDN, XDSL…

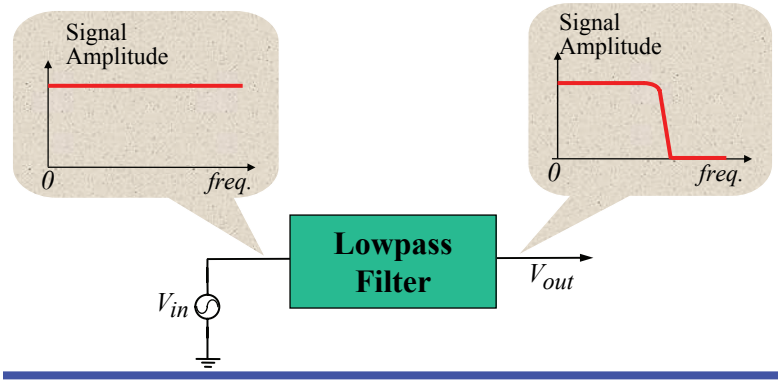
Books (on reserve @ Eng. Library)
(NOT required to be purchased)

- Filters
  - A. Williams and F. Taylor, *Electronic Filter Design Handbook*, 3rd edition, McGraw-Hill, 1995.
  - W. Heinlein & W. Holmes, "Active Filters for Integrated Circuits", Prentice Hall Int., Inc. Chap. 8, 1974. Good reference for signal flowgraph techniques
  - A. Zverev, *Handbook of Filter Synthesis*, Wiley, 1967. A classic; focus is on passive ladder filters. Tables for implementing ladder filters (replaces a CAD tool).
- Data Converters
  - R. van de Plassche, *Integrated Analog-to-Digital and Digital-to-Analog Converters,* 2nd edition, Kluwer, 2003.
  - B. Razavi, *Data Conversion System Design,* IEEE Press, 1995.
  - S. Norsworthy et al (eds), *Delta-Sigma Data Converters,* IEEE Press, 1997.
- General
  - Gray, Hurst, Lewis, Meyer, *Analysis & Design of Analog Integrated Circuits*, Wiley 2001.
  - Johns, Martin, *Analog Integrated Circuit Design*, Wiley 1997.

❖ Note: a list of relevant IEEE publications is posted on the course website. Some will be noted as mandatory reading and the rest optional

Introduction to Filters

- Filtering → Provide frequency selectivity and/or phase shaping
  - Oldest & most common type of signal processing

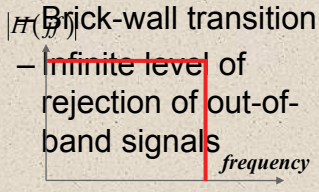


Introduction to Filters

- Typical filter applications:
  - Extraction of desired signal from many (radio, TV, cell phone, ADSL…..)
  - Separating signal and noise
  - Anti-aliasing
  - Phase equalization
  - Amplifier bandwidth limitations

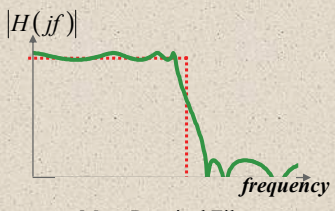
Ideal versus Practical Filters
Example: Lowpass Filter

- Ideal filter
  - Flat magnitude response in the passband
  - Brick-wall transition
  - Infinite level of rejection of out-of-band signals



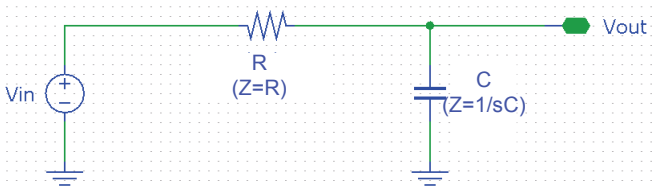
Ideal Lowpass Brick-Wall Filter

- Practical filter
  - Ripple in passband magnitude response
  - Limited rejection of out-of-band signals



More Practical Filter

Simplest Filter
First-Order Lowpass RC Filter



Steady-state frequency response:

$$H(s)=\frac{V_{out}(s)}{V_{in}(s)}=\frac{1/sC}{R+1/sC}=\frac{1}{1+RCs}$$

$$with \quad \omega_o=\frac{1}{RC} \quad \rightarrow \quad H(s)=\frac{1}{1+\frac{s}{\omega_o}}$$

S-Plane Poles and Zeros

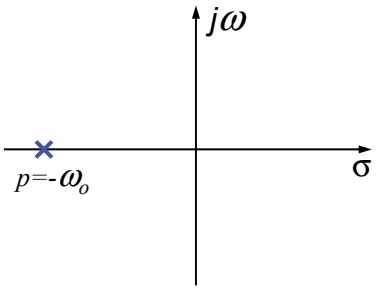
$$H(s)=\frac{1}{1+\frac{s}{\omega_o}}$$

Pole: $p=-\omega_o$

Zero: $z \rightarrow \infty$

$$|H(s)|=\left|\frac{1}{1+j\frac{\omega}{\omega_o}}\right|=\frac{1}{\sqrt{1+\frac{\omega^2}{\omega_o^2}}}$$

s-plane (pzmap):



Magnitude Response Characteristics

Typically magnitude response is plotted in terms of decibel:

$$20\log\left[\left|H(s)\right|\right] = 20\log\frac{1}{\sqrt{1+\frac{\omega^2}{\omega_o^2}}} = -10\log\left(1+\frac{\omega^2}{\omega_o^2}\right)$$

$$\omega = \omega_o \rightarrow 20\log\left[\left|H(s)\right|\right] = -3dB$$

The frequency where magnitude response changes by $3dB$ is typically called corner or cut-off frequency

Simplest Filter
First-Order Lowpass RC Filter Example

Steady-state frequency response:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{1+\frac{s}{\omega_o}}$$

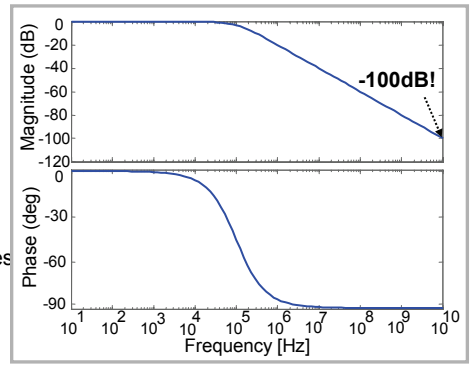
$$with \qquad \omega_o = \frac{1}{RC} = 2\pi \times \underline{100kHz}$$

Filter Frequency Response
Bode Plot

$$\left|H(s=j\omega)\right|_{\omega=0}=1$$

$$\left|H(s=j\omega)\right|_{\omega=\omega_0}=1/\sqrt{2}$$

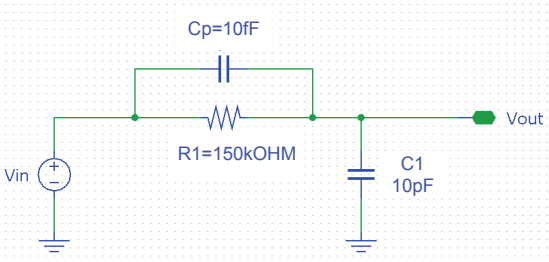
$$\left|H(s=j\omega)\right|_{\omega\to\infty}=0$$



Asymptotes:
- 20dB/dec magnitude rolloff
- 90degrees phase shift per 2 decades

Question:
can we really get 100dB attenuation at 10GHz?

First-Order Low-Pass RC Filter
Including Parasitics



$$H(s)=\frac{1+sRC_P}{1+sR(C+C_P)}$$

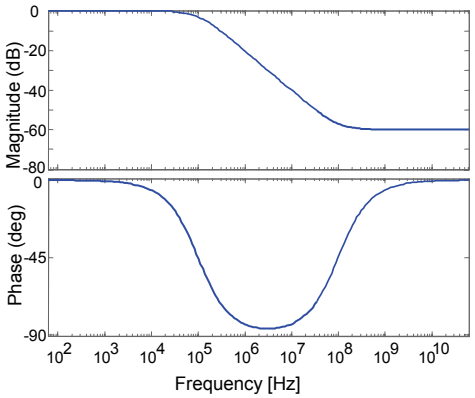
$$\text{Pole}: \quad p=-\frac{1}{R(C+C_P)}\approx-\frac{1}{RC}$$

$$\text{Zero}: \quad z=-\frac{1}{RC_P}$$

Filter Frequency Response

$$|H(j\omega)|_{\omega=0} = 1$$

$$|H(j\omega)|_{\omega\to\infty} = \frac{C_P}{C+C_P} \approx \frac{C_P}{C} = 10^{-3} = -60dB$$



- Beware of important parasitics & include them in the model …

Dynamic Range & Electronic Noise

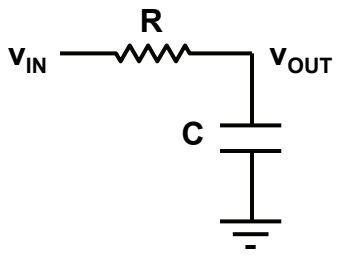
- Dynamic range is defined as the ratio of maximum possible signal handled by a circuit and the minimum useful signal
  - Maximum signal handling capability usually determined by maximum possible voltage swings which in turn is a function of supply voltage & circuit non-linearity
  - Minimum signal handling capability is normally determined by electronic noise
    - Amplifier noise due to device thermal and flicker noise
    - Resistor thermal noise
- Dynamic range in analog ckts has direct implications for power dissipation

Analog Dynamic Range
Example: First Order Lowpass Filter

- Once the poles and zeroes of the analog filter transfer function are defined then special attention must be paid to the actual implementation
- Of the infinitely many ways to build a filter with a given transfer function, **each of those combinations result in a different level of output noise!**
- As an example noise and dynamic range for the 1st order lowpass filter will be derived

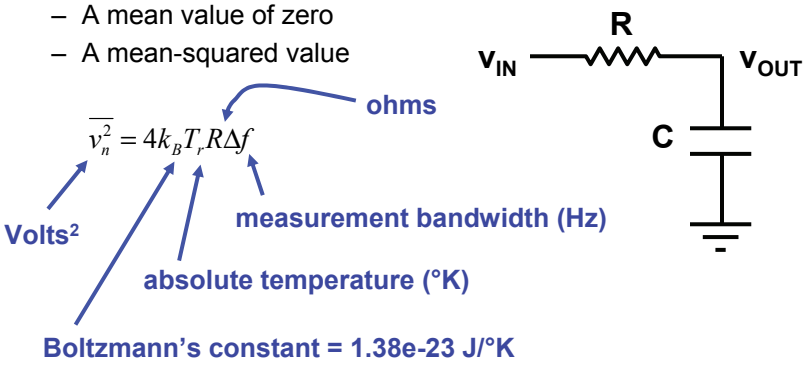
First Order Filter Noise

- Capacitors are noiseless
- Resistors have thermal noise
  - This noise is uniformly distributed in the frequency domain from dc to infinity
  - Frequency-independent noise is called "white noise"



Resistor Noise

- Resistor noise characteristics
  - A mean value of zero
  - A mean-squared value



$$\overline{v_n^2} = 4k_B T_r R \Delta f$$

ohms

Volts²

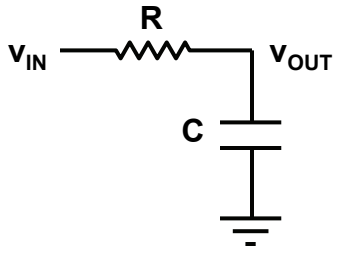
measurement bandwidth (Hz)

absolute temperature (°K)

Boltzmann's constant = 1.38e-23 J/°K

Resistor Noise

- Theoretically, resistor *rms* noise voltage in a 10Hz band centered at 1kHz is the same as resistor *rms* noise in a 10Hz band centered at 1GHz
- Resistor noise spectral density, N_0, is the *rms* noise per √Hz of bandwidth:



$$N_0 = \sqrt{\frac{\overline{v_n^2}}{\Delta f}} = \sqrt{4k_B T_r R}$$

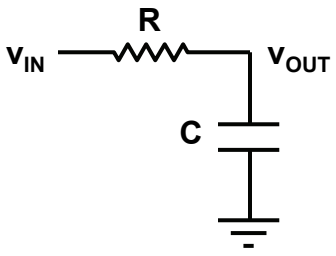
Resistor Noise

Good numbers to memorize:

- N_0 for a **1kΩ** resistor at room temperature is **4nV/√Hz**
- Scaling R,
  - A 10MΩ resistor gives 400nV/√Hz
  - A 50Ω resistor gives 0.9nV/√Hz
- Or, remember

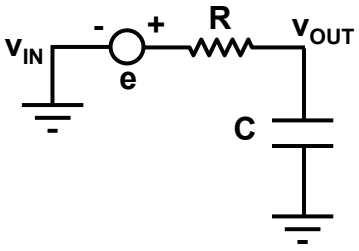
  $k_B T_r = 4 \times 10^{-21}$ J (T_r = 17 °C)
- Or, remember

  $k_B T_r / q = 26$mV ($q = 1.6 \times 10^{-19}$ C)



First Order Filter Noise

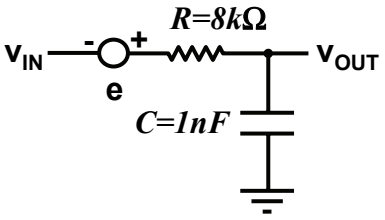
- To derive noise @ the output node:
  - Short circuit the input to ground.
  - Resistor noise gives the filter a non-zero output when v_{IN}=0
  - In this simple example, both the input signal and the resistor noise obviously have the same transfer functions to the output
  - Since noise has random phase, we can use any polarity convention for a noise source (but we have to use it consistently)



First Order Filter Noise

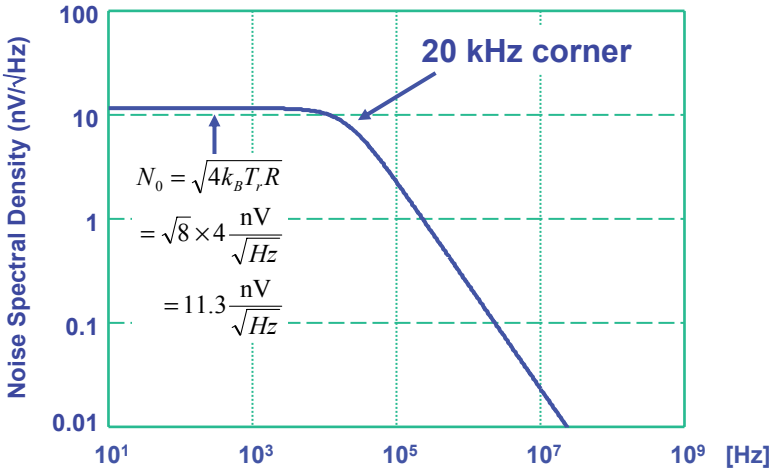
- What is the thermal noise of this RC filter?
- Let's ask SPICE!
  Netlist:

```
*Noise from RC LPF
vin vin 0 ac 1V
r1 vin vout 8kOhm
c1 vout 0 1nF
.ac dec 100 10Hz
1GHz
.noise V(vout) vin
.end
```



$$\omega_o = \frac{1}{RC} = 2\pi \times 20kHz$$

Output Noise Spectral Density



Total Noise

- Total noise is what the display on a volt-meter connected to v_o would show!
- Total noise is found by integrating the noise power spectral density within the frequency band of interest
- Note that noise is integrated in the mean-squared domain, because noise in a bandwidth df around frequency f_1 is uncorrelated with noise in a bandwidth df around frequency f_2
  - Powers of uncorrelated random variables add
  - Squared transfer functions appear in the mean-squared integral

$$\overline{v_o^2} = \int_{f_1}^{f_2} \overline{v_n^2} |H(j\omega)|^2 df$$

$$\overline{v_o^2} = \int_0^{\infty} 4k_B T R \, |H(2\pi jf)|^2 df$$

*Ref: "Analysis & Design of Analog Integrated Circuits", Gray, Hurst, Lewis, Meyer- Chapter 11

Total Noise

$$\overline{v_o^2} = \int_0^{\infty} 4k_B TR |H(2\pi jf)|^2 df$$

$$= \int_0^{\infty} 4k_B TR \left| \frac{1}{1+2\pi jfRC} \right|^2 df = 4k_B TR \int_0^{\infty} \frac{1}{1+(2\pi fRC)^2} = 4k_B TRx \frac{1}{2\pi RC} tan^{-1}(2\pi RCf) \Big|_0^{\infty}$$

$$\rightarrow \boxed{\overline{v_o^2} = \frac{k_B T}{C}}$$

- This interesting and somewhat counter intuitive result means that even though resistors are the components generating the noise, total noise is determined by noiseless capacitors!
- For a given capacitance, as resistance goes up, the increase in noise density is balanced by a decrease in noise bandwidth

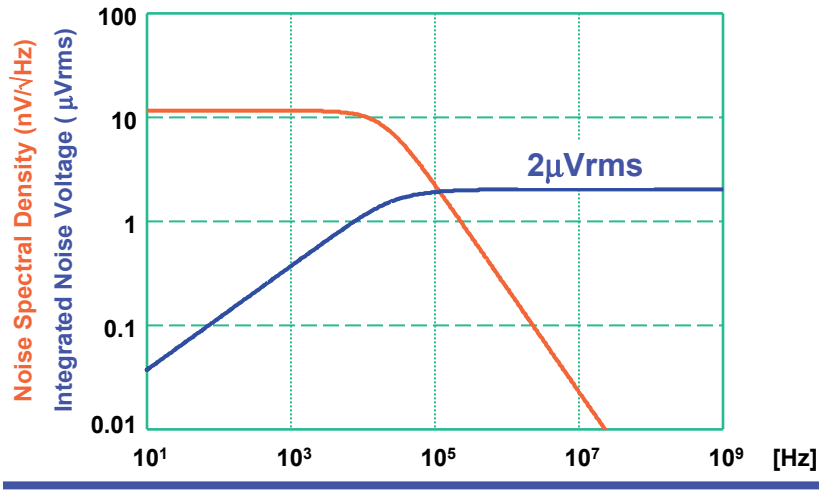
kT/C Noise

- kT/C noise is a fundamental analog circuit limitation
- The *rms* noise voltage of the simplest possible (first order) filter is $(k_B T/C)^{1/2}$
- For 1pF capacitor, $(k_B T/C)^{1/2}$ = 64 μV-rms (at 298°K)
- 1000pF gives 2 μV-rms
- The noise of a more complex & higher order filter is given by:

$$(\alpha \times k_B T/C)^{1/2}$$

where α depends on implementation and features such as filter order

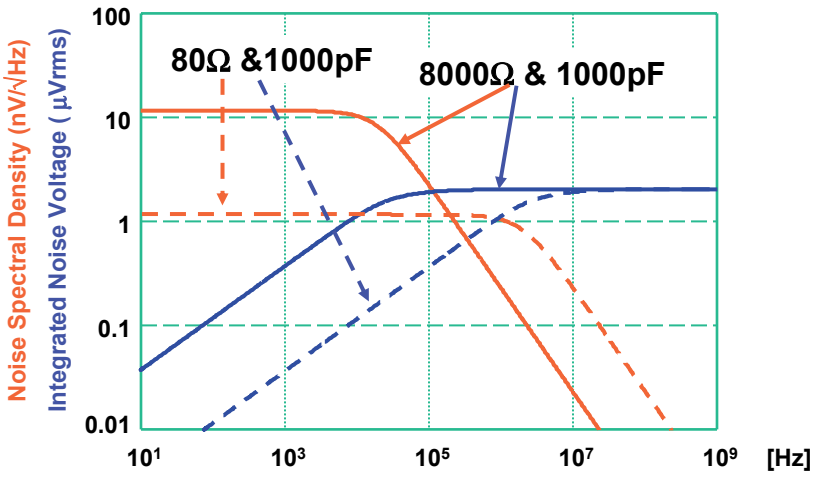
Lowpass Filter Total Output Noise



Lowpass Filter Output Noise

- Note that the integrated noise essentially stops growing above $100kHz$ for this lowpass filter with $f_{-3dB}=20kHz$
- Beware of faulty intuition which might tempt you to believe that an 80Ω, 1000pF filter has lower integrated noise compared to our 8000Ω, 1000pF filter…

Lowpass Filter Output Noise



Analog Circuit Dynamic Range

- Maximum voltage swing for analog circuits (assuming no inductors are used!) can at most be equal to power supply voltage V_{DD} (normally is smaller)
- Assuming a sinusoid signal → $V_{\max}(rms) = \frac{1}{\sqrt{2}} \frac{V_{DD}}{2}$
- Noise for a filter → $V_n(rms) = \sqrt{\alpha \frac{k_B T}{C}}$

$$D.R. = \frac{V_{\max}(rms)}{V_n(rms)} = \frac{V_{DD}\sqrt{C}}{\sqrt{8\alpha k_B T}} \qquad [\text{V/V}]$$

→ Dynamic range in dB is:

$$= 20\log_{10}\left(V_{DD}\sqrt{\frac{C}{\alpha}} \right) + 75 \qquad [\text{dB}] \text{ with C in [pF]}$$

Analog Circuit Dynamic Range

- For integrated circuits built in modern CMOS processes, ***VDD < 1.5V*** and ***C < 100pF***
  - ***D.R. < 98 dB*** *(assuming $\alpha = 1$)*
- For printed-circuit board type circuits built with "old-fashioned" ***30V*** opamps and discrete capacitors of < ***100nF***
  - ***D.R . < 140dB***
  - A ***42dB*** advantage!

Dynamic Range versus Number of Bits

- Number of bits and dynamic range in terms of dB are related:

$$D.R. = (1.76 + 6.02N)\ [\text{dB}] \qquad N \rightarrow \text{number of bits}$$

  - see "quantization noise", later in the course

- Hence

98 dB	→	***16 Bits***
140 dB	→	***23 Bits***

Dynamic Range versus Power Dissipation

- Each extra bit corresponds to 6dB extra dynamic range
- Increasing dynamic range by one bit → 6dB less noise → decrease in noise power by 4x!
- This translates into 4x larger capacitors
- To keep speed constant (speed prop G_m/C): G_m must increase 4x
- Power dissipation is proportional to G_m increases by 4x(for fixed supply and V_{dsat})

In analog circuits with performance limited by thermal noise,
1 extra bit costs 4x extra power dissipation
E.g. 16Bit ADC at 200mW → 17Bit ADC at 800mW

Do not overdesign the dynamic range of analog circuits!

Noise & Dynamic Range Summary

- Thermal noise is a fundamental property of (electronic) circuits
- In filters, noise is closely related to
  - Capacitor size
- In higher order filters, noise is a function of C, filter order, Q, and depends on implementation
- Operational amplifiers used in active filters can contribute significant levels of extra noise to overall filter noise
- Reducing noise in most analog circuits is costly in terms of power dissipation and chip area