Efficient Processing of Deep Neural Networks

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Abstract

This book provides a structured treatment of the key principles and techniques for enabling efficient processing of deep neural networks (DNNs). DNNs are currently widely used for many artificial intelligence (AI) applications, including computer vision, speech recognition, and robotics. While DNNs deliver state-of-the-art accuracy on many AI tasks, it comes at the cost of high computational complexity. Therefore, techniques that enable efficient processing of deep neural networks to improve key metrics—such as *energy-efficiency*, *throughput*, and *latency*—without sacrificing accuracy or increasing hardware costs are critical to enabling the wide deployment of DNNs in AI systems.

The book includes background on DNN processing; a description and taxonomy of hardware architectural approaches for designing DNN accelerators; key metrics for evaluating and comparing different designs; features of DNN processing that are amenable to hardware/algorithm co-design to improve energy efficiency and throughput; and opportunities for applying new technologies. Readers will find a structured introduction to the field as well as formalization and organization of key concepts from contemporary work that provide insights that may spark new ideas.

Contents

Preface

Deep neural networks (DNNs) have become extraordinarily popular; however, they come at the cost of high computational complexity. As a result, there has been tremendous interest in enabling efficient processing of DNNs. The challenge of DNN acceleration is threefold:

- to achieve high performance and efficiency,
- to provide sufficient flexibility to cater to a wide and rapidly changing range of workloads, and
- to integrate well into existing software frameworks.

In order to understand the current state of art in addressing this challenge, this book aims to provide an overview of DNNs, the various tools for understanding their behavior, and the techniques being explored to efficiently accelerate their computation. It aims to explain foundational concepts and highlight key design considerations when building hardware for processing DNNs rather than trying to cover all possible design configurations, as this is not feasible given the fast pace of the field (see Figure 1). It is targeted at researchers and practitioners who are familiar with computer architecture who are interested in how to efficiently process DNNs or how to design DNN models that can be efficiently processed. We hope that this book will provide a structured introduction to readers who are new to the field, while also formalizing and organizing key concepts to provide insights that may spark new ideas for those who are already in the field.

Organization

This book is organized into three modules that each consist of several chapters. The first module aims to provide an overall background to the field of DNN and insight on characteristics of the DNN workload.

- Chapter 1 provides background on the context of why DNNs are important, their history, and their applications.
- Chapter 2 gives an overview of the basic components of DNNs and popular DNN models currently in use. It also describes the various resources used for DNN research and development. This includes discussion of the various software frameworks, and the public datasets that are used for training and evaluation.

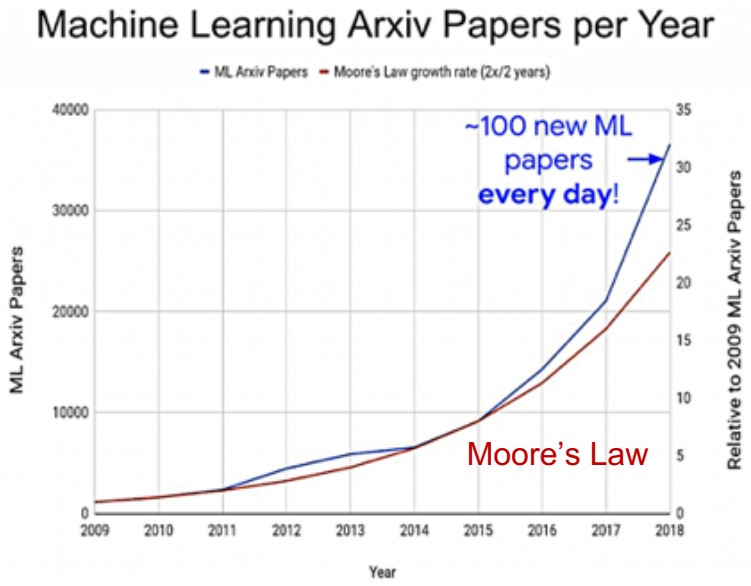

Figure 1: It's been observed that the number of ML publications are growing exponentially at a faster rate than Moore's law! (Figure from [1].)

The second module focuses on the design of hardware for processing DNNs. It discusses various architecture design decisions depending on the degree of customization (from general purpose platforms to full custom hardware) and design considerations when mapping the DNN workloads onto these architectures. Both temporal and spatial architectures are considered.

- Chapter 3 describes the key metrics that should be considered when designing or comparing various DNN accelerators.
- Chapter 4 describes how DNN kernels can be processed, with a focus on temporal architectures such as CPUs and GPUs. To achieve greater efficiency, such architectures generally have a cache hierarchy and coarser-grained computational capabilities, e.g., vector instructions, making the resulting computation more efficient. Frequently for such architectures, DNN processing can be transformed into a matrix multiplication, which has many optimization opportunities. This chapter also discusses various software and hardware optimizations used to accelerate DNN computations on these platforms without impacting application accuracy.
- Chapter 5 describes the design of specialized hardware for DNN processing, with a focus on spatial architectures. It highlights the processing order and resulting data movement in the hardware used to process a DNN, and the relationship to a loop nest representation of a DNN. The order of the loops in the loop nest is referred to as the *dataflow*, and it determines how often each piece of data needs to be moved. The limits of the loops in the loop nest describe how to break the DNN workload into smaller pieces, referred to as *tiling/blocking* to account for the limited storage capacity at different levels of the memory hierarchy.
- Chapter 6 presents the process of *mapping* a DNN workload on to a DNN accelerator. It describes the steps required to find an optimized mapping including enumerating all legal mappings, and searching those mappings by employing models that project throughput and energy efficiency.

The third module discusses how additional improvements in efficiency can be achieved either by moving up the stack through the co-design of the algorithms and hardware, or down the stack by using mixed signal circuits, and new memory or device technology. In the cases where the algorithm is modified, the impact on accuracy must be carefully evaluated.

- Chapter 7 describes how reducing the precision of data and computation can result in increased throughput and energy efficiency. It discusses how to reduce precision using quantization and the associated design considerations, including hardware cost and impact on accuracy.
- Chapter 8 describes how exploiting sparsity in DNNs can be used to reduce the footprint of the data, which provides an opportunity to reduce storage requirements, data movement, and arithmetic operations. It describes various sources of sparsity and techniques to increase sparsity. It then discusses how sparse DNN accelerators can translate sparsity into improvements in energy-efficiency and throughput. It also presents a new abstract data representation that can be used to express and obtain insight about the dataflows for a variety of sparse DNN accelerators.
- Chapter 9 describes how to optimize the structure of the DNN models (i.e., the 'network architecture' of the DNN) to improve both throughput and energy efficiency while trying to minimize impact on accuracy. It discusses both manual design approaches as well as automatic design approaches (i.e., neural architecture search).
- Chapter 10, on advanced technologies, discusses how mixed-signal circuits and new memory technologies can be used to bring the compute closer to the data (e.g., processing in memory) to address the expensive data movement that dominates throughput and energy consumption of DNNs. It also briefly discusses the promise of reducing energy consumption and increasing throughput by performing the computation and communication in the optical domain.

What's New?

This book is an extension of a tutorial paper written by the same authors entitled "Efficient Processing of Deep Neural Networks: A Tutorial and Survey" that appeared in the *Proceedings of the IEEE* in 2017 and slides from short courses given at ISCA and MICRO in 2016, 2017, and 2019 (slides available at http://eyeriss.mit.edu/tutorial.html). This book includes recent works since the publication of the tutorial paper along with a more in-depth treatment of topics such as dataflow, mapping, and processing in memory. We also provide updates on the fast-moving field of co-design of DNN models and hardware in the areas of reduced precision, sparsity, and efficient DNN model design. As part of this effort, we present a new way of thinking about sparse representations and give a detailed treatment of how to handle and exploit sparsity. Finally, we touch upon recurrent neural networks, auto encoders, and transformers, which we did not discuss in the tutorial paper.

Scope of book

The main goal of this book is to teach the reader how to tackle the computational challenge of efficiently processing DNNs rather than how to design DNNs for increased accuracy. As a result, this book does not cover training (only touching on it lightly), nor does it cover the theory of deep learning or how to design

DNN models (though it discusses how to make them efficient) or use them for different applications. For these aspects, please refer to other references such as Goodfellow's book [2] and Stanford cs231n course notes [3].

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As mentioned earlier in the Preface, this book is an extension of an earlier tutorial paper, which was based on tutorials we gave at ISCA and MICRO. We would like to thank David Brooks for encouraging us to do the first tutorial at MICRO in 2016, which sparked the effort that led to this book.

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Part II

Design of Hardware for Processing DNNs

Chapter 3

Key Metrics and Design Objectives

Over the past few years, there has been a significant amount of research on efficient processing of DNNs. Accordingly, it is important to discuss the key metrics that one should consider when comparing and evaluating the strengths and weaknesses of different designs and proposed techniques and that should be incorporated into design considerations. While efficiency is often only associated with the number of operations per second per Watt (e.g., floating-point operations per second per Watt as FLOPS/W or tera-operations per second per Watt as TOPS/W), it is actually composed of many more metrics including accuracy, throughput, latency, energy consumption, power consumption, cost, flexibility, and scalability. Reporting a comprehensive set of these metrics is important in order to provide a complete picture of the trade-offs made by a proposed design or technique.

In this chapter, we will

- discuss the importance of each of these metrics;
- breakdown the factors that affect each metric. When feasible, present equations that describe the relationship between the factors and the metrics;
- describe how these metrics can be incorporated into design considerations for both the DNN hardware and the DNN model (i.e., workload); and
- specify what should be reported for a given metric to enable proper evaluation.

Finally, we will provide a case study on how one might bring all these metrics together for a holistic evaluation of a given approach. But first, we will discuss each of the metrics.

3.1 Accuracy

Accuracy is used to indicate the quality of the result for a given task. The fact that DNNs can achieve state-of-the-art accuracy on a wide range of tasks is one of the key reasons driving the popularity and wide use of DNNs today. The units used to measure accuracy depend on the task. For instance, for image classification,

accuracy is reported as the percentage of correctly classified images, while for object detection, accuracy is reported as the mean average precision (mAP), which is related to the trade off between the true positive rate and false positive rate.

Factors that affect accuracy include the difficulty of the task and dataset.[1] For instance, classification on ImageNet is much more difficult than on MNIST, and object detection or semantic segmentation is more difficult than classification. As a result, a DNN model that performs well on MNIST may not necessarily perform well on ImageNet.

Achieving high accuracy on difficult tasks or datasets typically requires more complex DNN models (e.g., a larger number of MAC operations and more distinct weights, increased diversity in layer shapes, etc.), which can impact how efficiently the hardware can process the DNN model.

Accuracy should therefore be interpreted in the context of the difficulty of the task and dataset.[2] Evaluating hardware using well-studied, widely used DNN models, tasks, and datasets can allow one to better interpret the significance of the accuracy metric. Recently, motivated by the impact of the SPEC benchmarks for general purpose computing [113], several industry and academic organizations have put together a broad suite of DNN models, called *MLPerf*, to serve as a common set of well-studied DNN models to evaluate the performance and enable fair comparison of various software frameworks, hardware accelerators, and cloud platforms for both training and inference of DNNs [114].[3] The suite includes various types of DNNs (e.g., CNN, RNN, etc.) for a variety of tasks including image classification, object identification, translation, speech-to-text, recommendation, sentiment analysis, and reinforcement learning.

3.2 Throughput and Latency

Throughput is used to indicate the amount of data that can be processed or the number of executions of a task that can be completed in a given time period. High throughput is often critical to an application. For instance, processing video at 30 frames per second is necessary for delivering real-time performance. For data analytics, high throughput means that more data can be analyzed in a given amount of time. As the amount of visual data is growing exponentially, high-throughput big data analytics becomes increasingly important, particularly if an action needs to be taken based on the analysis (e.g., security or terrorist prevention; medical diagnosis or drug discovery). Throughput is often generically reported as the number of operations per second. In the case of inference, throughput is reported as inferences per second or in the form of runtime in terms of seconds per inference.

Latency measures the time between when the input data arrives to a system and when the result is generated. Low latency is necessary for real-time interactive applications, such as augmented reality, autonomous navigation, and robotics. Latency is typically reported in seconds.

Throughput and latency are often assumed to be directly derivable from one another. However, they are actually quite distinct. A prime example of this is the well-known approach of batching input data (e.g., batching

[1] Ideally, robustness and fairness should be considered in conjunction with accuracy, as there is also an interplay between these factors; however, these are areas of on-going research and beyond the scope of this book.

[2] As an analogy, getting 9 out of 10 answers correct on a high school exam is different than 9 out of 10 answers correct on a college-level exam. One must look beyond the score and consider the difficulty of the exam.

[3] Earlier DNN benchmarking efforts including DeepBench [115] and Fathom [116] have now been subsumed by MLPerf.

multiple images or frames together for processing) to increase throughput since it amortizes overhead, such as loading the weights; however, batching also increases latency (e.g., at 30 frames per second and a batch of 100 frames, some frames will experience at least 3.3 second delay), which is not acceptable for real-time applications, such as high-speed navigation where it would reduce the time available for course correction. Thus, achieving low latency and high throughput simultaneously can sometimes be at odds depending on the approach and both should be reported.[4]

There are several factors that affect throughput and latency. In terms of throughput, the number of inferences per second is affected by

$$\frac{\text{inferences}}{\text{second}} = \frac{\text{operations}}{\text{second}} \times \frac{1}{\frac{\text{operations}}{\text{inference}}}, \tag{3.1}$$

where the number of *operations per second* is dictated by both the DNN hardware and DNN model, while the number of *operations per inference* is dictated by the DNN model.

When considering a system comprised of multiple processing elements (PEs), where a PE corresponds to a simple or primitive core that performs a single MAC operation, the number of operations per second can be further decomposed as follows:

$$\frac{\text{operations}}{\text{second}} = \underbrace{\left(\frac{1}{\frac{\text{cycles}}{\text{operation}}} \times \frac{\text{cycles}}{\text{second}}\right)}_{\text{for a single PE}} \times \text{number of PEs} \times \text{utilization of PEs}. \tag{3.2}$$

The first term reflects the peak throughput of a single PE, the second term reflects the amount of parallelism, while the last term reflects degradation due to the inability of the architecture to effectively utilize the PEs.

Since the main operation for processing DNNs is a MAC, we will use number of operations and number of MAC operations interchangeably.

One can increase the peak throughput of a single PE by increasing the number of *cycles per second*, which corresponds to a higher clock frequency, by reducing the critical path at the circuit or micro-architectural level, or the number of *cycles per operations*, which can be affected by the design of the MAC (e.g., a non-pipelined multi-cycle MAC would have more cycles per operation).

While the above approaches increase the throughput of a single PE, the overall throughput can be increased by increasing the *number of PEs*, and thus the maximum number of MAC operations that can be performed in parallel. The number of PEs is dictated by the area density of the PE and the area cost of the system. If the area cost of the system is fixed, then increasing the number of PEs requires either increasing the area

[4]The phenomenon described here can also be understood using Little's Law [117] from queuing theory, where the relationship between average throughput and average latency are related by the average number of tasks in flight, as defined by

$$\overline{\text{throughput}} = \frac{\overline{\text{tasks-in-flight}}}{\overline{\text{latency}}}.$$

A DNN-centric version of Little's Law would have throughput measured in inferences per second, latency measured in seconds, and inferences-in-flight, as the tasks-in-flight equivalent, measured in the number of images in a batch being processed simultaneously. This helps to explain why increasing the number of inferences in flight to increase throughput may be counterproductive because some techniques that increase the number of inferences in flight (e.g., batching) also increase latency.

density of the PE (i.e., reduce the area per PE) or trading off on-chip storage area for more PEs. Reducing on-chip storage, however, can affect the utilization of the PEs, which we will discuss next.

Increasing the density of PEs can also be achieved by reducing the logic associated with delivering operands to a MAC. This can be achieved by controlling multiple MACs with a single piece of logic. This is analogous to the situation in instruction-based systems such as CPUs and GPUs that reduce instruction bookkeeping overhead by using large aggregate instructions (e.g., single-instruction, multiple-data (SIMD) / Vector Instructions; single-instruction, multiple-threads (SIMT) / Tensor Instructions), where a single instruction can be used to initiate multiple operations.

The number of PEs and the peak throughput of a single PE only indicate the theoretical maximum throughput (i.e., peak performance) when all PEs are performing computation (100% utilization). In reality, the achievable throughput depends on the actual utilization of those PEs, which is affected by several factors as follows:

$$\text{utilization of PEs} = \frac{\text{number of active PEs}}{\text{number of PEs}} \times \text{utilization of active PEs}. \tag{3.3}$$

The first term reflects the ability to distribute the workload to PEs, while the second term reflects how efficiently those active PEs are processing the workload.

The *number of active PEs* is the number of PEs that receive work; therefore, it is desirable to distribute the workload to as many PEs as possible. The ability to distribute the workload is determined by the flexibility of the architecture, for instance the on-chip network, to support the layer shapes in the DNN model.

Within the constraints of the on-chip network, the *number of active PEs* is also determined by the specific allocation of work to PEs by the mapping process. The mapping process involves the placement and scheduling in space and time of every MAC operation (including the delivery of the appropriate operands) onto the PEs. Mapping can be thought of as a compiler for the DNN hardware. The design of on-chip networks and mappings are discussed in Chapters 5 and 6.

The *utilization of the active PEs* is largely dictated by the timely delivery of work to the PEs such that the active PEs do not become idle while waiting for the data to arrive. This can be affected by the bandwidth and latency of the (on-chip and off-chip) memory and network. The bandwidth requirements can be affected by the amount of data reuse available in the DNN model and the amount of data reuse that can be exploited by the memory hierarchy and dataflow. The dataflow determines the order of operations and where data is stored and reused. The amount of data reuse can also be increased using a larger batch size, which is one of the reasons why increasing batch size can increase throughput. The challenge of data delivery and memory bandwidth are discussed in Chapters 5 and 6. The *utilization of the active PEs* can also be affected by the imbalance of work allocated across PEs, which can occur when exploiting sparsity (i.e., avoiding unnecessary work associated with multiplications by zero); PEs with less work become idle and thus have lower utilization.

There is also an interplay between the number of PEs and the utilization of PEs. For instance, one way to reduce the likelihood that a PE needs to wait for data is to store some data locally near or within the PE. However, this requires increasing the chip area allocated to on-chip storage, which, given a fixed chip area, would reduce the number of PEs. Therefore, a key design consideration is how much area to allocate to compute (which increases the number of PEs) versus on-chip storage (which increases the utilization of

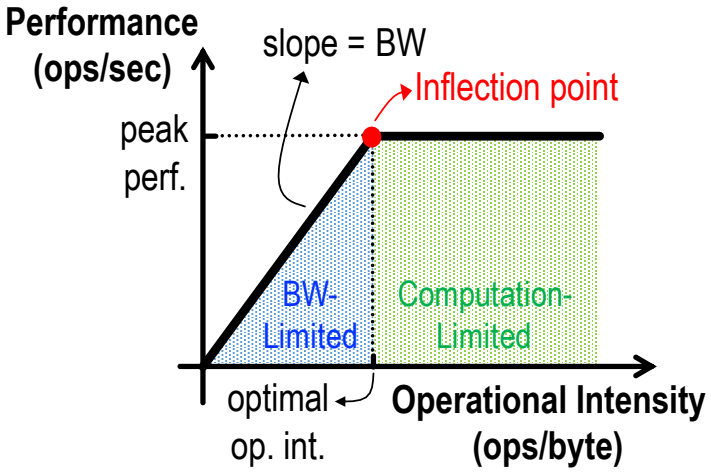


Figure 3.1: The roofline model. The peak *operations per second* is indicated by the bold line; when the operation intensity, which dictates by amount of compute per byte of data, is low, the *operations per second* is limited by the data delivery. The design goal is to operate as close as possible to the peak *operations per second* for the operation intensity of a given workload.

PEs).

The impact of these factors can be captured using Eyexam, which is a systematic way of understanding the performance limits for DNN processors as a function of specific characteristics of the DNN model and accelerator design. Eyexam includes and extends the well-known roofline model [118]. The roofline model, as illustrated in Figure 3.1, relates average bandwidth demand and peak computational ability to performance. Eyexam is described in Chapter 6.

While the number of *operations per inference* in Equation (3.1) depends on the DNN model, the *operations per second* depends on both the DNN model and the hardware. For example, designing DNN models with efficient layer shapes (also referred to efficient network architectures), as described in Chapter 9, can reduce the number of MAC operations in the DNN model and consequently the number of *operations per inference*. However, such DNN models can result in a wide range of layer shapes, some of which may have poor utilization of PEs and therefore reduce the overall *operations per second*, as shown in Equation (3.2).

A deeper consideration of the *operations per second*, is that all operations are not created equal and therefore *cycles per operation* may not be a constant. For example, if we consider the fact that anything multiplied by zero is zero, some MAC operations are ineffectual (i.e., they do not change the accumulated value). The number of ineffectual operations is a function of both the DNN model and the input data. These ineffectual MAC operations can require fewer cycles or no cycles at all. Conversely, we only need to process effectual (or non-zero) MAC operations, where both inputs are non-zero; this is referred to as exploiting sparsity, which is discussed in Chapter 8.

Processing only effectual MAC operations can increase the *(total) operations per second* by increasing the *(total) operations per cycle*.[5] Ideally, the hardware would skip all ineffectual operations; however, in practice, designing hardware to skip all ineffectual operations can be challenging and result in increased

[5]By *total* operations we mean both effectual and ineffectual operations.

hardware complexity and overhead, as discussed in Chapter 8. For instance, it might be easier to design hardware that only recognizes zeros in one of the operands (e.g., weights) rather than both. Therefore, the ineffectual operations can be further divided into those that are exploited by the hardware (i.e., skipped) and those that are unexploited by the hardware (i.e., not skipped). The number of operations actually performed by the hardware is therefore *effectual operations plus unexploited ineffectual operations*.

Equation (3.4) shows how *operations per cycle* can be decomposed into

1. the number of *effectual operations plus unexploited ineffectual operations per cycle*, which remains somewhat constant for a given hardware accelerator design;
2. the ratio of *effectual operations* over *effectual operations plus unexploited ineffectual operations*, which refers to the ability of the hardware to exploit ineffectual operations (ideally unexploited ineffectual operations should be zero, and this ratio should be one); and
3. the number of *effectual operations out of (total) operations*, which is related to the amount of sparsity and depends on the DNN model.

As the amount of sparsity increases (i.e., the number of *effectual operations out of (total) operations* decreases), the *operations per cycle* increases, which subsequently increases *operations per second*, as shown in Equation (3.2):

$$\begin{aligned}\frac{\text{operations}}{\text{cycle}} = &\frac{\text{effectual operations + unexploited ineffectual operations}}{\text{cycle}} \\ &\times \frac{\text{effectual operations}}{\text{effectual operations + unexploited ineffectual operations}} \times \frac{1}{\frac{\text{effectual operations}}{\text{operations}}}.\end{aligned} \tag{3.4}$$

However, exploiting sparsity requires additional hardware to identify when inputs are zero to avoid performing unnecessary MAC operations. The additional hardware can increase the critical path, which decreases cycles per second, and also reduce area density of the PE, which reduces the number of PEs for a given area. Both of these factors can reduce the *operations per second*, as shown in Equation (3.2). Therefore, the complexity of the additional hardware can result in a trade off between reducing the number of *unexploited ineffectual operations* and increasing critical path or reducing the number of PEs.

Finally, designing hardware and DNN models that support reduced precision (i.e., fewer bits per operand and per operations), which is discussed in Chapter 7, can also increase the number of *operations per second*. Fewer bits per operand means that the memory bandwidth required to support a given operation is reduced, which can increase the utilization of PEs since they are less likely to be starved for data. In addition, the area of each PE can be reduced, which can increase the number of PEs for a given area. Both of these factors can increase the *operations per second*, as shown in Equation (3.2). Note, however, that if *multiple* levels of precision need to be supported, additional hardware is required, which can, once again, increase the critical path and also reduce area density of the PE, both of which can reduce the *operations per second*, as shown in Equation (3.2).

In this section, we discussed multiple factors that affect the number of inferences per second. Table 3.1 classifies whether the factors are dictated by the hardware, by the DNN model or both.

Table 3.1: Classification of factors that affect inferences per second.

Factor	Hardware	DNN Model	Input Data
operations per inference		✓	
operations per cycle	✓		
cycles per second	✓		
number of PEs	✓		
number of active PEs	✓	✓	
utilization of active PEs	✓	✓	
effectual operations out of (total) operations		✓	✓
effectual operations plus unexploited ineffectual operations per cycle	✓		

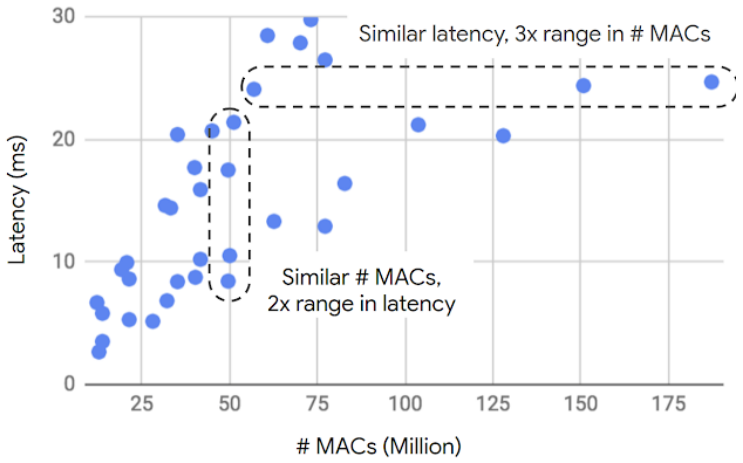


Figure 3.2: The number of MAC operations in various DNN models versus latency measured on Pixel phone. Clearly, the number of MAC operations is not a good predictor of latency. (Figure from [119].)

In summary, the number of MAC operations in the DNN model alone is not sufficient for evaluating the throughput and latency. While the DNN model can affect the number of MAC operations per inference based on the network architecture (i.e., layer shapes) and the sparsity of the weights and activations, the overall impact that the DNN model has on throughput and latency depends on the ability of the hardware to add support to recognize these approaches without significantly reducing utilization of PEs, number of PEs, or cycles per second. This is why the number of MAC operations is not necessarily a good proxy for throughput and latency (e.g., Figure 3.2), and it is often more effective to design efficient DNN models with hardware in the loop. Techniques for designing DNN models with hardware in the loop are discussed in Chapter 9.

Similarly, the number of PEs in the hardware and their peak throughput are not sufficient for evaluating the throughput and latency. It is critical to report actual runtime of the DNN models on hardware to account for other effects such as utilization of PEs, as highlighted in Equation (3.2). Ideally, this evaluation should be performed on clearly specified DNN models, for instance those that are part of the MLPerf benchmarking suite. In addition, batch size should be reported in conjunction with the throughput in order to evaluate latency.

3.3 Energy Efficiency and Power Consumption

Energy efficiency is used to indicate the amount of data that can be processed or the number of executions of a task that can be completed for a given unit of energy. High energy efficiency is important when processing DNNs at the edge in embedded devices with limited battery capacity (e.g., smartphones, smart sensors, robots, and wearables). Edge processing may be preferred over the cloud for certain applications due to latency, privacy, or communication bandwidth limitations. Energy efficiency is often generically reported as the number of operations per joule. In the case of inference, energy efficiency is reported as inferences per joule or the inverse as energy consumption in terms of joules per inference.

Power consumption is used to indicate the amount of energy consumed per unit time. Increased power consumption results in increased heat dissipation; accordingly, the maximum power consumption is dictated by a design criterion typically called the thermal design power (TDP), which is the power that the cooling system is designed to dissipate. Power consumption is important when processing DNNs in the cloud as data centers have stringent power ceilings due to cooling costs; similarly, handheld and wearable devices also have tight power constraints since the user is often quite sensitive to heat and the form factor of the device limits the cooling mechanisms (e.g., no fans). Power consumption is typically reported in watts or joules per second.

Power consumption in conjunction with energy efficiency limits the throughput as follows:

$$\frac{\text{inferences}}{\text{second}} \leq \text{Max}\left(\frac{\text{joules}}{\text{second}}\right) \times \frac{\text{inferences}}{\text{joule}}. \tag{3.5}$$

Therefore, if we can improve energy efficiency by increasing the number of *inferences per joule*, we can increase the number of *inferences per second* and thus throughput of the system.

There are several factors that affect the energy efficiency. The number of inferences per joule can be decomposed into

$$\frac{\text{inferences}}{\text{joule}} = \frac{\text{operations}}{\text{joule}} \times \frac{1}{\frac{\text{operations}}{\text{inference}}}, \tag{3.6}$$

where the number of operations per joule is dictated by both the hardware and DNN model, while the number of operations per inference is dictated by the DNN model.

There are various design considerations for the hardware that will affect the energy per operation (i.e., joules per operation). The energy per operation can be broken down into the energy required to move the input and output data, and the energy required to perform the MAC computation

$$\text{Energy}_{total} = \text{Energy}_{data} + \text{Energy}_{MAC}. \tag{3.7}$$

For each component the joules per operation[6] is computed as

[6]Here, an operation can be a MAC operation or a data movement.

Operation:	Energy (pJ)
8b Add	0.03
16b Add	0.05
32b Add	0.1
16b FP Add	0.4
32b FP Add	0.9
8b Multiply	0.2
32b Multiply	3.1
16b FP Multiply	1.1
32b FP Multiply	3.7
32b SRAM Read (8KB)	5
32b DRAM Read	640

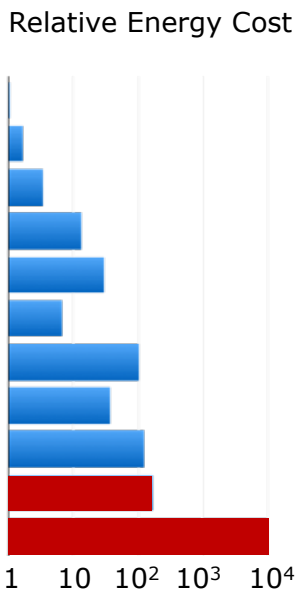


Figure 3.3: The energy consumption for various arithmetic operations and memory accesses in a 45 nm process. The relative energy cost (computed relative to the 8b add) is shown on a log scale. The energy consumption of data movement (red) is significantly higher than arithmetic operations (blue). (Figure adapted from [120].)

$$\frac{\text{joules}}{\text{operation}} = \alpha \times C \times {V_{DD}}^2, \tag{3.8}$$

where C is the total switching capacitance, V_{DD} is the supply voltage, and α is the switching activity, which indicates how often the capacitance is charged.

The energy consumption is dominated by the data movement as the capacitance of data movement tends to be much higher that the capacitance for arithmetic operations such as a MAC (Figure 3.3). Furthermore, the switching capacitance increases the further the data needs to travel to reach the PE, which consists of the distance to get out of the memory where the data is stored and the distance to cross the network between the memory and the PE. Accordingly, larger memories and longer interconnects (e.g., off-chip) tend to consume more energy than smaller and closer memories due to the capacitance of the long wires employed. In order to reduce the energy consumption of data movement, we can exploit data reuse where the data is moved once from distant large memory (e.g., off-chip DRAM) and reused for multiple operations from a local smaller memory (e.g., on-chip buffer or scratchpad within the PE). Optimizing data movement is a major consideration in the design of DNN accelerators; the design of the dataflow, which defines the processing order, to increase data reuse within the memory hierarchy is discussed in Chapter 5. In addition, advanced device and memory technologies can be used to reduce the switching capacitance between compute and memory, as described in Chapter 10.

This raises the issue of the appropriate scope over which energy efficiency and power consumption should be reported. Including the entire system (out to the fans and power supplies) is beyond the scope of this book. Conversely, ignoring off-chip memory accesses, which can vary greatly between chip designs, can easily result in a misleading perception of the efficiency of the system. Therefore, it is critical to not only report the

energy efficiency and power consumption of the chip, but also the energy efficiency and power consumption of the off-chip memory (e.g., DRAM) or the amount of off-chip accesses (e.g., DRAM accesses) if no specific memory technology is specified; for the latter, it can be reported in terms of the total amount of data that is read and written off-chip per inference.

Reducing the joules per MAC operation itself can be achieved by reducing the switching activity and/or capacitance at a circuit level or micro-architecture level. This can also be achieved by reducing precision (e.g., reducing the bit width of the MAC operation), as shown in Figure 3.3 and discussed in Chapter 7. Note that the impact of reducing precision on accuracy must also be considered.

For instruction-based systems such as CPUs and GPUs, this can also be achieved by reducing instruction bookkeeping overhead. For example, using large aggregate instructions (e.g., single-instruction, multiple-data (SIMD) / Vector Instructions; single-instruction, multiple-threads (SIMT) / Tensor Instructions), a single instruction can be used to initiate multiple operations.

Similar to the throughput metric discussed in Section 3.2, the number of *operations per inference* depends on the DNN model, however the *operations per joules* may be a function of the ability of the hardware to exploit sparsity to avoid performing ineffectual MAC operations. Equation (3.9) shows how *operations per joule* can be decomposed into:

1. the number of *effectual operations plus unexploited ineffectual operations per joule*, which remains somewhat constant for a given hardware architecture design;
2. the ratio of *effectual operations* over *effectual operations plus unexploited ineffectual operations*, which refers to the ability of the hardware to exploit ineffectual operations (ideally unexploited ineffectual operations should be zero, and this ratio should be one); and
3. the number of *effectual operations out of (total) operations*, which is related to the amount of sparsity and depends on the DNN model.

$$\begin{aligned}\frac{\text{operations}}{\text{joule}} = &\frac{\text{effectual operations + unexploited ineffectual operations}}{\text{joule}} \\ &\times \frac{\text{effectual operations}}{\text{effectual operations + unexploited ineffectual operations}} \\ &\times \frac{1}{\frac{\text{effectual operations}}{\text{operations}}}.\end{aligned} \tag{3.9}$$

For hardware that can exploit sparsity, increasing the amount of sparsity (i.e., decreasing the number of *effectual operations out of (total) operations*) can increase the number of *operations per joule*, which subsequently increases *inferences per joule*, as shown in Equation (3.6). While exploiting sparsity has the potential of increasing the number of *(total) operations per joule*, the additional hardware will decrease the *effectual operations plus unexploited ineffectual operations per joule*. In order to achieve a net benefit, the decrease in *effectual operations plus unexploited ineffectual operations per joule* must be more than offset by the decrease of *effectual operations out of (total) operations*.

In summary, we want to emphasize that the number of MAC operations and weights in the DNN model are not sufficient for evaluating energy efficiency. From an energy perspective, all MAC operations or weights are not created equal. This is because the number of MAC operations and weights do not reflect where the data is accessed and how much the data is reused, both of which have a significant impact on the *operations per joule*. Therefore, the number of MAC operations and weights is not necessarily a good proxy for energy consumption and it is often more effective to design efficient DNN models with hardware in the loop. Techniques for designing DNN models with hardware in the loop are discussed in Chapter 9.

In order to evaluate the energy efficiency and power consumption of the entire system, it is critical to not only report the energy efficiency and power consumption of the chip, but also the energy efficiency and power consumption of the off-chip memory (e.g., DRAM) or the amount of off-chip accesses (e.g., DRAM accesses) if no specific memory technology is specified; for the latter, it can be reported in terms of the total amount of data that is read and written off-chip per inference. As with throughput and latency, the evaluation should be performed on clearly specified, ideally widely used, DNN models.

3.4 Hardware Cost

In order to evaluate the desirability of a given architecture or technique, it is also important to consider the *hardware cost* of the design. Hardware cost is used to indicate the monetary cost to build a system.[7] This is important from both an industry and a research perspective to dictate whether a system is financially viable. From an industry perspective, the cost constraints are related to volume and market; for instance, embedded processors have a much more stringent cost limitations than processors in the cloud.

One of the key factors that affect cost is the chip area (e.g., square millimeters, mm^2) in conjunction with the process technology (e.g., 45 nm CMOS), which constrains the amount of on-chip storage and amount of compute (e.g., the number of PEs for custom DNN accelerators, the number of cores for CPUs and GPUs, the number of digital signal processing (DSP) engines for FPGAs, etc.). To report information related to area, without specifying a specific process technology, the amount of on-chip memory (e.g, storage capacity of the global buffer) and compute (e.g., number of PEs) can be used as a proxy for area.

Another important factor is the amount of off-chip bandwidth, which dictates the cost and complexity of the packaging and printed circuit board (PCB) design (e.g., High Bandwidth Memory (HBM) [121] to connect to off-chip DRAM, NVLink to connect to other GPUs, etc.), as well as whether additional chip area is required for a transceiver to handle signal integrity at high speeds. The off-chip bandwidth, which is typically reported in gigabits per second (Gbps), sometimes including the number of I/O ports, can be used as a proxy for packaging and PCB cost.

There is also an interplay between the costs attributable to the chip area and off-chip bandwidth. For instance, increasing on-chip storage, which increases chip area, can reduce off-chip bandwidth. Accordingly, both metrics should be reported in order to provide perspective on the total cost of the system.

[7]There is also cost associated with operating a system, such as the electricity bill and the cooling cost, which are primarily dictated by the energy efficiency and power consumption, respectively. There is also cost associated with designing the system. The operating cost is covered by the section on energy efficiency and power consumption and we limited our coverage of design cost to the fact that custom DNN accelerators have a higher design cost than off-the-shelf CPUs and GPUs. We consider anything beyond this, e.g., the economics of the semiconductor business, including how to price platforms, is outside the scope of this book.

Of course reducing cost alone is not the only objective. The design objective is invariably to maximize the throughput or energy efficiency for a given cost, specifically, to maximize *inferences per second per cost* (e.g., $) and/or *inferences per joule per cost*. This is closely related to the previously discussed property of utilization; to be cost efficient, the design should aim to utilize every PE to increase inferences per second, since each PE increases the area and thus the cost of the chip; similarly, the design should aim to effectively utilize all the on-chip storage to reduce off-chip bandwidth, or increase operations per off-chip memory access as expressed by the roofline model (see Figure 3.1), as each byte of on-chip memory also increases cost.

3.5 Flexibility

The merit of a DNN accelerator is also a function of its *flexibility*. Flexibility refers to the range of DNN models that can be supported on the DNN processor and the ability of the software environment (e.g., the mapper) to maximally exploit the capabilities of the hardware for any desired DNN model. Given the fast-moving pace of DNN research and deployment, it is increasingly important that DNN processors support a wide range of DNN models and tasks.

We can define *support* in two tiers: the first tier requires that the hardware only needs to be able to *functionally* support different DNN models (i.e., the DNN model can run on the hardware). The second tier requires that the hardware should also *maintain efficiency* (i.e., high throughput and energy efficiency) across different DNN models.

To maintain efficiency, the hardware should not rely on certain properties of the DNN models to achieve efficiency, as the properties cannot be guaranteed. For instance, a DNN accelerator that can efficiently support the case where the entire DNN model (i.e., all the weights) fits on-chip may perform extremely poorly when the DNN model grows larger, which is likely given that the size of DNN models continue to increase over time, as discussed in Section 2.4.1; a more flexible processor would be able to efficiently handle a wide range of DNN models, even those that exceed on-chip memory.

The degree of flexibility provided by a DNN accelerator is a complex trade-off with accelerator cost. Specifically, additional hardware usually needs to be added in order to flexibly support a wider range of workloads and/or improve their throughput and energy efficiency. We all know that specialization improves efficiency; thus, the design objective is to reduce the overhead (e.g., area cost and energy consumption) of supporting flexibility while maintaining efficiency across the wide range of DNN models. Thus, evaluating flexibility would entail ensuring that the extra hardware is a net benefit across multiple workloads.

Flexibility has become increasingly important when we factor in the many techniques that are being applied to the DNN models with the promise to make them more efficient, since they increase the diversity of workloads that need to be supported. These techniques include DNNs with different network architectures (i.e., different layer shapes, which impacts the amount of required storage and compute and the available data reuse that can be exploited), as described in Chapter 9, different levels of precision (i.e., different number of bits for across layers and data types), as described in Chapter 7, and different degrees of sparsity (i.e., number of zeros in the data), as described in Chapter 8. There are also different types of DNN layers and computation beyond MAC operations (e.g., activation functions) that need to be supported.

Actually getting a performance or efficiency benefit from these techniques invariably requires additional

hardware, because a simpler DNN accelerator design may not benefit from these techniques. Again, it is important that the overhead of the additional hardware does not exceed the benefits of these techniques. This encourages a hardware and DNN model *co-design* approach.

To date, exploiting the flexibility of DNN hardware has relied on mapping processes that act like static per-layer compilers. As the field moves to DNN models that change dynamically, mapping processes will need to dynamically adapt at runtime to changes in the DNN model or input data, while still maximally exploiting the flexibility of the hardware to improve efficiency.

In summary, to assess the flexibility of DNN processors, its efficiency (e.g., inferences per second, inferences per joule) should be evaluated on a wide range of DNN models. The MLPerf benchmarking workloads are a good start; however, additional workloads may be needed to represent efficient techniques such as efficient network architectures, reduced precision and sparsity. The workloads should match the desired application. Ideally, since there can be many possible combinations, it would also be beneficial to define the range and limits of DNN models that can be *efficiently* supported on a given platform (e.g., maximum number of weights per filter or DNN model, minimum amount of sparsity, required structure of the sparsity, levels of precision such as 8-bit, 4-bit, 2-bit, or 1-bit, types of layers and activation functions, etc.).

3.6 Scalability

Scalability has become increasingly important due to the wide use cases for DNNs and emerging technologies used for scaling up not just the size of the chip, but also building systems with multiple chips (often referred to as chiplets) [122] or even wafer-scale chips [123]. Scalability refers to how well a design can be scaled up to achieve higher throughput and energy efficiency when increasing the amount of resources (e.g., the number of PEs and on-chip storage). This evaluation is done under the assumption that the system does not have to be significantly redesigned (e.g., the design only needs to be replicated) since major design changes can be expensive in terms of time and cost. Ideally, a scalable design can be used for low-cost embedded devices and high-performance devices in the cloud simply by scaling up the resources.

Ideally, the throughput would scale linearly and proportionally with the number of PEs. Similarly, the energy efficiency would also improve with more on-chip storage, however, this would be likely be nonlinear (e.g., increasing the on-chip storage such that the entire DNN model fits on chip would result in an abrupt improvement in energy efficiency). In practice, this is often challenging due to factors such as the reduced utilization of PEs and the increased cost of data movement due to long distance interconnects.

Scalability can be connected with cost efficiency by considering how *inferences per second per cost* (e.g., $) and *inferences per joule per cost* changes with scale. For instance, if throughput increases linearly with number of PEs, then the *inferences per second per cost* would be constant. It is also possible for the *inferences per second per cost* to improve super-linearly with increasing number of PEs, due to increased sharing of data across PEs.

In summary, to understand the scalability of a DNN accelerator design, it is important to report its performance and efficiency metrics as the number of PEs and storage capacity increases. This may include how well the design might handle technologies used for scaling up, such as inter-chip interconnect.

3.7 Interplay Between Different Metrics

It is important that all metrics are accounted for in order to fairly evaluate all the design trade-offs. For instance, without the accuracy given for a specific dataset and task, one could run a simple DNN and easily claim low power, high throughput, and low cost—however, the processor might not be usable for a meaningful task; alternatively, without reporting the off-chip bandwidth, one could build a processor with only multipliers and easily claim low cost, high throughput, high accuracy, and low *chip* power—however, when evaluating *system* power, the off-chip memory access would be substantial. Finally, the test setup should also be reported, including whether the results are measured or obtained from simulation[8] and how many images were tested.

In summary, the evaluation process for whether a DNN system is a viable solution for a given application might go as follows:

1. the accuracy determines if it can perform the given task;
2. the latency and throughput determine if it can run fast enough and in real time;
3. the energy and power consumption will primarily dictate the form factor of the device where the processing can operate;
4. the cost, which is primarily dictated by the chip area and external memory bandwidth requirements, determines how much one would pay for this solution;
5. flexibility determines the range of tasks it can support; and
6. the scalability determines whether the same design effort can be amortized for deployment in multiple domains, (e.g., in the cloud and at the edge), and if the system can efficiently be scaled with DNN model size.

[8] If obtained from simulation, it should be clarified whether it is from synthesis or post place-and-route and what library corner (e.g., process corner, supply voltage, temperature) was used.

Chapter 10

Advanced Technologies

As highlighted throughout the previous chapters, data movement dominates energy consumption. The energy is consumed both in the access to the memory as well as the transfer of the data. The associated physical factors also limit the bandwidth available to deliver data between memory and compute, and thus limits the throughput of the overall system. This is commonly referred to by computer architects as the "memory wall."[1]

To address the challenges associated with data movement, there have been various efforts to bring compute and memory closer together. Chapters 5 and 6 primarily focus on how to design spatial architectures that distribute the on-chip memory closer to the computation (e.g., scratch pad memory in the PE). This chapter will describe various other architectures that use *advanced memory*, *process*, and *fabrication technologies* to bring the compute and memory together.

First, we will describe efforts to bring the off-chip high-density memory (e.g., DRAM) closer to the computation. These approaches are often referred to as *processing near memory* or *near-data processing*, and include memory technologies such as embedded DRAM and 3-D stacked DRAM.

Next, we will describe efforts to integrate the computation *into* the memory itself. These approaches are often referred to as *processing in memory* or *in-memory computing*, and include memory technologies such as Static Random Access Memories (SRAM), Dynamic Random Access Memories (DRAM), and emerging non-volatile memory (NVM). Since these approaches rely on mixed-signal circuit design to enable processing in the analog domain, we will also discuss the design challenges related to handling the increased sensitivity to circuit and device non-idealities (e.g., nonlinearity, process and temperature variations), as well as the impact on area density, which is critical for memory.

Significant data movement also occurs between the sensor that collects the data and the DNN processor. The same principles that are used to bring compute near the memory, where the weights are stored, can be used to bring the compute *near* the sensor, where the input data is collected. Therefore, we will also discuss how to integrate some of the compute *into* the sensor.

Finally, since photons travel much faster than electrons and the cost of moving a photon can be *independent* of distance, processing in the optical domain using light may provide significant improvements in energy

[1] Specifically, the memory wall refers to data moving between the off-chip memory (e.g., DRAM) and the processor.

Table 10.1: Example of recent works that explore processing near memory. For I/O, TSV refers to through-silicon vias, while TCI refers to ThruChip Interface which uses inductive coupling. For bandwidth, *ch* refers to number of parallel communication channels, which can be the number of tiles (for eDRAM) or the number of vaults (for stacked memory). The size of stacked DRAM is based on Hybrid Memory Cube (HMC) Gen2 specifications.

	Technology	**Size**	**I/O**	**Bandwidth**	**Evaluation**
DaDianNao [151]	eDRAM	32MB	on-chip	18 ch×310 GB/s = 5580 GB/s	Simulated
Neurocube [315]	Stacked DRAM	2GB	TSV	16 ch×10 GB/s = 160 GB/s	Simulated
Tetris [316]	Stacked DRAM	2GB	TSV	16 ch×8 GB/s = 128 GB/s	Simulated
Quest [317]	Stacked SRAM	96MB	TCI	24 ch×1.2 GB/s = 28.8 GB/s	Measured
N3XT [318]	monolithic 3-D	4GB	ILV	16 ch×48 GB/s = 768 GB/S	Simulated

efficiency and throughput over the electrical domain. Accordingly, we will conclude this chapter by discussing the recent work that performs DNN processing in the optical domain, referred to as *Optical Neural Networks*.

10.1 Processing Near Memory

High-density memories typically require a different process technology than processors and as a result are often fabricated as separate chips; as a result, accessing high-density memories requires going off-chip. The bandwidth and energy cost of accessing high-density off-chip memories are often limited by the number of I/O pads per chip and the off-chip interconnect channel characteristics (i.e., its resistance, inductance, and capacitance). Processing near memory aims to overcome these limitations by bringing the compute near the high-density memory to reduce access energy and increase memory bandwidth. The reduction in access energy is achieved by reducing the length of the interconnect between the memory and compute, while the increase in bandwidth is primarily enabled by increasing the number of bits that can be accessed per cycle by allowing for a wider interconnect and, to a lesser extent, by increasing the clock frequency, which is made possible by the reduced interconnect length.

Various recent advanced memory technologies aim to enable processing near memory with differing integration costs. Table 10.1 summarizes some of these efforts, where high-density memories on the order of tens of megabytes to gigabytes are connected to the compute engine at bandwidths of tens to hundreds of gigabytes per second. Note that currently most academic evaluations of DNN systems using advanced memory technologies have been based on simulations rather than fabrication and measurements.

In this section, we will describe the cost and benefits of each technology and provide examples of how they have been used to process DNNs. The architectural design challenges of using processing-near-memory include how to allocate data to memory since the access patterns for high-density memories are often limited (e.g., data needs to be divided into different banks and vaults in the DRAM or stacked DRAM, respectively), how to design the network-on-chip between the memory and PEs, how to allocate the chip area between on-chip memory and compute now that off-chip communication less expensive, and how to design the memory hierarchy and dataflow now that the data movement costs are different.

10.1.1 Embedded High-Density Memories

Accessing data from off-chip memory can result in high energy cost as well as limited memory bandwidth (due to limited data bus width due to number of I/O pads, and signaling frequency due to the channel characteristics of the off-chip routing). Therefore, there has been a significant amount of effort toward embedding high-density memory on-chip. This includes technology such as *embedded DRAM (eDRAM)* [319] as well as *embedded non-volatile (eNVM)* [320], which includes embedded Flash (eFlash) [321], magnetic random-access memory (MRAM) [322], resistive random-access memory (RRAM) [323, 324], and phase change memory (PCRAM) [325].

In DNN processing, these high-density memories can be used to store tens of megabytes of weights and activations on chip to reduce off-chip access. For instance, DaDianNao [151] uses 16×2MB eDRAM tiles to store the weights and 2×2MB eDRAM tiles to store the input and output activations; furthermore, all these tiles (each with 4096-bit rows) can be accessed in parallel, which gives extremely high memory bandwidth.[2] The downside of eDRAM is that it has a lower density than off-chip DRAM and can increase the fabrication cost of the chip. In addition, it has been reported that eDRAM scaling is slower than SRAM scaling [326], and thus the density advantage of eDRAM over SRAM will reduce over time. In contrast, eNVMs have gained popularity in recent years due to its increased density as well as its non-volatility properties and reduction in standby power (e.g., leakage, refresh, etc.) compared to eDRAM [326].

10.1.2 Stacked Memory (3-D Memory)

Rather than integrating DRAM into the chip itself, the DRAM can also be stacked on top of the chip using through-silicon vias (TSVs). This technology is often referred to as *3-D memory*,[3] and has been commercialized in the form of Hybrid Memory Cube (HMC) [327] and High Bandwidth Memory (HBM) [121]. 3-D memory delivers an order of magnitude higher bandwidth and reduces access energy by up to 5× relative to existing 2-D DRAMs, as TSVs have lower capacitance than typical off-chip interconnects.

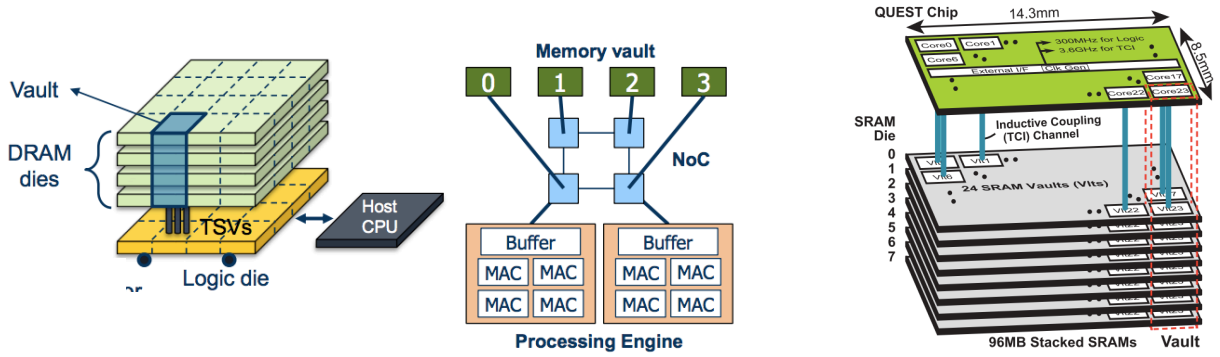
Recent works have explored the use of HMC for efficient DNN processing in a variety of ways. For instance, Neurocube [315], shown in Figure 10.1(a), uses HMC to bring the memory and computation closer together. Each DRAM vault (vertically stacked DRAM banks) is connected to a PE containing a buffer and several MACs. A 2-D mesh network-on-chip (NoC) is used to connect the different PEs, allowing the PEs to access data from different vaults. One major design decision involves determining how to distribute the weights and activations across the different vaults to reduce the traffic on the NoC.

Another example that uses HMC is Tetris [316], which explores the use of HMC with the Eyeriss spatial architecture and row-stationary dataflow. It proposes allocating more area to computation than on-chip memory (i.e., larger PE array and smaller global buffer) in order to exploit the low-energy and high-throughput properties of the HMC. It also adapts the dataflow to account for the HMC and smaller on-chip memory.

SRAM can also be stacked on top of the chip to provide 10× lower latency compared to DRAM [317]. For instance, Quest [317], shown in Figure 10.1(b), uses eight 3-D stacked SRAM dies to store both the weights

[2] DaDianNao [151] assumes that the DNN model can fit into the 32MB of eDRAM allocated to the weights. In practice, this implies that the design either limits the size of DNN model, or requires access to off-chip memory if the size of the DNN model exceeds the capacity of the eDRAM.

[3] Also referred to as "in-package" memory since both the memory and compute can be integrated into the same package.



(a) Neurocube (Figure from [315])

(b) Quest (Figure from [328])

Figure 10.1: Stacked memory systems. (a) DRAM using through-silicon vias (TSV) and (b) SRAM using inductive coupling.

and the activations of the intermediate feature maps when processing layer by layer. The SRAM dies are connected to the chip using inductive-coupling die-to-die wireless communication technology, known as a ThruChip Interface (TCI) [329], which has lower integration cost than TSV.

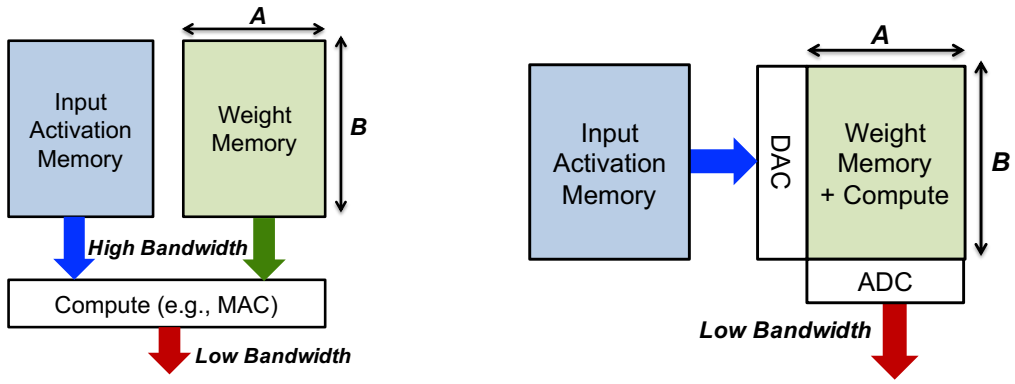
The above 3-D memory designs involve using TSV or TCI to connect memory and logic dies that have been separately fabricated. Recent breakthroughs in nanotechnology have made it feasible to directly fabricate thin layers of logic and memory devices on top of each other, referred to as monolithic 3-D integration. Interlayer vias (ILVs), which have several orders of magnitude denser vertical connectivity than TSV, can then be used to connect the memory and compute. Current monolithic 3-D integration systems, such as N3XT, use on-chip non-volatile memory (e.g., resistive RAM (RRAM), spin-transfer torque RAM (STT-RAM) / magnetic RAM (MRAM), phase change RAM (PCRAM)), and carbon nanotube logic (CNFET). Based on simulations, the energy-delay product of ILVs can be up to two orders of magnitude lower than 2-D systems on deep neural network workloads, compared to 8× for TSV [318].[4]

In order to fully understand the impact of near memory processing it is important to analyze the impact that the added storage layer has on the mappings that are now available. Specifically, the new memories are faster, but also smaller, so optimal mappings will be different.

10.2 Processing in Memory

While the previous section discussed methods to bring the compute near the memory, this section discusses *processing in memory*, which brings the compute *into* the memory. We will first highlight the differences between processing in memory and conventional architectures, then describe how processing in memory can be performed using different memory technologies including NVM, SRAM, and DRAM. Finally, we will highlight various design challenges associated with processing-in-memory accelerators that are commonly found across technologies.

[4]The savings are highest for DNN models and configurations with low amounts of data reuse (e.g., FC layers with small batch size) resulting in more data movement across ILV.



(a) Conventional (b) Processing in memory

Figure 10.2: Comparison of conventional processing and processing in memory.

DNN processing can be performed using matrix-vector multiplication (see Figures 4.2 and 4.3), as discussed in Chapter 4. For conventional architectures, both the input activation vector and the weight matrix are read out from their respective memories and processed by a MAC array, as shown in Figure 10.2(a); the number of weights that can be read at once is limited by the memory interface (e.g., the read out logic and the number of memory ports). This limited memory bandwidth for the weights (e.g., a row of A weights per cycle in Figure 10.2(b)) can also limit the number of MAC operations that can be performed in parallel (i.e., operations per cycle) and thus the overall throughput (i.e., operations per second).

Processing-in-memory architectures propose moving the compute into the memory that stores the weight matrix, as shown in Figure 10.2(b). This can help reduce the data movement of the weights by avoiding the cost of reading the weight matrix; rather than reading the weights, only the computed results such as the partial sums or the final output activations are read out of the memory. Furthermore, processing in memory architectures can also increase the memory bandwidth, as the number of weights that can be accessed in parallel is no longer limited by the memory interface; in theory, the entire weight matrix (e.g., $A \times B$ in Figure 10.2(b)) could be read and processed in parallel.

Figure 10.3 shows a weight-stationary dataflow architecture that is typically used for processing in memory. The word lines (WLs) are used to deliver the input activations to the storage elements, and the bit lines (BLs) are used to read the computed output activations or partial sums. The MAC array is implemented using the storage elements (that store the weights), where a multiplication is performed at each storage element, and the accumulation across multiple storage elements on the same column is performed using the bit line. In theory, a MAC array of B rows of A elements can access all $A \times B$ weights at the same time, and perform up to A dot products in parallel, where each sums B elements (i.e., $A \times B$ MAC operations per cycle).

Similar to other weight-stationary architectures, the input activations can be reused across the different columns (up to A times for the example given in Figure 10.3), which reduces number of input activation reads. In addition, since a storage element tends to be smaller in area than the logic for a digital MAC (10 to 100× smaller in area and 3 to 10× smaller in edge length [330]), the routing capacitance to deliver the input activations can also be reduced, which further reduces the energy cost of delivering the input activations. Depending on the format of the inputs and outputs to the array, digital-to-analog converters (DACs) and analog-to-digital converters (ADCs) may also be required to convert the word line and bit line values, respectively; the cost of the DAC scales with the precision of the input activations driven on the word

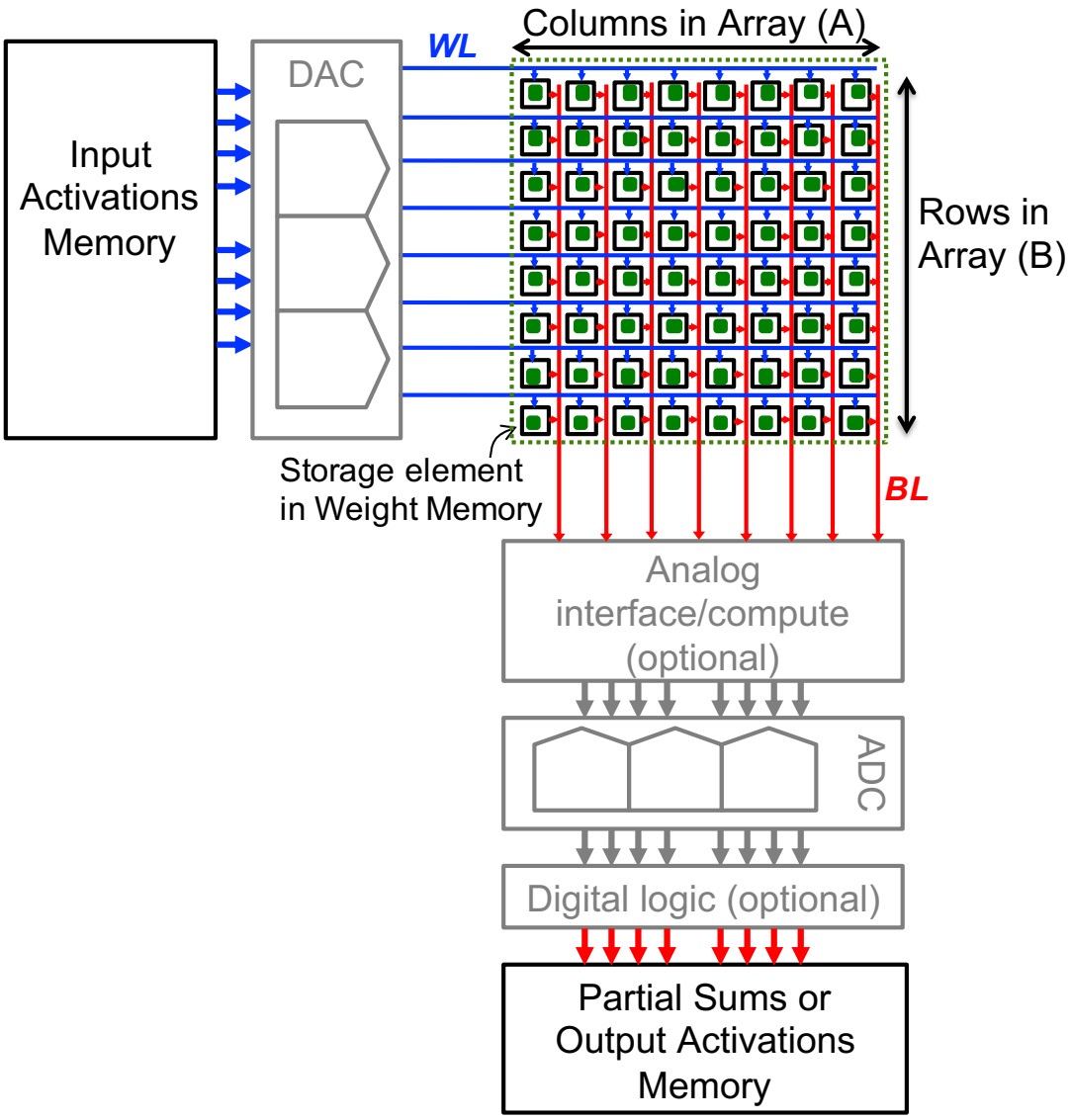


Figure 10.3: Typical dataflow for processing-in-memory accelerators.

line, while the cost of the ADC scales with the precision of the partial sums, which depends on the precision of the weights and input activations, and the number of values accumulated on the bit line (up to B).[5]

An alternative way to view processing in memory is to use the loop nest representation introduced in Chapter 5. Design 20 illustrates a processing-in-memory design for an FC layer with M output channels and where the input activations are flattened along the input channel, height and width dimensions (CHW). The computation take place in one cycle computing all the results in a single cycle in line 7. For this design, some of the mapping constraints are that $A \geq M$ and $B \geq C \times H \times W$.[6] Note, that when $A \neq M$ or $B \neq C \times H \times W$ under-utilization will occur, as described in Section 10.2.4.

Design 20 FC layer for Processing in Memory

```
1    i = Array(CHW)          # Input activations
2    f = Array(M, CHW)       # Filter weights
3    o = Array(M)            # Output partial sums
4
5    parallel-for m in [0, M):
6        parallel-for chw in [0, CHW):
7                o[m] += i[chw] * f[m, chw]
```

A processing in memory design can also handle convolutions, as illustrated in the loop nest in Design 21. Here, we show a toy design of just a 1-D convolution with multiple input channels (C) and multiple output channels (M). The entire computation takes Q steps as the only temporal step is the **for** loop (line 8). Interpreting the activity in the body of the loop (line 10), we see that in each cycle all filter weights are used ($M \times S \times C$) each as part a distinct MAC operation, the same input activation is used multiple times ($C \times S$) and multiple output partial sums are accumulated into (M). This design reflects the Toeplitz expansion of the input activations (see Section 4.1), so the same input activations will be delivered multiple times, since the same value for the input activation index w will be generated for different qs. For the processing in memory convolution design, some of the mapping constraints are that $A \geq M$ and $B \geq C \times S$. Note, that when $A \neq M$ or $B \neq C \times S$ under-utilization will occur, as described in Section 10.2.4.

In the next few sections (Sections 10.2.1, 10.2.2, and 10.2.3), we will briefly describe how processing in memory can be performed using different memory technologies. Section 10.2.4 will then give an overview of some of the key design challenges and decisions that should be considered when designing processing-in-memory accelerators for DNNs. For instance, many of these designs are limited to reduced precision (i.e., low bit-width) due to the non-idealities of the devices and circuits used for memories.

[5]The number of bits that an ADC can correctly resolve also depends on its thermal noise (typically some multiple of kT/C, where k is the Boltzmann constant, T is the temperature, and C is the capacitance of the sampling capacitor). For instance, an N-bit ADC has 2^{N-1} decision boundaries (see Section 7.2.1). However, if the thermal noise is large, the location of the 2^{N-1} decision boundaries will move around, dynamically and randomly, and this will affect the resulting accuracy of the DNN being processed. Therefore, designing a low noise ADC is an important consideration. Note that the thermal noise of the ADC scales with the power consumption and the area of the ADC. Accordingly, it is important that the ADC's thermal noise be considered when evaluating the accuracy as demonstrated in [331, 332, 333], as the design of the ADC involves a trade-off between power, area, and accuracy.

[6]For this example, we disallow the cases where $A < M$ or $B < C \times H \times W$, since that would require multiple passes and updates of the weights, which reduces the potential benefits of processing in memory.

Design 21 1-D Weight-Stationary Convolution Dataflow for Processing in Memory

```
i = Array(C, W)          # Input activations
f = Array(M, C, S)       # Filter weights
o = Array(M, Q)          # Output partial sums

parallel-for m in [0, M):
    parallel-for s in [0, S):
        parallel-for c in [0, C]:
            for q in [0, Q):
                w = q + s
                o[m, q] += i[c, w] * f[m, c, s]
```

10.2.1 Non-Volatile Memories (NVM)

Many recent works have explored enabling processing-in-memory using *non-volatile memories (NVM)* due to their high density and thus potential for replacing off-chip memory and reducing off-chip data movement. Advanced non-volatile high-density memories use programmable resistive elements, commonly referred to as *memristors* [334], as storage elements. These NVM devices enable increased density since memory and computation can be densely packed with a similar density to DRAM [335].[7]

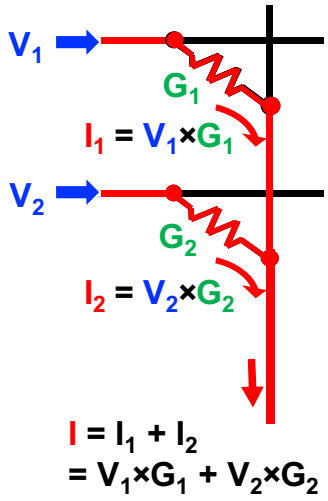
Non-volatile memories exploit Ohm's law by using the conductance (i.e., the inverse of the resistance) of a device to represent a filter weight and the voltage across the device to represent the input activation value. So the resulting current can be interpreted as the product (i.e., a partial sum). This is referred to as a *current-based* approach. For instance, Figure 10.4(a) shows how a multiplication can be performed using the conductance of the NVM device as the weight, and the voltage on the word line as the input activation, and the current output to the bit line as the product of the two. The accumulation is done by summing the currents on the bit line based on Kirchhoff's current law. Alternatively, for Flash-based NVM, the multiplication is performed using the current-voltage (IV) characteristics of the floating-gate transistor, where the threshold voltage of the floating-gate transistor is set based on the weight, as shown in Figure 10.4(c). Similar to the previously described approaches, a voltage proportional to the input activation can be applied across the device, and the accumulation is performed by summing output current of the devices on the bit line.

NVM-based processing-in-memory accelerators have several unique challenges, as described in [339, 340]. First, the cost of programming the memristors (i.e., writing to non-volatile memory) can be much higher than SRAM or DRAM; thus, typical solutions in this space require that the non-volatile memory to be sufficiently large to hold *all* weights of the DNN model, rather than changing the weights in the memory for each layer or filter during processing.[8] As discussed in Chapter 3, this may reduce flexibility as it can limit the size of the DNN model that the accelerator can support.

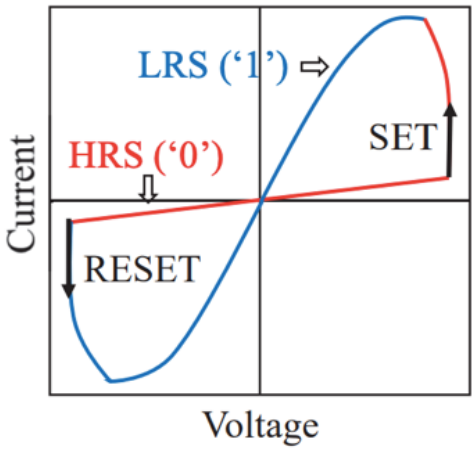
Second, the NVM devices can also suffer from device-to-device and cycle-to-cycle variations with nonlinear conductance across the conductance range [339, 340, 341]. This affects the number of bits that can be stored per device (typically 1 to 4) and the type of signaling used for the input and output activations. For instance,

[7] To improve density, the resistive devices can be inserted between the cross-point of two wires and in certain cases can avoid the need for an access transistor [336]. Under this scenario, the device is commonly referred to as a cross-point element.

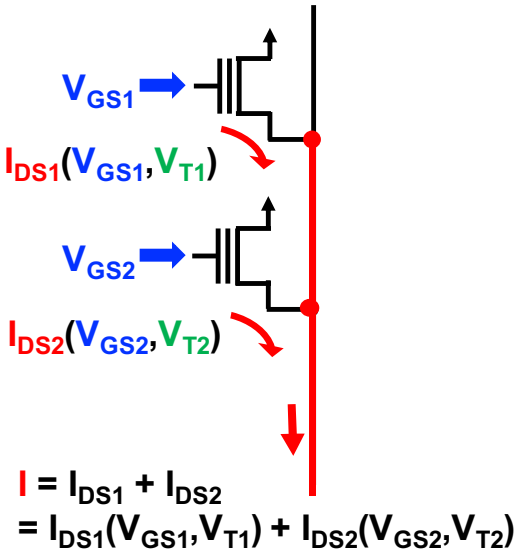
[8] This design choice to hold all weights of the DNN is similar to the approach taken in some of the FPGA designs such as Brainwave [208] and FINN [225], where the weights are pinned on the on-chip memory of the FPGA during synthesis.



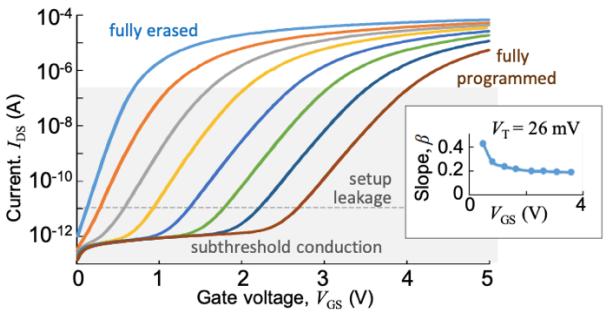
(a) MAC operation using *resistive* NVM devices.



(b) Example I-V curve of a resistive NVM device. (Figure from [337])



(c) MAC operation using *floating gate* NVM devices.



(d) I-V curve of floating gate device.

Figure 10.4: Performing a multiplication and accumulation using the storage element. Input activation is encoded as a voltage amplitude (V_i). (a) For memristors, G_i is the conductance (i.e., 1/resistance) of a resistive device set according to the weight, and bit line current I is the accumulated partial sum value [328]. (b) The current-voltage (I-V) characteristics of the resistive device. The slope of the curve is inversely proportional to the resistance (recall $R = V/I$). Typically, the device can take on just two states: LRS is the low resistive state (also referred to as R_{ON}) and HRS is the high resistive state (also referred to as R_{OFF}).(c) and (d) For floating-gate transistors, the multiplication is performed using its current-voltage (I-V) characteristics, where the weight sets the threshold voltage (as illustrated by the different color lines representing different threshold voltages), and bit line current I is the accumulated partial sum value [338].

rather than encoding the input activation in terms of voltage amplitude, the input can also be encoded in time using pulse width modulation with a *fixed* voltage (i.e., a unary coding), and the resulting current can be accumulated over time on a capacitor to generate the output voltage [342].

Finally, the NVM devices cannot have negative resistance, which presents a challenge for supporting negative weights. One approach is to represent signed weights using differential signaling that requires two storage elements per weight; accordingly, the weights are often stored using two separate arrays [343]. Another approach is to avoid using signed weights. For instance, in the case of binary weights, rather than representing the weights as $[-1, 1]$ and performing binary multiplications, the weights can be represented as $[0, 1]$ and perform XNOR logic operations, as discussed in Chapter 7, or NAND logic operations, as discussed in [344].

There are several popular candidates for NVM devices including phase change RAM (PCRAM), resistive RAM (RRAM or ReRAM), conductive bridge RAM (CBRAM), and spin transfer torque magnetic RAM (STT-MRAM) [345]. These devices have different trade-offs in terms of endurance (i.e., how many times it can be written), retention time (i.e., how often it needs to be refreshed and thus how frequently it needs to be written), write current (i.e., how much power is required to perform a write), area density (i.e., cell size), variations, and speed. An in-depth discussion of how these device properties affect the performance of DNN processing can be found in [340]; Gokmen et al. [342] flips the problem and describes how these devices should be designed such that they can be better suited for DNN processing.[9]

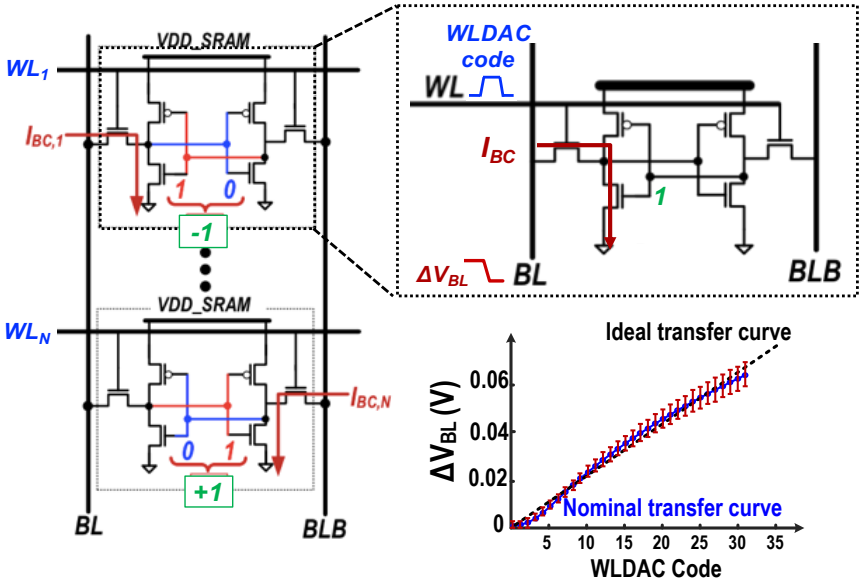
Recent works on NVM-based processing-in-memory accelerators have reported results from both simulation [328, 337, 346, 347] as well as fabricated test chips [348, 343]. While works based on simulation demonstrate functionality on large DNN models such as variants of VGGNet [72] for image classification on ImageNet, works based on fabricated test chips still demonstrate functionality on simple DNN models for digit classification on MNIST [348, 343]. Simulations often project capabilities beyond the current state-of-the-art. For instance, while works based on simulation often assume that all 128 or 256 rows can be activated at the same time, works based on fabricated test chips only activate up to 32 rows at once to account for process variations and limitations in the read out circuits (e.g., ADC); these limitations will be discussed more in Section 10.2.4. It should also be noted that fabricated test chips typically only use one bit per memristor [348, 343, 349].

10.2.2 Static Random Access Memories (SRAM)

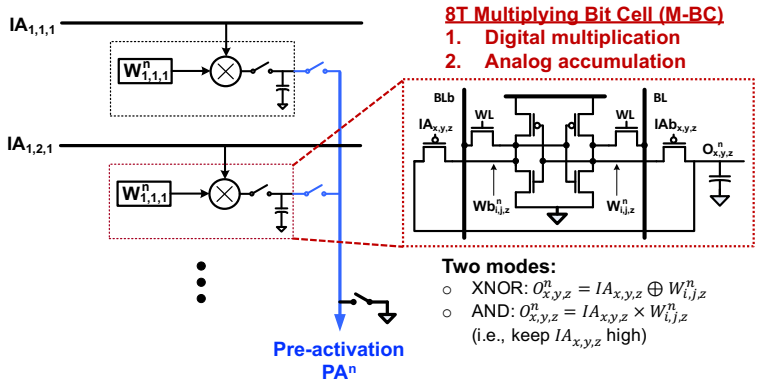
Many recent works have explored the use of the SRAM bit cell to perform computation. They can be loosely classified into current-based and charge-based designs.

Current-based designs use the current-voltage (IV) characteristics of the bit cell to perform a multiplication, which is similar to the NVM current-based approach described in Section 10.2.1. For instance, Figure 10.5(a) shows how the input activation can be encoded as a voltage amplitude on the word line that controls the current through the pull-down network of a bit cell (I_{BC}) resulting in a voltage drop (V_{BL}) proportional to the word line voltage [350]. The current from multiple bit cells (across different rows on the same column) add together on the bit line to perform the accumulation [350]. The resulting voltage drop on the bit line is then proportional to the dot product of the weights and activations of the column.

[9] [340, 342] also describe how these devices might be used for training DNNs if the weights can be updated in parallel and in place within the memristor array.



(a) Multiplication using a 6T SRAM bit-cell and accumulation by current summing on bit lines. (Figure from [350])



(b) Multiplication using a 8T SRAM bit-cell and a local capacitor and accumulation using charge sharing across local capacitors. (Figure from [351])

Figure 10.5: Performing a multiplication and accumulation using the storage element. (a) Multiplication can be performed using a SRAM bit-cell by encoding the input activation as a voltage amplitude on the word line that controls the current through the pull-down network of the bit cell (I_{BC}) resulting in a voltage drop (V_{BL}) proportional to the word line voltage. If a zero (weight value of -1) is stored in the bit cell, the voltage drop occurs on BL, while if a one (weight value of $+1$) is stored the voltage drop occurs on BLB. The current from multiple bit-cells within a column add together. (b) Binary multiplication (XNOR) is performed by connection transistors and local capacitor. Accumulation is performed by charge sharing across local capacitors in bit-cells from the same column.

The above current-based approach is susceptible to the variability and nonlinearity of the word line voltage-to-current relationship of the pull-down network in the bit cell; this create challenges in representing the weights precisely. Charge-based approaches avoid this by using *charge sharing* for the multiplication, where the computation based on the capacitance ratio between capacitors, which tends to be more linear and less sensitive to variations.

Figure 10.5(b) shows how a binary multiplication (i.e., XNOR) via charge sharing can be performed by conditionally charging up a local capacitor within a bit cell, based on the XNOR between the weight value stored in the bit cell and the input activation value that determines the word line voltage [351]. Accumulation can then be performed using charge sharing across the local capacitors of the bit cells on a bit line [351]. Other variants of this approach include performing the multiplication directly with the bit line [352], and charge sharing across different bit lines to perform the accumulation [352, 353, 354].

One particular challenge that exists for SRAM-based processing-in-memory accelerators is maintaining bit cell stability. Specifically, the voltage swing on the bit line typically needs to be kept low in order to avoid a read disturb (i.e., accidentally flipping the value stored in the bit cell when reading). This limits the voltage swing on the bit line, which affects the number of bits that can be accumulated on the bit line for the partial sum; conventional SRAMs only resolve one bit on the bit line. One way to address this is by adding extra transistors to isolate the storage node in the bit cell from the large swing of the bit line [352]; however, this would increase the bit cell area and consequently reduce the overall area density.

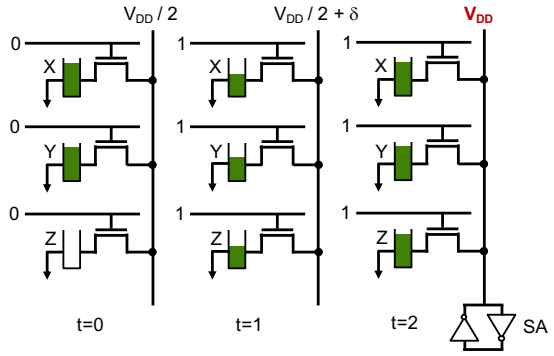
Recent works on SRAM-based processing-in-memory accelerators have reported results from fabricated test chips [350, 351, 352, 353, 354]. In these works, they demonstrate functionality on simple DNN models for digit classification on MNIST, often using layer-by-layer processing, where the weights are updated in the SRAM for each layer. Note that in these works, the layer shapes of the DNN model are often custom designed to fit the array size of the SRAM to increase utilization; this may pose a challenge in terms of flexibility, as discussed in Chapter 3.[10]

10.2.3 Dynamic Random Access Memories (DRAM)

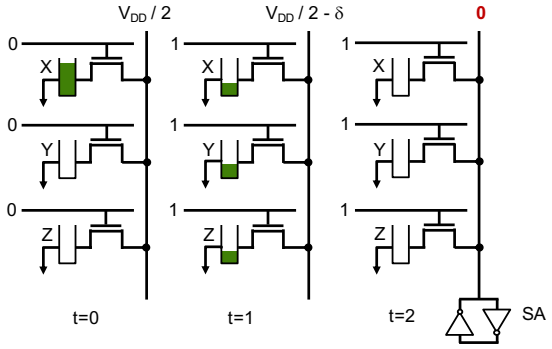
Recent works have explored how processing in memory may be feasible using DRAM by performing bit-wise logic operations when reading multiple bit cells. For instance, Figure 10.6 shows how AND and OR operations can be performed by accessing three rows in parallel [355]. When three rows are accessed at the same time, the output bit line voltage will depend on the average of the charge stored in the capacitors of the bit cells in three rows (note that the charge stored in capacitor of a bit cell depends on if the bit cell is storing a one or zero). Therefore, if the majority of the values of the bit cells are one (at least two out of three), then the output is a one; otherwise, the output is a zero. More precisely, if X, Y, and Z represent the logical values of the three cells, then the final state of the bit line is $XY + YZ + ZX$. If $Z = 1$, then this is effectively an OR operation between X and Y; if $Z = 0$, then this is effectively an AND operation between X and Y. The bit-wise logic operations can be built up into MAC operations across multiple cycles [356], similar to bit-serial processing described in Chapter 7.

It is important to note that the architecture of processing in memory with DRAM differs from the processing in memory with NVM and SRAM (described in Sections 10.2.1 and 10.2.2, respectively) in that: (1) for

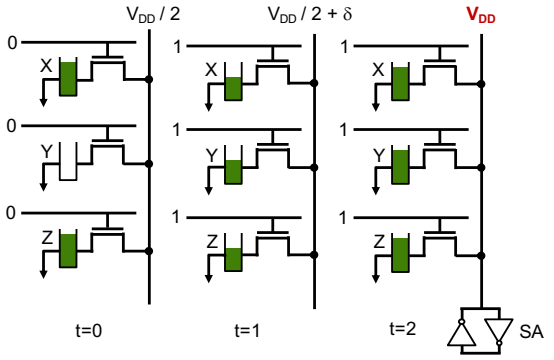
[10] It should be noted that since SRAM is less dense than typical off-chip memory (e.g., DRAM), they are not designed to replace off-chip memory or specifically addressing the "memory wall," which pertains to off-chip memory bandwidth; instead, most SRAM-based processing-in-memory accelerators focus on reducing the on-chip data movement.



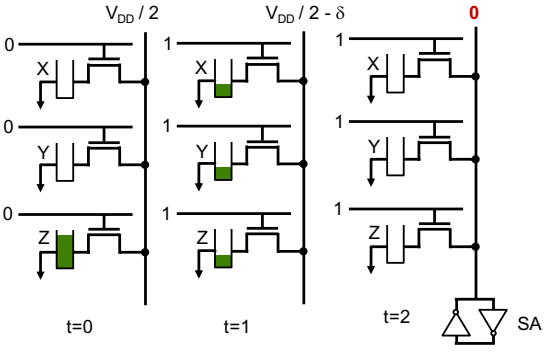
(a) Z=0 and AND (X=1, Y=1) = 1.



(b) Z=0 and AND (X=1, Y=0) = 0.



(c) Z=1 and OR (X=1, Y=0) = 1.



(d) Z=1 and OR (X=0, Y=0) = 0.

Figure 10.6: Compute in DRAM based on charge sharing. Z controls whether an AND or OR is performed on input X and Y. At time $t = 0$, the local capacitor of the bit cells for X, Y and Z are charged to V_{DD} for one and 0 for zero, and the bit line is pre-charged to $V_{DD}/2$. At time $t = 1$, the accessed transistors to the bit cells are enabled, and the capacitors are shorted together with the bit line. Charge sharing distributes the charge between the capacitors to ensure that the voltage across each capacitor is the same; therefore the resulting voltage on the bit line is proportional to the average charge across the three capacitors. If the majority of the capacitors stored at one (i.e., V_{DD}), then the voltage on the bit line would be above $V_{DD}/2$ (i.e., $+\delta$); otherwise, the voltage on the bit line drops below $V_{DD}/2$ (i.e., $-\delta$). At time $t = 2$, the sense amplifiers (SA) on the bit line amplify the voltage to full swing (i.e., $V_{DD}/2+\delta$ becomes V_{DD} or $V_{DD}/2-\delta$ becomes 0), such that the output of the logic function $XY + YZ + ZX$ can be resolved on the bit line. Note that this form of computing is destructive, so we need to copy data beforehand.

DRAM, a bit-wise operation requires three storage elements from different rows, whereas for NVM and SRAM, a MAC operation can be performed with a single storage element; and (2) for DRAM, only one bit-wise operation is performed per bit line and the accumulation occurs over time, whereas for NVM and SRAM, the accumulation of multiple MAC operations is performed on the bit line.[11] As a result, for DRAM the parallel processing can only be enabled across bit lines (A in Figure 10.3), since only one operation can be performed per bit line, whereas for NVM and SRAM, the parallel processing can be enabled across both the bit lines and the word lines (A and B in Figure 10.3), since multiple operations can be performed per bit line. In addition, for DRAM, multiple cycles are required to build up a MAC operation from a bit-wise logic operation, which reduces throughput. Thus, a challenge for DRAM-based processing-in-memory accelerators is to ensure that there is sufficient parallelism across bit lines (A) to achieve the desired improvements in throughput.

Other challenges for DRAM-based processing-in-memory accelerators include variations in the capacitance in the different bit cells, changing charge in capacitor of bit cell over time due to leakage, and detecting small changes in the bit line voltage. In addition, additional hardware may be required in the memory controller to access multiple rows at once and/or to convert the bit-wise logic operations to MAC operation, all of which can contribute to energy and area overhead.

While many of the recent works on DRAM-based processing-in-memory accelerators have been based on simulation [355, 356], it should be noted that performing AND and OR operations have been demonstrated on off-the shelf, unmodified, commercial DRAM [358]. This was achieved by violating the nominal timing specification and activating multiple rows in rapid succession, which leaves multiple rows open simultaneously and enables charge sharing on the bit line.

10.2.4 Design Challenges

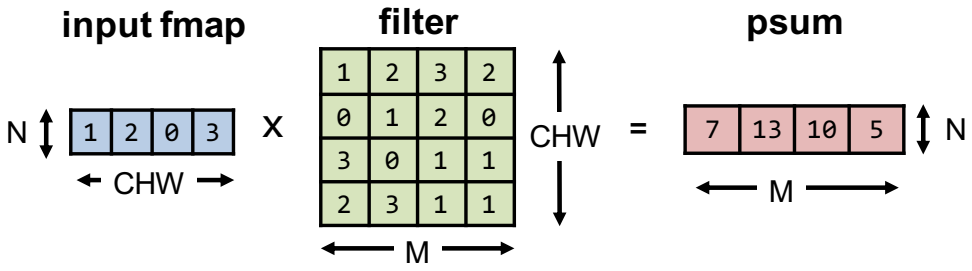
Processing-in-memory accelerators offer many potential benefits including reduced data movement of weights, higher memory bandwidth by reading multiple weights in parallel, higher throughput by performing multiple computations in parallel, and lower input activation delivery cost due to increased density of compute. However, there are several key design challenges and decisions that need to be considered in practice. Analog processing is typically required to bring the computation into the array of storage elements or into its peripheral circuits; therefore the major challenges for processing in memory are its sensitivity to circuit and device non-idealities (i.e., nonlinearity and process, voltage and temperature variations).[12] Solutions to these challenges often require trade offs between energy efficiency, throughput, area density, and accuracy,[13] which reduce the achievable gains over conventional architectures. Architecture-level energy and area estimation tools such as Accelergy can be used to help evaluate some of these trade offs [359].

In this section, when applicable we will use a toy example of a matrix vector multiplication based on a FC layer shown in Figure 10.7. A loop-nest representation of the design is shown in Design 22, where

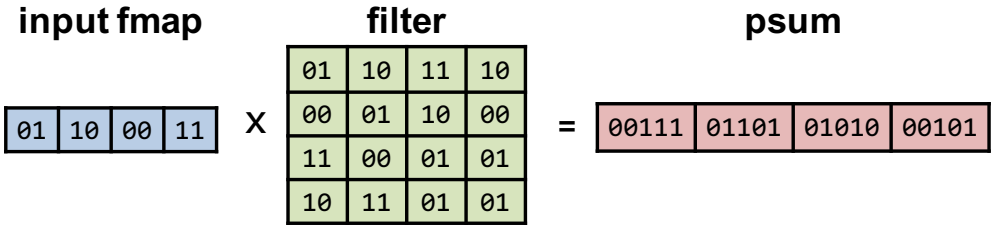
[11] This bit-wise (bit-serial) approach has also been explored for SRAM [357].

[12] Note that per chip training (i.e., different DNN weights per chip instance) may help address nonlinearity and chip to chip variability, but is expensive in practice. In addition, while adapting the weights can help address *static* variability, *dynamic* variability, such as a change in temperature, remains a challenge.

[13] It should be noted that the loss in accuracy might not only be due to the reduced precision of the computations in the DNN model (discussed in Chapter 7), which can be replicated on a conventional processor, but also due to circuit/device non-idealities and limitations, including ADC precision and thermal noise. Unfortunately, these factors have rarely been decoupled during reporting in literature, which can make it difficult to understand the design trade offs.



(a) Decimal



(b) Binary

Figure 10.7: Toy example of matrix vector multiplication for this section. This example uses an FC layer with $N = 1$, $CHW = 4$, and $M = 4$.

Design 22 Toy matrix multiply loop nest

```
i = Array(CHW)          # Input activations
f = Array(CHW, M)       # Filter weights
o = Array(M)            # Output partial sums

parallel-for m in [0, M):
    parallel-for chw in [0, CHW):
        o[m] += i[chw] * f[chw, m]
```

$CHW = M = 4$. In theory, the entire computation should only require one cycle as all the 16 weights can be accessed in parallel and all the 16 MAC operations can be performed in parallel.

Number of Storage Elements per Weight

Ideally, it would be desirable to be able to use one storage element (i.e., one device or bit cell) per weight to maximize density. In practice, multiple storage elements are required per weight due to the limited precision of each device or bit cell (typically on the order of 1 to 4 bits). As a result, multiple low-precision storage elements are used to represent a higher precision weight. Figure 10.8 shows how this applies to our toy example.

For non-volatile memories (e.g., RRAM), multiple storage elements can also be used per weight to reduce the effect of devices variation (e.g., average 3×3 devices per weight [341]) or to represent a signed weight

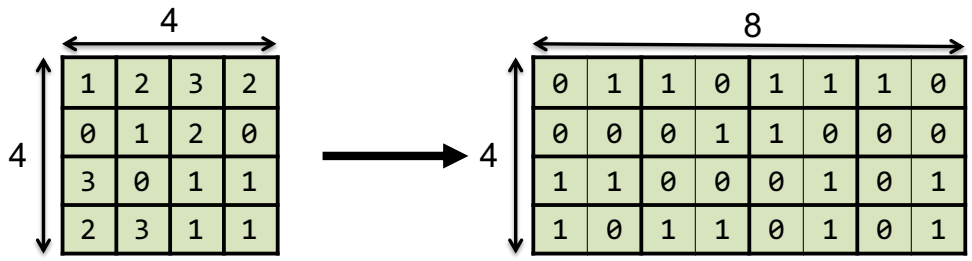


Figure 10.8: Example of multiple storage elements per weight. In our toy example we use 2 bits per weight so the storage cost goes from 4×4 to 4×8.

(i.e., since resistance is naturally non-negative, differential coding using two arrays is often used [341]). Finally, in the case of SRAMs, often additional transistors are required in the bit cell to perform an operation, which increases the area per bit cell. All of the above factors reduce the density and/or accuracy of the system.

Array Size

Ideally, it would be desirable to have a large array size ($A \times B$) in order to allow for high weight read bandwidth and high throughput. In addition, a larger array size improves the area density by further amortizing the cost of the peripheral circuits, which can be significant (e.g., the peripheral circuits, i.e., ADC and DAC, can account for over 50% of the energy consumption of NVM-based designs [328, 348]). In practice, the size of array limited by several factors.

1. The resistance and capacitance of word line and bit line wires, which impacts robustness, speed, and energy consumption.

   For instance, the bit line capacitance impacts robustness for charge domain approaches where charge sharing is used for accumulation, as a large bit line capacitance makes it difficult to sense the charge stored on the local capacitor in the bit cell; the charge stored on the local capacitor can be an input value for DRAM-based designs or a product of weight and input activation for SRAM-based designs. An example of using charge sharing to sense the voltage across a local capacitor is shown in Figure 10.9. Specifically, the change in bit line voltage (ΔV_{BL}) is

   $$\Delta V_{BL} = (V_{DD} - V_{local}) \frac{C_{local}}{C_{local} + C_{BL}} \tag{10.1}$$

   where C_{local} and C_{BL} are the capacitance of the local capacitor and bit line, respectively, and V_{local} is the voltage across the local capacitor (due to the charge stored on the local capacitor), and V_{DD} is the supply voltage. If the local capacitor is only storing binary values, then V_{local} can either be V_{DD} or 0. ΔV_{BL} must be sufficiently large such that we can measure any change in V_{local}; the more bits we want to measure on the bit line (i.e., bits of the partial sum or output activation), the larger the required ΔV_{BL}. However, the size of C_{local} is limited by the area density of the storage element; for instance, in [351], C_{local} is limited to 1.2fF. As a result, the minimum value of ΔV_{BL} limits the size of C_{BL}, which limits the length of the bit line.

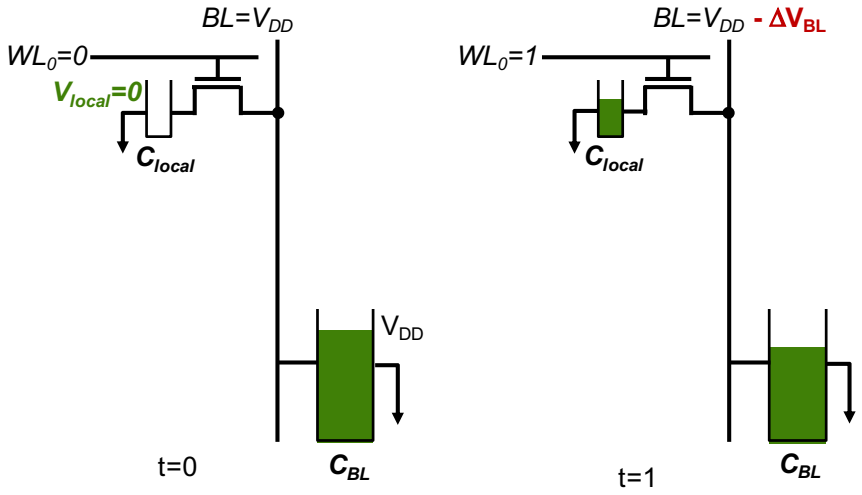


Figure 10.9: Change in bit line voltage ΔV_{BL} is proportional to $\frac{C_{local}}{C_{local}+C_{BL}}$. The bit line is precharged to V_{DD} at $t = 0$, and we read the value on the local capacitor at $t = 1$.

Similarly, the bit line resistance impacts robustness for current domain approaches where current summing is used for accumulation, as a large bit line resistance makes it difficult to sense the change in the resistance in the NVM device, as shown in Figure 10.10. Specifically, the change in bit line voltage due to change on the resistance is

$$\Delta V_{BL} = V_{HIGH} - V_{LOW} = V_{in} R_{BL} \frac{R_{OFF} - R_{ON}}{(R_{ON} + R_{BL})(R_{OFF} + R_{BL})} \tag{10.2}$$

where R_{ON} and R_{OFF} are the minimum and maximum resistance of the NVM device (proportional to the weight), respectively, R_{BL} is the resistance of the bit line, and V_{in} is the input voltage (proportional to the input activation). The $R_{OFF} - R_{ON}$ is limited by the NVM device [341]. As a result, the minimum value of ΔV_{BL} limits the size of R_{BL}, which again limits the length of the bit line.

2. The utilization of the array will drop if the workload cannot fill entire column or entire row, as shown in Figure 10.11(a). If the DNN model has few weights per filter and does not require large dot products, e.g., $C \times H \times W \leq B$, where C, H and W, are the dimensions of the filter (FC layer), and B is the number of rows in the array, then there will be $B - C \times H \times W$ idle rows in the array. If the DNN model has few output channels and does not have many dot products, e.g., $M \leq A$, where M is the number of output channels and A is the number of columns in the array, then there will be $A - M$ idle columns in the array.[14] This becomes more of an issue when processing efficient DNN models, as described in Chapter 9, where the trend is to reduce the number of weights per filter. In digital designs, flexible mapping can be used to increase utilization across different filter shapes, as discussed in Chapter 6; however, this is much more challenging to implement in the analog domain. One option is to redesign the DNN model specifically for processing in memory with larger filters and fewer

[14]Note that if $C \times H \times W > B$ or $M > A$, temporal tiling will need to be applied, as discussed in Chapter 4, and multiple passes (including updating weights in the array) will be required to complete the MAC operations. Furthermore, recall that if the completed sum (final psum) can be computed within a single pass (i.e., $C \times H \times W \leq B$), then precision of the ADC can be reduced to the precision of the output activation. However, when multiple passes are needed, the ADC needs greater precision because the results of each pass need to be added together to form the completed sum; otherwise, there may be an accuracy loss.

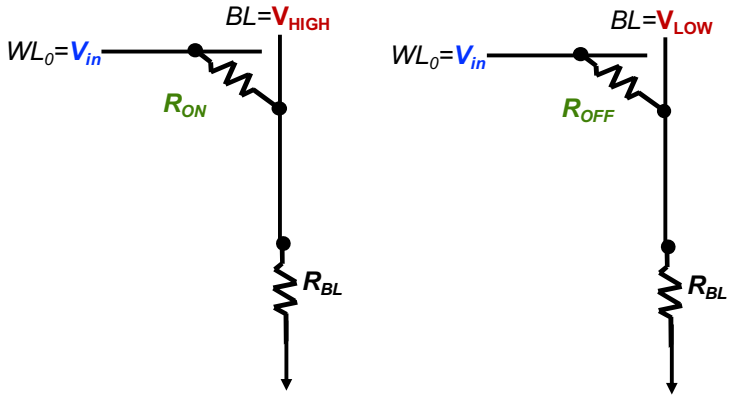


Figure 10.10: Change in bit line voltage $\Delta V_{BL} = V_{HIGH} - V_{LOW}$ is proportional to $R_{BL}\frac{R_{OFF}-R_{ON}}{(R_{ON}+R_{BL})(R_{OFF}+R_{BL})}$. R_{ON} (also referred to as LRS) and R_{OFF} (also referred to as HRS) are the minimum and maximum resistance of the NVM device, respectively.

layers [314], which increases utilization of the array and reduces input activation data movement; however, the accuracy implications of such DNN models requires further study. Figure 10.11(b) shows how this applies to our toy example.

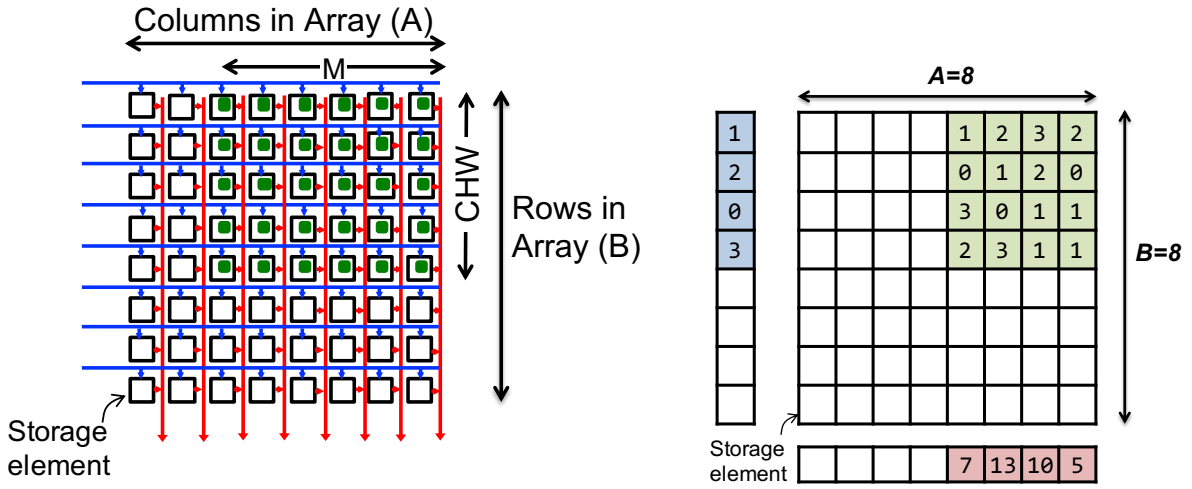
As a result, typical fabricated array sizes range from 16b×64 [352] to 512b×512 [351] for SRAM and from 128×128 to 256×256 [341] for NVM. This limitation in array size affects throughput, area density and energy efficiency. Multiple arrays can be used to scale up the design in order to fit the entire DNN Model and increase throughput [328, 346]. However, the impact on amortizing the peripheral cost is minimal. Furthermore, an additional NoC must be introduced between the arrays. Accordingly, the limitations on energy efficiency and area density remain.

Number of Rows Activated in Parallel

Ideally, it would be desirable to use all rows (B) at once to maximize parallelism for high bandwidth and high throughput. In practice, the number of rows that can be used at once is limited to by several factors.

1. The number of bits in the ADC, since more rows means more bits are required to resolve the accumulation (i.e., the partial sums will have more bits). Some works propose using fewer bits for ADC than the maximum required [360, 361], however, this can reduce the accuracy.[15]
2. The cumulative effect of the device variations can decrease the accuracy.

[15]The number of bits required by the ADC depends on the number of values being accumulated on the bit line (i.e., number of rows activated in parallel), whether the values are sparse [360] (i.e., zero values will not contribute to the accumulated sum), and whether the accumulated sum is a partial sum or a fully accumulated sum (i.e., it only needs to go through a nonlinear function to become an output activation). Using less than the maximum required ADC bits for the fully accumulated sum has less impact on accuracy than on the partial sum, since the fully accumulated sum is typically quantized to the bit-width of the input activation for the next layer, as discussed in Chapter 7. However, the ability to fully accumulate the sum on a bit line depends on the whether the number of rows in the array is large enough to hold all the weights for a given filter (i.e., $B \geq C \times H \times W$).



(a) Workload size versus array size

(b) Toy Example

Figure 10.11: Array utilization. (a) Impact of array size on utilization. (b) Example of utilization if size of weight memory was 8×8. Even though in theory we should be able to perform 64 MAC operations in parallel, only 16 of the storage elements are used (utilization of 25%); as a result, only 16 MAC operations are performed in parallel, specifically, 4 dot products of 4 elements.

3. The maximum voltage drop or accumulated current that can be tolerated by the bit line.[16] This can be particularly challenging for advanced process technologies (e.g., 7 nm and below) due to the increase in bit line resistance and increased susceptibility to electromigration issues, which limits the maximum current on the bit line.

As a result, the typical number of rows activated in parallel is 64 [341] or below [343]. A digital accumulator can be used after each ADC to accumulate across all B rows in B/64 cycles [341]; however, this reduces throughput and increases energy due to multiple ADC conversions. To reduce the additional ADC conversion, recent work has explored performing the accumulation in the analog domain [347]. Figure 10.12 shows how this applies to our toy example. Design 23 shows the corresponding loop nest, and illustrates the multiple cycles it takes to perform all the MACs.

Number of Columns Activated in Parallel

Ideally, it would be desirable to use all columns (A) at once to maximize parallelism for high bandwidth and high throughput. In practice, the number of columns that can be used are limited by whether the area of ADC can pitch-match the width of the column, which is required for a compact area design; this can be challenging when using high-density storage elements such as NVM devices. A common solution is to time multiplex the ADC across a set of eight columns, which means that only A/8 columns are used in parallel [341]; however, this reduces throughput. Figure 10.13 shows how this applies to our toy example, and Design 24 shows the corresponding loop nest.

[16] For instance, for a 6T SRAM bit cell, a large voltage drop on the bit line can cause the bit cell to flip (i.e, an unwanted write operation on the bit cell); using 8T bit cell can prevent this at the cost of increased area.

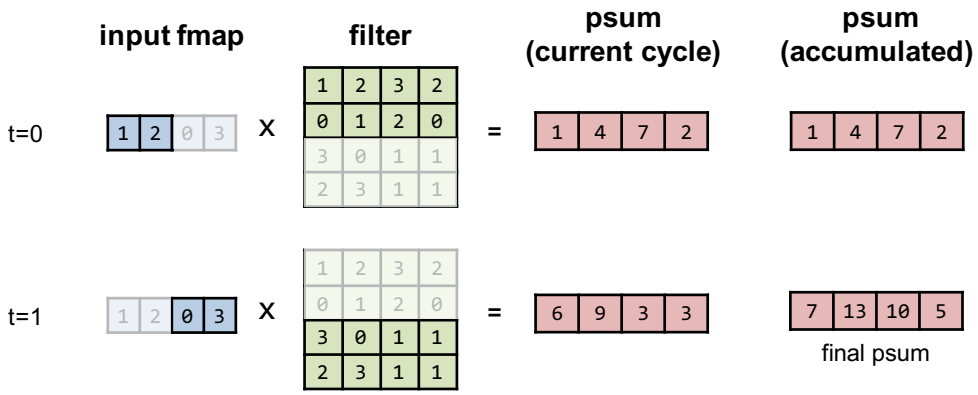


Figure 10.12: Example of limited number of rows activated in parallel. If the ADC is only 3-bits, only two rows can be used at a time. It would take two cycles (time steps) to complete the computation. There are two columns for psum in the figure: (1) psum (current cycle) corresponds to psum resulting from the dot product computed at the current cycle; (2) psum (accumulated) corresponds to the accumulated value of the psums across cycles. At $t = 1$, the psum of [6, 9, 3, 3] is computed and added (e.g., with a digital adder) to the psum at $t = 0$ of [1, 4, 7, 2] to achieve the final psum [7, 13, 10, 5], as shown in the figure.

Design 23 Toy matrix multiply loop nest with limited number of parallel active rows

```
i = Array(CHW)          # Input activations
f = Array(CHW, M)       # Filter weights
o = Array(M)            # Output partial sums

parallel-for m in [0, M):
    parallel-for chw1 in [0, CHW/2):
        for chw0 in [0, 2):
            chw = chw1*2 + chw0
            o[m] += i[chw] * f[chw, m]
```

Design 24 Toy matrix multiply loop nest with limited number of parallel active columns

```
i = Array(CHW)          # Input activations
f = Array(CHW, M)       # Filter weights
o = Array(CHW)          # Output partial sums

parallel-for m1 in [0, M/2):
    parallel-for chw in [0, CHW):
        for m0 in [0, 2):
            m = m1*2 + m0
            o[m] += i[chw] * f[chw, m]
```

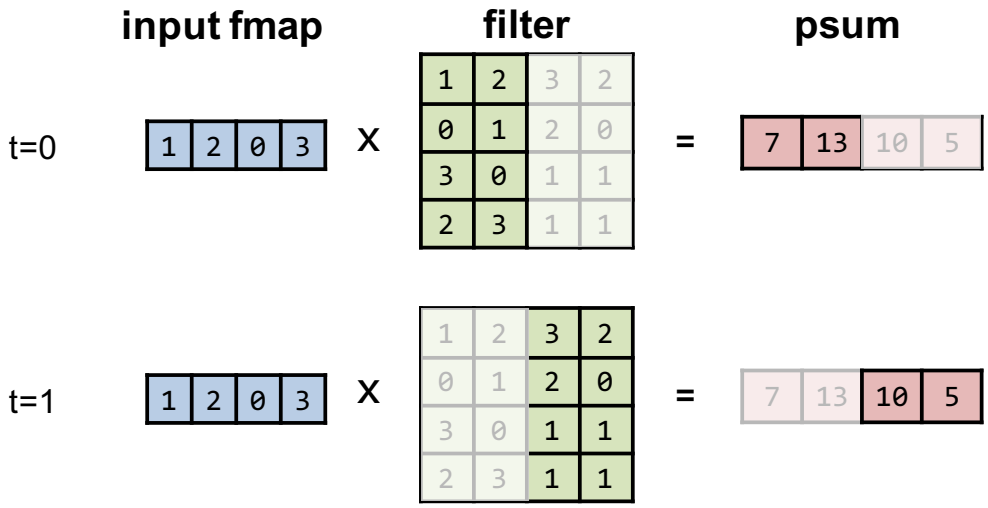


Figure 10.13: Example of limited number of columns activated in parallel. If the width of an ADC is equal to two columns, then the columns need to be time multiplexed. It would take two cycles to complete the computation. If we combined this with the previously described parallel row limitations, it would take four cycles to complete the computation.

Time to Deliver Input

Ideally, it would be desirable for all bits in the input activations to be encoded onto the word line in the minimum amount of time to maximize throughput; a typical approach is to use voltage amplitude modulation [350]. In practice, this can be challenging due to

1. the nonlinearity of devices makes encoding input value using voltage amplitude modulation difficult, and
2. the complexity of the DAC that drives the word line scales with the number of bits

As a result, the input activations are often encoded in time (e.g., pulse-width modulation [353, 354] or number of pulses [361][17]), with a fixed voltage (DAC is only 1-bit) where the partial sum is determined by accumulating charge over time; however, this reduces throughput.[18] Figure 10.14 shows how this applies to our toy example. One approach to reduce the complexity of the DAC or current accumulation time is to reduced the precision of the input activations, as discussed in Chapter 7; however, this will also reduce accuracy.

[17] Using pulses increases robustness to nonlinearity at the cost of increased switching activity.

[18] Alternatively, a single pulse can be used for the input activations if the weights are replicated across multiple rows (e.g., 2^{N-1} rows for an N-bit activation) [332]. This is a trade-off between time and area.

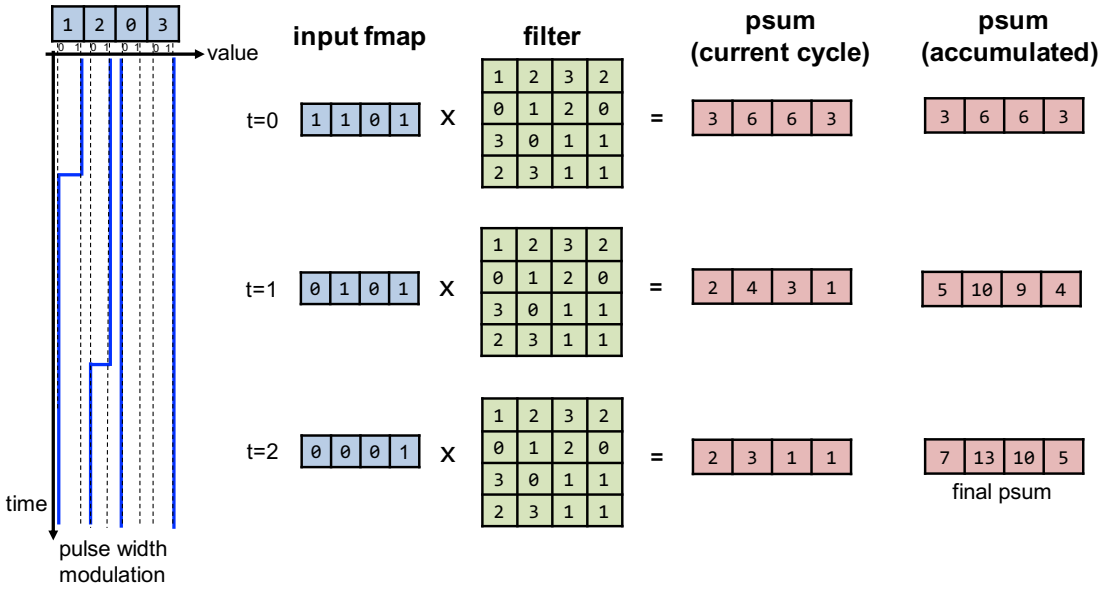


Figure 10.14: Example of performing pulse-width modulation of the input activations with a 1-bit DAC. It would take three cycles to complete the computation if all weights can be used at once. Specifically, the input activations would be signaled across time as $[1, 1, 0, 1] + [0, 1, 0, 1] + [0, 0, 0, 1] = [1, 2, 0, 3]$, where the width of the pulse in time corresponds to the value of the input. There are two columns for psum in the figure: (1) psum (current cycle) corresponds to psum resulting from the dot product computed at the current cycle; (2) psum (accumulated) corresponds to the accumulated value of the psums across cycles. Note that if we combined the limitation illustrated in this figure with the previously described parallel row and columns limitations, it would take 12 cycles to complete the computation.

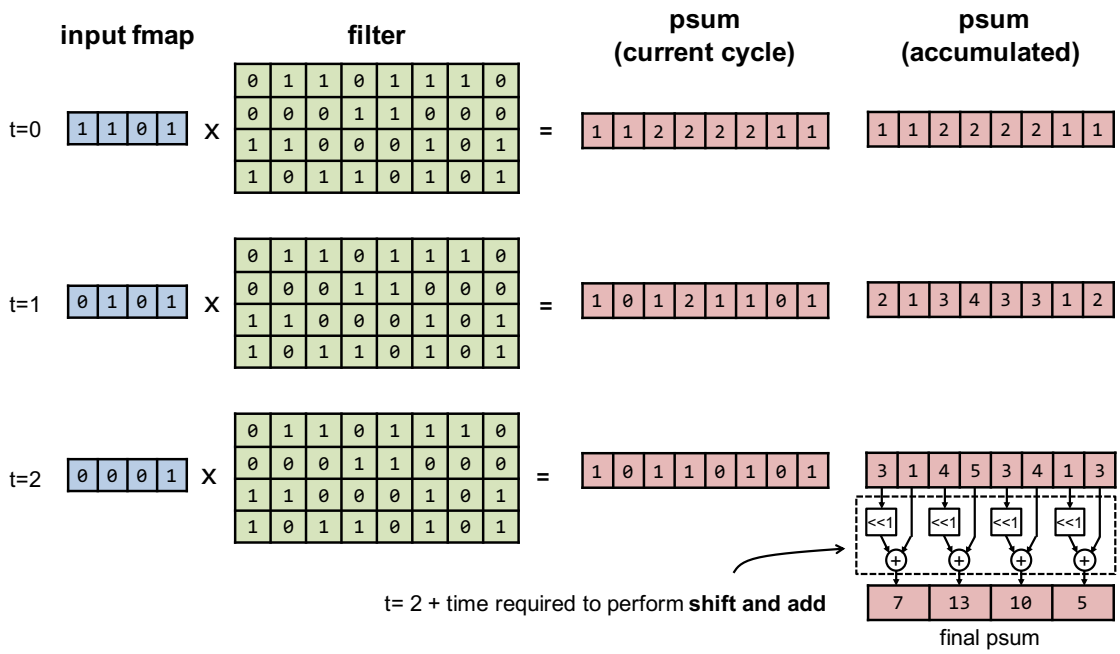


Figure 10.15: Example of time to compute MAC operation if each storage element can only perform one-bit operations. It takes three cycles to deliver the input (similar to Figure 10.14). There are two columns for psum in the figure: (1) psum (current cycle) corresponds to psum resulting from the dot product computed at the current cycle; (2) psum (accumulated) corresponds to the accumulated value of the psums across cycles. In addition, extra cycles are required at the end to combine accumulated bits from each bit line to form the final output sum. The number of cycles required to perform the shift and add would depend on the number of bit lines divide by the number of sets of shift-and-add logic.

Time to Compute a MAC

Ideally, it would be desirable for a MAC to be computed in a single cycle. In practice, the storage element (bit cell or device) typically can only perform one-bit operations (e.g., XNOR and AND), and thus multiple cycles are required to build up to a multi-bit operation (e.g., full adder and multiplication) [330]. Figure 10.15 shows how this applies to our toy example. This also requires additional logic after the ADC to combine the one-bit operations into a multi-bit operation. However, this will reduce both the throughput, energy and density.

10.3 Processing in Sensor

In certain applications, such as image processing, the data movement from the sensor itself can account for a significant portion of the overall energy consumption. Accordingly, there has been work on bringing the processing near or into the sensor, which is similar to the work on bringing the processing near or into memory discussed in the previous sections. In both cases, the goal is to reduce the amount of data read out of the memory/sensor and thus the number of ADC conversions, which can be expensive. Both cases also

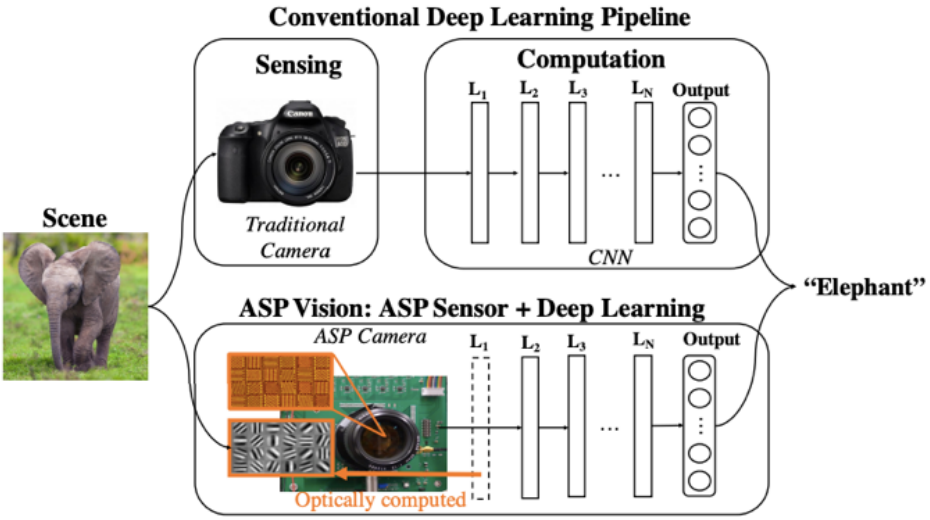


Figure 10.16: Use ASP in front end to perform processing of first layer (Figure from [366])

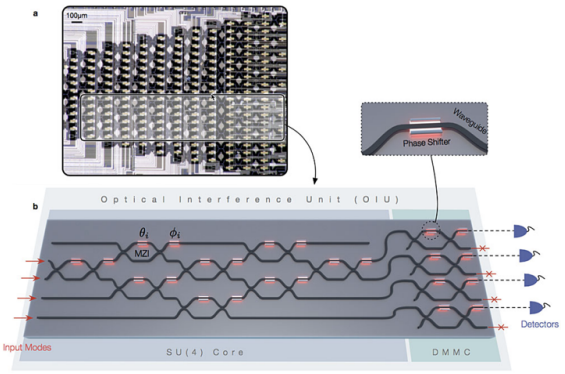
require moving the computation into the analog domain and consequently suffer from increased sensitivity to circuit non-idealities. While processing near memory and processing in memory focus on reducing data movement of the weights of the DNN model, processing near sensor and processing in sensor focus on reducing the data movement of the inputs to the DNN model.

Processing near sensor has been demonstrated for image processing applications, where computation can be performed in the analog domain before the ADC in the peripheral of the image sensor. For instance, Zhang et al. [362] and Lee et al. [363] use switched capacitors to perform 4-bit multiplications and 3-bit by 6-bit MAC operations, respectively. RedEye [364] proposes performing the entire convolution layer (including convolution, max pooling and quantization) in the analog domain before the ADC. It should be noted that the results in [364] are based on simulations, while [362, 363] report measurements from fabricated test chips.

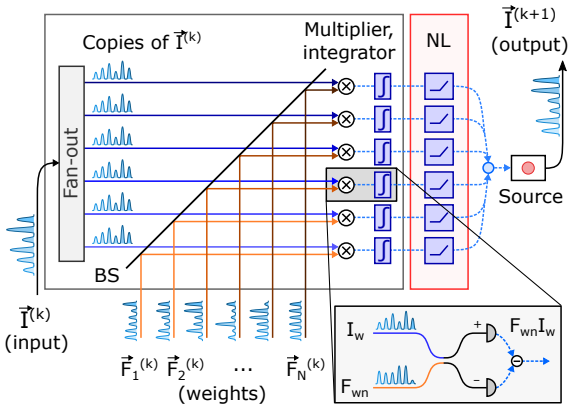
It is also feasible to embed the computation not just before the ADC, but directly into the sensor itself (i.e., processing in sensor). For instance, in [365] an Angle Sensitive Pixels sensor is used to compute the gradient of the input, which along with compression, reduces the data movement from the sensor by 10×. In addition, since the first layer of the DNN often outputs a gradient-like feature map, it may be possible to skip the computations in the first layer, which further reduces energy consumption, as discussed in [366, 367].

10.4 Processing in the Optical Domain

Processing in the optical domain is an area of research that is currently being explored as an alternative to all-electronic accelerators [368]. It is motivated, in part, by the fact that photons travel much faster than electrons, and the cost of moving a photon can be *independent* of distance. Furthermore, multiplication can be performed passively (for example with optical interference [369, 370], with reconfigurable filters [371],



(a) Optical neural network using optical interference units. (Figure from [369])



(b) Optical neural network using coherent detection. BS: beamsplitter; NL: nonlinearity. (Figure from [370])

Figure 10.17: Optical neural networks

or static phase masks [372]) and detection can occur at over 100 GHz. Thus, processing in the optical domain may provide significant improvements in energy efficiency and throughput over the electrical domain.

Much of the recent work in the optical computing has focused on performing matrix multiplication, which can be used for DNN processing; these works are often referred to as photonic accelerators or *optical neural networks*. For instance, Shen et al. [369] present a programmable nanophotonic processor where the input activations are encoded in the amplitudes of optical pulses (light) that travel through an array of on-chip interferometers (composed of beamsplitters) that represent the weight matrix, where the weights determine the amount of light that is passed to the output. This is effectively a weight-stationary dataflow. The accumulation is performed based on the accumulated light from various waveguides at the photodetector.

Alternatively, Hamerly et al. [370], shown in Figure 10.17(b), demonstrate matrix multiplication based on coherent detection, where both the weights and activations are encoded on-the-fly into light pulses, and are interfered in free-space on a beamsplitter to perform multiplication. Since, in this scheme, there is no need for on-chip interferometers (which have a large footprint), this approach may be more scalable, at the cost of added complexity in alignment. This is effectively an output-stationary dataflow, where the output is accumulated on the photodetector as an analog electronic signal.

There is negligible power loss in the computation when processing in the optical domain. Most of the power dissipation occurs when converting between electrical and optical domains, specifically, in the converter to generate the light and the detector to collect the photons. Therefore, similar to the processing in memory work, the larger the array (or in this case the matrix), the more these conversion costs can be amortized.

Note, however, that while computing in the optical domain may be energy efficient, the non-idealities in the optical devices (e.g., crosstalk between detectors, errors in phase encoding, photodetection noise) can lead to a reduction in accuracy. To address this accuracy loss, Bernstein et al. [373] propose a hybrid electronic-optics approach where the data transfer is done in the optical domain to exploit the distance-independent cost of photons, while the computation itself (i.e., MAC operation) is performed digitally in the electrical domain to avoid the non-idealities of the optical devices.

Recent works on optical neural networks have reported results based on simulations [370] or simulations

based on data that has been extrapolated from experimental results [369]. These works demonstrate functionality on simple DNN models for digit classification and vowel recognition.

Chapter 11

Conclusion

The use of deep neural networks (DNNs) has recently seen explosive growth. They are currently widely used for many artificial intelligence (AI) applications including computer vision, speech recognition, and robotics and are often delivering better than human accuracy. However, while DNNs can deliver this outstanding accuracy, it comes at the cost of high computational complexity. With the stagnation of improvements in general-purpose computation [10], there is a movement toward more domain-specific hardware, and in particular for DNN processing. Consequently, techniques that enable efficient processing of DNNs to improve *energy-efficiency* and *throughput* without sacrificing *accuracy* with cost-effective hardware are critical to expanding the deployment of DNNs in both existing and new domains.

Creating a system for efficient DNN processing should begin with understanding the current and future applications and the specific computations required for both now and the potential evolution of those computations. Therefore, this book surveyed a number of the current applications, focusing on computer vision applications, the associated algorithms, and the data being used to drive the algorithms. These applications, algorithms, and input data are experiencing rapid change. So extrapolating these trends to determine the degree of flexibility desired to handle next generation computations becomes an important ingredient of any design project.

During the design-space exploration process, it is critical to understand and balance the important system metrics. For DNN computation these include the accuracy, energy, throughput and hardware cost. Evaluating these metrics is, of course, key, so this book surveyed the important components of a DNN workload. In specific, a DNN workload has two major components. First, the workload consists of the "network architecture" of the DNN model including the "shape" of each layer and the interconnections between layers. These can vary both within and between applications. Second, the workload consists of the specific data input to the DNN. This data will vary with the input set used for training or the data input during operation for inference.

This book also surveyed a number of avenues that prior work have taken to optimize DNN processing. Since data movement dominates energy consumption, a primary focus of some recent research has been to reduce data movement while maintaining accuracy, throughput, and cost. This means selecting architectures with favorable memory hierarchies like a spatial array, and developing dataflows that increase data reuse at the low-cost levels of the memory hierarchy. We have included a taxonomy of dataflows and an analysis of their characteristics. Understanding the throughput and energy efficiency of a DNN accelerator depends upon

how each DNN workload maps to the hardware. Therefore, we discussed the process of optimally mapping workloads to the accelerator and the associated throughput and energy models.

The DNN domain also affords an excellent opportunity for hardware/algorithm co-design. Many works have aimed to save storage space and energy by changing the representation of data values in the DNN. We distill and present the key concepts from these approaches. Still other work saves energy and sometimes increases throughput by increasing and then exploiting sparsity of weights and/or activations. We presented a new abstract data representation that enables a systematic presentation of designs focused on exploiting sparsity. Co-design needs to be aware of the impact on accuracy. Therefore, to avoid losing accuracy it is often useful to modify the network or fine-tune the network's weights to accommodate these changes. Thus, this book both reviewed a variety of these techniques and discussed the frameworks that are available for describing, running and training networks.

Finally, DNNs afford the opportunity to use mixed-signal circuit design and advanced technologies to improve efficiency. These include using memristors for analog computation and 3-D stacked memory. Advanced technologies can also facilitate moving computation closer to the source by embedding computation near or within the sensor and the memories. Of course, all of these techniques should also be considered in combination, while being careful to understand their interactions and looking for opportunities for joint hardware/algorithm co-optimization.

In conclusion, although much work has been done, DNNs remain an important area of research with many promising applications and opportunities for innovation at various levels of hardware design. We hope this book provides a structured way of navigating the complex space of DNN accelerators designs that will inspire and lead to new advances in the field.

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