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EGO BALLOON EXPERIMENT
DATA PROCESSOR

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GODDARD SPACE FLIGHT CENTER
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EGO BALLOON EXPERIMENT

DATA PROCESSOR

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EGO BALLOON EXPERIMENT DATA PROCESSOR

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I. INTRODUCTION

The EGO balloon experiment data processor (Figure 1) is designed to operate on prelaunch data for the EGO series satellites: specifically, experiments Mark II, Mark III, and Mark IV. These experiments, carried by balloon flights into the upper atmosphere, provide experimental data concerning identification of particles and measurement of their energies which are recorded on magnetic tape (Figure 2). Upon retrieval of the recorded tapes, the EGO data processor serves as a quick-look facility in the field by processing samplings of the data throughout each tape, converting each sampling to decimal form for both decimal display and decimal printout.

Input signals to the EGO data processor are the reproduce-amplifier signals from the tape transport. The processor detects the signals of each channel, assembles the information, and by digital techniques converts the data when the data point is logically determined to be of value to the experimenter or the field technician. The data formats processible by the unit, for similar experiments, are made programmable by a patch panel, which also controls selection or rejection of a data point. The unit is designed to tolerate transport skew, transport speed variation, signal noise, and signal amplitude variation. A simulation mode for rapid checkout in the field is incorporated in the processor.

auth,
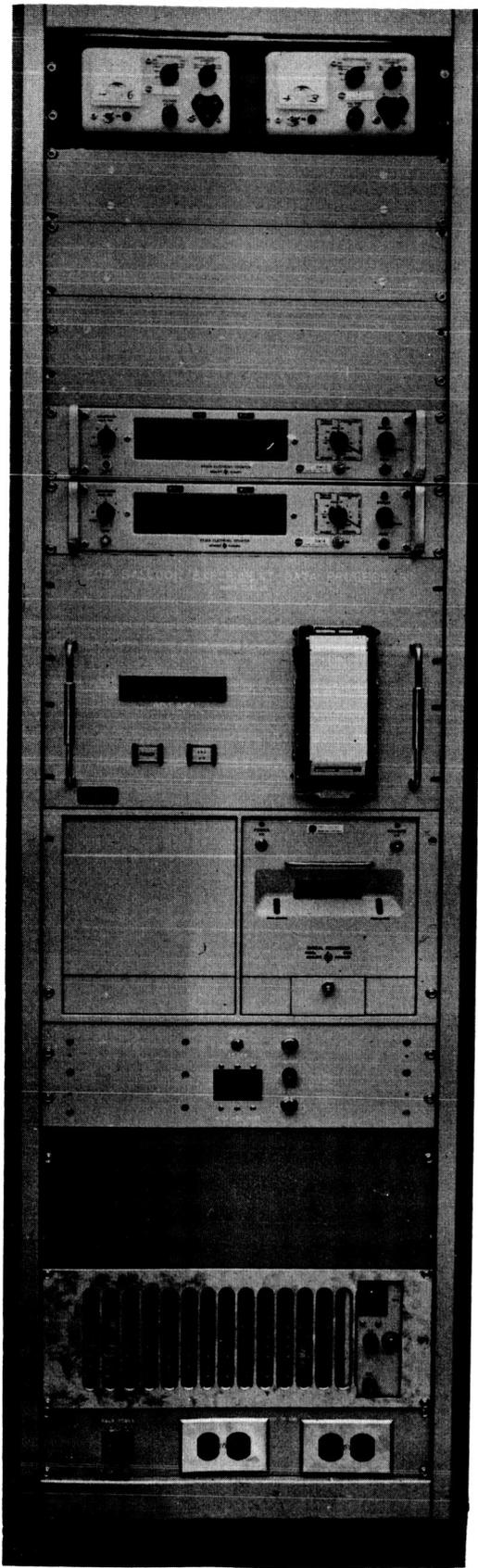
Figure 1—EGO Data Processor,
Overall Unit
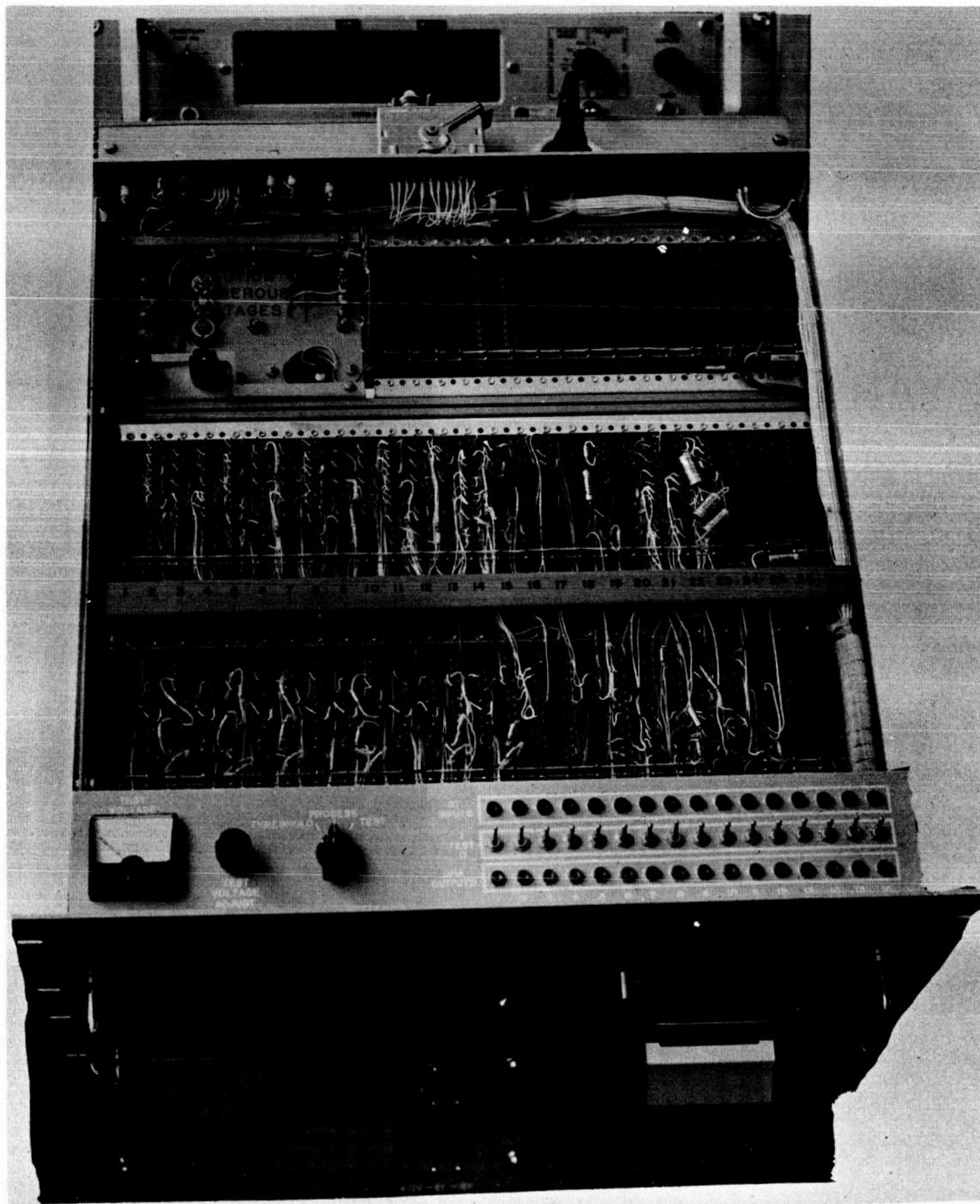
Figure 2—Pull-out View of Arithmetic Unit

II. SPECIFICATIONS

SYSTEM INPUTS:

Parallel binary data entered on 16 separate data lines

Experiment data events:

> Events occur asynchronous with time.
> For Mark II and Mark III, one event consists of one entry of 16 bits in parallel.
> For Mark IV, one event consists of the entry of two groups of 16 bits in parallel.

Index and ID timing:

> Presence of a data word is indicated by an index marker on any specified line.
> The first part of the event of Mark IV is indicated by the presence of an index marker plus an identification (ID) marker.
> The second part of the event of Mark IV is indicated by an index marker that has been preceded in the first part of the event by a time greater than 0.8 millisecond but less than 1.2 msec, and the absence of an ID marker.

Index and ID pulse:

> Pulsed-negative excursion from the dc level of the steady-state signal
> The magnitude of the excursion must be between -1 and -10 volts.

Binary one:

> Pulsed-negative excursion from the dc level of the steady-state signal occurring in coincidence with an index marker
> The magnitude of the excursion must be between -1 volt and -10 volts.

Binary zero:

> Absence of a negative excursion from the steady-state signal when the index marker is present

Repetition rate:

> Asynchronous, between 0 cps and 1000 cps

Maximum skew:

> ±108 degrees of the maximum repetition rate (1000 cps) cycle, referenced to the index marker

Maximum speed variation:

> ±10 percent of nominal speed

Input impedance:

Input threshold level:	Impedance:
-1.0 volt	5,000 ohms minimum
-2.0 volts	10,000 ohms minimum

Data line input:

24-pin Amphenol connector

SYSTEM OUTPUTS:

- Decimal display by Nixie tubes
- Decimal printout

    Maximum printout rate is 5 prints per second.

POWER REQUIREMENTS:

105 to 125 volts ac; 58 to 62 cycles per second; 600 watts maximum

TEMPERATURE RANGE:

0°C to 50°C

DIMENSIONS:

Panel height:

System requires 37-1/4 inches of panel height.

Maximum depth:

21-3/4 inches

Maximum width:

19-1/4 inches

Weight:

135 lb.

MOUNTING:

All units are mountable in a standard 19-inch relay rack. The main unit, containing the 3-C modules, is provided with chassis-track slides for accessibility.

OPERATING CONTROLS:

- Programmable patch panel on front panel
- Normal operating controls on front panel
- Simulation and system calibration controls are mounted on the rear of the front panel of the arithmetic unit.

III. DATA FORMAT

MARK II AND MARK III

The Mark II and Mark III EGO balloon experiment presents asynchronous parallel binary data entered on 16 separate data lines. The parallel 16-bit entry is subdivided into two 7-bit words, an identification bit (C), and an index bit that indicates the presence of the parallel data. One 16-bit parallel entry consitutes an event[1]. The format is shown in Table 1. The subscript indicates the relative significance of the binary bit.

Table 1
Mark II and Mark III Format

Track Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Word I	A_0	A_1	A_2	A_3	A_4	A_5	A_6	B_0	B_1	B_2	B_3	B_4	B_5	B_6	C	Index

MARK IV

The Mark IV EGO balloon experiment presents asynchronous parallel binary data entered on 16 separate data lines, an event consisting of two 16-bit words. One event is composed of 28 data bits, two ID bits, and two index bits. The event is multiplexed in the form of two words, Word I and II; Word II follows Word I by a fixed time interval. Words I and II are subdivided into three 9-bit words plus a sensitivity bit. The other four positions are used to indicate the presence of a word and to differentiate between Word I and Word II. An index bit appears each time a word is present; when an ID bit is present, it indicates that the word is Word I. The absence of an ID bit when a word is present indicates that the word is Word II. The format is shown in Table 2.

Table 2
Mark IV Format

Track Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Word I	A_0	A_1	A_2	A_3	A_4	A_5	A_6	ID	Index	A_7	A_8	C_0	C_1	C_2	C_3	C_4
Word II	B_0	B_1	B_2	B_3	B_4	B_5	B_6	$\overline{ID}$	Index	B_7	B_8	C_5	C_6	C_7	C_8	Sens.

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[1]An event is one set of experimental measurements, constituting one data point.

IV. OPERATING INSTRUCTIONS [1]

CABLE CONNECTIONS:

Rear connections:

All rear connections should be made with the power turned off.

Connect the six-pin dc power cable from the Computer Control Company power-supply unit to the data-processor unit.

Connect the ac power cable to a 117-volt 60-cycle source.

Connect the tape-reproduce amplifiers to the 24-pin Amphenol connector (C-1) of the data processor unit.

Connect the 14-pin Amphenol connector (C-2) from the data-processor unit to the printer.

Connect the 50-pin Amphenol connector (C-5) from the printer to counter "A".

Connect the 50-pin Amphenol connector (C-6) from the printer to counter "B".

OPERATING PROCEDURE:

Turn on all power.

Set the commercial counter-selector switches to START of the MANUAL mode.

Set the commercial counter SENSITIVITY controls to "3".

Throw toggle switch on rear of printer to the EGO position.

Set main unit THRESHOLD – PROCESS – TEST switch to the PROCESS position.

(A) Insert the programmable patch panel for Mark II, and Mark III.

(B) Insert the programmable patch panel for the Mark IV experiment.

(A) Set the mode control to either $AB\overline{C}$ or AB. ($AB\overline{C}$ is the mode in which data will be processed only if C is an "0"; AB is the mode in which data will be processed regardless of the state of C.)

(B) This control is inoperative for the Mark IV mode of operation.

Throw printer RECORD switch to ON.

TEST PROCEDURE:

Set the commercial counters and printer for normal EGO operation as given in the operating instructions. Do not set main unit THRESHOLD – PROCESS – TEST switch to the PROCESS position.

Set the THRESHOLD – PROCESS – TEST control to the THRESHOLD position.

Adjust the meter to read the desired threshold voltage by varying the TEST VOLTAGE ADJUST control. The voltage is normally set for 2 volts for best noise immunity. If all the indicator lights on the front panel do not light, refer to the Calibration Section for threshold level adjustment.

Set the THRESHOLD – PROCESS – TEST control to the TEST position.

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[1]Paragraphs with an "A" refer to Mark II and Mark III. Paragraphs with a "B" refer to Mark IV. Paragraphs without an "A" or a "B" refer to all three, Mark II, Mark III, and Mark IV.

(A) Throw the toggle switch in the index track (track 16) to the "1" position. Place all other toggle switches in the "0" position.

(B) When testing for Mark IV, the ID channel (track 8) toggle switch must be thrown to the "1" position in addition to throwing the index track (channel 9) to the "1" position.

Throw each switch, in a chronological order, to the "1" position for 5 seconds and then to the "0" position. The appropriate front panel lamp should light for the time the switch is in the "1" position, and the digital printout should read as follows:

Table 3
Mark II – III Printout

Switch number in the "1" position (all others in the "0" position except the index track)	Digital Printout		
	Word A	Word B	Word C
1	001	000	0
2	002	000	0
3	004	000	0
4	008	000	0
5	016	000	0
6	032	000	0
7	064	000	0
8	000	001	0
9	000	002	0
10	000	004	0
11	000	008	0
12	000	016	0
13	000	032	0
14	000	064	0
15	000	000	1[2]
16 (index track ON AT ALL TIMES)	000	000	0

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[2]This figure will not print if the front panel control is set for the $\overline{ABC}$ mode.

Table 4
Mark IV Simulation Printout

Switch number in the "1" position (all others in the "0" position except index channel (9) and ID channel (8))	Word A	Word B	Word C	Sens.
1	001	001	000	0
2	002	002	000	0
3	004	004	000	0
4	008	008	000	0
5	016	016	000	0
6	032	032	000	0
7	064	064	000	0
10	128	128	000	0
11	256	256	000	0
12	000	000	033	0
13	000	000	066	0
14	000	000	132	0
15	000	000	264	0
16	000	000	016	1

CALIBRATION:

Threshold level adjustment

The THRESHOLD – PROCESS – TEST control must be in the THRESHOLD position to make this adjustment. Each level-detector threshold can be adjusted by varying a potentiometer[3] that will light a front-panel indicator.

The TEST VOLTAGE meter should be set by varying the TEST VOLTAGE ADJUST control for the desired threshold voltage (2 volts usually give the best noise immunity).

The potentiometer[4] on the module associated with the indicator should then be set so that the indicator light is just beyond the threshold of being turned on. This is accomplished by turning the module potentiometer counterclockwise (CCW) until the appropriate indicator light turns on, then backing off clockwise (CW) on the potentiometer until the light extinguishes. When the potentiometer is in this position, it should be turned slowly CCW until the light just turns on. The potentiometer is now at the optimum setting.

Adjustment of the temporary memories (DMA's)

The THRESHOLD – PROCESS – TEST control must be in the TEST position and the toggle switch of the track being adjusted must be in the "1" position.

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[3]Refer to Figure 17 in the section containing diagrams, for appropriate potentiometer adjustment.
[4]Refer to Figure 17 for appropriate potentiometer adjustment.

The output of each temporary memory can be monitored by an oscilloscope connected to the appropriate DMA OUTPUT pin jack on the rear of the front panel. The duration of each temporary memory (DMA), with the exception of the index bit, is set for 0.6 millisecond by adjusting a potentiometer on the appropriate module.[4] The maximum duty cycle of these modules is 67 percent. For a maximum data-repetition rate of 1 kc, the maximum delay can be set for 0.67 millisecond, but the normal setting is 0.6 msec. The delay of the index bit is set for one-half of the data-bit temporary memory delay, or 0.3 msec. The trailing edge of this pulse is used to strobe the information into a storage register. Placing the strobe in the center of the temporary memory-storage cycle allows for maximum skew.[5]

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[5]See Section V-D for discussion of setting the index bit for optimum data recovery.

V. THEORY OF OPERATION

A. GENERAL

The EGO balloon experiment data processor is designed to operate on 16 parallel signals from a 16-track magnetic-tape reproducer. The signals of each channel carry information in binary form, a "one" being represented by one half-wave rectified sinewave pulse having a period of 1 millisecond and a peak amplitude of -5 millivolts at the reproduce heads. A zero is represented by the absence of any signal excursion when an index pulse is present. Before entering the processor, each channel is amplified by 60 db so that a "one" pulse is a -5v peak half-wave rectified sinewave pulse.

The block diagram[1] for the EGO balloon shows that each experiment data processor amplified channel is applied to a threshold detector. The threshold detectors are employed to recognize the leading edge of the negative excursion of a "one" pulse. The detectors are normally set to recognize only those signals which exceed a negative 2 volts. In tandem with each detector is a temporary memory which serves the purpose of storing the occurrence of a "one" pulse for a finite length of time. This technique is employed to compensate for tape skew.[2]

The output of the detector on the index channel (the signal which indicates to the processor the presence of a parallel word) is applied to the strobe delay, initiating a delayed read pulse through the control portion to the temporary memories. The read pulse stores the complement of the state of each bit memory into the appropriate binary register by way of the patch panel. The assembly of the experiment words (in one's complement form) is generated by two parallel input words for Mark IV and a single parallel input word for Mark II and Mark III. To distinguish between the initial word and the delayed word for Mark IV, the identification channel carries an ID pulse for the initial word and an $\overline{\text{ID}}$ pulse for the delayed word. The control section recognizes the presence of the index and the ID to assemble word I, and the presence of the index and $\overline{\text{ID}}$ to assemble word II.

With the appropriate assembly of experiment words in one's complement form in registers A, B, and C, and the storage of the sensitivity bit in the decimal counter, the control section provides a serial count pulse to each of the three experiment word binary registers[3] converting the one's complement representation to two's complement representation. Following this is a serial readout of each of the binary registers into modified commercial decimal counters.[4] The numbers stored in the decimal counter will then be the decimal equivalent of the binary experiment word.[5] The sensitivity bit is stored in the decimal counter also. Storage of each word and the sensitivity bit are kept independent from each other through modification of the decimal counters.

The magnitude of the word stored in register A before serial readout determines whether the data point (the information contained in all registers) will be accepted.[6] If the magnitude of the count stored in register A is greater than a patched preset number, the information will be accepted and serial readout will proceed; if the count is less than the patched preset number, then the processing of information for that data point will be stopped and cleared so that the next event or parallel input word will be accepted.

After the experiment words are stored in decimal form in the decimal counters, a print-command pulse is generated to a commercial printer[7] which prints the information stored in the counters. The print cycle requires 200 milliseconds. During the time of printing, the control section

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[1]See Figure 16 in section containing schematic diagrams.

[2]See discussion on tape skew, part D of this section.

[3]For Mark II and Mark III, only two experiment words (A and B) are employed.

[4]Hewlett-Packard Model 5532A.

[5]See discussion in Section V-B on conversion of binary to decimal form.

[6]See discussion in Section V-C on recognition of a data point that exceeds a preselected number.

[7]Hewlett-Packard Model 562A.

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generates a lockout pulse that inhibits the generation of new data strobes, thereby preventing the entrance or processing of any new data until the termination of printing.

Incorporated in the EGO balloon experiment data processor is a simulation mode in which the data-line inputs are switched out and simulated data are applied to the threshold detectors. By observation of front panel indicator lights and operator control of simulated data words, the unit can be checked for proper operation.

B. BINARY-TO-DECIMAL CONVERSION

A translation can be made from the binary to the decimal system by first placing the 2's complement of the binary number into a register which also can operate as a binary counter, then applying a serial train of pulses simultaneously to both the binary counter and a decimal counter. The conversion is obtained by counting the number of counts in the decimal counter required to clear or recycle the binary register.

An algorithm* for determining the complement of a number N is:

$$\bar{N} = r\text{'s complement} = r^n - N$$

where: n = number of digits in the number N

N = the number

r = the radix or base

Transposing: $\bar{N} + N = r^n$

Since a counter can count to $r^n - 1$, the counter has to pass through a zero count or recycle if the original number is serially added to the complement previously stored in the register; i.e., if N counts are added to a binary counter storing $\bar{N}$ (the two's complement of N in this case), then the counter will end in a "0" state.

For ease of implementation, the 1's complement is entered into the binary register and this number is converted to 2's complement by adding a count to the counter.

An algorithm for relating 2's complement (radix complement) to 1's complement (diminished radix complement) is:

$$\bar{\bar{N}} = r^n - N - r^{-m}$$

$$\bar{N} = \bar{\bar{N}} - r^{-m}$$

where: $\bar{\bar{N}}$ = diminished radix complement

For the 1's complement, $m = 0$, so that

$$\bar{\bar{N}} = r^n - N - 1$$

$$= \bar{N} - 1$$

or

$$\bar{N} = \bar{\bar{N}} + 1$$

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*Reference 1.

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The translation to decimal form by serial readout begins after the 1's complement has been converted to the 2's complement. As an illustration, consider the conversion of the binary number 0011101 (29_{10}) that is stored in a seven-stage binary register to a decimal number:

Formulas	Carry		
$\bar{\bar{N}} = r^n - N - 1$	1	0000000	($r^n = 2^7$)
		$\underline{\quad\quad -1}$	
		1111111	($r^n - 1$)
		-0011101	($-N$)
		1100010	($\bar{\bar{N}}$)
$\bar{N} = \bar{\bar{N}} + 1$		$\underline{\quad\quad +1}$	
$\bar{N} + N = r^n$		1100011	($\bar{N}$)
		$\underline{+0011101}$	($+N = 29_{10}$)
	1	0000000	(r^n)

recycle ⟶

C. RECOGNITION OF A DATA POINT THAT EXCEEDS A PRESELECTED NUMBER

The limited speed of the digital printer makes it necessary to obtain printouts of only good data points, because these printouts represent only 0.5 percent of the maximum data rate. In the Mark II, Mark III, and Mark IV experiments there are certain conditions under which low counts can be discarded before the time-consuming conversion begins. When accepting data, the data processor will determine whether or not a data point exceeds a predetermined level. When the processor decides to accept a data point for processing, a lockout or inhibit mode is generated which prevents the processor from accepting any additional data points until the digital print cycle is completed.

The decision process is illustrated by the truth table on the following page.

The 1's complement of the data point is stored in the binary register. The set side of the most significant bits of the register are connected to a gate that generates a "stop" condition when all of the inputs are true (1), and a "go" condition if any one of the inputs is false (0). The logic is illustrated in Figure 3.

For example, consider a situation in which any data point with a count less than 8 can be discarded. The set side of the register from bit 4 (2^3) to bit $n(\overline{2^{n-1}})$ is programmed to the gate. When all the inputs are true (1), which corresponds to a digital number of less than 8, a stop condition is generated. When any stage of the set side of the register programmed to the gate becomes false (0), the number equals or exceeds 8 and a go condition is generated.

Table 5
Truth Table for Word A Greater Than Preset

Bit 6 $\overline{2}^5$	Bit 5 $\overline{2}^4$	Bit 4 $\overline{2}^3$	Bit 3 $\overline{2}^2$	Bit 2 $\overline{2}^1$	Bit 1 $\overline{2}^0$	Output of Gate	Digital Equivalent
1	1	1	1	1	1	0	0
1	1	1	1	1	0	0	1
1	1	1	1	0	1	0	2
1	1	1	1	0	0	0	3
1	1	1	0	1	1	0	4
1	1	1	0	1	0	0	5
1	1	1	0	0	1	0	6
1	1	1	0	0	0	0	7
1	1	0	1	1	1	1	8
1	1	0	1	1	0	1	9

$$A - (2^3)$$
$$B - (2^4)$$
$$M - (2^n)$$

NAND
(Sheffer Stroke)

$$\overline{AB\ldots M} = \overline{A} + \overline{B} + \ldots \overline{M}$$
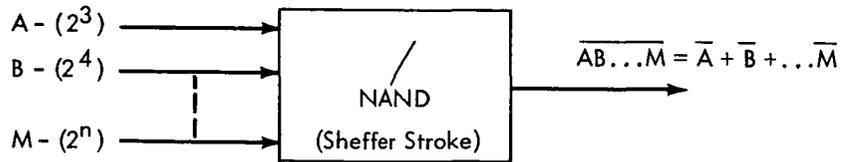
Figure 3—The NAND Function

The processor can be programmed to recognize any data point that has a count exceeding 2^n where n equals zero or any integer. There is also a provision which enables the processor to process all data, regardless of the count.

D. COMPENSATION FOR TAPE SKEW

To recover the maximum amount of data when skew problems are present, the incoming data bits are stored in temporary memories at a fixed time interval after occurrence of the INDEX bit, and the information is simultaneously strobed from all the bit memories into binary registers for further processing.

A delay multivibrator with a 67-percent duty cycle is used as a temporary memory device. For a maximum repetition rate of 1 kc, the maximum memory duration that can be obtained is 0.67 ms. As a margin of safety, all the data memories are preset to provide a storage time of 0.60 ms, and the data-strobe delay generator is preset to provide a delay equal to half the memory duration, or 0.3 ms. This is the optimum setting for recovering data with the greatest symmetrical skew.

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If the recorded tape has static skew or if the playback head stack is misaligned, the strobe pulse can be elongated or shortened, depending on the time bias introduced by the skew.

The following examples illustrate data recovery with dynamic skew.

Example 1:

In Figure 4, the data-information pulse is in phase with the index pulse that generates the data-sampling strobe. The data could, therefore, be strobed at the center of the data memory-storage cycle as shown. This would be the setting of the data strobe delay for an ideal situation where no skew or misaligned data pulses are present.
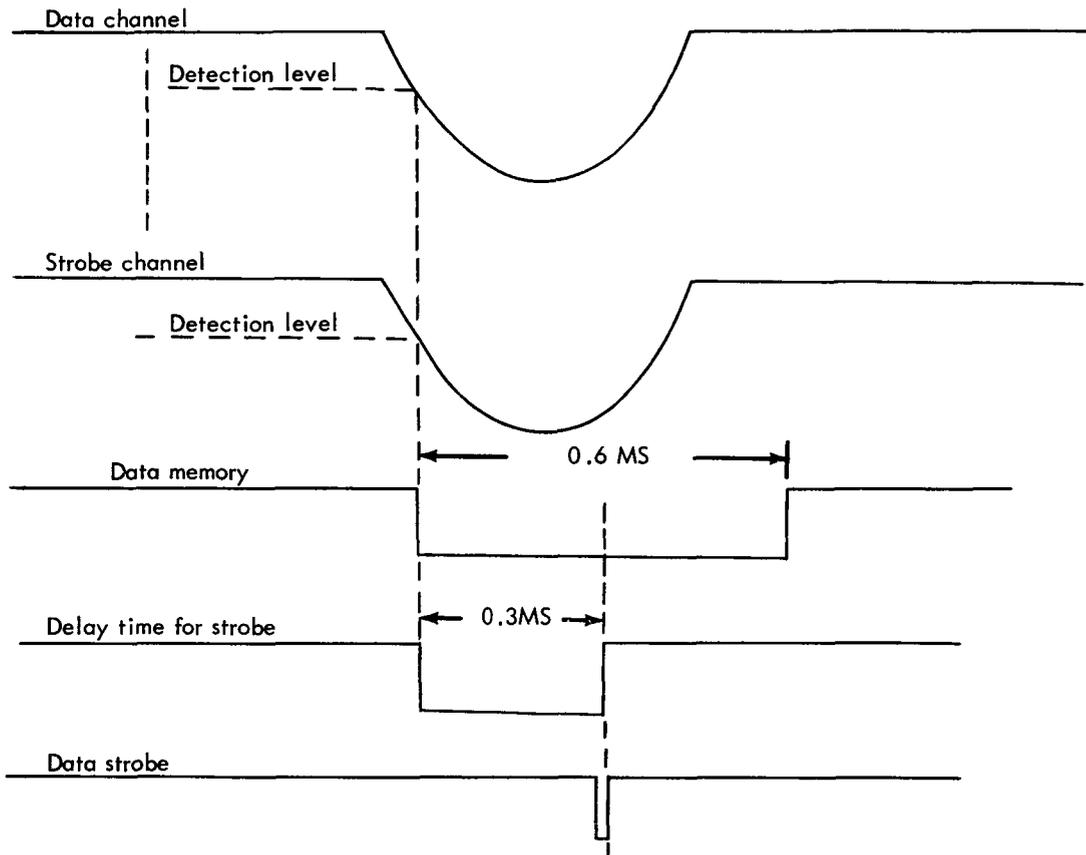
Strobe samples data in the center of its memory cycle. No skew – data tracks and index track displaced by 0°.

Figure 4—Bit Detection with 0° Skew

Example 2:

In Figure 5, the information pulse from the data channel was delayed by 108° (0.3 msec) with reference to the pulse that produces the generated strobe. The sampling strobe, which is generated from the trailing edge of the delayed strobe pulse, will sample the data pulse at the leading edge of the data memory pulse.

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Strobe samples data on the leading edge of the memory cycle.
Data track displaced from index track by -108°.
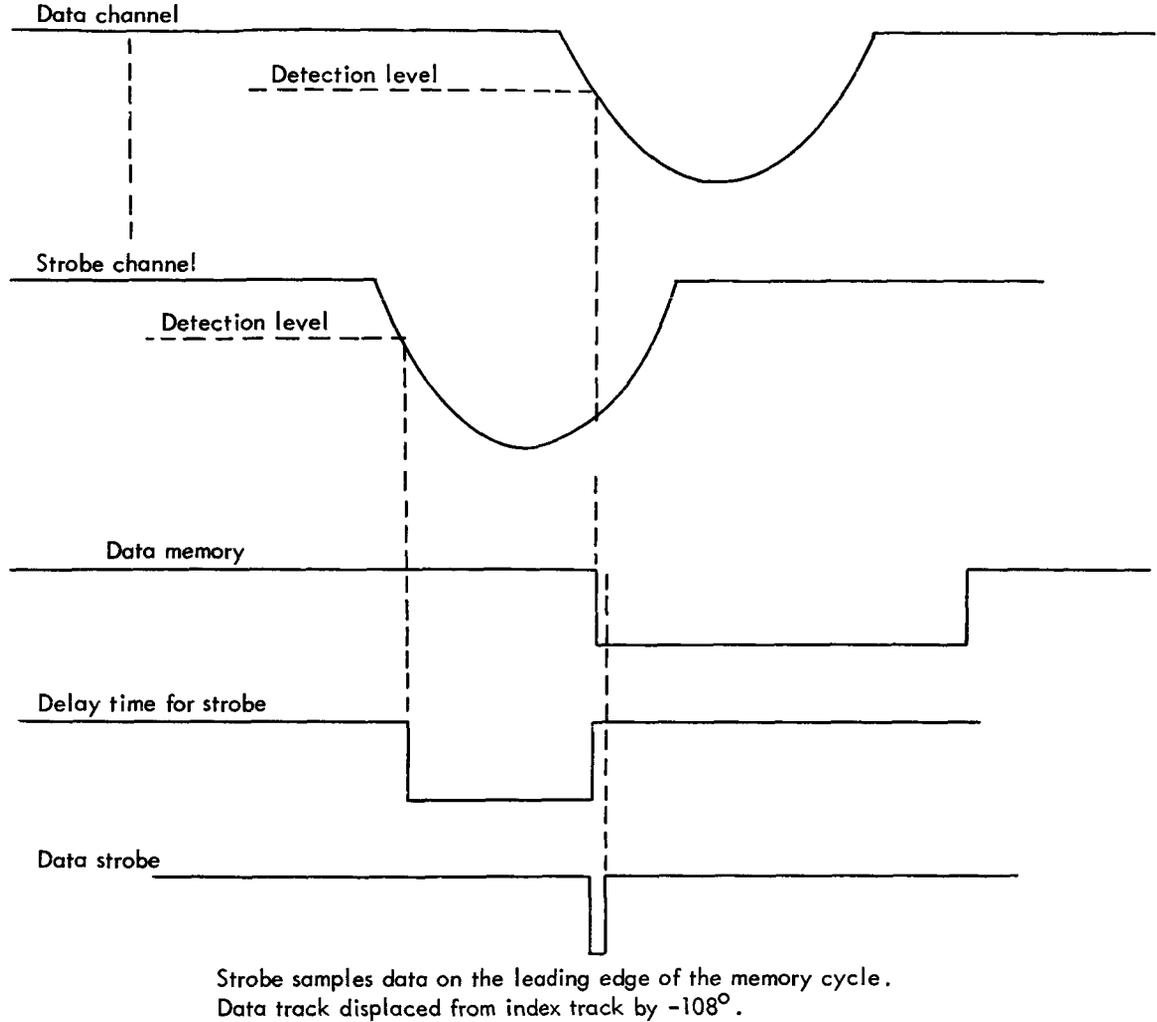
Figure 5—Bit Detection with -108° Skew

Example 3:

In Figure 6, the information pulse from the data channel precedes the pulse that generates the strobe by 108° (0.3 msec). The sample strobe now samples the data pulse at its trailing edge.

Under actual operating conditions, all three of the examples can happen simultaneously; i.e., for a given word the data pulses in the various tracks can lead, lag, and be in phase with the index pulse that generates the strobe. When the memories and strobe delay are set for the values previously mentioned, the system will accurately process data that vary within ±108° with reference to the index bit that produces the sampling strobe.
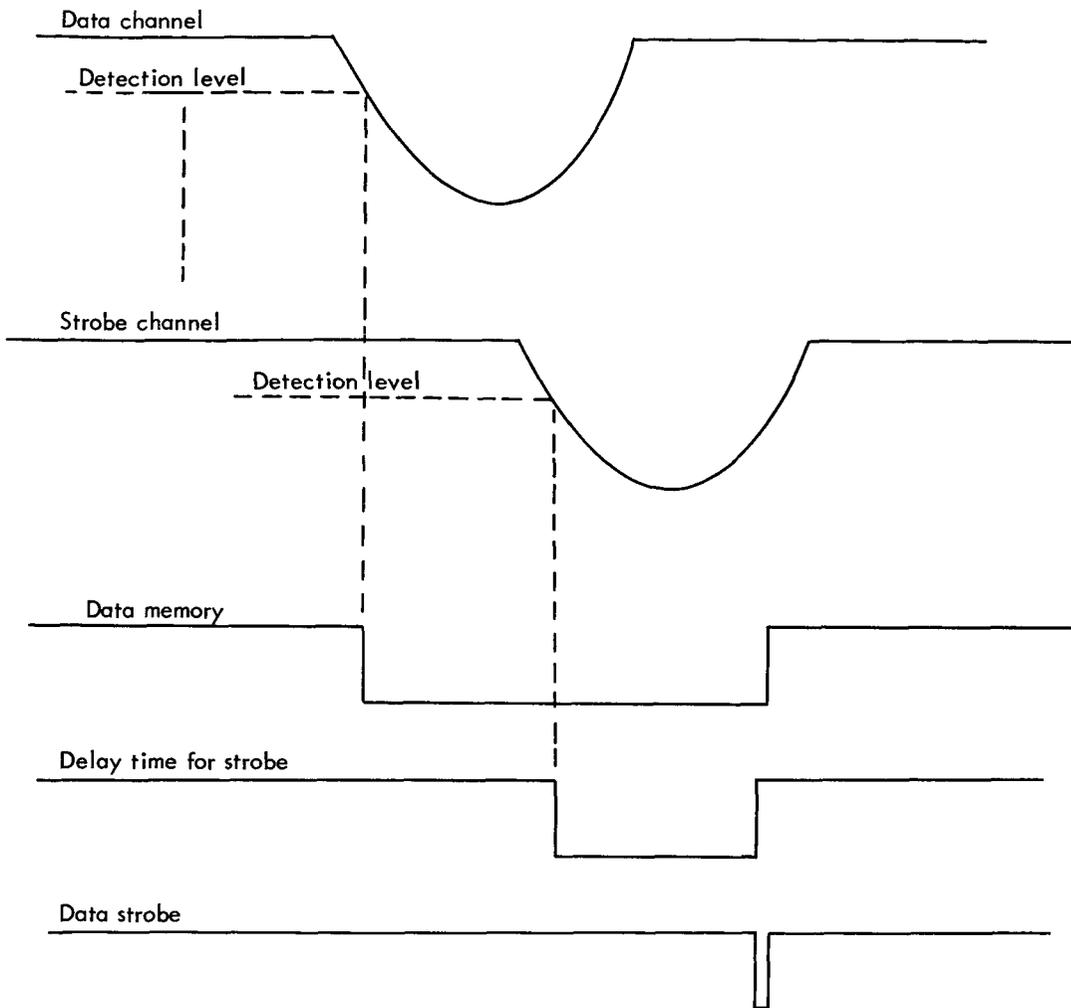
Strobe samples data on the trailing edge of the memory cycle. Data track displaced from index track by +108°.

Figure 6—Bit Detection with +108° Skew

VI. DESCRIPTION OF LOGIC

A. Control Unit

Mark IV Control Logic[1]

The incoming data signals, after being detected by the Schmitt triggers, are stored in a temporary memory (delay multivibrator) until the complement of the data word is strobed into a binary register. The index and the ID pulses are detected by their respective Schmitt triggers (I-8-27 and I-9-10). When they are in coincidence, an initial strobe (I-23-13) is generated from the trailing edge of the index pulse (TLN-7).[2]

The initial strobe (I.S.) generates a gating pulse approximately 2 msec long (I-22-17). When another index pulse appears within this interval and no ID pulse is present, a delayed strobe (DS) pulse is produced (TLN-10).

The initial strobe (IS) samples the incoming data lines and enters the complement of the data in the appropriate binary registers. A comparison is made between the data word entered in the "A" register and a preprogrammed word;[3] if the incoming data word is equal to or greater than the programmed word, a gate is enabled that allows the delayed strobe (DS), with a 10-μs delay (II-21-16), to add an extra count to the three binary registers, reset the commercial decimal counters, and (after a 100-μs delay) gate a multivibrator's output to the input of the three registers. The data are then passed through level-matching circuits to the inputs of the decimal counters.[4]

The sensitivity bit is gated with the delayed strobe (I-20-16) to set a flipflop (I-18-27), whose output is gated with the extra count pulse through a level-matching circuit directly to the split input of the decimal counter. The sensitivity word has only two states, true (-6 volts) and false (0 volts). The true condition in the printout is represented by a decimal "1", the false condition by a "0".

The same pulse that gated the multivibrator's output to the registers also initiates a 10-msec delay pulse (I-21-11) that turns off the multivibrator after the conversion.

The pulse that generated the extra count (TLN-11) initiates a 200-msec inhibit (II-21-34) that disables the control input (I-23-13) so that new data will not be accepted for processing while the printer is operating.

If the data word entered in the "A" register is less than the preset number, the delayed strobe, with an additional 20-μsec delay, is used to generate a 200-μsec pulse (I-22-31) that resets the binary registers and allows the system to accept new data.

Mark II-III Control Logic[5] (Refer to diagram GD-EGO-111-4531)

The index pulse is detected by the Schmitt trigger and the leading edge of the pulse is delayed by approximately 0.3 msec and this edge is used to generate a 10-μsec strobe pulse (I-22-10). The strobe pulse is gated with the $\overline{C}$[6] bit (I-23-9) in the AB$\overline{C}$ mode of operation. When in the ABC mode of operation and with the absence of the C bit ($\overline{C}$), the 10-μsec pulse is used to strobe the complement of the data into the appropriate binary registers. If the C bit is present, the

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[1]See Figures 18 and 19 in the section containing diagrams.

[2]The notation TLN- will be used to refer the reader to the timing line numbers on Figure 22 in the section containing diagrams.

[3]Refer to Figure 23 for appropriate programming.

[4]The six-stage decimal counters are split internally into two three-stage counter circuits, so that each counter can accept two different inputs and can convert binary numbers to an equivalent decimal count of 999.

[5]See Figure 18 in the section containing diagrams.

[6]The control switch AB$\overline{C}$-AB is located on the front panel.

10-μsec pulse is inhibited and no further processing occurs. When in the AB mode, all data are processed regardless of the condition of the C bit.

After entry of the complement of the data word into A register, the processing is the same as in the Mark IV mode of operation.

B. REGISTERS A, B, AND C

(Diagrams GD-EGO-1114-532, 533, 534)[1]

Register A (Diagram GD-EGO-1114-532)

The output of the Schmitt trigger data detection circuit is connected to a gate whose output, when strobed, sets the dc-set side of a binary register. When no data pulse is present at the occurrence of an input word, the gate is enabled and the initial data strobe[2] sets each binary register of the counter to the complement of the input. When a data pulse is present, the gate is inhibited and the register is left in the reset or the false condition; i.e., the register is set to true (-6 volts) when the input data line is false, or to false (0 volts) when the input data line is true.

After data have been entered into register A, a comparison against a programmed number is performed. If the stored data in register A are equal to or greater than the programmed number, the output of the comparison gate (II-16-9) is true (-6 volts), which indicates a "go" or "process data" condition.

Upon acceptance of data for processing, an extra count pulse is added to the binary registers through an "OR" gate (II-14-16), making the stored number in the register the two's complement of the data word.

A start pulse from the control logic sets a flipflop (II-15-27) which provides a synchronous start for the free-running multivibrator (II-17-35) that counts out the contents of the register. The multivibrator is turned off after 10 msec by resetting the control flipflop with a pulse generated by a delay multivibrator. The start pulse from the control logic also sets a flipflop (II-15-12) that gates the output of the multivibrator to the binary register and the decimal counters. Upon recycling, the output of the binary register (II-6-20) produces a pulse whose leading edge triggers a delay multivibrator that resets flipflop (II-15-12), thereby turning off the gated output to both the decimal and binary counters.

(Registers B and C, diagrams DG-EGO-1114-533 and -534, operate the same as register A but do not have a comparison circuit to evaluate the incoming data. The free-running multivibrator used for reading out register A is shared by all three registers and is turned off 10 msec after the start command.)

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[1]See Figures 19, 20, 21 in section containing diagrams.

[2]For the Mark IV experiment, the data strobe to register A is the initial strobe; for the Mark II-III experiments, the data strobe is the delayed strobe. (The initial strobe is not generated for these two experiments.)

VII. SIGNAL SIMULATION

The Mark IV simulated signal is generated by a free-running multivibrator (MV-16) set for 1000 cycles per second, the maximum data-reduction frequency of the processor. The output of the multivibrator triggers a delay multivibrator (DM-15) which generates a pulse 0.5-msec long. This pulse, after being inverted through a power-amplifier stage (PA-17), is used to simulate the index and the data pulses. The ID pulse which occurs at one-half the frequency of the index pulse is generated by connecting the MV output to a binary counter (BC-18) which divides the MV frequency by two. The output of the binary counter is connected to the ID channel. A coincidence of the index and the ID channels creates a Word I strobe; an index and an $\overline{\text{ID}}$ create a Word II strobe. A "one" is detected by the level detectors if the individual toggle switch for that channel is thrown to the "one" position and the master control switch* is in the "test" position.

Mark II-III simulation differs from the Mark IV in that the BC output is not used; the PA output is used to generate all the signals to be detected by the level detectors.

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*The toggle switches and the master control switch are located on the rear of the front panel.

VIII. POWER

(Diagram GC-EGO-1109-650) *

The data processor uses 115-volt 60-cycle single-phase power. The processor unit has an ON-OFF toggle switch that connects the ac power through a 1-ampere fuse to the Muffin fans, the Technipower power supply, and a 1.5v step-down transformer.

The indicator thyratron tubes on the front panel derive a 50-volt dc plate potential from the Technipower power supply, and their 1.5v ac filament voltage from the step-down transformer. The 3-C RP30 power supply uses 115v 60-cycle single-phase power. An interconnecting cable between the 3-C power supply and the processor is used to supply the -6, -18, and +12 volts of dc current between the two units.

_____

*See Figure 24 in the section containing diagrams.

IX. CONVENTIONS AND SYMBOLS USED IN THE DRAWINGS AND THE LITERATURE

The EGO data processor system uses Computer Control Company's S-Pac 1-Mc digital modules. The 3-C (Computer Control Company) reference manual should be used when referring to the detail logic diagrams. When reference is made to a circuit on the drawing, its location is designated by the S-bloc within the unit, the module's position number, and the pin number in that order; e.g., III-4-8 refers to S-bloc III, module 4, pin 8.

Configurations for several circuits which bear explanation are shown here by examples:

Module type:	DI
Module number:	7
Input pins:	26 and 30
Output pin:	23

Figure 7—NAND Circuit Symbol

Module type:	DN
Module number:	19 & 8
Input pins:	14, 15, 16 module 19 30, 31, module 8
Output pin:	17, module 19 , 32, module 8

Figure 8—NAND Circuit with Extended Fan-In Symbol

Module type:	DI
Module number:	8
Input pins:	9 and 14
Output pin:	7
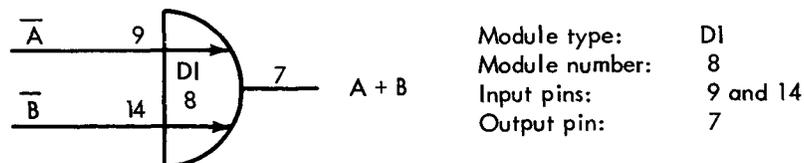
Figure 9—NOR Circuit Symbol
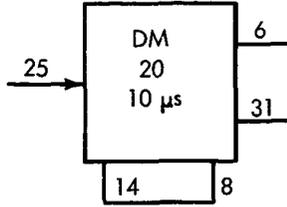
Module type: DM
Module number: 20
Toggle input pin: 25
Assertion output
            pin: 6
Negation output
            pin: 31
Delay node pins (Those which
when connected, give time
delay shown)   :   14 and 8

Figure 10—Monostable Multivibrator Circuit Symbol
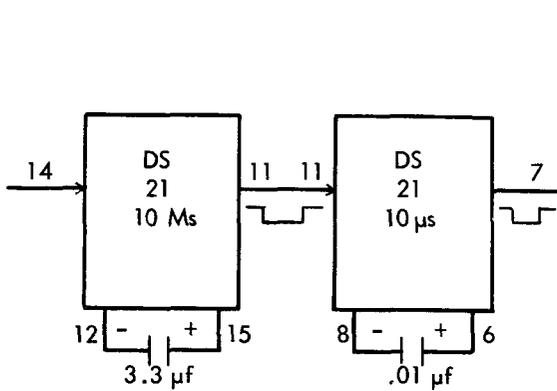
Module type: DS
Module number: 21
Toggle input: 14
Assertion output: 11 (delay time)
Assertion output: 7 (output pulse
    with indicated delay) 12 and
    15 determine the delay time; 8
    and 6 determine the output
    pulse width.

Figure 11—Delayed Pulse Generator Symbol
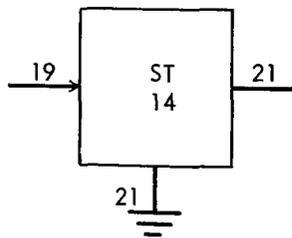
Module type: ST
Module number: 14
Input: 19
Output: 21

Figure 12—Schmitt Trigger Symbol
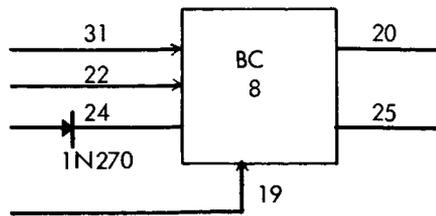
Module type:	BC
Module number:	8
Complementary toggle input pin:	22
Set input:	31
Reset input (common to 4 BC circuits:	19
Reset input (for individual circuit):	24
Set output:	20
Reset output:	25

Figure 13—Binary Counter Circuit Symbol
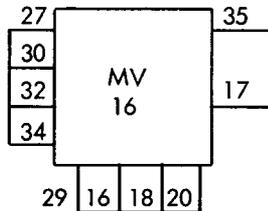
Module type:	MV
Module number:	16
$\overline{MV}$ output:	17
MV output:	35

Determination of frequency range: Pin 27 to 30, 32,34, and 29 to 16, 18, 20 (Frequency can be varied within overall range by a potentiometer on top of the module.)

Figure 14—Multivibrator Clock Symbol
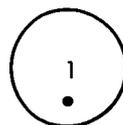
The number within the circle gives the location of the light on the front panel.

Figure 15—Light Indicator Symbol

X. MODIFICATIONS TO HEWLETT-PACKARD DIGITAL COUNTERS AND PRINTER

(Diagram GC-EGO-1109-651)*

Modifications to counters:

1. Board A-6

   (a) R23, R24 – 3.9-K ohm resistor added in parallel
   (b) Jumper removed between pin 10 (A-5) and pin 7 (A-6)

2. Shielded wire added to the following

   Pin connections on the 50-pin connector on rear of counter:

	FROM	TO
	45 (count A)	Input to Counter
"A" Counter	46 (count C)	Pin 7 (A-6)
	21 (reset)	Pin 11 (A-18)
	45 (count B)	Input to counter
"B" Counter	46 (sensitivity)	Pin 7 (A-6)
	21 (reset)	Pin 11 (A-18)

Modifications to digital printer:

A double-pole double-throw toggle switch was added to the back of the printer to enable acceptance of the print command from the processor in the EGO position, and from the electronic counters in the NORMAL position. The two reset lines and the sensitivity (or Word C count) line from the processor are routed to the decimal counters via the printer through the Amphenol connectors and the counter-printer interconnecting cables. The lines from the processor to the printer are brought in by a 14-pin Amphenol connector.

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*See Figure 25 in section containing diagrams.

XI. REFERENCES

1. Chu, Yaohan, Digital Computer Design Fundamentals, McGraw-Hill Book Company, Inc., New York (1962)

2. Instruction Manual for S-Pac Digital Modules, 3C Computer Control Company, Inc.

3. Preliminary Operating and Servicing Manual (for Hewlett-Packard Company Model 5232A/5532A electronic counter)

4. Operating and Service Manual (for Hewlett-Packard Company 562A digital recorder)

Figure 16—EGO Data Processor, Block Diagram (GC-EGO-1109925)

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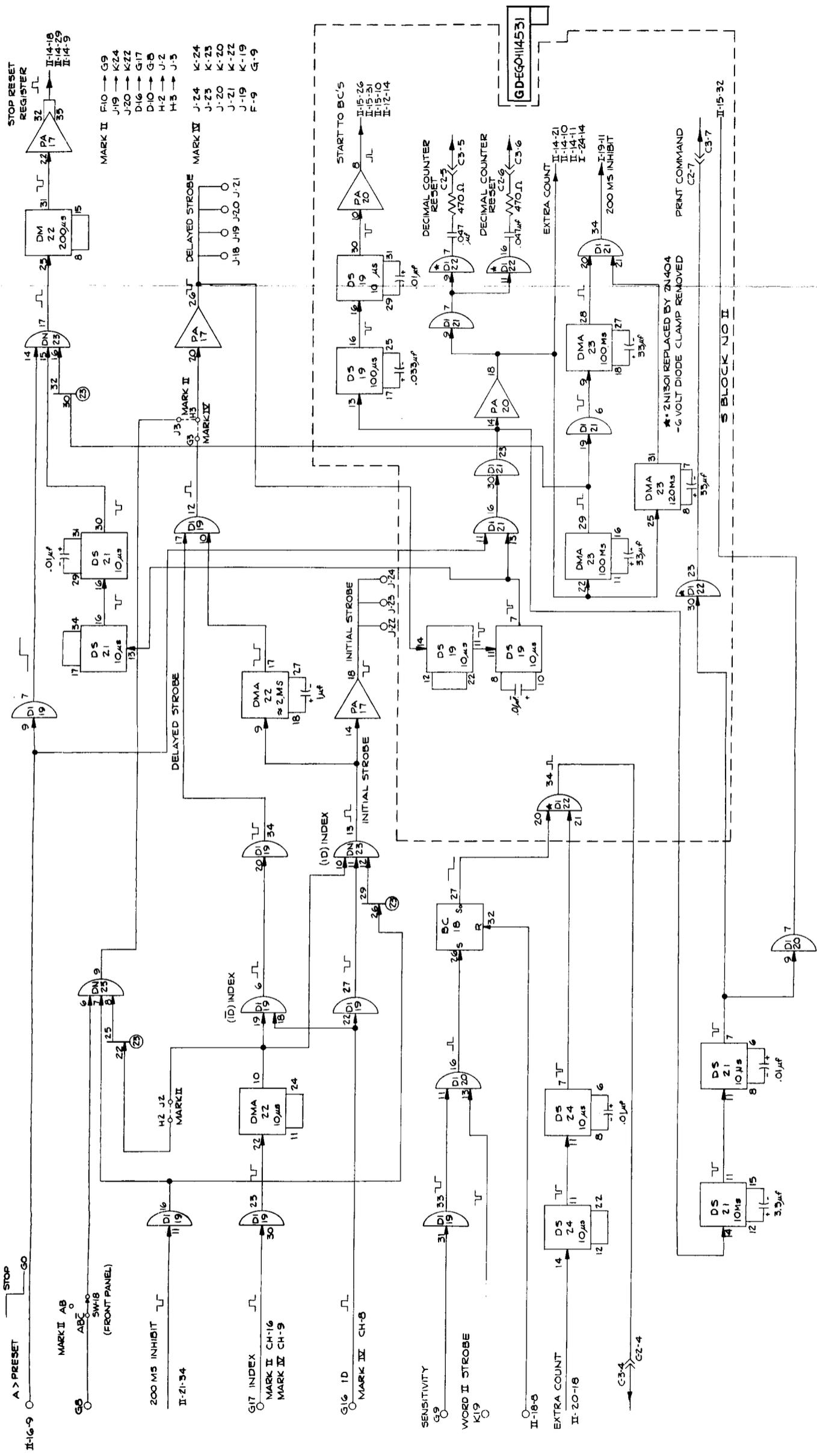Figure 17—Input Detection and Simulation Logic
(GD-EGO-1114530)

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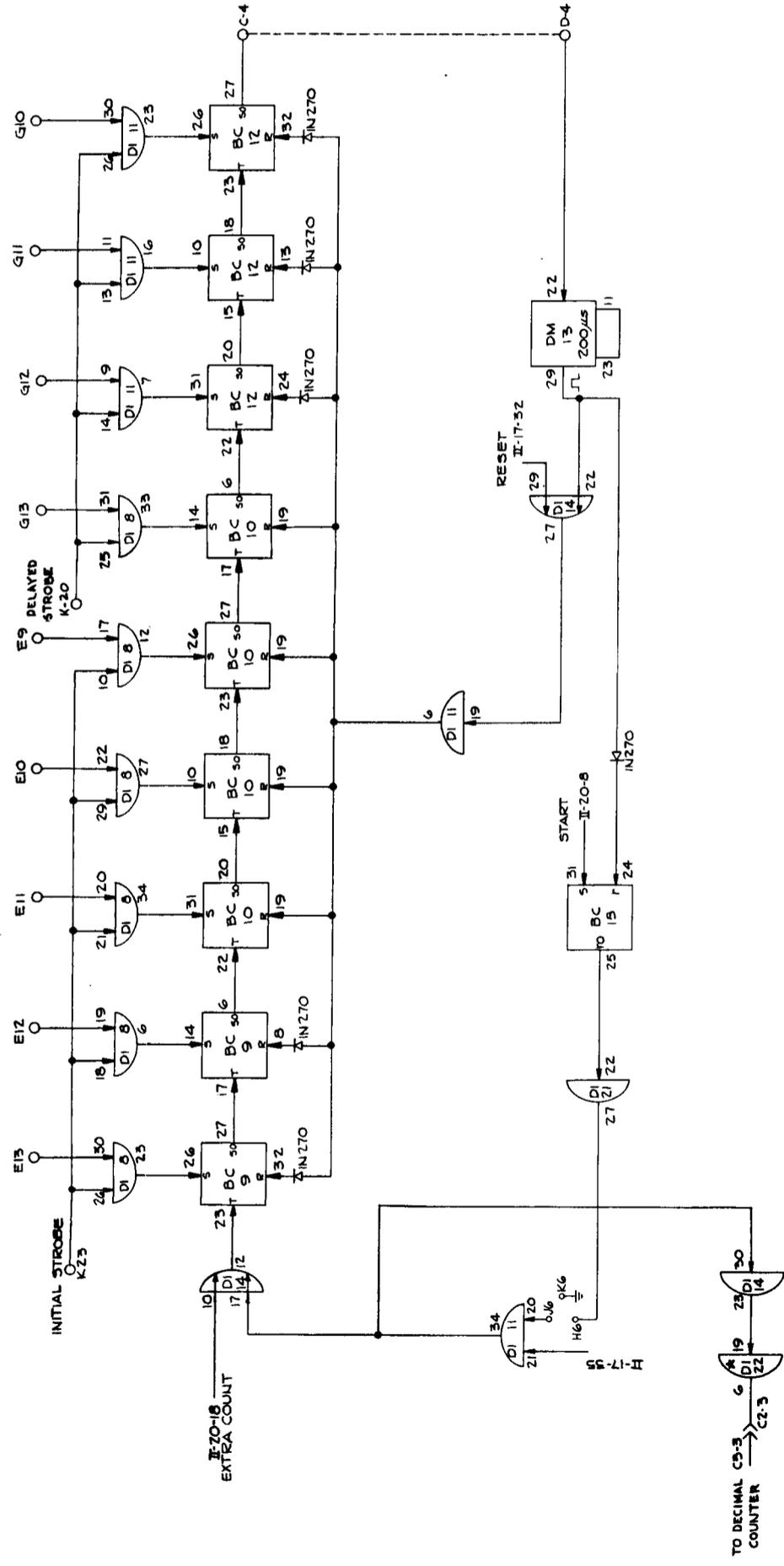Figure 18—Control Logic (GD-EGO-1114531)
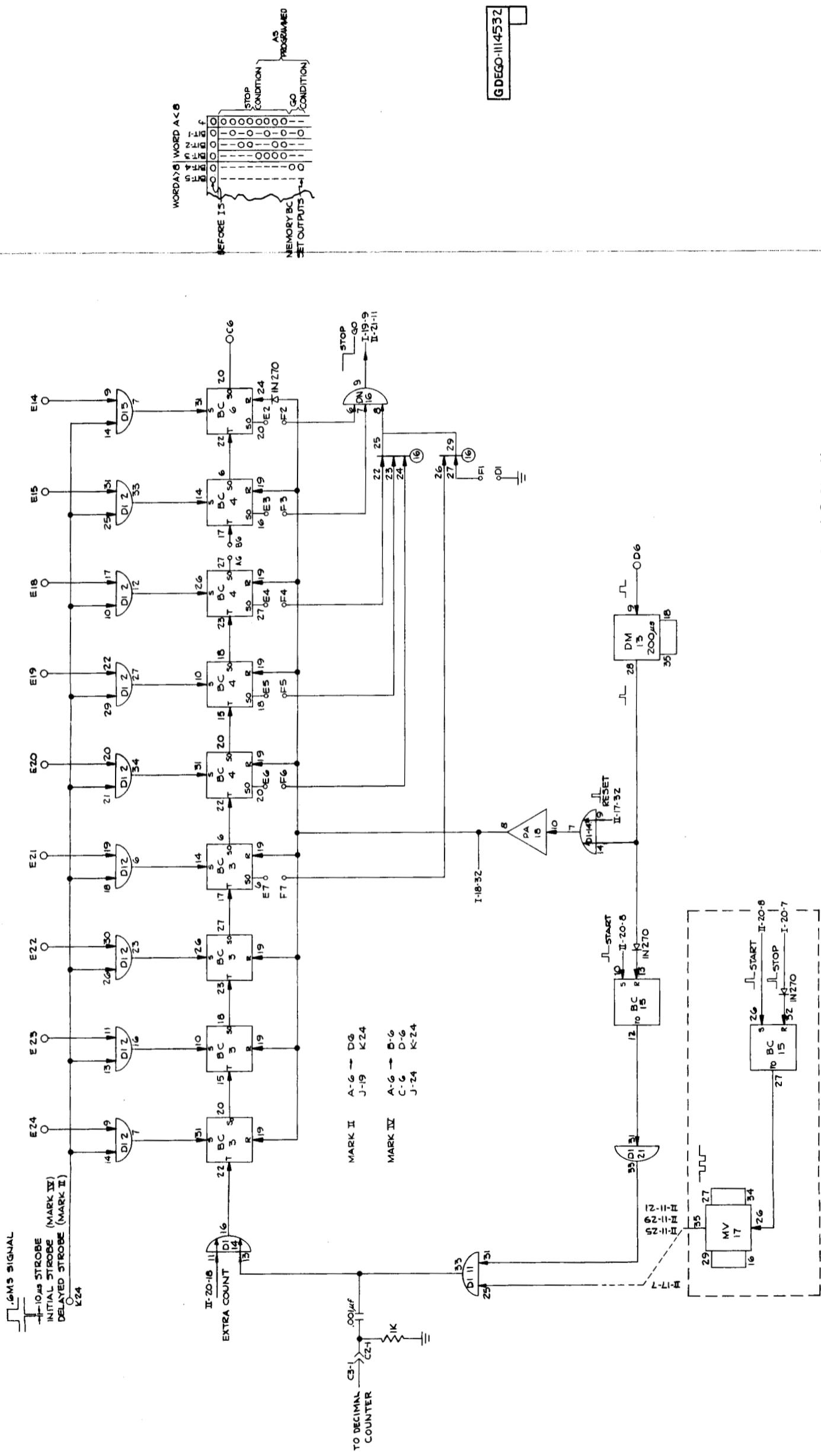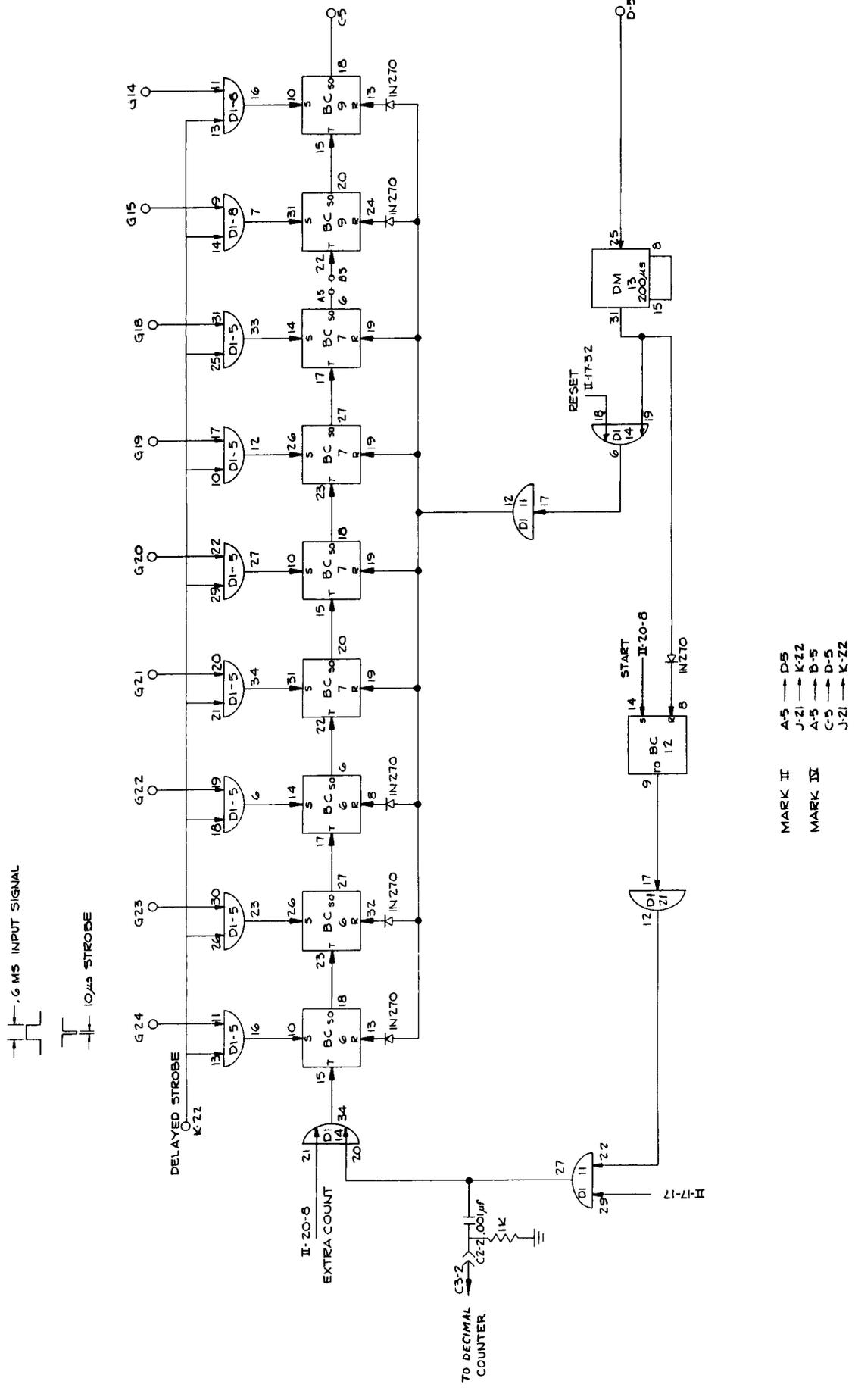
Figure 19—Word A Logic (GD-EGO-1114532)

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Figure 20—Word B Logic (GD-EGO-1114533)

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S-BLOCK II

Figure 21—Word C Logic (GD-EGO-1114534)

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TIMING DIAGRAM
NOT TO SCALE

1 INDEX (INPUT TO INDEX SCHMITT TRIGGER)

2 ID (INPUT TO ID SCHMITT TRIGGER)

3 S.T. DETECTION OF INDEX

4 S.T. DETECTION OF ID
   0.3Ms

5 DMA OUTPUT FOR INDEX I-7-28
   0.6Ms

6 DMA OUTPUT FOR ID I-7-29

7 IS (INITIAL STROBE) I-17-18
   10µs

8 OUTPUT OF COMPARISON CIRCUIT
   ON "A" COUNTER II-16-9   "A"< PRESET
                                 "A"> PRESET

9 GATE TO ENABLE D.S. ≃ 2ms I-22-17

10 D.S. (I-17-26)   D.S. (DELAYED STROBE)

11 A> PRESET (DECIMAL COUNTER RESET-EXTRA COUNT) (II-20-18)
   10µs
   10µs

12 START TO BC's (II-20-8)

13 200ms INHIBIT FOR PROCESS CONDITION (I-21-34)
   100µs
   Δt=100µs

14 PRINT COMMAND-TURN OFF MV.
                                 READY FOR NEW DATA

15 "A"< PRESET (DO NOT PROCESS)
   20µs

16 STOP-RESET REGISTERS - READY FOR NEW DATA

CONDITION I

CONDITION II

CONDITION I - REGISTER "A" GREATER THAN PRESET COUNT PROCESS DATA
             AND INHIBIT NEW DATA FOR 200ms

CONDITION II - REGISTER "A" LESS THAN PRESET COUNT DO NOT PROCESS DATA
              RESET ALL REGISTERS AND ACCEPT NEW DATA.

Figure 22—Timing Waveforms

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MARK IV

TEST

FROM	TO
A-24	B-24
A-23	B-23
A-22	B-22
A-21	B-21
A-20	B-20
A-19	B-19
A-18	B-18
A-16	B-16
A-15	B-15
A-14	B-14
A-13	B-13
A-12	B-12
A-11	B-11
A-10	B-10
A-9	B-9
A-8	B-17

OPERATE

FROM	TO
A-5	B-5 (9 STAGE REGISTER 'B')
A-6	B-6 (9 STAGE REGISTER 'A')
D-6	C-6 (TURN OFF 'A' REG.)
D-4	C-4 (TURN OFF 'C' REG)
D-5	C-5 (TURN OFF 'A' REG)
D-24	E-24 A_0
D-23	E-23 A_1
D-22	E-22 A_2
D-21	E-21 A_3
D-20	E-20 A_4
D-19	E-19 A_5
D-18	E-18 A_6
D-17	E-17 ID
D-16	E-16 INDEX
D-15	E-15 A_7
D-14	E-14 A_8
D-13	E-13 C_0
D-12	E-12 C_1
D-11	E-11 C_2
D-10	E-10 C_3
D-9	E-9 C_4
F-24	G-24 B_0
F-23	G-23 B_1
F-22	G-22 B_2
F-21	G-21 B_3
F-20	G-20 B_4
F-19	G-19 B_5
F-18	G-18 B_6
F-17	G-17 ID
F-16	G-16 INDEX
F-15	G-15 B_7
F-14	G-14 B_8
F-13	G-13 C_5
F-12	G-12 C_6
F-11	G-11 C_7
F-10	G-10 C_8
F-9	G-9 SENS
H-6	J-6 (COUNT 'C' START)
H-5	J-5 (ST-9 → DMA9)
H-4	J-4 (ST-16 → DMA16)
H-3	G-3 (DELAYED STROBE)

OPERATE

FROM	TO
J-24	K-24 ('A' INITIAL STROBE)
J-23	K-23 ('C' INITIAL STROBE)
J-21	K-22 ('B' DELAYED STROBE)
J-20	K-20 ('C' DELAYED STROBE)
J-19	K-19 (SENS 'DELAYED STROBE)

TO BE PROCESSED COUNT MUST BE ≥ N

FROM	TO	
E-7	F-7	8
E-6	F-6	16
E-5	F-5	32
E-4	F-4	64
E-3	F-3	128
E-2	F-2	256
F-1	D-1 PROCESS ALL DATA	
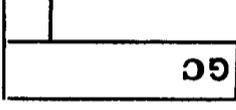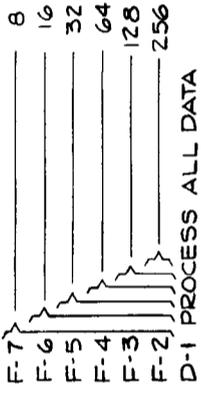
MARK II

TEST

FROM	TO
A-24	B-24
A-23	B-23
A-22	B-22
A-21	B-21
A-20	B-20
A-19	B-19
A-18	B-18
A-17	B-17
A-16	B-16
A-15	B-15
A-14	B-14
A-13	B-13
A-12	B-12
A-11	B-11
A-10	B-10
A-9	B-9

OPERATE

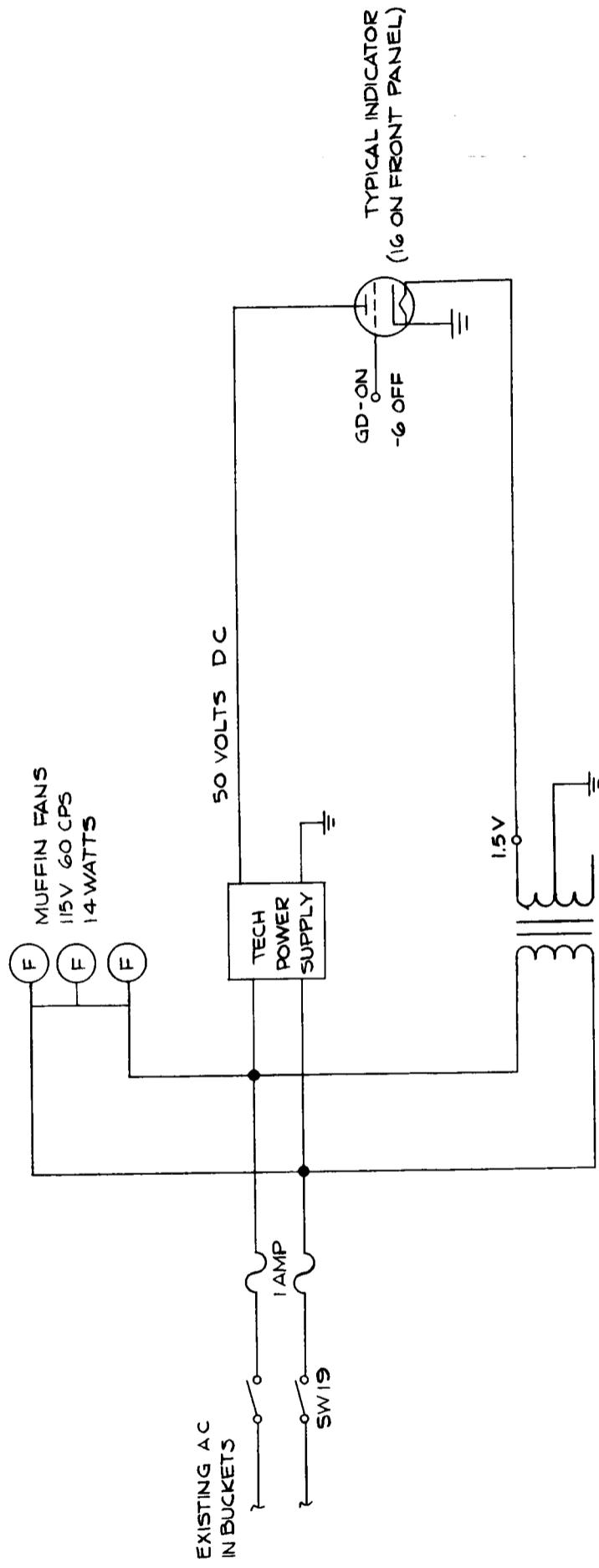| FROM	TO
A-5	D-5 (TURN OFF 'B' REGISTER)
A-6	D-6 (TURN OFF 'A' REGISTER)
D-24	E-24 A_0
D-23	E-23 A_1
D-22	E-22 A_2
D-21	E-21 A_3
D-20	E-20 A_4
D-19	E-19 A_5
D-18	E-18 A_6
D-17	G-24 B_0
D-9	G-23 B_1
D-15	G-22 B_2
D-14	G-21 B_3
D-13	G-20 B_4
D-12	G-19 B_5
D-11	G-18 B_6
J-6	K-6 (GROUND 'C' REGISTER)
H-2	J-2 (STROBE)
H-3	J-3 (STROBE)
D-10	G-8 ('C' INHIBIT)
D-16	G-17 (INDEX)
F-10	G-9 ('C' INHIBIT PRINT)
J-19	K-19 ('C' STROBE)
J-20	K-22 ('A' STROBE)
J-21	K-24 ('B' STROBE)
J-4	H-5 (ST-9 → DMA-16)
J-5	H-4 (ST-16 → DMA-9)

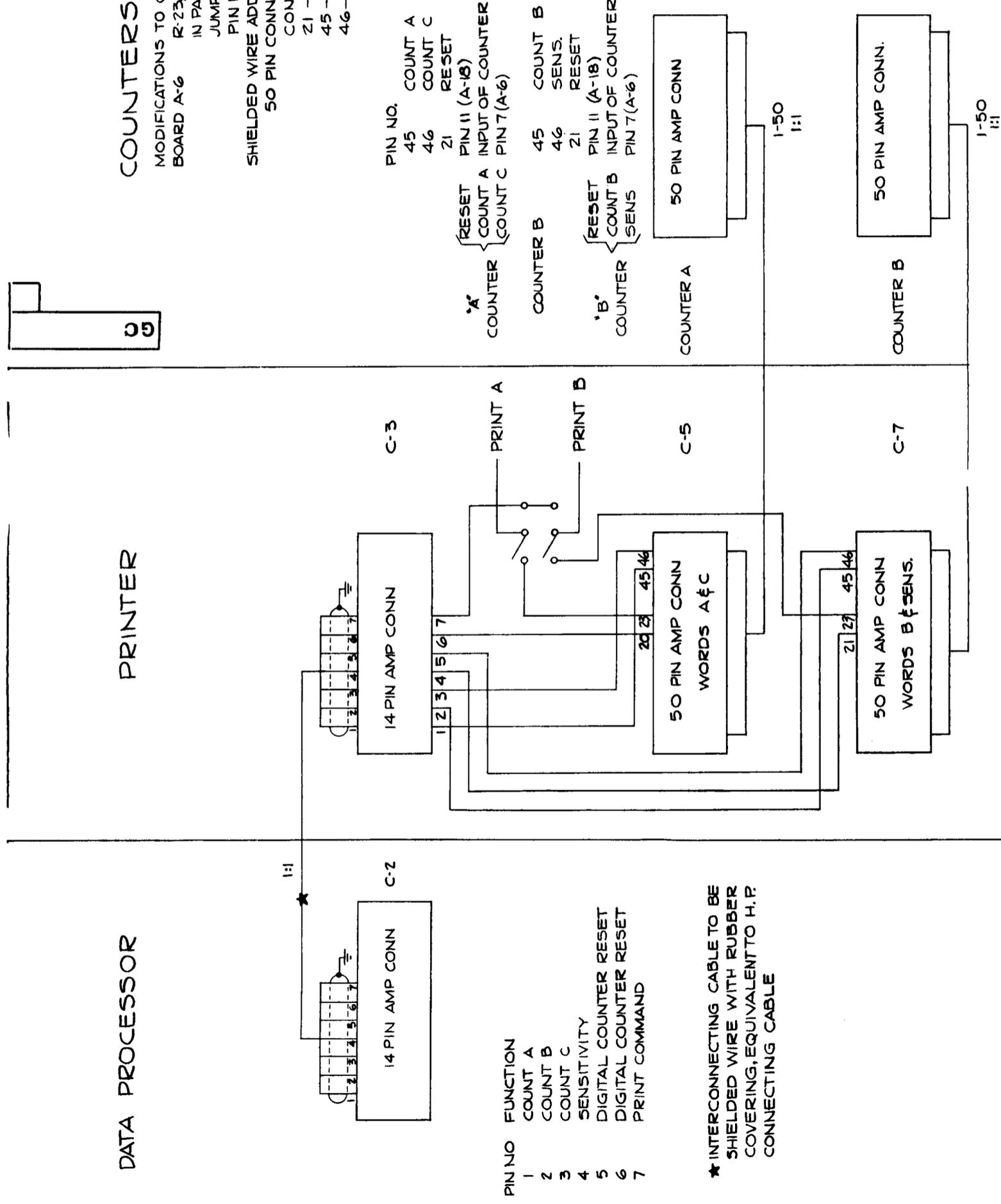Figure 23—Programming (GD-EGO-1109652)

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Figure 24—Power (GD-EGO-1109650)

Figure 25—Interconnecting Cabling
(GD-EGO-1109651)

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