Electrical Property Modelling of Photodiode Type CMOS Active Pixel Sensor (APS)

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Abstract— **In this research, few electrical characteristics of photodiode (PD) type CMOS Active Pixel Sensor (APS) pixel were modeled. BSIM3v3 threshold voltage equation was simplified for hand calculation with better than 2% peak-to-peak error for full back-gate bias and supply voltages for CMOS process technologies that has minimum feature sizes between 0.18μm and 2.0μm. Two fitting function coefficients (FFC) were included in the BSIM threshold model equations for simplification of the equation. FFCs were extracted by using circuit simulation for given process. Using the simplified threshold equation, electrical characteristics of 3T CMOS PD-APS pixel were modeled. Models include; photodiode reset level, pixel amplifier signal range, and pixel reset level boosting factor. Models were evaluated by using wide variety of available CMOS process technologies and compared with the simulation results. Pixel reset level and signal range model equations produce better than 6% and 12% peak-to-peak accuracy with simple hand calculation, respectively. Models were also confirmed with a designed photodiode-type CMOS APS pixel. A CMOS photodiode type APS imager fabricated in a 0.5μm, 2P3M, 5Volt CMOS process with 15μm square pixel size was used for comparison.**

I. INTRODUCTION

In CMOS Active Pixel Sensor (APS) imagers [1], performance of the imaging pixel depends on the process technology parameters, process type, and the physical design rules of manufacturing process. Best pixel performance, thus, can be obtained by optimizing the process related parameters. However, considering most of the CMOS based image sensor companies do not have their own manufacturing facilities, and use foundry services, it is necessary to develop technology based models for evaluating individual processes and to optimize electrical and physical performance of imaging pixel.

In this research [2], few electrical parameters of photodiode (PD) type CMOS Active Pixel Sensor (APS) pixel were modelled for hand calculation by using modified BSIM3v3 model equations [3]. BSIM3v3 threshold voltage equation was simplified for hand calculation for CMOS process technologies that has minimum feature sizes between 0.18μm and 2.0μm.

II. HYBRID THRESHOLD VOLTAGE MODEL

A CMOS active pixel sensor (APS) contains a number of NMOS transistors in each pixel. Theses transistors are used either as a switch or as an active amplifying element. In a typical three transistor (3T), photodiode type CMOS APS pixel, one transistor (M1) is used to reset the photosensitive region (PD) and other two are used as access switch (M3) and as amplifying element (M2), Figure 1.

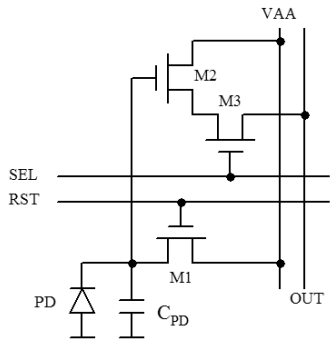

Figure 1. CMOS Active Pixel Sensor (APS) pixel schematic.

Typical timing diagram of 3T CMOS APS pixel is shown in Figure 2. Scene integration starts when photodiode is reset at time T1 through the reset transistor, M1. During integration, photodiode voltage (V_{PD}) drops because of the photogenerated charges. During readout, pixel access transistor (M3) is turned on, and photodiode voltage is sampled (SHS) on a column sample-and-hold circuits. Next, reset transistor (M1) is turned on to start next integration period, and the reset level of the photodiode for correlated double sampling operation (SHR) is sampled at time T2. Thus, the integration time is defined by the time difference between T1 and T2.

Reset transistor (M1) is typically sized to have the minimum allowable feature size to maximize pixel fill factor, and to reduce charge injection to the photosensitive region after reset operation. During operation, all transistors have very large back-gate biases which severely modulate threshold voltage of each transistor depending on photodiode voltage. This is mainly because; NMOS transistors are used

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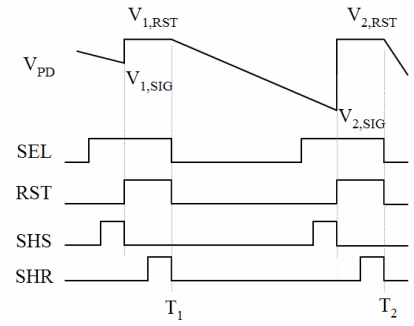

Figure 2. A typical 3T CMOS APS pixel timing diagram.

in typical 3T CMOS APS pixel, and the photodiode reset voltage is close to the supply voltage, VAA. These signal dependent threshold fluctuations results in variations in photodiode reset level and pixel amplifier gain.

Threshold voltage and other physical parameters of MOS transistor are well defined and modeled for circuit simulators [3,4,5]. However, it become increasingly complicated to hand calculate the threshold voltage accurately because the numbers of model parameters were increased dramatically when the device sizes were shrank to deep-submicrometer levels.

A hybrid MOS threshold model equation was proposed [2] based on BSIM3v3 model equations [3] for simple and accurate representation of back-gate bias effect on the threshold voltage. In the hybrid model, it was assumed that the MOS transistor has one to three times the minimum width (W_{min}) and has a minimum channel length (L_{min}). Threshold voltage of an NMOS transistor is given in (1), [3].

$$V_{TH} = V_{TH0} + K_1 \cdot \left(\sqrt{\Phi_S + V_{SB}} - \sqrt{\Phi_S}\right) + K_2 \cdot V_{SB} + \Delta V_{TH} \quad (1)$$

There are four terms in (1). First term (V_{TH0}) is the zero back–gate bias threshold voltage, and can be determined by means of simulation or provided by foundry. It includes all of the built–in potentials and zero back–gate bias conditions for non–uniform substrate doping profile. Uncovered charges in the doping profile in the first term are covered by the second and third terms. First and second order body-effect coefficients (K_1 and K_2) are used to determine these terms. Last term, or the delta term (ΔV_{TH}), includes most of the short channel effects, and has significantly complicated model equations and large number of model parameters. It includes lightly doped drain (LDD) effect, narrow width with short channel expressions, charge sharing, and drain induced barrier lowering (DIBL) effects. Back-gate bias voltage (V_{SB}) is incorporated in the second, third, and forth terms. Φ_S is the surface potential.

It is very complicated to determine the delta term in (1) with simple hand calculation because of the number of model parameters involved. This term is function of parameters K_1, K_2, V_{SB}, Φ_S, W, and L. In case of fixed L and W, delta term can be distributed between the second and third terms of (1) with two fitting function coefficients (FFCs) as shown in (2)

$$V_{TH} = V_{TH0} + K_1 \cdot (1+\eta_1) \cdot \sqrt{\Phi_S + V_{SB}} - K_1 (1+\eta_2) \cdot \sqrt{\Phi_S} + K_2 \cdot V_{SB} \quad (2)$$

The η_1 and η_2 are the FFCs. They are determined through the simple circuit simulation. They are valid for any back-gate bias voltages and limited device sizes. Simulation setup shown in Figure 3 was used to determine FFCs.

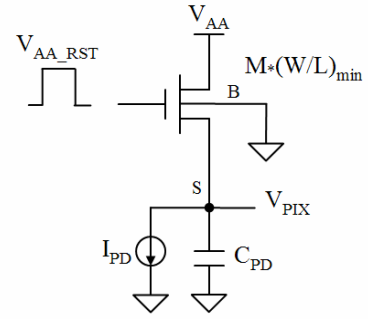

Figure 3. Simulation setup to determine fitting function coefficients (FFC), η_1 and η_2.

Simulation setup composes of an NMOS transistor connected between pixel supply voltage (V_{AA}) and photodiode node (S). Capacitor (C_{PD}) represents the diffusion and other parasitic capacitances of the photodiode. Current source (I_{PD}) represents the photo generation current.

A transient simulation was performed to determine FFCs. The gate of the reset transistor pulsed from ground to V_{AA_RST} in where V_{AA_RST} is equal or larger than the pixel supply voltage, V_{AA}. After reset level is settled on node (S), reset pulse is turned off, allowing the photo generation current (I_{PD}) to discharge the photodiode node capacitance (C_{PD}). During discharge, few voltage points were collected on node (S). The delta term in (1) was calculated for minimum size transistor and plotted against the body factor term ($\sqrt{\Phi_S + V_{SB}}$) as shown in Figure 4 for a 5Volt, 2P3M, 0.5µm CMOS process for multiple M values. A first order linear fit function was then used to determine the FFCs. The η_1 represents the slope of the linear fit line where the η_2 represents the offset.

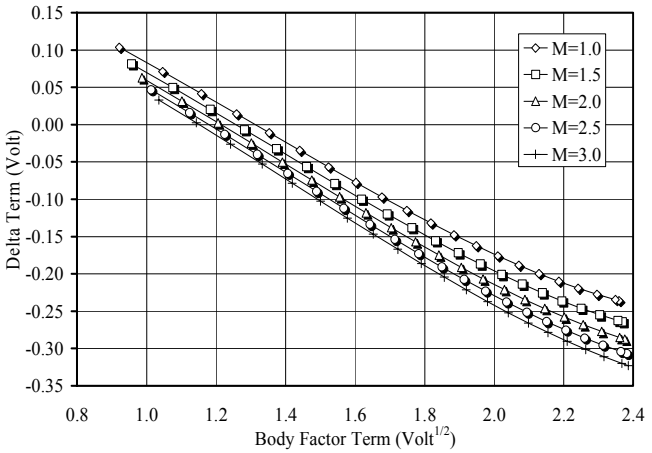

Figure 4. Delta term (ΔV_{TH}) versus the body factor term ($\sqrt{\Phi_S + V_{SB}}$) for ($L=L_{min}$).

After FFCs were determined, the threshold voltage can easily be calculated by using (2) for any back-gate bias condition with certain level of error. The delta term versus the device size for fixed channel width is shown in Figure 5. The delta term less depends on the channel width than the channel length, [2]. The slope term (η_1) varies twelve percent (12%) or less for device multiplication factor of three or less (M<3) for minimum channel length NMOS transistor. Under same conditions, the offset term (η_2) varies only four percent (4%). Both terms vary drastically if the channel length is increased and channel width is set to minimum.

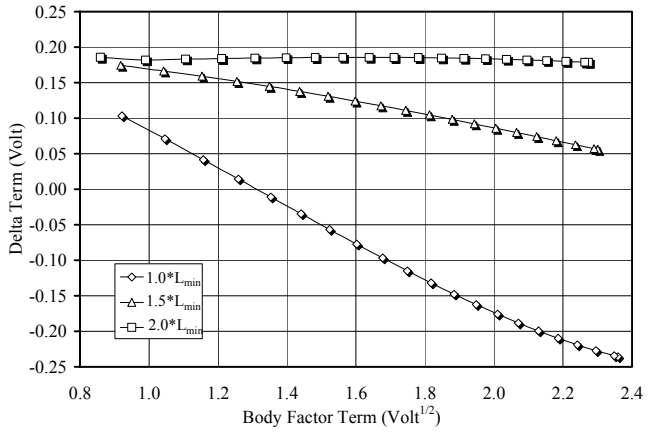

Figure 5. Dependency of delta term (ΔV_{TH}) on channel length ($W=W_{min}$).

Hybrid threshold model FFCs were determined for ten sub-micron CMOS processes that have been widely used by the fabless CMOS image sensor companies. Threshold model (2) was compared with the simulation results for all the processes, [2]. Threshold model (2) resulted in better than 3% peak-to-peak calculation error in full power supply range and beyond for the back-gate bias voltages of all the CMOS processes.

III. CMOS APS Pixel Reset Voltage Model

Reset level was modeled for photodiode type, 3T CMOS APS pixel composing of a photodiode, three NMOS transistors, and a common load transistor on the column bus as shown in the simulation setup in Figure 6.

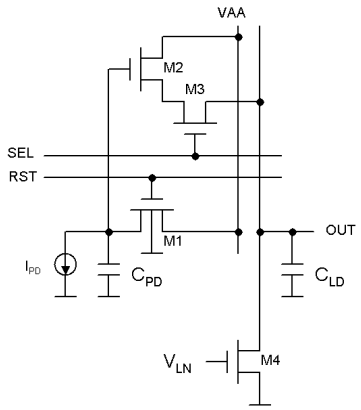

Figure 6. CMOS APS pixel simulation setup.

Load (M4) and buffer (M2) transistors form a source follower amplifier when the pixel select transistor (M3) was turned on. The photodiode (PD) node is reset to the pixel supply voltage (V_{AA}) through the reset transistor (M1). Transistor M1 turns off when the pixel PD node voltage reaches one threshold below the driving supply voltage (V_{AA_RST}) of reset pulse, RST. Typically, reset transistor (M1) is designed to have a minimum device size to increase the fill factor of the pixel and reduce the charge injection to the PD node after reset. Thus, the pixel reset level could be calculated accurately by using the hybrid threshold voltage (2). Back-gate bias voltage of reset transistor equals to the photodiode (PD) node voltage in all conditions. Threshold voltage of the reset transistor ($V_{TH,M1}$) is also modulated by the photodiode node voltage and changes when the pixel-reset signal is activated. Reset transistor goes into subthreshold operation regime when the photodiode node voltage exceeds its threshold voltage minus the driving supply voltage (V_{AA_RST}) of reset pulse.

$$V_{PD,RST} = V_{SB,M1} = V_{AA\_RST} - V_{TH,M1} \tag{3}$$

Photodiode reset voltage and the threshold voltage of the reset transistor can be found by substituting (3) in (2) and solving for $V_{SB,M1}$. It can be found as:

$$V_{PD,RST} = V_{SB,M1} = \Psi^2 - \Phi_S \tag{4}$$

$$\Psi = -\xi + \sqrt{\xi^2 + 2\cdot\xi\cdot\frac{(1+\eta_2)}{(1+\eta_1)}\cdot\sqrt{\Phi_S} + \Phi_S + \frac{2\cdot\xi\cdot(V_{AA\_RST} - V_{TH0})}{K_1\cdot(1+\eta_1)}} \tag{5}$$

$$\xi = \frac{K_1\cdot(1+\eta_1)}{2\cdot(1+K_2)} \tag{6}$$

Equation (4) defines the reset voltage of the pixel photodiode node for given technology parameters, FFCs, and the V_{AA_RST} level. Maximum achievable pixel reset voltage is set by the pixel supply voltage (V_{AA}). This can be achieved by setting V_{AA_RST} higher than the V_{AA}.

Reset level of the pixel and the threshold voltage of the reset transistor with minimum feature size were simulated by using the setup shown in Figure 6, and calculated by using the reset model equations (3) and (4). First, the PD reset level ($V_{PD,RST}$) was calculated by using reset model (4). Than, the threshold voltage of the reset transistor was calculated by using the (3). Finally, the error was determined between simulation and calculation results for both. Pixel reset pulse, RST, was driven by different voltage levels (V_{AA_RST}) to allow reset transistor to charge the pixel photodiode node up to pixel supply voltage (V_{AA}). Pixel reset level calculation errors are shown in Figure 7 for different CMOS processes. Error represents the difference between the reset level calculation by using (4) and the reset level found by using the circuit simulator. The reset model (4) estimates the pixel reset level with better than 6% (peak-to-peak) accuracy for different reset pulse levels (V_{AA_RST}) and process technologies.

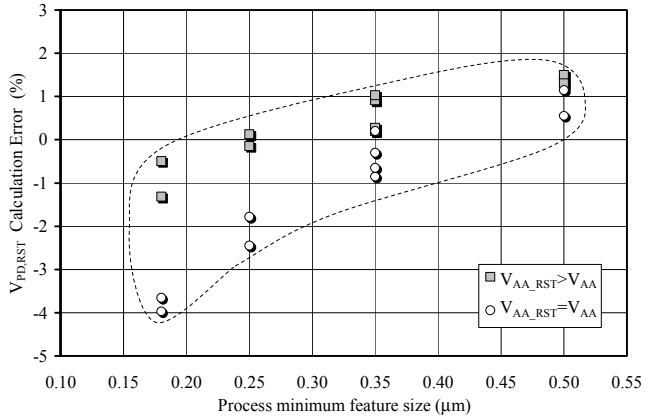

Figure 7. Pixel reset level calculation error versus CMOS processes.

Threshold voltage calculation errors are shown in Figure 8 for the CMOS processes. Error represents the difference between the threshold calculation by using (3) and the threshold level found by using the circuit simulator. Threshold model (3) estimates the threshold voltage with better than 2% (peak-to-peak) accuracy for different reset pulse levels, and processes.

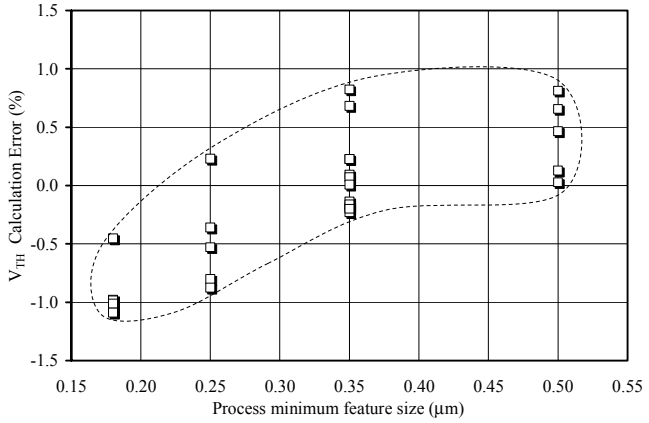

Figure 8. Threshold voltage calculation error versus CMOS processes.

Calculated reset voltages for the CMOS processes are shown in Figure 9. If driving supply voltage level of the pixel reset signal is set to pixel supply voltage level, (V_{AA_RST}=V_{AA}) then almost 30% of the pixel signal range is lost due to the incomplete reset operation. This signal range loss could be recovered by boosting the reset pulse level (V_{AA_RST}) to higher than the pixel supply voltage (V_{AA}). Boosting amount was described as a fraction of zero-bias threshold voltage (V_{TH0}). It was called boosting factor (B). Optimum boosting factor to reset photodiode node to pixel supply voltage was found to be in between 1.5 and 2.0 times the zero-bias threshold voltages of the processes. In general, relation between minimum feature size, supply voltage and the boosting factor was found to be:

$$B = \frac{1}{4} \cdot V_{AA} \cdot L_{min} + 1.5 \tag{7}$$

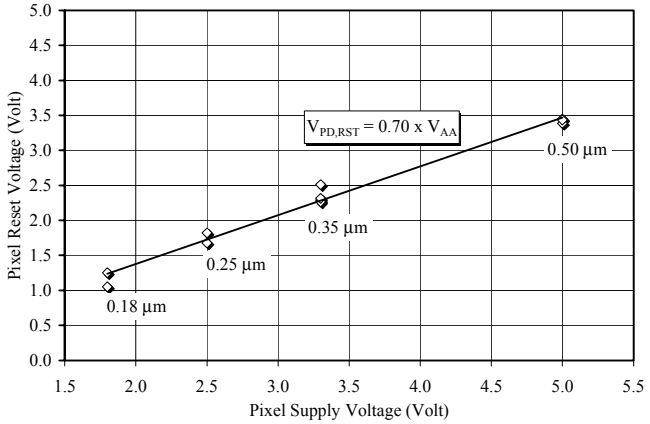

Figure 9. Photodiode FD reset voltage with no boosting on RST signal.

IV. CMOS APS Minimum Pixel Voltage Model

In 3T photodiode type CMOS APS pixels, pixel signal range is limited by the pixel amplifier's ability to buffer photodiode node voltages. Buffering high photodiode node voltages are not a limiting factor for the source follower amplifier, if NMOS devices were used in the pixel. Highest photodiode node voltage is set by pixel supply voltage (V_{AA}) and driver supply voltage (V_{AA_RST}) of the reset pulse. Lowest input limit is set by the threshold voltage of buffer transistor (M2). It goes out of linear operation range when the pixel photodiode node voltage drops below the threshold voltage of this transistor. Large signal input-output transfer function of the pixel source follower amplifier could be written when the transistors M2 and M4 are working in saturation with (8).

$$V_{OUT} = V_{PIX} - V_{TH,M2}(@\, V_{SB,M2} = V_{OUT}) \tag{8}$$

In this equation, threshold voltage of the buffer transistor, M2, is modulated by the output voltage. Considering this effect, the output voltage can be written as a function of the pixel photodiode node voltage with the following equations.

$$V_{OUT} = V_{SB,M2} = \Omega^2 - \Phi_S \tag{9}$$

$$\Omega = -\xi + \sqrt{\xi^2 + 2 \cdot \xi \cdot \frac{(1+\eta_2)}{(1+\eta_1)} \cdot \sqrt{\Phi_S} + \Phi_S + \frac{(V_{PIX} - V_{TH0})}{(1+K_2)}} \tag{10}$$

Absolute minimum photodiode node voltage ($V_{PIX,MIN0}$) that can be buffered by the source follower can be found from the (9) by setting the output voltage to zero and extracting the pixel voltage (V_{PIX}). Linear gain range of the pixel source follower, on the other hand, ends at the operation point where the output voltage equals to overdrive voltage range of load transistor (M4). Thus, the $V_{PIX,MIN0}$ value could be calculated with the following equation.

$$V_{PIX,MIN0} = 2 \cdot \xi \cdot \left[\frac{\eta_1 - \eta_2}{1+\eta_1} \right] \cdot \sqrt{\Phi_S} \cdot (1+K_2) + \Phi_S + V_{TH0} \tag{11}$$

Minimum pixel photodiode node voltage could be found by adding overdrive voltage of the load transistor to (11).

$$V_{PIX,MIN} = m \cdot V_{TH0} + V_{PIX,MIN0} \quad (12)$$

where m is the overdrive voltage ratio of the load transistor. Minimum photodiode node voltages for the CMOS processes were calculated by using (12) and compared with the simulation results. Simulation was performed by using the setup shown in Figure 6 with minimum feature size transistors. During simulation, overdrive ratio of the load transistor was set between 0.1 and 0.8, effectively setting the column bias current between 1 and 25 µA. It was found that the overdrive ratio (m) should be set to about 0.3 and 0.5 to have 5 µA and 10 µA column current, respectively. It was found that the (12) estimates the minimum pixel voltage that can be linearly buffered by the pixel source follower amplifier with ±7% accuracy over wide range of process technologies and column bias currents.

V. CMOS APS PIXEL SIGNAL RANGE MODEL

Pixel photodiode node voltage range that can be buffered by the pixel source follower amplifier depends on device sizes of pixel source follower, overdrive voltage of the load transistor, power supply voltage used to drive the reset transistor, and transistor's process related parameters. If there was no boosting applied to the reset pulse, than the pixel signal range could be calculated by subtracting (12) from (4). If an optimum boosting voltage (V_{AA_RST}) applied to the reset pulse in where pixel's photodiode node is reset to pixel supply voltage (V_{AA}), than the pixel signal range can be calculated by subtracting (12) from the pixel supply voltage (V_{AA}). Thus, the pixel voltage range (V_{PR}) could be written with following equation.

$$V_{PR} = V_{PD,RST} - V_{PIX,MIN} \quad \text{(No boosting)} \quad (14)$$

$$V_{PR} = V_{AA} - V_{PIX,MIN} \quad \text{(Optimum boosting)} \quad (15)$$

Pixel voltage ranges for the CMOS processes were calculated by using model equations (14) and (15) for no-boosting and optimum boosting conditions at 5µA column bias current. Supply voltage of each process, and the calculation results are shown in Figure 15. If no boosting was applied to the reset pulse, then the pixel voltage range is around 50% of the supply voltage of the process. When the optimum boosting was applied, this range increases 80% of the supply voltage. Even with 1.8 volt supply voltage, a 1.0 volt pixel voltage range could be achievable if the boosting is adapted. For no boosting condition, pixel voltage range drops around 0.5 volt.

Pixel voltage range is related to the column current. It is because the minimum pixel voltage range is directly related to the overdrive voltage of the load transistor. Increasing overdrive voltage results in increase in the column current and reduction in the pixel signal range. Optimum bias current has to be determined for the image sensor architecture to satisfy best speed and noise performance and the pixel signal range during the design process.

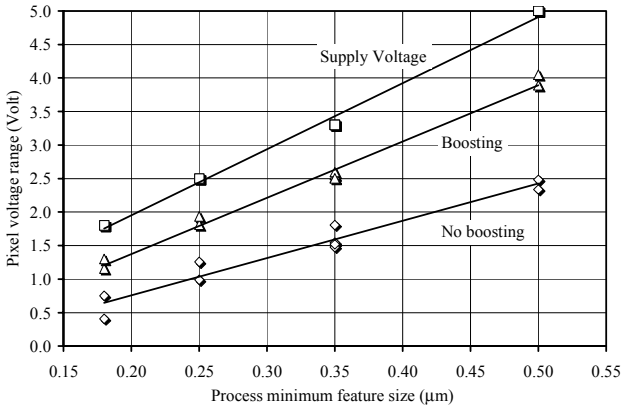

Figure 10. Pixel signal range for optimum boosting and no boosting.

Reset feedthrough effect becomes significant when the pixel photodiode capacitance is comparable to the size of the reset transistor's gate to source overlap capacitance. This effect also increases when the reset signal is boosted.

VI. MEASUREMENTS AND CONCLUSIONS

A 3T CMOS photodiode type APS imager with 15µm square pixel size was used to verify the models. Other parameters of the imager were reported in [6]. A 0.5µm, 2P3M, 5Volt CMOS process was used for the design. Reset level and signal range of the pixel was measured directly. It was found that the model equations predict the measurement results with less than 10% accuracy.

In conclusion a hybrid threshold voltage equation was proposed for minimum feature size MOS transistors with two fitting function coefficients. Based on the new model equations few pixel properties of CMOS APS were determined for hand calculation including pixel reset level, pixel signal range, and boosting factor. Model equations were also confirmed with measurement results.

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