Electromigration-induced extrusion failures in Cu/low-*k* interconnects

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Electromigration experiments were conducted to investigate the thresholds required for electromigration-induced extrusion failures in Cu/low-*k* interconnect structures. Extrusions at the anode were observed after long periods of void growth. Characterization of failure sites was carried out using scanning and transmission electron microscopy, which showed that failures occurred through delamination at the interface between the silicon-nitride-based capping layer diffusion barrier and the underlying Cu, Ta liner, and interlevel dielectric (ILD) materials. This interface is subjected to near tensile (mode I) loading with a mode mixity angle between 4° and 7°, estimated using finite-element-method analysis, as electromigration leads to a compressive stress in the underlying Cu. Comparisons of the fracture toughness for interfaces between the capping layer and individual underlayer materials indicate that the extrusion process initially involves plane-strain crack propagation. As Cu continues to extrude, the crack geometry evolves to become elliptical. An analysis of the critical stress required for extrusions based on these observations leads to a value of approximately 710 MPa, which agrees well with the value determined through estimation of the volume of material extruded and the required stress to accomplish this extrusion. The analysis of the critical stress required for extrusion formation also indicates that sparsely packed, intermediate to wide interconnect lines are most susceptible to electromigration-induced extrusion damage, and that extrusion failures are favored by ILDs with low stiffness (low elastic moduli) and thin liners, both of which are needed in future interconnect systems. *© 2008 American Institute of Physics*.
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I. INTRODUCTION

Reduction of resistance-capacitance (*RC*) delay in high-performance integrated circuits (ICs) requires the use of Cu interconnects with low-dielectric-constant (*k*) interlevel dielectric (ILD) materials. Accurate assessment of the reliability of Cu/low-*k* interconnects is imperative, due to the ever-increasing total interconnect length, reduced interconnect cross-sectional dimensions, and increasing operating current densities required in future technology.[1] Electromigration, current-induced atomic diffusion due to momentum transfer from conducting electrons, is one of the major reliability concerns for Cu/low-*k* metallization.

In general, low values of *k* are correlated with low values of the elastic modulus. Therefore, as ILDs with lower *k* values are used in IC technology, a decrease in the overall stiffness in the materials surrounding Cu wiring is expected. Consequently, the thresholds required for electromigration-induced failures decrease as well, because the rate of electromigration depends not only on the current density and the intrinsic diffusive response of the interconnect, but also on the mechanical properties of the materials that surround the Cu wiring, including the ILD. Failure can occur either by formation of voids that lead to unacceptable resistance increases, or due to extrusion of Cu, leading to shorts with neighboring lines. Quantitative experimental and modeling analyses of the effects of mechanical properties on failures by electromigration-induced void growth have been described by Hau-Riege *et al.*[2] and Wei *et al.*[3] Observations of extrusions in Cu/Methylsiloxane (MSQ) and Cu/organic ILD interconnects have also been reported by Lu *et al.*[4] However, the critical stress required for extrusion of Cu in a Cu/low-*k* system has not been determined through experiments or modeling analyses. In this paper, we present detailed analyses of the thresholds required for electromigration-induced extrusion failures, as observed in experiments, and of the dependencies of the critical stress for extrusion failure on the layout and mechanical properties of Cu/low-*k* interconnect systems.

II. ELECTROMIGRATION AND THE EFFECTIVE MODULUS *B*

In via-terminated dual-damascene Cu/low-*k* interconnects, the refractory metal liners, usually Ta-based, at the base of vias do not electromigrate. Therefore, the vias serve as boundaries that block electromigration. As electromigration takes place inside interconnects, the electron wind force causes Cu atoms to deplete near the cathode end and to ac-

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cumulate near the anode end. These changes in atomic concentration dC_a/C_a are related to changes in stress $\partial\sigma$ by[5]

$$\frac{dC_a}{C_a} = -\frac{\partial\sigma}{B}. \tag{1}$$

Here, C_a is the atomic concentration, which is the difference between the lattice site concentration,C_l, and the vacancy concentration C_v,[9] σ is the hydrostatic stress in the metal, and B is the overall effective bulk modulus of the Cu/ILD materials system, which is a function of the moduli and dimensions of all the materials surrounding the metal, including the liner, the ILD, and the capping layers. B is determined using finite-element-method (FEM) modeling.[6] As the modulus of the ILD decreases, B decreases also.

A depletion of atoms generates a tensile stress, while an accumulation of atoms generates a compressive stress [see Eq. (1)]. As electromigration proceeds inside interconnects, the changes in the local atomic concentration cause changes in the local chemical potential. Since electromigration occurs through a vacancy exchange mechanism, the chemical potential function can be expressed as $(\mu_0+\Omega\sigma)$,[7] where μ_0 is a reference potential and Ω is the atomic volume. The chemical potential gradient $\Omega(\partial\sigma/\partial x)$ in one dimension corresponds to a back-stress force opposite to the electron wind force, whose magnitude is intimately related to B. Therefore, electromigration in a via-terminated segment can be described by[5,8–10]

$$J_a = \frac{D_{\text{eff}}C_a}{kT}(F_{e\text{-wind}} + F_{\text{back}}) = \frac{D_{\text{eff}}C_a}{kT}\rho|j|z^*q + \frac{D_{\text{eff}}C_a}{kT}\Omega\frac{\partial\sigma}{\partial x}, \tag{2}$$

and

$$\frac{\partial\sigma}{\partial t} = \frac{\frac{\Omega}{kT}\frac{\partial}{\partial x}\left[D_{\text{eff}}C_v\left(\frac{z^*q\rho j}{\Omega} + \frac{\partial\sigma}{\partial x}\right)\right]}{\frac{C}{B}\left(1 + \frac{B\Omega}{kT}\frac{C_v}{C}\right)}, \tag{3}$$

where J_a is the atomic flux, D_{eff} is the effective diffusivity, ρ is the resistivity, j is the current density, z^* is the effective valence of the atoms, q is the fundamental charge, k is Boltzmann's constant, T is temperature, and x is a spatial dimension along the length of an interconnect segment. Since the effective diffusivity depends on σ,[9] Eq. (3) is nonlinear and can only be solved numerically. We have developed a MATLAB-based solver, XSIM, which uses the backward Euler finite-discretization method to obtain numerically stable solutions for time-dependent C_a and σ spatial distributions.[10]

If the blocking boundaries do not fail under the stresses that develop inside the interconnect, the electron wind and back-stress forces will come into balance, resulting in a steady state for which

$$\Omega\frac{\Delta\sigma_{\max}}{L} = z^*q\rho j, \tag{4}$$

where $\Delta\sigma_{\max}$ is the difference between the stress at the anode and the cathode and L is the length of the segment. Usually, the critical stress required for void nucleation, $\sigma_{\text{crit.,nuc}}$, is much smaller than the critical stress for metal extrusion, $\sigma_{\text{crit,ext}}$. Therefore, once a void has nucleated at or near the cathode, all tensile stress in the segment will relax and $\Delta\sigma_{\max}$ will become equal to the compressive stress at the anode. From Eq. (1), it can be seen that as B decreases, the stress gradient that opposes electromigration, the back-stress force, is reduced. The material surrounding the anode end of an interconnect segment will therefore experience an increase in strain for a given amount of transported material. Therefore, $\sigma_{\text{crit,ext}}$ is expected to decrease as B decreases.

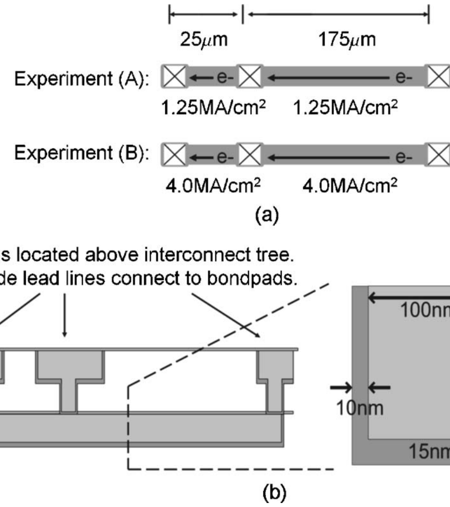

FIG. 1. (a) Top-view illustrations of the interconnect test structure. The arrows indicate the direction of electron transport and the current density in the two sets of experiments. Though a via was present 25 μm from the anode end of the line, the lines were stressed at a constant current density along the full length of the 200 μm long lines. Both experiments were performed at 325 °C. (b) Side and cross-sectional views of the Cu/low-*k* interconnect test structure.

III. EXPERIMENTS AND RESULTS

We performed package-level electromigration experiments using interconnects fabricated by Advanced Micro Devices (AMD). The experimental details, including the descriptions of the low-*k* ILD and the dimensions of the features, are the same as those described in Ref. 3. Figure 1 shows a schematic layout of the test structures, as well as an illustration of the testing conditions for experiments A and B. While these test structures had three vias, including one located 25 μm from the anode, only the vias at the ends of the lines were used in the experiments to be discussed in this paper. In this case, the tests were equivalent to testing of via-terminated segments of 200 μm length, at either an electron current density of 1.25 or 4.0 MA/cm^2. The results discussed here were part of a larger set of experiments on multisegment interconnect structures.[3]

A. Failure statistics and resistance profiles

Qualitau MIRA electromigration testing systems were used to perform experiments A and B at 325 °C. Figure 2 shows the time-to-failure results plotted on a lognormal graph with linear fits. Here, the criterion for failure was a 10% increase of the initial resistances (10%ΔR_0), a com-

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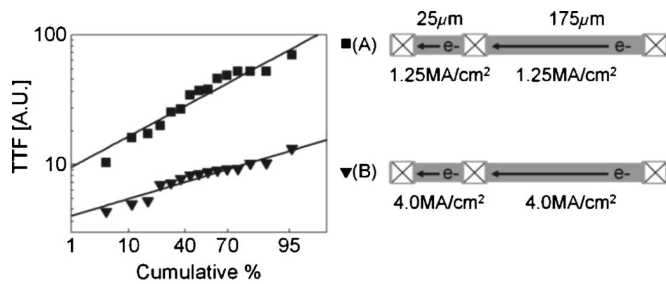

FIG. 2. Times to failure determined using a $10\%\Delta R_0$ failure criterion for experiments A and B, plotted on a lognormal graph with linear fits to the data. The ordinate is normalized to arbitrary time units (AU). Both tests were carried out at 325 °C.

monly used convention. The absolute time unit for the ordinate in Fig. 2 has been rescaled to arbitrary units (AU).

Figures 3(a) and 3(b) show the resistance versus time (R versus t) traces for all the samples in experiments A and B, respectively. The resistances were measured over the entire lengths of the 200 μm long lines. Figure 3(c) shows a single typical R versus t curve from experiment B. Similar R versus t traces were also observed for all the samples in the larger sets of experiments on multi-segment interconnect structures.[3] In all cases, the initial resistance of the interconnect segment remained almost constant at R_0 until time t_0, at which point a rapid increase in resistance of 50–100 Ω occurred. This "jump" in resistance was almost always sufficiently large to satisfy the $10\%\Delta R_0$ failure criterion. The jump is followed by a period of steady increase in the resistance, characterized by a constant slope dR/dt. Both experiments A and B were continued long after the $10\%\Delta R_0$ failure criterion had been reached: more than 1000 hr in experiment A and close to 1000 hr in experiment B. However, no abrupt open-circuit failures were observed for any line in either experiment. In both experiments A and B, dR/dt decreased after the abovementioned linear regime, which occurred a long period of time beyond t_0 [see Figs. 3(a)].

The R versus t behavior discussed here is usually associated with void growth and has been observed in other investigations.[11–13] However, it is very unusual for void growth not to lead to open failure in such long segments. Also, while a decreasing dR/dt is sometimes observed in experiments on short lines that are approaching a force balance, this is not expected for lines of 200 μm in length.

B. Microscopic analysis of the cathode end of the lines

We performed failure analyses near the cathode on nearly half of the populations in both experiments A and B, using a focused ion beam/scanning electron microscope (FIB/SEM). In all cases, very large voids that almost entirely spanned the cross section of the interconnect segments, rather than slit-like voids forming directly below the cathode via, were observed near the cathode, as shown in Figs. 4(a)–4(d). The increases in the final resistance of the samples correlate well with the observed void lengths (see the normalized R versus t plots in Fig. 4 as examples). The resistance-per-void-length ratio is consistent among all the samples subjected to failure analysis, and also agrees with the expected resistance increase based on calculations using the reported electrical resistivity for Ta-based refractory thin films[14] and the cross-sectional geometry of the line [Fig. 1(b)].

The unusually high resistances and correlated large void sizes attained here suggest that the electron flux has shunted over long lengths of the Ta-based liner without causing sufficient Joule heating to lead to open-circuit failures. Furthermore, this observation also indicates that copious amounts of Cu must have electromigrated toward the anode end in both experiments A and B, which should lead either to very high compressive stresses, or to Cu extrusions. During failure analysis, we did not observe any damage to the Ta-based liner, such as evidence of melting or fracture, even when extremely large voids had formed (9.5 and 11 μm long in

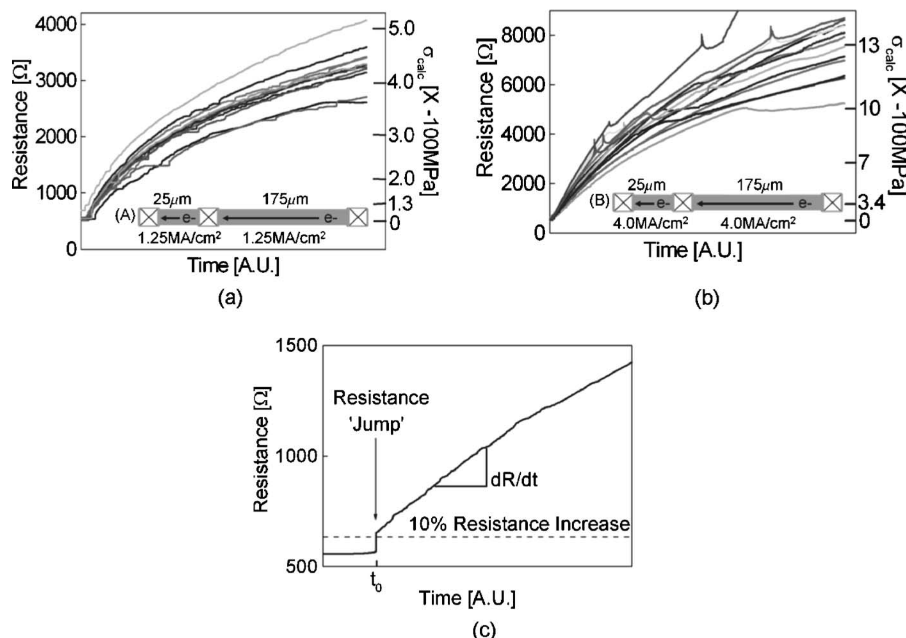

FIG. 3. In all experiments associated with the interconnect structure used, including those presented in Ref. 3, the R vs t plots had similar features. (a) and (b) are the R vs t plots for experiments A and B, respectively. (c) shows a single representative R vs t plot, along with labels of its key features. Calculated compressive stresses shown on the right axis of each plot are based on the assumption that there have been no extrusions.

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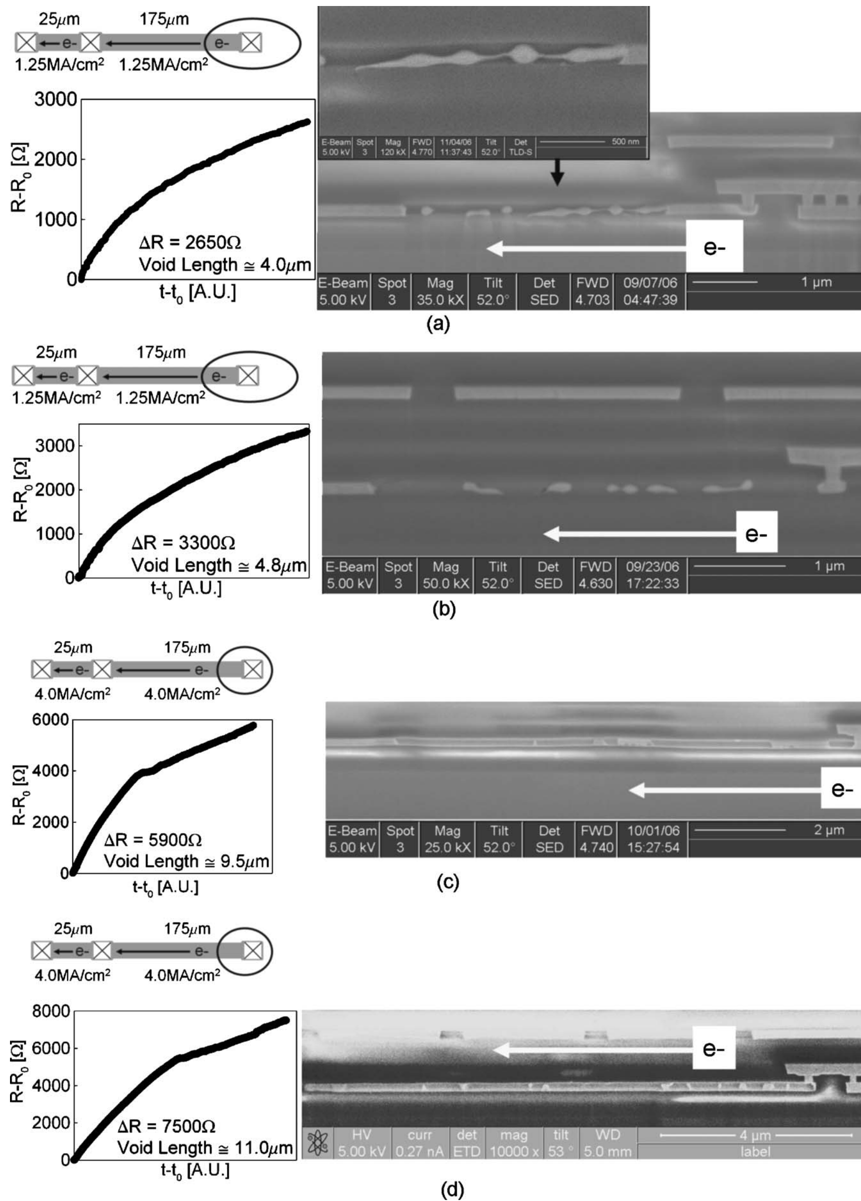

FIG. 4. SEM micrographs near the cathode end of tested interconnect segments sectioned using an FIB. All parts show images of large voids, along with measured void lengths, the overall resistance increase, and the corresponding normalized resistance traces. In all cases, as in the cases for all other samples subjected to failure analysis, no damage to the Ta-based liner was observed. (a) and (b) show Cu in the void region in the form of dewetted nanoparticles or chains of nanoparticles, respectively. (c) and (d) show two voids that are >10 μm in length, and fully span the cross section of the line.

Figs. 4(c) and 4(d), respectively). However, on occasion, Cu residues in the voids were observed to have morphologies that suggested high temperatures had been reached in the voids, presumably due to resistive heating of the refractory metal liner. Figures 4(a) and 4(b) show such cases, in which some of the Cu in the voided region dewetted to form nanoparticles or a nanoparticle "chains." This morphology, seen in Figs. 4(a) and 4(b), implies that the Cu wire was beading through a Rayleigh-like instability,[15,16] which requires high atomic mobilities and therefore relatively high temperatures, though not temperatures above the melting temperature of Cu.

IV. DISCUSSION

The unusual robustness of the Ta-based liners used in these experiments allowed continued electromigration well beyond the $10\%\Delta R_0$ failure criterion. As discussed in Ref. 3, the linear dependence of R on t, observed following the resistance jumps, can be used to determine kinetic parameters for the electromigration process, giving $(Dz^*)_{0,\text{eff}}=3.9\times10^{-10}$ m^2/s and $z^*=0.40\pm0.12$.[3]

Applying these kinetic parameters in numerical solutions of Eqs. (2) and (3) using XSIM,[10] the amount of Cu transported toward the anode and the corresponding stress increase at the anode can both be calculated. The time-dependent changes in C_a near the cathode can be correlated with a void volume, which can be translated to an increase in resistance of the test structure by assuming that the void fully spans the width and thickness of the line (not including the Ta liner). Based on the assumption that no extrusion of Cu occurred, $\Delta\sigma_{\max}$ values of 0.51 and 1.64 GPa at the anode in experiments A and B, respectively, are predicted. While the decreasing slopes of the R versus t curves in Fig. 3 suggest that a steady state is being approached, it is unreasonable to expect that the liner and ILD could resist compressive stresses of these magnitudes without failure. Under a high compressive stress, the anode ends of Cu interconnects are likely to fail by one of the following four mechanisms:

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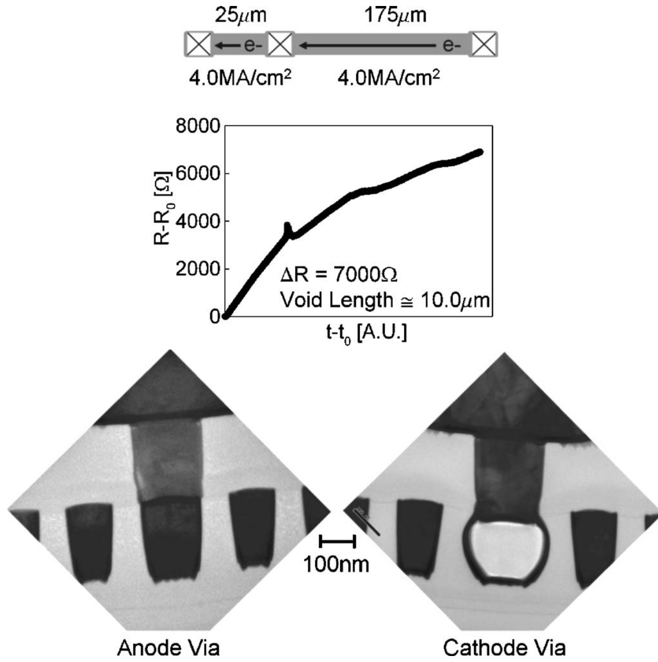

FIG. 5. TEM micrographs of cross sections perpendicular to the length axis of the line, at both the cathode and anode vias in a tested structure in which a 10 μm long void is expected from the observed resistance increase. The cathode via micrograph shows a fully voided region in the test line below the via, where the side walls have buckled, presumably due the vacuum-induced forces created when the void formed. Both micrographs show the liner to be continuous and intact at the base of the vias.

(i) liner rupture at the base of either the cathode or anode via,
(ii) volumetric expansion at the anode of the interconnect segment,
(iii) stress-induced Cu seepage through the thin refractory liner into the ILD, or
(iv) decohesion and Cu extrusion along the capping layer/ILD interface.

A. Failure analysis of the anode end

1. Mechanism (i)

Transmission electron microscopy (TEM) was used to determine if the liner membranes at the bottom of the vias had ruptured. Several samples containing very long voids (about 10 μm long) were selected based on either direct observation of the voids during failure analysis of the cathode end or through correlation with a large resistance increase during testing. Figure 5 shows the cathode and anode vias in a sample in which a 10 μm long void was expected. Here, the viewing plane of the TEM micrographs is perpendicular to the length axis of the test line. In addition to showing the vias located above the test structure, Fig. 5 also shows Cu dummy interconnect lines on either side of the test structure. There are ten, closely spaced, isolated dummy Cu lines (five on either side of the test line, see Fig. 6) that do not have any electrical lead lines connecting to the surface of the wafer. These lines have the same dimensions as those of the test segment, and are fabricated to emulate the packing density encountered in an actual IC at lower metallization levels. Figure 5 shows that underneath the cathode via, the side walls of the test structure buckled during the electromigration experiment. This may be due to surface forces associated with the vacuum created when the void forms. The TEM micrographs show that despite this buckling, the Ta-based barriers of the test structure around the void and the liner at the base of both vias are still continuous and intact. Since the magnitudes of the stresses are the highest at the terminal vias, and no damage to the liner was seen, these results suggest that mechanism (i) is not responsible for the transport of large amounts of Cu.

2. Mechanism (ii)

Though unlikely, because of the brittleness of the ILD and the Ta-based liner, the large amount of electromigrated Cu could, in principle, be accommodated by an increase in interconnect volume near the anode end. In order to determine if this behavior occurred, cross-sectional micrographs of the test structure under the same magnification were obtained at various length intervals (1–2 μm steps) approaching the anode via. No volumetric expansion was detected. As the cross-sectional viewing plane approached closer to the anode end, the cross-sectional areas of the test structure remained unchanged with respect to position along the length axis, as well as with respect to the nearby dummy lines that

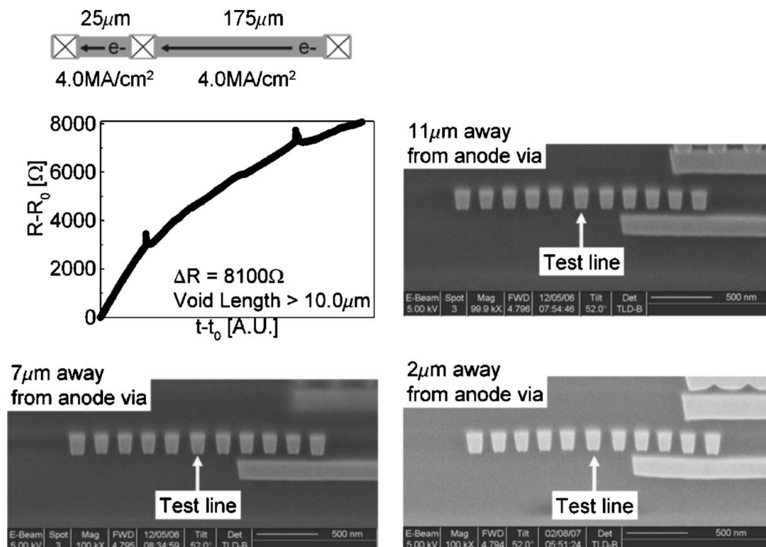

FIG. 6. SEM micrographs, at the same magnification, viewing FIB-sectioned surfaces normal to the length axis of a test line, at different distances from the anode via. The cross-sectional area of the tested interconnect is similar to those of the dummy Cu lines on either side, and does not change with distance from the anode via.

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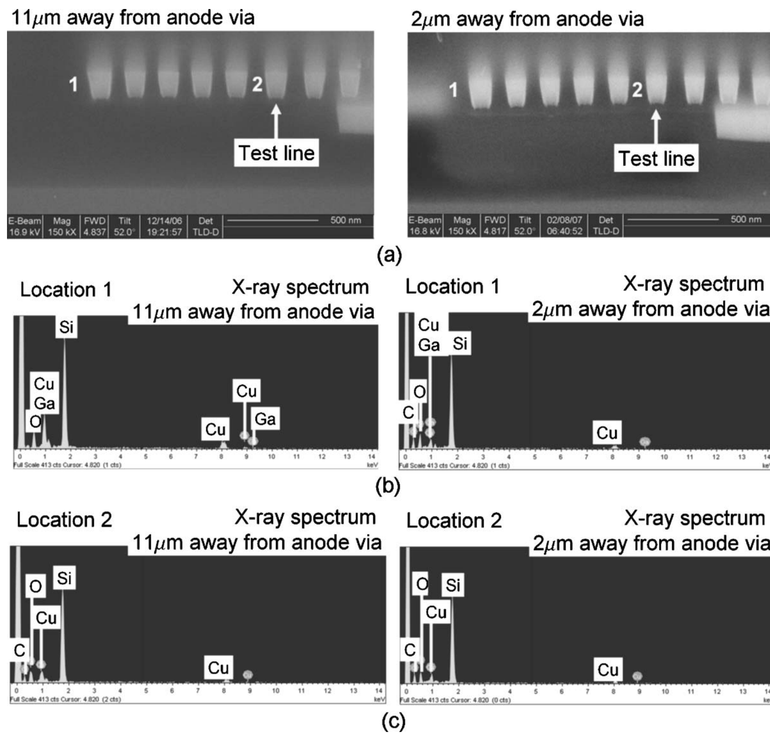

FIG. 7. (a) SEM micrographs at 11 and 2 μm away from the anode via in the same sample shown in Fig. 6, sectioned using an FIB. The sectioned plane contains two locations, 1 and 2, where EDX analyses were made. (b) and (c) contrast the EDX spectra generated at locations 1 and 2 on the two different section planes shown in (a).

were not subjected to electromigration. Examples of these observations are shown in Fig. 6, for a sample in which a void with length >10 μm was expected at the cathode. Therefore, mechanism (ii) also cannot account for the electromigrated Cu.

3. Mechanism (iii)

For all the samples subjected to the analysis of mechanism (ii), at each sectioning plane, chemical analyses at various locations in the ILD were performed using energy dispersive x-ray analysis (EDX). The spectra from different locations relative to the test structure, on the same sectioning plane, as well as the locations with the same relative distances to the test structure, on different section planes, were compared. The observed EDX spectra remained the same at all sampling locations. Figure 7(a) shows examples of two of the sampling locations in the ILD, positions 1 and 2, on two different FIB sectioning planes, 11 and 2 μm away from an anode via. Figures 7(b) and 7(c) show corresponding EDX spectra for the respective axial locations and cutting planes. Comparisons show that the size of the Cu spectral peaks generated at various positions remained unchanged in relation to those of Si, which is constant at all locations in the ILD. Additionally, the magnitudes of the Cu spectral peaks are similar to those of Ga peaks, the ion source of the FIB system. Therefore, the spectra are consistent with Cu being a minor impurity on the cross-sectional plane, as a result of either minute amounts of Cu leakage into the ILD or, most likely, due to redistribution of materials during the FIB sectioning process. Therefore, it does not seem likely that mechanism (iii) can account for the enormous amount of missing Cu.

4. Mechanism (iv)

Cu extrusions consistent with mechanism (iv) *were* observed in samples from experiment B (see Fig. 8), for which $\Delta\sigma_{max}$ was predicted to be 1.64 GPa, but not in samples from experiment A, for which $\Delta\sigma_{max}$ was predicted to be 0.51 GPa. The SiN-based capping layer decohered from the layer below, and Cu extruded from the test segment into the interfacial crack. This resulted in a thin patch of extruded Cu near the anode end, just below the capping layer. Cross-sectional TEM observations [see Fig. 8(b)] show that the Cu extrusions have a characteristic thickness of 30 nm. Also, based on the cross-sectional SEM micrographs containing the extruded Cu patch at known axial positions along the length of the test segments [see Fig. 8(c)], the shapes of the extrusion patches are estimated as elliptical, with a major axis of 2.5 to 3.0 μm and a minor axis of about 1.0 μm. Correspondingly, the volume of Cu extrusions is estimated to be 0.058 to 0.071 μm^3.

B. Failure-analysis-based assessment of $\sigma_{crit,ext}$

As mentioned previously, the changes in resistance recorded during the experiments correlate well with the sizes of the voids observed in failure analysis. A volumetric difference exists between the observed extrusion patch at the anode and the void near the cathode. This is the amount of Cu electromigrated upon reaching the critical stress for extrusion. Using XSIM, we calculated the compressive stress corresponding to such a volumetric difference, $\sigma_{crit,ext}=630$ MPa. This result is consistent with the fact that no extrusions were observed in samples from experiment A, in which the testing conditions produced an expected $\Delta\sigma_{max}$ less than 630 MPa.

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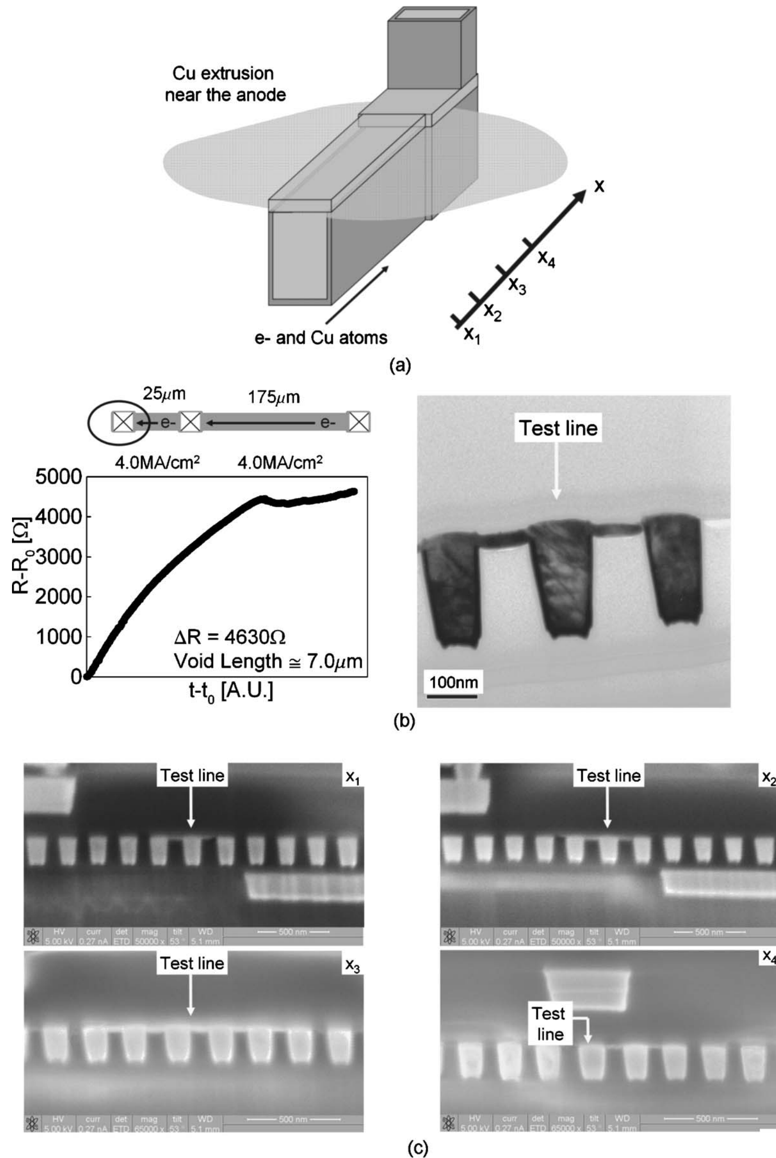

FIG. 8. (a) Schematic illustration of the Cu extrusion observed in a test line from experiment B. (b) TEM micrograph of the Cu extrusion formed in a structure where a 6.6 μm long void was expected. (c) Cross-sectional SEM micrographs, each showing the extrusion at one of four different locations sequentially closer to the anode via. The measurements of the width of the extrusion at the four locations enabled the determination of the shape of the extruded patch.

V. EFFECTS OF MECHANICAL PROPERTIES ON $\sigma_{\text{crit,ext}}$

Failure analysis of the extrusions suggests that they result from near tensile (mode I) loading of the interface between the capping layer with the underlying materials. (As to be shown in later sections, the mode mixity angle is determined to be $4°-7°$.) Once the loading leads to fracture at this interface, Cu extrudes into the crack. The effects of the mechanical properties of this interface on the critical stress for fracture, in this case on $\sigma_{\text{crit,ext}}$, are accounted for in the critical stress intensity factor, $K_{I,C}$. However, the appropriate expression for evaluation of $K_{I,C}$ depends on the geometry of the flaw by which the crack initiates.

A. The incipient crack flaw

Using the chevron-notched double cantilever beam test,[17] we determined the pure mode I critical energy release rate for the interface between Ta and SiN films. The Ta was deposited using e-beam evaporation onto SiN films, which had been deposited using plasma-enhanced chemical vapor deposition (PECVD). A Cu film was used as a "glue" layer between the Ta layer and the other Cu-coated cantilever. Using chevron-notched double cantilevers fabricated in this fashion, the critical strain energy release rate for decohesion at the Ta/SiN interface was estimated to be $G_{I,\text{crit}}(\text{SiN/Ta}) = 1.1\ \text{J/m}^2$.[18]

The critical energy release rate for the interface between carbon-doped SiO_2 (COD) low-k blanket films, with various values of k, with SiN films has been reported to be about $3.0\ \text{J/m}^2$,[19,20] determined using the four-point bending technique. Empirically, for mixed-mode interfacial cracking, like that produced in four-point bend tests, the critical energy release rate can be expressed as [21]

$$\Gamma = G_{I,C} \cdot [1 + \tan^2((1-\lambda)\cdot\psi)], \tag{5}$$

where ψ is the mode mixity angle and λ is an adjustable fitting parameter, usually between 0 and 1. For the four-point bending test-specimen geometry similar to that in Ref. 19 and 20, ψ has been reported to be $40°-45°$.[21–23] The limit $\lambda=1$ represents an "ideally brittle" interface with crack initiation occurring when $\Gamma = G_{I,C}$ for all mode combinations. This gives the possible range of $1.5\ \text{J/m}^2$

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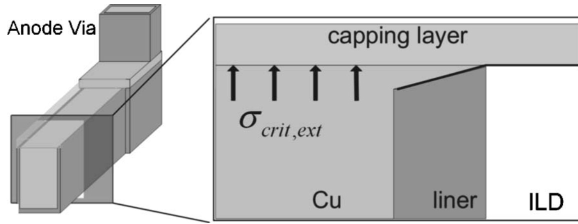

FIG. 9. Illustration of the incipient crack flaw, showing debonding of the sidewall liner from the capping layer.

$\leq G_{I,\text{crit}}(\text{SiN/ILD}) \leq 3.0\ \text{J/m}^2$, which is larger than the mode I critical energy release rate for the capping layer and Ta-liner interface. This comparison also implies that the liner/capping-layer interface does not serve as a barrier to crack propagation, but instead decoheres before the threshold for capping layer/ILD interfacial cracking is reached. Therefore, the load-bearing Cu/capping-layer interface and the narrow liner/capping-layer interface on either side of the interconnect near the anode can be considered as the incipient crack flaw (see Fig. 9). Under such circumstances, plane-strain conditions provide the most appropriate description for such geometries. Therefore,

$$\sigma_{\text{crit,ext}} = \sqrt{\frac{G_{I,\text{crit}} \cdot M}{\pi \cdot a}}, \tag{6}$$

where a is half of the line width and M is the effective plane-strain modulus of the Cu/low-k interconnect system.

B. $\sigma_{\text{crit,ext}}$ calculation

The critical energy release rate of the interface between SiN and parallel-patterned Cu lines has been estimated to be $8.0\ \text{J/m}^2$ for orthogonally propagating cracks,[19,24] with measurements made using the four-point bending technique. Compared to the much lower toughness of the SiN/ILD interface, the increase in adhesion energy is due to the substantial strain energy dissipation required for crack propagation across the ductile Cu lines. It should also be noted that this value of the adhesion energy is a strong function of the patterned line spacing and orientation.[19,24] When lines are more sparsely packed, the adhesion energy of the interface will decrease. Nevertheless, λ is clearly less than 1 for the interface of interest in the structures studied here. Therefore, $4.0\ \text{J/m}^2 \leq G_{I,\text{crit}}(\text{cap/lines}) < 8.0\ \text{J/m}^2$.

We performed FEM calculations using the ADINA software package to obtain the effective plane-strain modulus of the Cu/low-k system. We used shell elements to construct the cross-sectional geometry of the interconnects [see Fig. 10(a)]. Mirror symmetry with respect to the midplane of the interconnects was applied. In this analysis, the elements corresponding to Cu were subjected to known amounts of pressure loading P, while the deflection of the Cu/capping layer interface, GH in Fig. 10(a), was tracked as a function of P. In this model, the elements ensured that the out-of-plane strain was zero, so that the plane-strain loading condition was satisfied. For plane-strain cracks in a uniform material, the crack opening displacement must have the following form:[25]

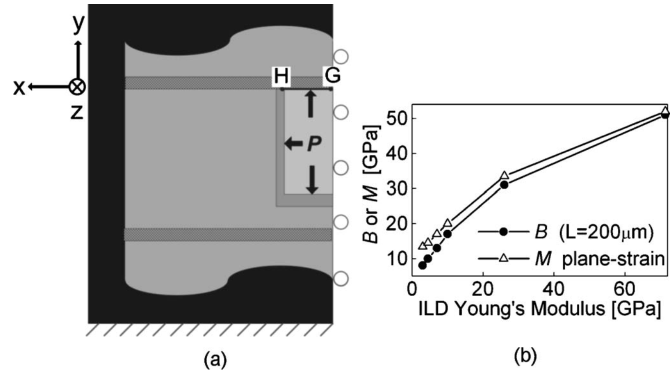

FIG. 10. (a) Schematic of the interconnect cross-section generated in FEM modeling. (b) The calculated effective plane-strain modulus is compared with the effective bulk modulus, both as a function of the Young's modulus of the ILD.

$$u_y = \frac{4}{M} \cdot \sqrt{a^2 - x^2} \cdot P. \tag{7}$$

Therefore, the effective plane-strain modulus for the material system, M, was approximated as a fitting parameter in describing the shape of GH as a function of P, and was determined to be 20 GPa. For the interconnect dimensions considered in this investigation, B and M are contrasted in Fig. 10(b) as a function of Young's modulus of the ILD. The magnitudes of B and M are similar because the interconnect lines in this investigation have an extremely large aspect ratio—the line length (200 μm) is much larger than the dimensions of the cross section (0.10 μm). Therefore, the conditions used in the FEM calculations that were used to calculate B, following Ref. [6], were also nearly plane-strain. Also, as expected, both moduli decrease as Young's modulus of the ILD decreases.

Applying the value of M appropriate for the Cu/low-k material system for this study in Eq. (6) yields $\sigma_{\text{crit,ext}} \approx 710$ MPa, which is in approximate agreement with the value determined in the preceding section (630 MPa).

The FEM calculations can also help to estimate the mode mixity angle ψ for the extrusion process,

$$\psi = \tan^{-1}\frac{K_{II}}{K_I} = \tan^{-1}\frac{\sigma_{xy}}{\sigma_{yy}}, \tag{8}$$

where σ_{xy} and σ_{yy} are the in-plane shear and normal tensile components of the stress at the edge of the incipient crack, H in Fig. 10. Within the range of compressive stresses for the extrusion process, ψ is determined to be between 4° and 7°, which indicates that the liner/capping-layer decohesion process is nearly mode I.

C. $\sigma_{\text{crit,ext}}$: post-extrusion stress relaxation

As failure analysis revealed, the continuously extruded Cu patch generally takes on an oval shape. Presumably, the extrusion would ultimately evolve toward a circular shape to achieve a uniform stress field and a minimum surface energy. Through the expansion processes of the Cu patch, the characteristic length of the crack flaw, a, also increases. Thus, the compressive stress near the anode continuously relaxes. However, it is worth noting that unlike the stress relaxations

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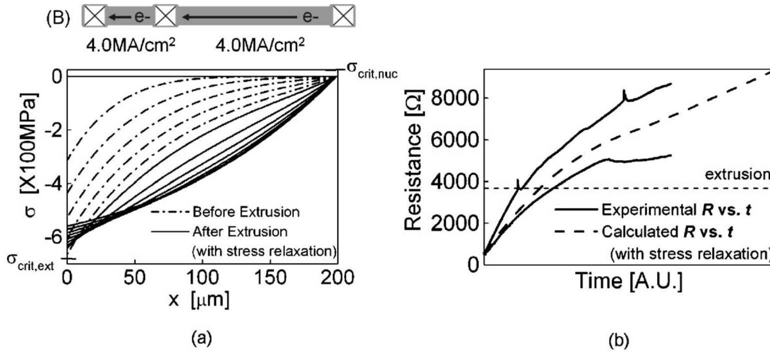

FIG. 11. (a) Calculated time-dependent spatial stress profiles for experiment B, both before and after $\sigma_{\mathrm{crit,ext}}$ is reached, using XSIM. (b) Calculated R vs t traces for experiment B, along with two experimental R vs t curves, which are the upper and lower bounds in the results of experiment B.

associated with void nucleation, Cu extrusions do not instantaneously relax all the stress that has built up before the extrusion initiates. The crack volume merely accommodates the Cu atoms that cannot be elastically contained within the interconnect. Consequently, extrusion failures are not catastrophic and do not have signatures in R versus t traces.

The relaxed stress associated with an ellipse is[26]

$$\sigma_{\mathrm{relax}} \cong \frac{\sqrt{\pi}}{2} \cdot \sqrt{\frac{c}{a}} \cdot \sqrt{\frac{G_{I,\mathrm{crit}} \cdot M}{a}}, \tag{9}$$

where $2a$ and $2c$ are the minor and major axis lengths of the elliptical crack, respectively. By the end of the electromigration experiments in this study, $2a$ and $2c$ reached approximately 1.0 and 2.5–3.0 μm, respectively. As a result, σ at the anode decreases from $\sim$710 to $\sim$610 MPa.

D. Stress development accounting for $\sigma_{\mathrm{crit,ext}}$

The post-extrusion evolution of the resistance of a segment can be simulated using XSIM and values for σ_{relax} and $\sigma_{\mathrm{crit,ext}}$, to analyze conditions corresponding to experiment B. The fully blocking boundary condition is changed at the anode once $\sigma_{\mathrm{crit,ext}}$ is reached. As a increases, a known amount of Cu atoms extrude while $\sigma_{\mathrm{crit,ext}}$ relaxes toward σ_{relax}. Numerically, this leads to an increase in the stress gradient near the anode [see Fig. 11(a)] and an associated increase in the back-stress force. Consequently, void growth slows down, which agrees with the experimental observations of dR/dt. Due to the lack of a blocking boundary at the anode, a linear spatial profile is not a stable solution for the stresses inside the interconnect. Instead, a concave-up spatial profile in stress develops, as seen in Fig. 11(a).

XSIM calculations can also be used to track the amount of Cu that has electromigrated away form the cathode, both before and after Cu extrusion is initiated. Assuming that the corresponding Cu volume is present in the form of a void that fully spans both the width and thickness of the line, the corresponding resistance change can also be calculated, as shown in Fig. 11(b). Figure 11(b) also shows two experimental R versus t curves, which are the upper and lower bounds of the experimental observations. The good agreement between the calculated and experimental R versus t traces further validates the analysis of $\sigma_{\mathrm{crit,ext}}$ described above.

E. Surface energy contributions

The aforementioned analysis uses critical energy release rates determined through fracture toughness experiments. However, in the Cu extrusion process studied here, the newly formed crack surfaces are subsequently covered by the extruded Cu patch instead of being free surfaces exposed in fracture toughness tests. Therefore, the difference in interfacial/surface energies for the two scenarios must be contrasted.

Generally, fracturing processes are expected to have work contributions from both the energies of the newly created surfaces and the plasticity required for fracture,[27]

$$G_C = 2 \cdot (\gamma_{\mathrm{surf}} + \gamma_{\mathrm{plastic}}). \tag{10}$$

The effect on γ_{surf} is accounted for in the following way for the case of fracture toughness tests:

$$\Delta\gamma_{\mathrm{surf}}(\text{fracture test}) = -\gamma_{\mathrm{SiN/Cu}} - \gamma_{\mathrm{SiN/SiO_2}} + \gamma_{\mathrm{vac/Cu}} + \gamma_{\mathrm{SiN/vac}} + \gamma_{\mathrm{SiO_2/vac}}, \tag{11}$$

and for the Cu extrusion process,

$$\Delta\gamma'_{\mathrm{surf}}(\text{extrusion}) = -\gamma_{\mathrm{SiN/SiO_2}} + \gamma_{\mathrm{SiN/Cu}} + \gamma_{\mathrm{SiO_2/Cu}}, \tag{12}$$

where the capping layer is approximated as SiN, and the ILD is approximated as SiO_2. The difference between Eqs. (11) and (12) is the correction needed for comparisons between the analysis shown here and the referenced experimental results,

$$\text{correction} = (\gamma_{\mathrm{vac/Cu}} - \gamma_{\mathrm{SiN/Cu}}) + (\gamma_{\mathrm{SiN/vac}} - \gamma_{\mathrm{SiN/Cu}}) + (\gamma_{\mathrm{SiO_2/vac}} - \gamma_{\mathrm{SiO_2/Cu}}). \tag{13}$$

However, because Cu, SiN, and SiO_2 are virtually inert in reactions with each other, most of the interface energies are equivalent to those with free surfaces, about 1.0 J/m^2. $\gamma_{\mathrm{Cu/vac}}=1.2$ J/m^2,[28] $\gamma_{\mathrm{SiN/Cu}}\leq 0.90$ J/m^2,[29] $\gamma_{\mathrm{SiN/vac}}=1.1$ J/m^2,[30] $\gamma_{\mathrm{SiO_2/vac}}=1.0$ J/m^2,[31] and $\gamma_{\mathrm{SiO_2/Cu}}=0.84$ J/m^2.[32] Therefore, the surface energy correction can be ignored for the $G_{I,C}$ used in the analysis presented above.

F. Implications of results

In the analysis presented here, both σ_{relax} and $\sigma_{\mathrm{crit,ext}}$ depend on not only M, which depends on the Young's modulus of the ILD, but also $G_{I,\mathrm{crit}}$(cap/lines), which is a strong function of the patterned line spacing and orientations, as

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well as of the width of the stressed line (a is one half of line width when the crack initiates). This result implies that sparsely packed, intermediate to wide interconnect lines could be more susceptible to electromigration-induced extrusion damage. For example, consider a 0.8 μm wide, 0.5 μm thick, and 200 μm long Cu/low-k interconnect segment embedded in an ILD with a Young's modulus of 3 GPa (corresponding to $M=8$ GPa), which is far enough away from other interconnect segments that $G_{I,\mathrm{crit}}(\mathrm{SiN/ILD})$ can be used to approximate its capping layer adhesion. These conditions give $\sigma_{\mathrm{crit,ext}} \cong 100$ MPa. Such a compressive stress development corresponds to growth of a fully spanning void of length 0.4 μm. Using common via redundancy schemes at the cathode, it is plausible that such an interconnect segment could fail due to extrusions before failing due to void growth. Electromigration-induced extrusion, in this example, is a competing failure mechanism with void growth.

VI. CONCLUSIONS

We performed electromigration experiments using 200 μm long Cu/low-k interconnects bound by a Ta-based diffusion-barrier liner on three sides, SiN-based capping layer on the top, and embedded in an ILD consisting of a form of carbon-doped SiO_2-based material deposited by PECVD. The unusual robustness of the Ta-based diffusion barrier allowed continued testing and void growth well after observation of $10\% R_0$ resistance increases without occurrence of open-circuit failures. Voids that fully spanned the width and thickness of the lines and with lengths of 10 μm or more were observed during microscopic analysis at the cathode end of the test lines. Through thorough microscopic analyses of the anode end of these test structures, it was also found that the Cu transported from the cathode end contributed to formation of extrusions of Cu along the ILD/SiN-capping-layer interface. This extrusion failure mode was modeled as near mode I (tensile) fracture, with a mode mixity angle of 4 °–7 °. The incipient crack flaw geometry corresponds to a plane-strain condition, and the effective plane-strain modulus was determined using FEM analyses. The critical stress required for extrusion, $\sigma_{\mathrm{crit,ext}}$, calculated in this way ($\sim$710 MPa) is consistent with the value estimated through comparison of the volumes of the extrusion and the corresponding void. This analysis further suggests that sparsely packed, intermediate to wide interconnect lines could be more susceptible to electromigration-induced extrusion damage, especially as low-k ILDs with lower stiffness and thinner liners are deployed.

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