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Electron-beam-evaporated Thin Films of Hafnium Dioxide for Fabricating Electronic Devices

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Abstract

Thin films of hafnium dioxide (HfO_2) are used widely as the gate oxide in fabricating integrated circuits (ICs) because of their high dielectric constants. In this paper, we report the growth of thin films of hafnium dioxide (HfO_2) using e-beam evaporation, and the fabrication of complementary metal-oxide semiconductor (CMOS) integrated circuits using this HfO_2 thin film as the gate oxide. We analyzed the thin films using high-resolution transmission electron microscopy (HRTEM) and electron diffraction, thereby demonstrating that the e-beam-evaporation-grown HfO_2 film has a polycrystalline structure and forms an excellent interface with silicon. Accordingly, we fabricated 31-stage CMOS ring oscillator to test the quality of the HfO_2 thin film as the gate oxide, and obtained excellent rail-to-rail oscillation waveforms from it, denoting that the HfO_2 thin film functioned very well as the gate oxide.

Key words: Hafnium dioxide (HfO_2) thin films; complementary metal-oxide semiconductor (CMOS) integrated circuits; CMOS ring oscillator.

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I. Introduction

Hafnium dioxide (HfO_2) thin films previously have been investigated extensively as the gate oxide for applications as metal-oxide-semiconductor field-effect transistors (MOSFETs) [1-3], due to the higher values of their dielectric constant (κ) compared to conventional silicon dioxide (SiO_2). Since the invention in 1968 of the silicon-based integrated circuit (IC), it has undergone tremendous improvements in functionality and performance, and the device's density has doubled every two years [4]. As MOSFETs continue to be scaled down, the tunneling currents through the gate dielectrics (the gate leakage current) has become a major concern in fabricating CMOS integrated circuits (ICs). High-κ dielectric-oxide materials could be a solution to the problem of the gate leakage current. These materials can assure that the equivalent oxide thickness (EOT) of the gate dielectric in MOSFETs continue to shrink, where $EOT=(\kappa_{SiO_2}/\kappa)T_{phys}$ and $\kappa_{SiO_2} = 3.9$, while keeping a relatively larger physical thickness (T_{phys}) for lowering the gate leakage current. Hafnium dioxide (HfO_2) thin films can be grown using various techniques, such as e-beam evaporation [5] and atomic-layer deposition (ALD) [6-13]. E-beam evaporation is a physical vapor deposition, does not use chemicals, and does not need too complex system. Thus, it is a safe, clean, and relatively simple process compared to the chemical vapor deposition.

Although there has been extensive research on the growth of hafnium dioxide (HfO_2) thin films and their application in the fabricating such devices [14, 15], research on the wafer-level fabrication of complementary metal-oxide semiconductor (CMOS) integrated circuits with the HfO_2 thin film as the gate oxide still is still interesting. In this paper, we report the growth of hafnium dioxide (HfO_2) thin films using e-beam evaporation, and our subsequent fabrication of

complementary metal-oxide semiconductor (CMOS) integrated circuits using the HfO_2 thin film as the gate oxide.

II. Experimental Details

We grew two sets of HfO_2 films on 3-inch-diameter (001) silicon substrates via electron-beam evaporation. We grew one at 400 ^oC with substrate heating, while the other one was grown at room temperature without substrate heating. We used hafnium dioxide powder (99.9% purity) as the source material for electron-beam evaporation. The substrate holder was rotated at the speed of 20 RPM during the deposition. The process chamber had a background pressure of 2×10^{-7} Torr. The growth rate of the films was about 0.04 Å/s, and an INFICON deposition monitor controlled their thicknesses. The HfO_2 film grown for the HRTEM analysis was relatively thicker (more than 20 nm). It is easier to make a TEM sample and perform the HRTEM analysis for a thicker film. The HfO_2 film, as the gate oxide in fabricating the CMOS devices was grown at 400 ^oC with substrate heating; it was about 20 nm thick. We chose the thickness of 20 nm for the HfO_2 thin film instead of a smaller thickness in the fabrication of devices, because of the relatively large feature size (channel length of FETs = 5 μm) in this research, and the chosen thickness is more reasonable for showing the performance of the HfO_2 gate oxide for the feature size. We designed and fabricated a 31-stage CMOS ring oscillator (Figure 1) to test the quality of the e-beam-evaporated HfO_2 film as the gate oxide. A 3-inch-diameter n-type (001) silicon wafer was used in making the complementary metal-oxide semiconductor (CMOS) devices. All the n-channel field-effect transistors (nFETs) in the oscillator had a channel length (L) of 5 μm, and a channel width (W) of 10 μm, while all the p-channel field-effect transistor (pFETs) also had a channel length (L) of 5 μm, but a channel width (W) of 30 μm. The fabrication processes

included boron doping for the fabricating the p-well and the source/drain of pFETs; phosphorous doping for the making the source/drain of nFETs; depositing the HfO_2 thin film for the gate oxide; and, depositing the aluminum (Al)/chromium (Cr)/gold (Au) thin films for the metal contact. Thermal diffusion was used for doping both with boron and phosphorous. Ultra-violet (UV) lithography was adopted for patterning in fabricating the device. We first deposited a metal contact, a 20- nm-thick aluminum (Al) thin film, only on the contact area for the Ohmic contact with silicon, and then overlaid it with a 5 nm-thick chromium (Cr)/100 nm-thick gold (Au) bilayer film for the final metallization of the device. After the fabrication was completed, we annealed the wafer at 400 ^{o}C under a vacuum of 5×10^{-5} Torr for 20 minutes. Using high-resolution transmission electron microscopy (HRTEM), we analyzed the cross-section morphology and crystalline structure of the HfO_2 films and their interface with the silicon substrate. We prepared the TEM samples by the In-situ Lift-out method using a dual-beam FIB (FEI Helios 600 dual beam FIB). The FIB's TEM membranes were imaged in a JEOL 2100F, high-resolution analytical transmission electron microscope at 200 k, and the fabricated devices were imaged in a JEOL JSM-6610LV scanning electron microscope. We employed an Agilent precision source/measurement unit and Agilent mixed-signal oscilloscope to measure the electrical properties of the fabricated devices. The input of the first CMOS inverter (the first stage) in the oscillator (Figure 1) was connected to the output of the last CMOS inverter (the 31st stage) for measuring the 31-stage oscillation waveform, while the input of the first CMOS inverter was connected to the output of the third CMOS inverter (the third stage) for measuring the 3-stage oscillation waveform. A voltage of 7.5 V was applied to the VDD in the ring oscillator for the electrical measurements.

III. Results and Discussion

Figure 2 shows the HRTEM image of a cross section of the electron-beam-evaporated HfO_2 thin films, with an electron-beam-diffraction inset. The left one shows the film grown at 400 ^oC with substrate heating, while the right one shows the film grown at room temperature without heating the substrate. The TEM shows that both HfO_2 films whether grown at 400 ^oC or at room temperature have an excellent interface with silicon. The selected electron diffraction (SAED) pattern shows the evidence of polycrystallinity in both films.

Figure 3 is a SEM image of a fabricated 31-stage CMOS ring oscillator, and an enlarged view of a CMOS inverter in the ring oscillator. The ring oscillator consists of 31 CMOS inverters (31 stages), wherein each inverter consists of an nFET and a pFET. As described in Section II, a 20 nm-thick aluminum (Al) thin film was deposited only on the contact area for the Ohmic contact with silicon, and a 5 nm-thick chromium (Cr)/100 nm-thick gold (Au) bilayered film was deposited for final metallization of the device. The Cr/Au bilayer film demonstrated excellent adhesion to the HfO_2 thin film during fabrication of the device, and established excellent electrical contact with the Al layer, which was demonstrated in our electrical measurements. The poor adhesion of an HfO_2 thin film to other materials, such as metals, is a common problem in the making the device. The Cr/Au bilayer film used in this research can solve this problem.

Figure 4 shows the drain-source current (I_{DS}) as a function of the drain-source voltage (V_{DS}) and gate voltage (V_{GS}) for the nFET (L=5 μm; W=10 μm) fabricated with HfO_2 as the gate oxide. Figure 5 shows the drain-source current (I_{DS}) as a function of the drain-source voltage (V_{DS}) and gate voltage (V_{GS}) for the pFET (L=5 μm; W=30 μm), again with HfO_2 as the gate oxide. Both

the nFET and pFET displayed the excellent electrical properties of FETs. Figure 6 shows the transfer characteristics of a CMOS inverter, which consists of an nFET (L=5 μm; W=10 μm) and pFET (L=5 μm; W=30 μm), for the VDD voltages of 5V, 6V, 7V, and 8V. The output voltage decreases sharply from a high voltage (VDD voltage) to a low voltage (GND voltage = 0V) for all the four cases (VDD = 5V, 6V, 7V and 8V), while the input voltage increases to the inverting voltage, indicating that the CMOS inverter has excellent electrical transfer characteristics. This is because both pFET and nFET in the CMOS inverter functioned very well. When the input voltage is low, the nFET is off and the pFET is on, the output is connected to VDD through the pFET, and the output voltage equals to the VDD voltage. When the input voltage increase to the inverting voltage, the pFET is off and the nFET is on, the output is connected to GND through the nFET, and the output voltage equals to the GND voltage (0V).

Figure 7 illustrates the 31-stage oscillation waveform measured from the CMOS ring oscillator at a VDD voltage of 7.5 V, while Figure 8 shows a 3-stage oscillation waveform measured from the CMOS ring oscillator at a VDD voltage of 7.5 V. The 31-stage oscillation has a frequency of about 100 kHz, while that of the 3-stage oscillation is about 1 MHz. More stages (more inverters) in an oscillator make the delay longer, so resulting in a lower oscillation frequency. Both Figure 7 and 8 show that the CMOS oscillator produces excellent rail-to-rail waveforms, following the VDD voltage (7.5V) and the GND voltage (0V). The peak-peak voltage is controlled exactly by the VDD and GND voltages. This is because the CMOS inverter in the oscillator has excellent electrical transfer characteristics as described above.

IV. Summary

We grew hafnium dioxide (HfO_2) thin films via e-beam evaporation, and successfully fabricated complementary metal-oxide semiconductor (CMOS) electronic circuits with the HfO_2 thin film as the gate oxide. The e-beam-evaporated HfO_2 thin film was analyzed by the high-resolution transmission electron microscopy (HRTEM) and electron diffraction, revealing polycrystalline structures and an excellent interface with silicon. We propose that a Cr/Au bilayer thin film could be used to solve the problem of the poor adhesion of an HfO_2 thin film to the metal contact in fabricating the device, and then we demonstrated its excellent adhesion to HfO_2 thin film, and also its good electrical contact with the aluminum layer. The MOSFETs, CMOS inverters, and CMOS ring oscillators fabricated with the HfO_2 thin film as the gate oxide all demonstrated highly satisfactory electrical properties, indicating that this thin film can be an excellent gate oxide for applications in CMOS integrated circuits (ICs).

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Figure Captions:

Fig. 1. Schematic of a 31-stage CMOS ring oscillator circuit.

Fig. 2. HRTEM image with an electron-beam diffraction inset of the cross section of the HfO_2 thin films grown at 400 ^oC (left), and at the room temperature (right).

Fig. 3. SEM image of a fabricated 31-stage CMOS ring oscillator (left), and the enlarged view of an inverter in the ring oscillator (right). The device is covered by a 20 nm-thick HfO_2 dielectric thin film, which acts as the gate oxide in the gate area of FETs.

Fig. 4. Drain-source current (I_{DS}) versus drain-source voltage (V_{DS}) and gate voltage (V_{GS}) for the nFET fabricated with the HfO_2 thin film as the gate oxide.

Fig. 5. Drain-source current (I_{DS}) versus drain-source voltage (V_{DS}) and gate voltage (V_{GS}) for the pFET fabricated with the HfO_2 thin film as the gate oxide.

Fig. 6. Transfer characteristics of the CMOS inverter fabricated with the HfO_2 thin film as the gate oxide.

Fig. 7. The 31-stage oscillation waveform of the CMOS ring oscillator at the VDD voltage of 7.5 V.

Fig. 8. The 3-stage scillation waveform at the VDD voltage of 7.5 V.

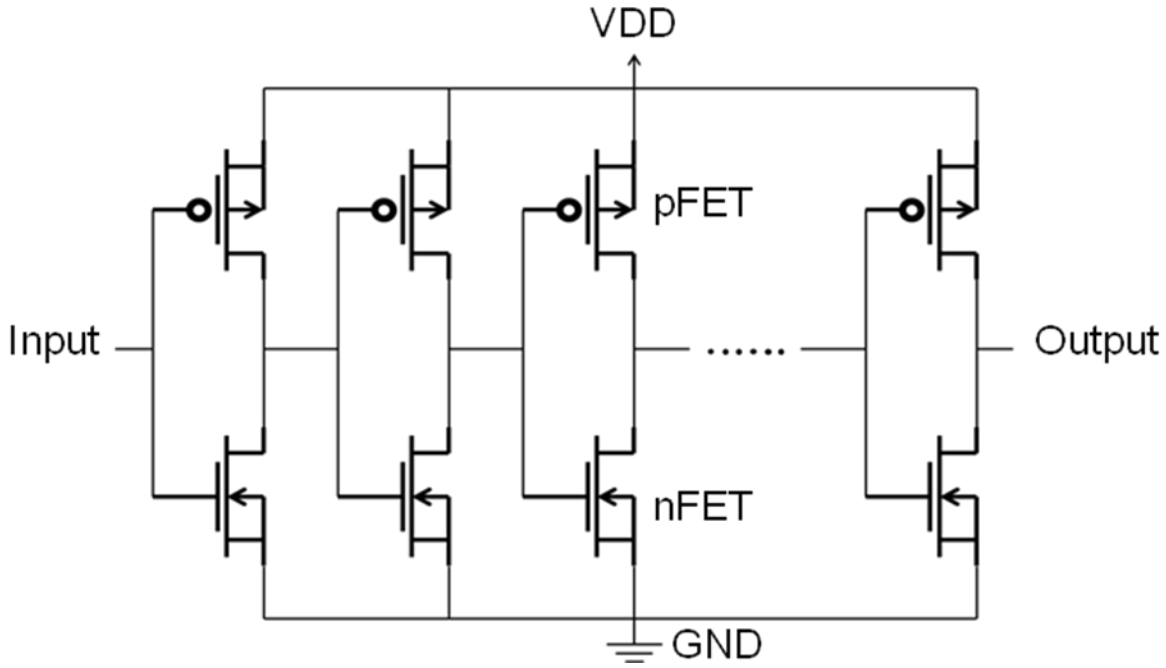


Fig. 1

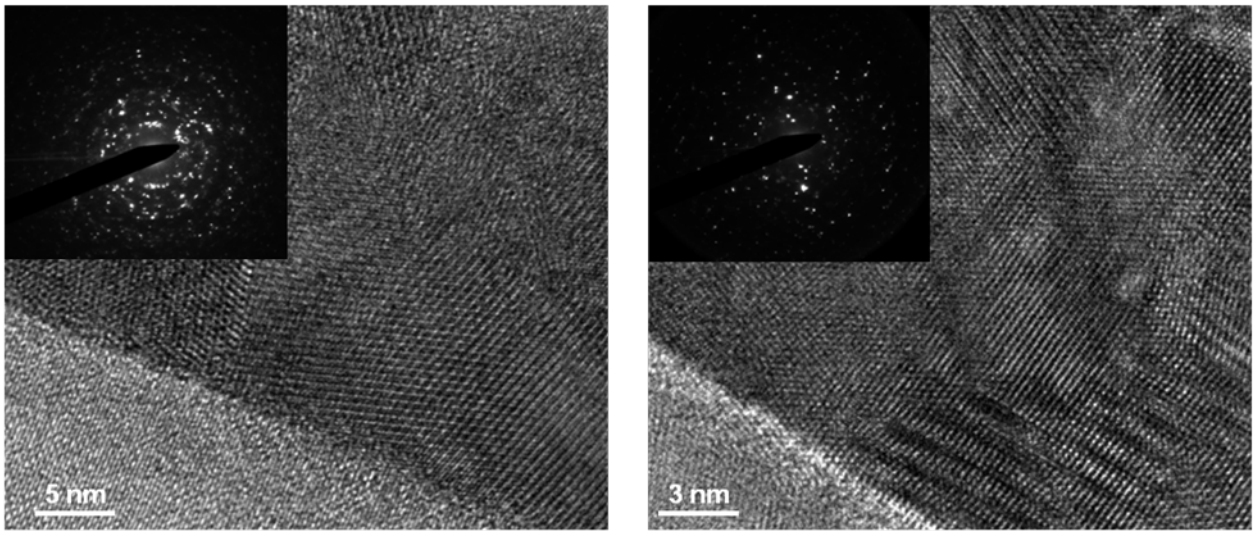
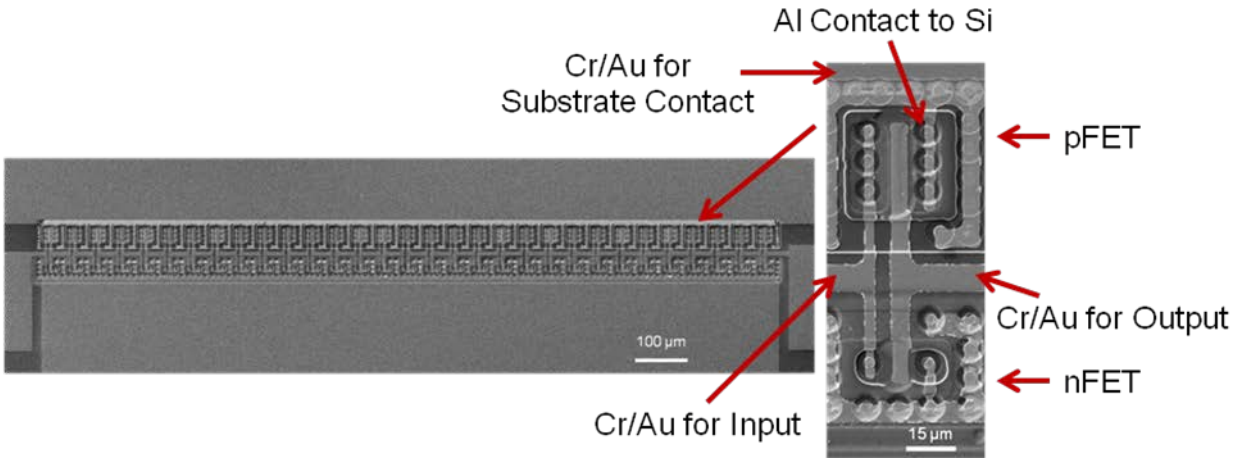


Fig. 2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Substrate Contact
pFET
Cr/Au for Output
nFET
Cr/Au for Input
100 µm
15 µm

Fig. 3

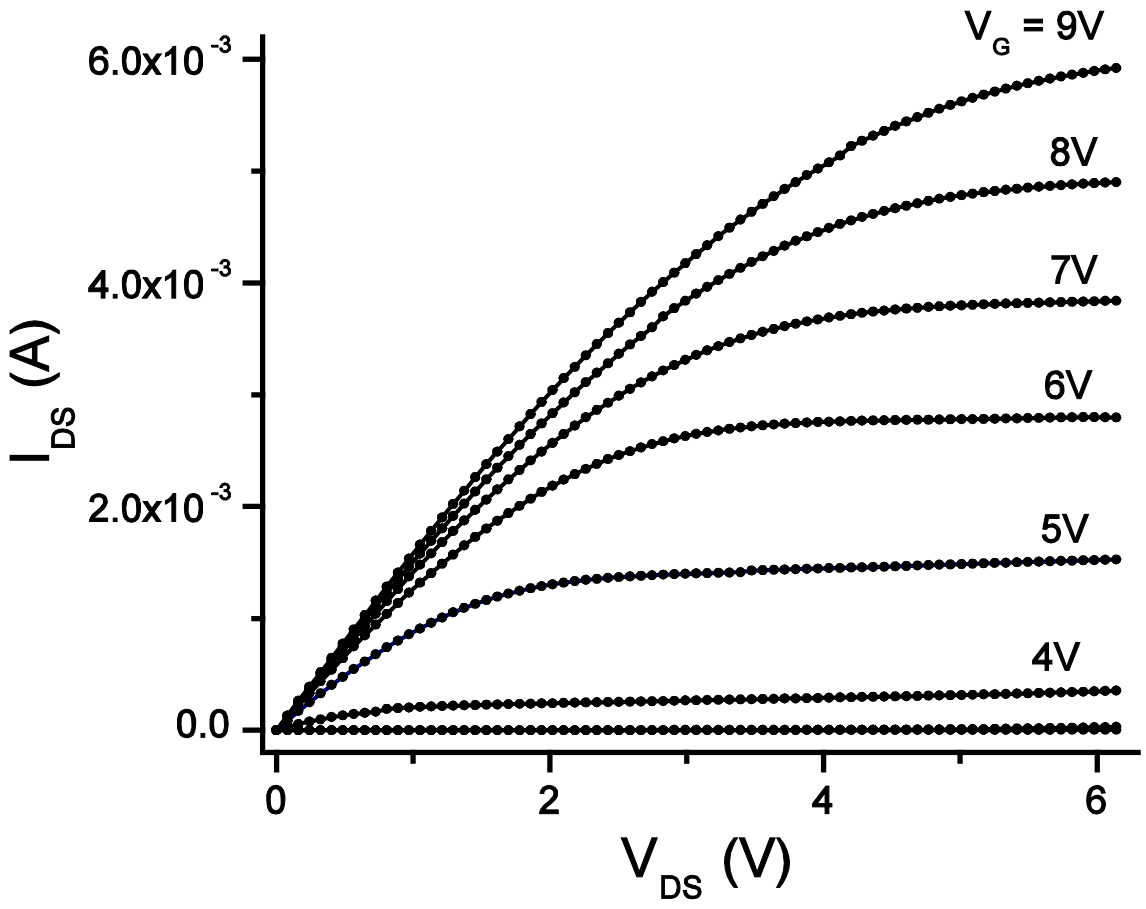

Fig. 4

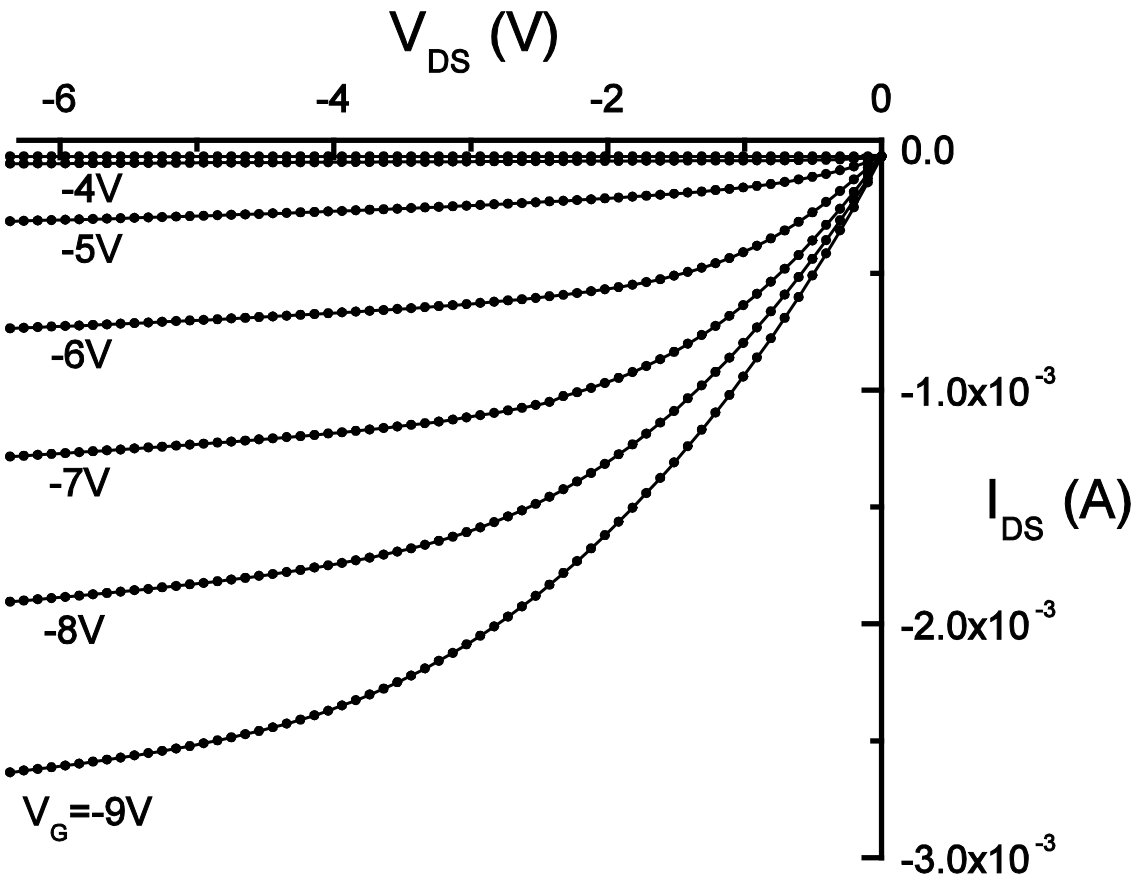

Fig. 5

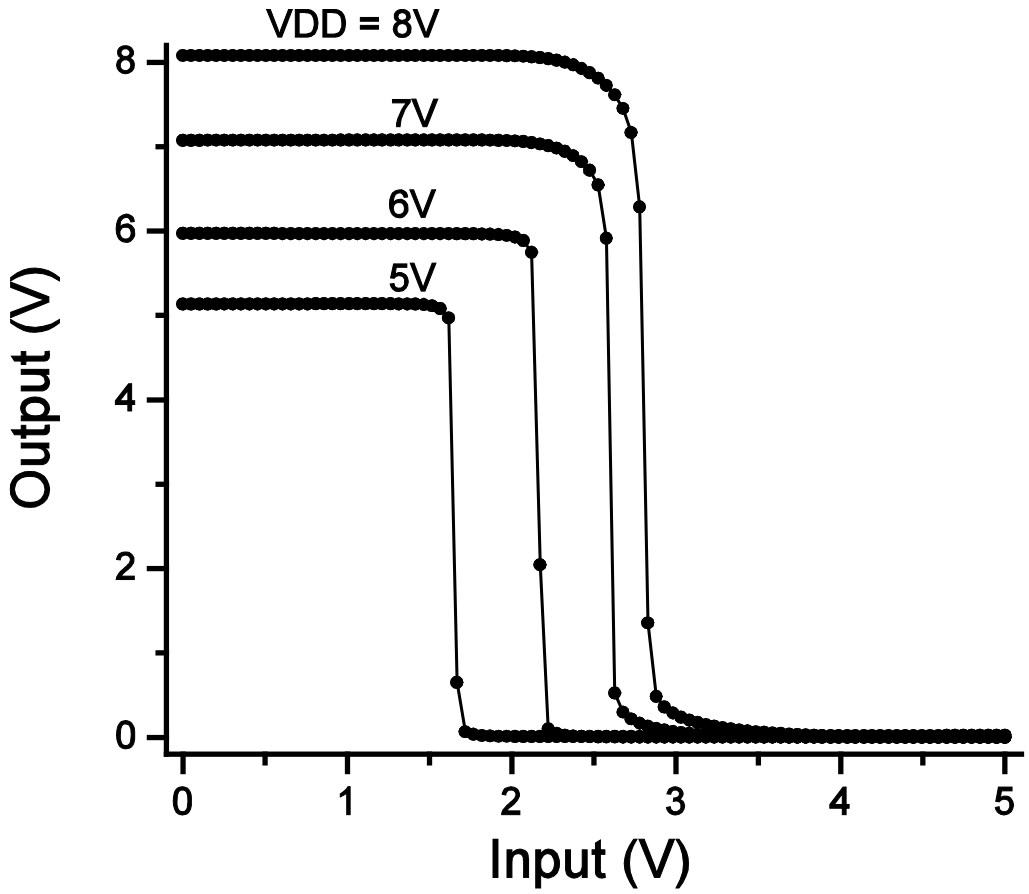

Fig. 6

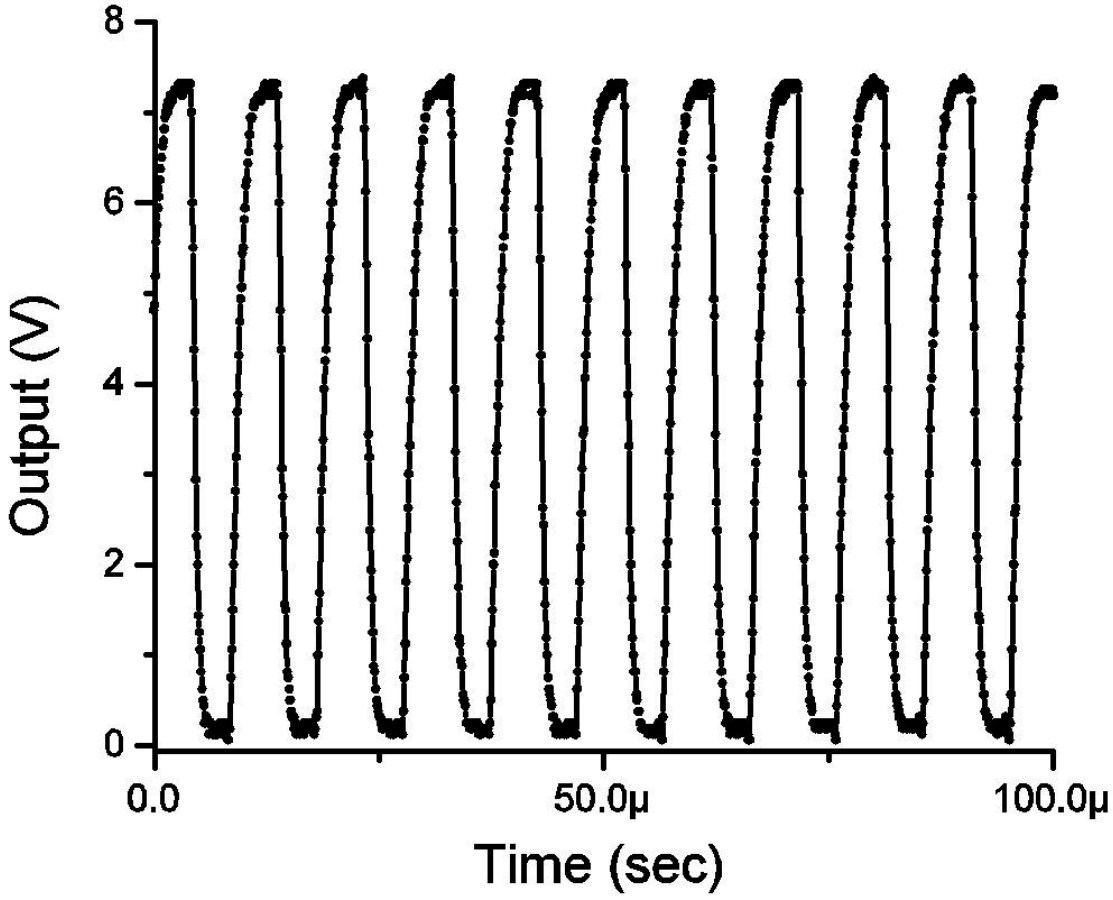

Fig. 7

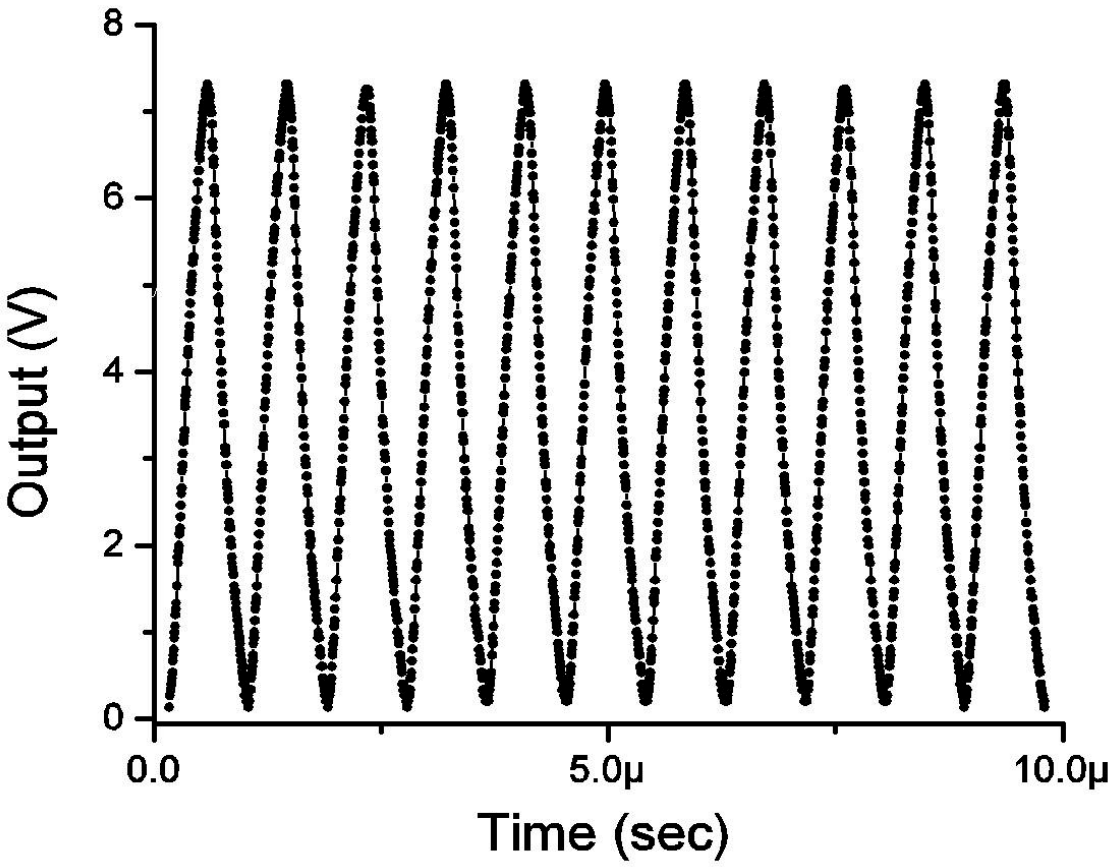

Fig. 8