

LAB MANUAL
ON
ELECTRONIC DEVICES & CIRCUITS LAB
II B.TECH I SEMESTER ECE
(JNTUA-R15)

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ELECTRONIC DEVICES & CIRCUITS LAB
LIST OF EXPERIMENTS

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Part A: Germanium Diode (Forward bias & Reverse bias)
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2. Zener Diode Characteristics
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1. P-N JUNCTION DIODE CHARACTERISTICS

- AIM:**
1. To plot Volt-Ampere Characteristics of Germanium and Silicon P-N Junction Diode.
 2. To find cut-in Voltage for Germanium and Silicon P-N Junction diode.
 3. To find static and dynamic resistances in both forward and reverse biased conditions of Germanium and Silicon (only forward bias) P-N Junction diode.

APPARATUS:

S.No	Name of the Apparatus	Range	Quantity
1	Diodes IN 4007 (Ge and Si)		1
2	Resistors	1K Ω , 100 Ω	1
3	Regulated Power Supply	(0-30)V DC	1
4	Bread Board		1
5	Digital Ammeter	(0-200) μ A/(0-200)mA	1
6	Digital Voltmeter	(0-20)V DC	1
7	Connecting Wires	As Required	

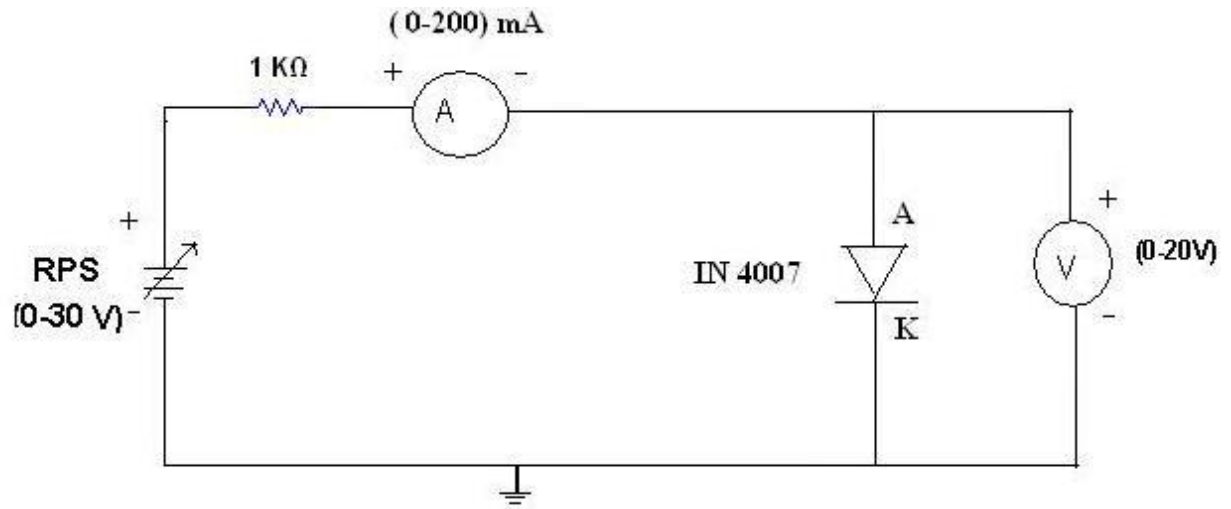
THEORY:-

A p-n junction diode conducts only in one direction. The V-I characteristics of the diode are curve between voltage across the diode and current through the diode. When external voltage is zero, circuit is open and the potential barrier does not allow the current to flow. Therefore, the circuit current is zero. When P-type (Anode is connected to +ve terminal and n- type (cathode) is connected to –ve terminal of the supply voltage, is known as forward bias. The potential barrier is reduced when diode is in the forward biased condition. At some forward voltage, the potential barrier altogether eliminated and current starts flowing through the diode and also in the circuit. The diode is said to be in ON state. The current increases with increasing forward voltage.

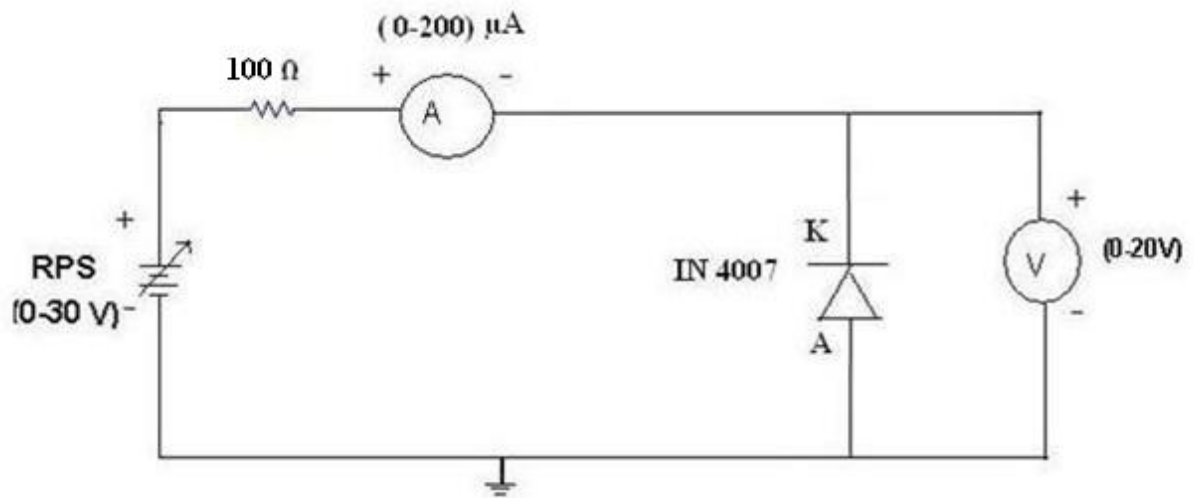
When N-type (cathode) is connected to +ve terminal and P-type (Anode) is connected to –ve terminal of the supply voltage is known as reverse bias and the potential barrier across the junction increases. Therefore, the junction resistance becomes very high and a very small current (reverse saturation current) flows in the circuit. The diode is said to be in OFF state. The reverse bias current due to minority charge carriers.

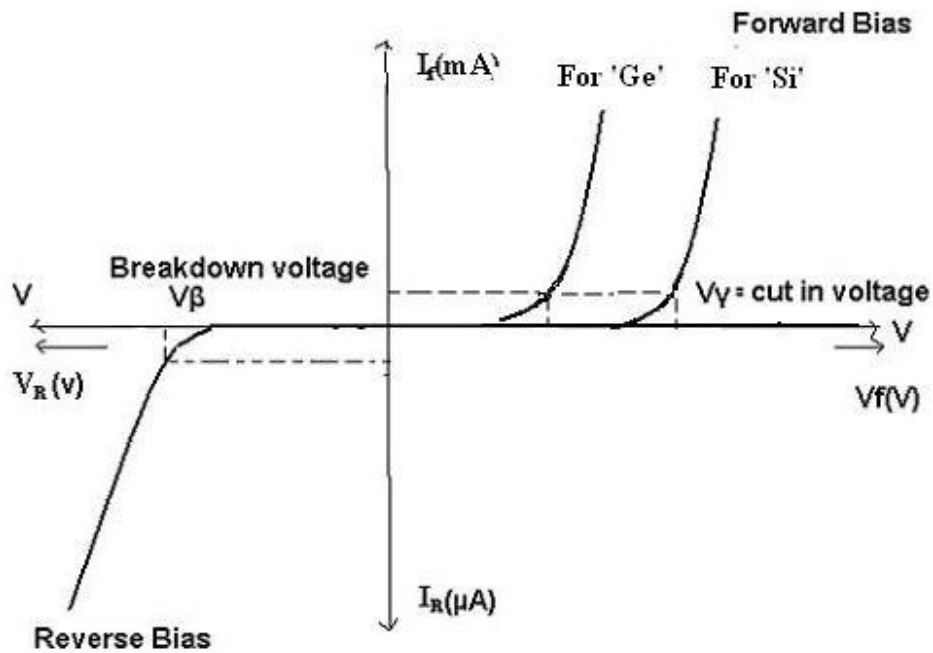
CIRCUIT DIAGRAM:

(i) **FORWARD BIAS:**



(ii) **REVERSE BIAS:**



V-I CHARACTERISTICS:**PROCEDURE:****(i) FORWARD BIAS (For 'Ge' and 'Si' Diode):**

1. Connections are made as per the circuit diagram.
2. For forward bias, the RPS +ve is connected to the anode of the diode and RPS -ve is connected to the cathode of the diode,
3. Switch ON the power supply and increases the input voltage (supply voltage) in Steps.
4. Note down the corresponding current flowing through the diode and voltage across the diode for each and every step of the input voltage.
5. The readings of voltage and current are tabulated.
6. Graph is plotted between voltage on x-axis and current on y-axis.

OBSERVATIONS:**(a) For 'Ge':**

S.No.	Applied voltage (volts)	Voltage across Diode (volts)	Current through Diode (mA)

(b) For 'Si':

S.No.	Applied voltage (volts)	Voltage across Diode (volts)	Current through Diode (mA)

PROCEDURE:**(ii) REVERSE BIAS (For 'Ge' Diode):**

1. Connections are made as per the circuit diagram.
2. For reverse bias, the RPS +ve is connected to the cathode of the diode and RPS -ve is connected to the anode of the diode.
3. Switch ON the power supply and increase the input voltage (supply voltage) in Steps.
4. Note down the corresponding current flowing through the diode and voltage across the diode for each and every step of the input voltage.
5. The readings of voltage and current are tabulated.
6. The Graph is plotted between voltage on x-axis and current on y-axis.

OBSERVATIONS:

(a) For 'Ge':

S.No.	Applied voltage (volts)	Voltage across Diode (volts)	Current through Diode (μA)

PRECAUTIONS:

1. While doing the experiment do not exceed the ratings of the diode. This may lead to damage the diode.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.

CALCULATIONS:

1. Cut-in Voltage of 'Ge' diode is _____

2. Cut-in Voltage of 'Si' diode is _____

3. Forward Bias:

(a) For 'Ge':

$$(i) \text{ Static forward Resistance } (R_{dc}) = \frac{V_f}{I_f}$$

$$(ii) \text{ Dynamic forward Resistance } (r_{ac}) = \frac{\Delta V_f}{\Delta I_f}$$

(b) For 'Si':

$$(i) \text{ Static forward Resistance } (R_{dc}) = \frac{V_f}{I_f}$$

$$(ii) \text{ Dynamic forward Resistance } (r_{ac}) = \frac{\Delta V_f}{\Delta I_f}$$

4. Reverse Bias:

(a) For 'Ge':

$$(i) \text{ Static reverse Resistance } (R_{dc}) = \frac{V_r}{I_r}$$

$$(ii) \text{ Dynamic reverse Resistance } (r_{ac}) = \frac{\Delta V_r}{\Delta I_r}$$

RESULT: The Forward and Reverse Bias characteristics for a p-n diode are observed. The cut-in voltage, static and dynamic resistances in both forward and reverse biased conditions for Germanium and Silicon P-N Junction diode are found.

- i) The Cut-in voltage of 'Ge' Diode is _____
- ii) The Cut-in voltage of 'Si' Diode is _____
- iii) The Static forward resistance of 'Ge' Diode is _____
- iv) The Dynamic forward resistance of 'Ge' Diode is _____
- v) The Static reverse resistance of 'Ge' Diode is _____
- vi) The Dynamic reverse resistance of 'Ge' Diode is _____
- vii) The Static forward resistance of 'Si' Diode is _____
- viii) The Dynamic forward resistance of 'Si' Diode is _____

VIVA QUESTIONS:

1. Define depletion region of a diode?
2. What is meant by transition & space charge capacitance of a diode?
3. Is the V-I relationship of a diode Linear or Exponential?
4. Define cut-in voltage of a diode and specify the values for Si and Ge diodes?
5. What are the applications of a p-n diode?
6. Draw the ideal characteristics of P-N junction diode?
7. What is the diode equation?
8. What is PIV?
9. What is the break down voltage?
10. What is the effect of temperature on PN junction diodes?

2. ZENER DIODE CHARACTERISTICS

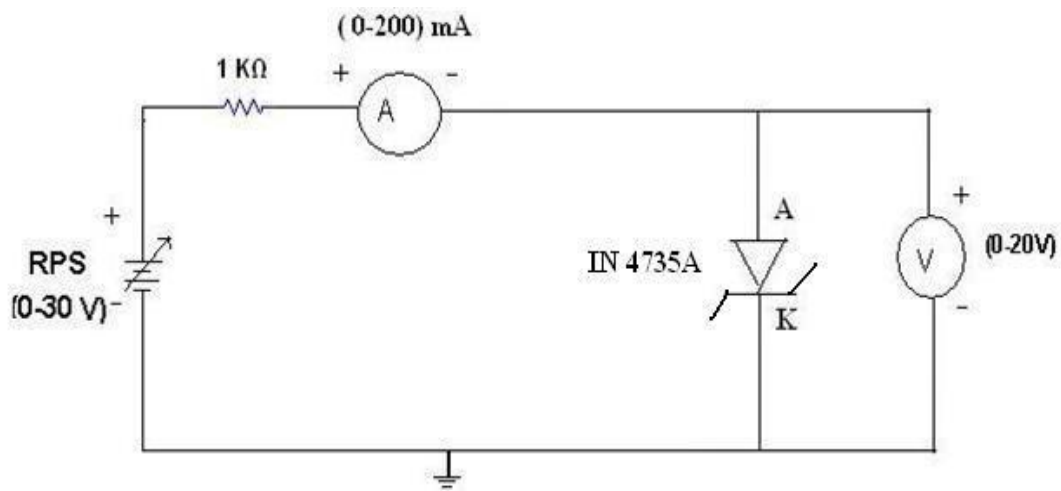
- AIM:**
1. To observe and draw the V-I characteristics and Regulation characteristics of a Zener diode.
 2. To find the Zener Break down voltage in reverse biased condition.
 3. To find the Static and Dynamic resistances of Zener diode in both forward and reverse biased conditions.

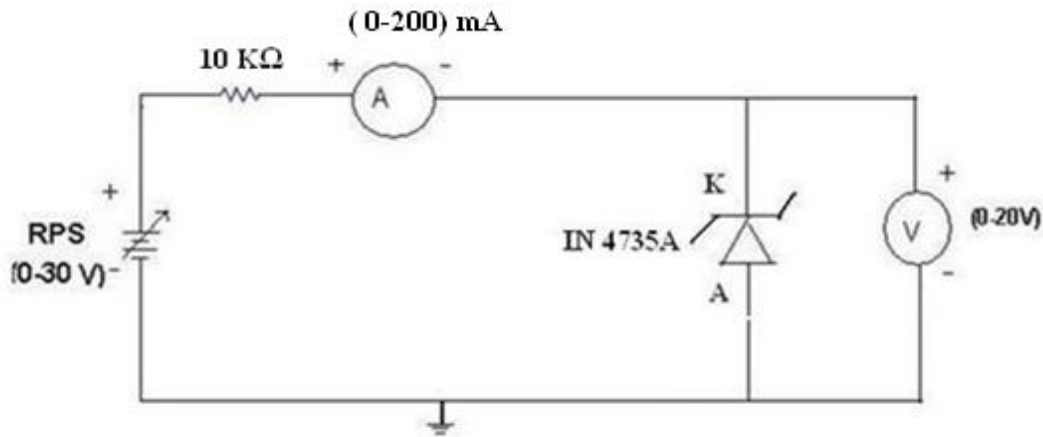
APPARATUS:

S.No	Name of the Apparatus	Range	Quantity
1	Zener Diode (IN 4735A)		1
2	Resistors	1K Ω , 10K Ω	1
3	Regulated Power Supply	(0-30)V DC	1
4	Bread Board		1
5	Digital Ammeter	(0-200)mA	1
6	Digital Voltmeter	(0-20)V DC	1
7	Connecting Wires	As Required	

CIRCUIT DIAGRAM:

(i) V-I CHARACTERISTICS:



(ii) REGULATION CHARACTERISTICS:**THEORY:**

A zener diode is heavily doped p-n junction diode, specially made to operate in the break down region. A p-n junction diode normally does not conduct when reverse biased. But if the reverse bias is increased, at a particular voltage it starts conducting heavily. This voltage is called Break down Voltage. High current through the diode can permanently damage the device

To avoid high current, we connect a resistor in series with zener diode. Once the diode starts conducting it maintains almost constant voltage across the terminals what ever may be the current through it, i.e., it has very low dynamic resistance. It is used in voltage regulators.

PROCEDURE:**(i) V-I CHARACTERISTICS:**

1. Connections are made as per the circuit diagram.
2. The Regulated power supply voltage is increased in steps.
3. The zener current (I_z), and the zener voltage (V_z) are observed and then noted in the tabular form.
4. A graph is plotted between zener current (I_z) on y-axis and zener voltage (V_z) on x-axis.

(ii) REGULATION CHARACTERISTICS:

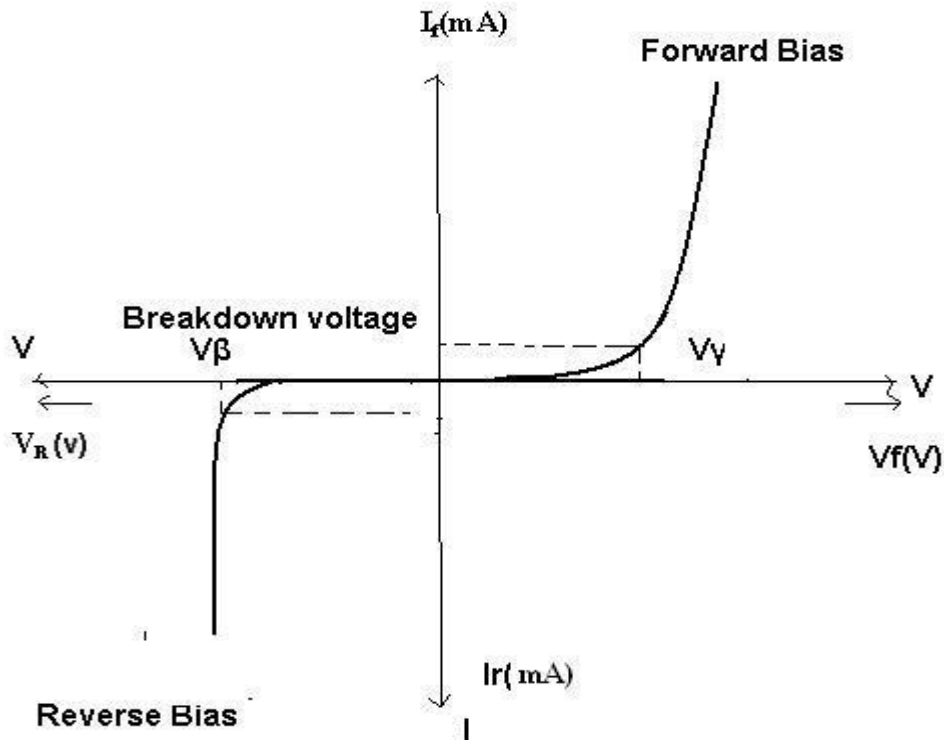
1. Connections are made as per the circuit diagram.
2. The Regulated power supply voltage is increased in steps.
3. The voltage across the diode (V_z) remains almost constant although the current through the diode increases. This voltage serves as reference voltage.
4. The zener current (I_z), and the zener voltage (V_z) are observed and then noted in the tabular form.
4. A graph is plotted between zener current (I_z) on y-axis and zener voltage (V_z) on x-axis.

OBSERVATIONS:**(i) V-I CHARACTERISTICS:**

S.No	Zener Voltage (V_z) (volts)	Zener Current (I_z) (mA)

(ii) REGULATION CHARACTERISTICS:

S.No	Zener Voltage (V_z) (volts)	Zener Current (I_z) (mA)

V-I & REGULATION CHARACTERISTICS:**PRECAUTIONS:**

1. While doing the experiment do not exceed the ratings of the zener diode. This may lead to damage the diode.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.

CALCULATIONS:

1. Zener Break down Voltage is _____

2. Forward Bias:

$$(i) \text{ Static forward Resistance } (R_{dc}) = \frac{V_f}{I_f}$$

$$(ii) \text{ Dynamic forward Resistance } (r_{ac}) = \frac{\Delta V_f}{\Delta I_f}$$

3. Reverse Bias:

$$(i) \text{ Static reverse Resistance } (R_{dc}) = \frac{V_r}{I_r}$$

$$(ii) \text{ Dynamic reverse Resistance } (r_{ac}) = \frac{\Delta V_r}{\Delta I_r}$$

RESULT: The V-I characteristics and Regulation characteristics of a zener diode are observed. The Zener Break down voltage in reverse biased condition, Static and Dynamic resistances of Zener diode in both forward and reverse biased conditions are calculated.

- i) The Zener Break down voltage is _____
- ii) The Static forward resistance of Zener Diode is _____
- iii) The Dynamic forward resistance of Zener Diode is _____
- iv) The Static reverse resistance of Zener Diode is _____
- v) The Dynamic reverse resistance of Zener Diode is _____

VIVA QUESTIONS:

1. What type of temperature Coefficient does the zener diode have?
2. If the impurity concentration is increased, how the depletion width effected?
3. Does the dynamic impedance of a zener diode vary?
4. Explain briefly about avalanche and zener breakdowns?
5. Draw the zener equivalent circuit?
6. Differentiate between line regulation & load regulation?
7. In which region zener diode can be used as a regulator?
8. How the breakdown voltage of a particular diode can be controlled?
9. What type of temperature coefficient does the Avalanche breakdown has?
10. By what type of charge carriers the current flows in zener and avalanche breakdown diodes?

3. RECTIFIERS (WITHOUT AND WITH C-FILTER)

(A) HALF WAVE RECTIFIER

AIM: 1.To obtain the load regulation and ripple factor of a half-wave rectifier by using

- (a). without Filter
- (b). with Filter

2. To observe the input and output waveforms of a half-wave rectifier.

APPARATUS:

S.No	Name of the Apparatus	Range	Quantity
1	Diodes IN 4007 (Si)		1
2	Decade Resistance Box	(1K Ω -10 K Ω)	1
3	Transformer	230 V AC	1
4	Capacitor	100 μ F	1
5	Bread Board		
6	Digital Voltmeter	(0-20)V (AC & DC)	2
7	Connecting Wires	As Required	

THEORY:

During positive half-cycle of the input voltage, the diode D1 is in forward bias and conducts through the load resistor R1. Hence the current produces an output voltage across the load resistor R1, which has the same shape as the +ve half cycle of the input voltage.

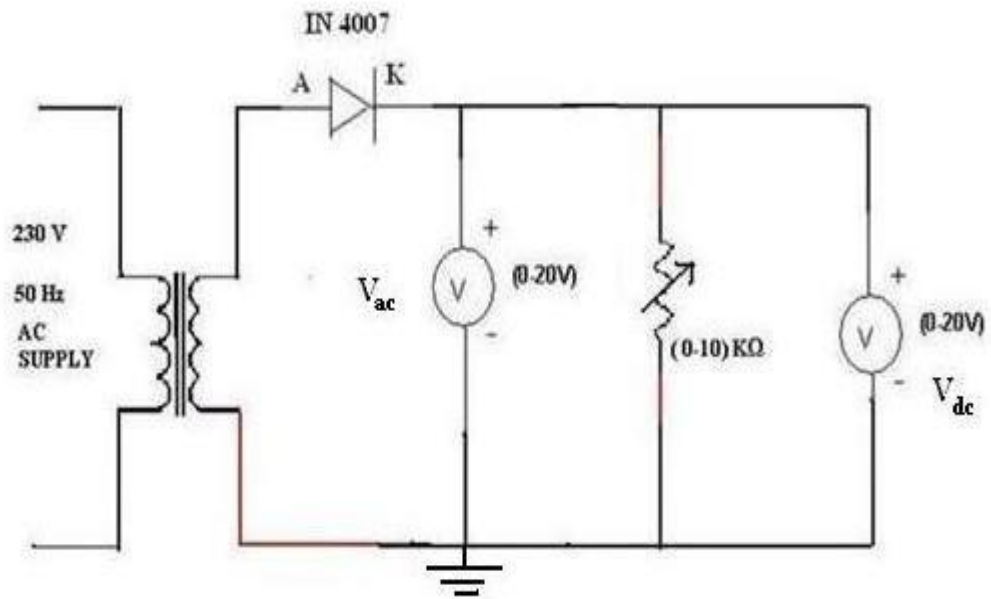
During the negative half-cycle of the input voltage, the diode is reverse biased and there is no current through the circuit. i.e, the voltage across R1 is zero. The net result is that only the +ve half cycle of the input voltage appears across the load. The average value of the half wave rectified o/p voltage is the value measured on dc voltmeter.

For practical circuits, transformer coupling is usually provided for two reasons.

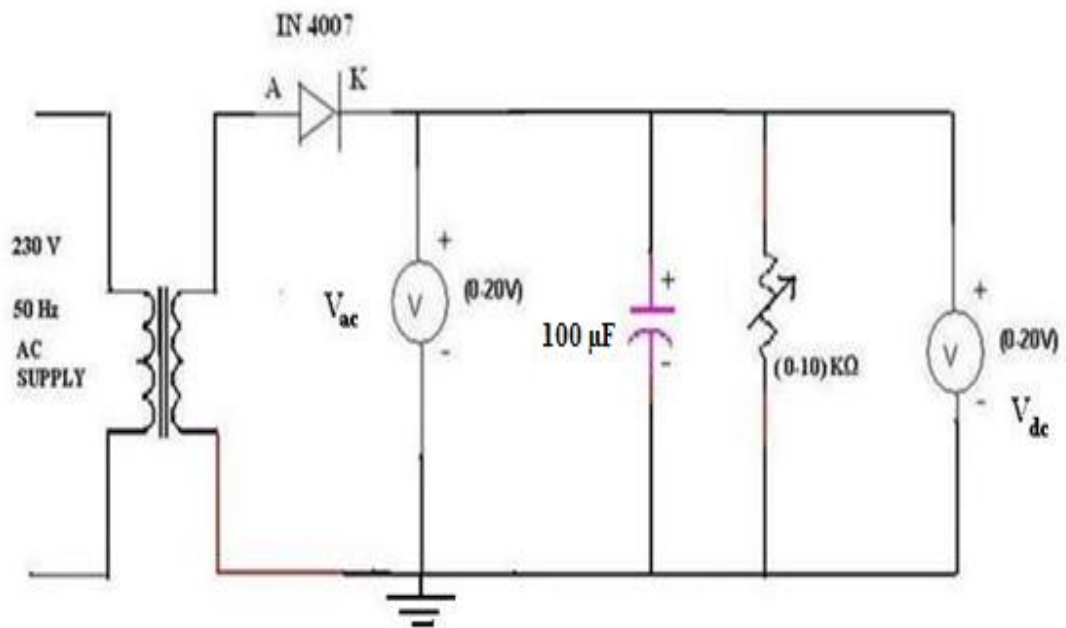
1. The voltage can be stepped-up or stepped-down, as needed.
2. The ac source is electrically isolated from the rectifier. Thus preventing shock hazards in the secondary circuit.

CIRCUIT DIAGRAM:

(a) WITHOUT FILTER:



(b) WITH FILTER:



PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Connect the primary side of the transformer to ac mains and the secondary side to the rectifier input.
3. By using the multimeter, measure the ac input voltage of the rectifier and, ac and dc voltage at the output of the rectifier.
4. Find the theoretical value of dc voltage by using the formula,

$$V_{dc} = V_m / \pi$$

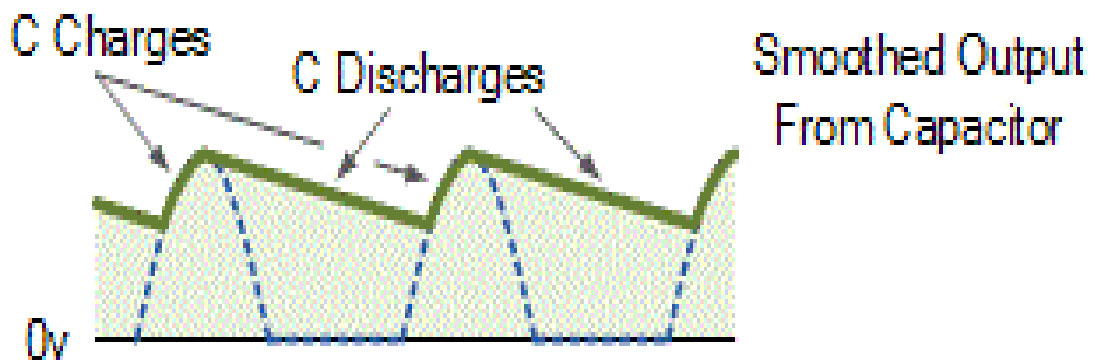
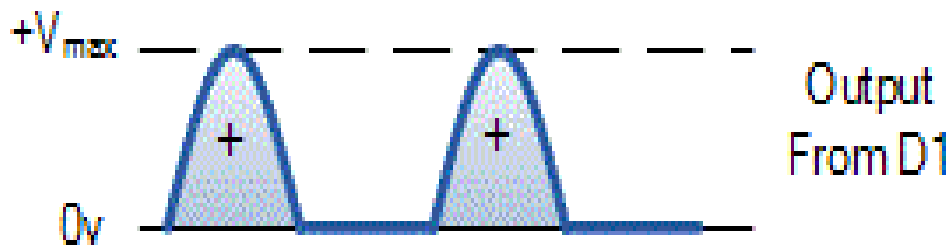
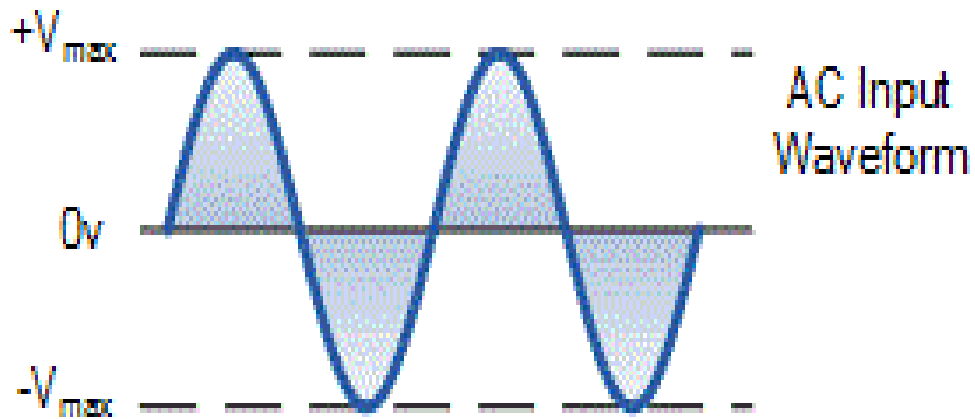
Where, $V_m = 2V_{rms}$, (V_{rms} = output ac voltage.)

Now, the Ripple factor is calculated by using the formula

$$\Gamma = \text{ac output voltage (} V_{ac} \text{) / dc output voltage (} V_{dc} \text{)}$$

5. By increasing the value of the resistance from 1 K Ω to 10K Ω , the voltage across the load (V_L) and current (I_L) flowing through the load are measured.
6. Draw a graph between load voltage (V_L) and load current (I_L) by taking V_L on X-axis and I_L on y-axis.
7. From the value of no-load voltage (V_{NL}), the % regulation is to be calculated from the theoretical calculations given below.

INPUT AND OUTPUT WAVEFORMS:



THEORETICAL CALCULATIONS FOR RIPPLE FACTOR & % REGULATION:

(a) WITH OUT FILTER:

For a Half-Wave Rectifier,

$$V_{rms} = V_m / 2$$

$$V_{dc} = V_m / \Pi$$

Therefore, Ripple factor $\Gamma = \sqrt{(V_{rms} / V_{dc})^2 - 1} = \underline{1.21}$

$$\% \text{ regulation} = [(V_{NL} - V_{FL}) / V_{FL}] * 100$$

(b) WITH FILTER:

Ripple factor for a Half-Wave Rectifier is $\Gamma = 1 / (2\sqrt{3} fRC)$.

Where $f = 50\text{Hz}$

$$C = 100\mu\text{F}$$

$$R = (1-10)\text{K}\Omega$$

Therefore, for $1\text{K}\Omega$, Ripple factor, $\Gamma = \underline{0.0577}$

$$\% \text{ regulation} = [(V_{NL} - V_{FL}) / V_{FL}] * 100$$

OBSERVATIONS:

(a) WITH OUT FILTER:

$$V_{NL} = \underline{\hspace{2cm}} \text{V}$$

S.No	Load Resistance (KΩ)	V _{ac} (v)	V _{dc} (v)	$\Gamma = V_{ac} / V_{dc}$	% Regulation

(b) WITH FILTER:

$$V_{NL} = \text{_____ V}$$

S.No	Load Resistance (K Ω)	V _{ac} (v)	V _{dc} (v)	$\Gamma = V_{ac} / V_{dc}$	% Regulation

PRECAUTIONS:

1. The primary and secondary sides of the transformer should be carefully identified.
2. The polarities of the diode should be carefully identified.
3. While determining the % regulation, first Full load should be applied and then it should be decremented in steps.

RESULT:

The Ripple factor and the % regulation for the Half-Wave Rectifier with and without filters are calculated.

1. The Ripple factor of Half-Wave Rectifier without filter is _____
2. The Ripple factor of Half-Wave Rectifier with filter is _____
3. The % Regulation of Half-Wave Rectifier without filter is _____
4. The % Regulation of Half-Wave Rectifier with filter is _____

(B) FULL WAVE RECTIFIER

AIM: 1. To obtain the load regulation and ripple factor of a full-wave rectifier by using

- (a). without Filter
- (b). with Filter

2. To observe the input and output waveforms of a full-wave rectifier.

APPARATUS:

S.No	Name of the Apparatus	Range	Quantity
1	Diodes IN 4007 (Si)		2
2	Decade Resistance Box	(1K Ω -10 K Ω)	1
3	Transformer	230 V AC	1
4	Capacitor	100 μ F	1
5	Bread Board		
6	Digital Voltmeter	(0-20)V (AC & DC)	2
7	Connecting Wires	As Required	

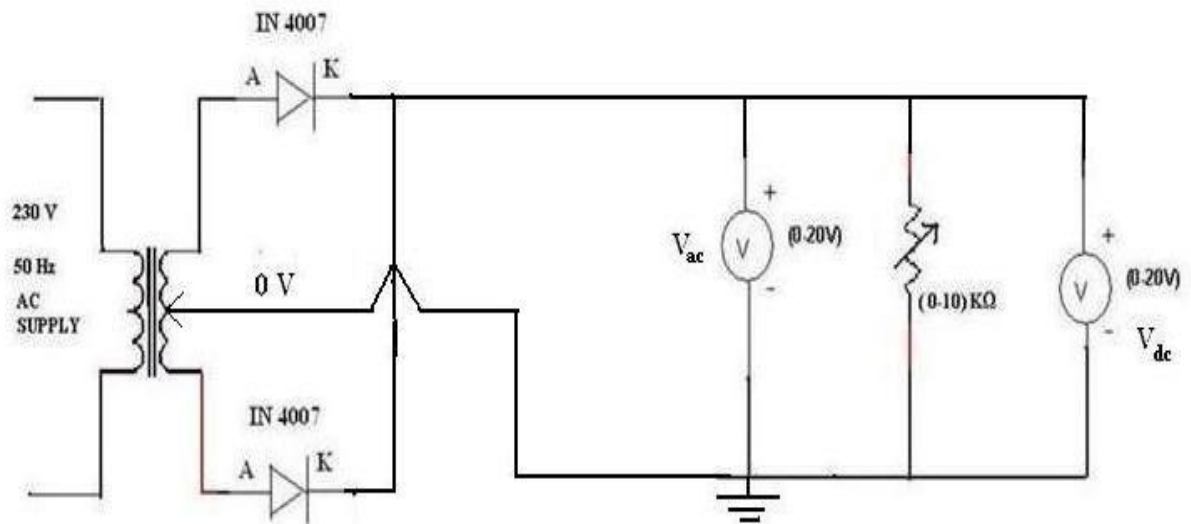
THEORY:

The circuit of a center-tapped full wave rectifier uses two diodes D1&D2. During positive half cycle of secondary voltage (input voltage), the diode D1 is forward biased and D2 is reverse biased.

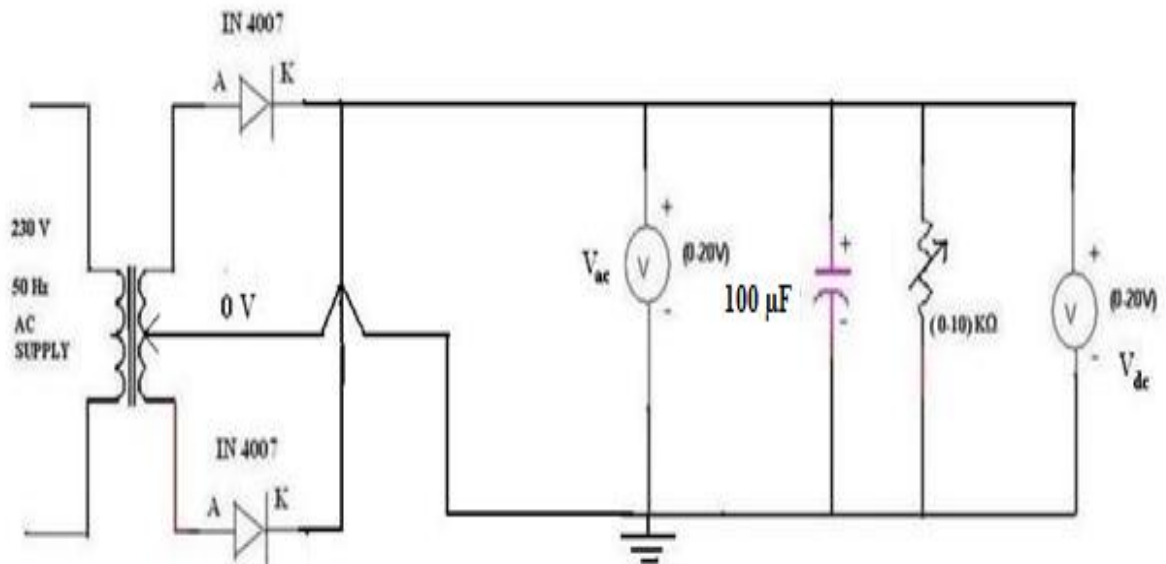
The diode D1 conducts and current flows through load resistor R_L . During negative half cycle, diode D2 becomes forward biased and D1 reverse biased. Now, D2 conducts and current flows through the load resistor R_L in the same direction. There is a continuous current flow through the load resistor R_L , during both the half cycles and will get unidirectional current as shown in the model graph. The difference between full wave and half wave rectification is that a full wave rectifier allows unidirectional (one way) current to the load during the entire 360 degrees of the input signal and half-wave rectifier allows this only during one half cycle (180 degree).

CIRCUIT DIAGRAM:

(a) WITHOUT FILTER:



(b) WITH FILTER:



PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Connect the primary side of the transformer to ac mains and the secondary side to the rectifier input.
3. By using the multimeter, measure the ac input voltage of the rectifier and, ac and dc voltage at the output of the rectifier.

4. Find the theoretical value of dc voltage by using the formula,

$$V_{dc} = 2V_m / \pi$$

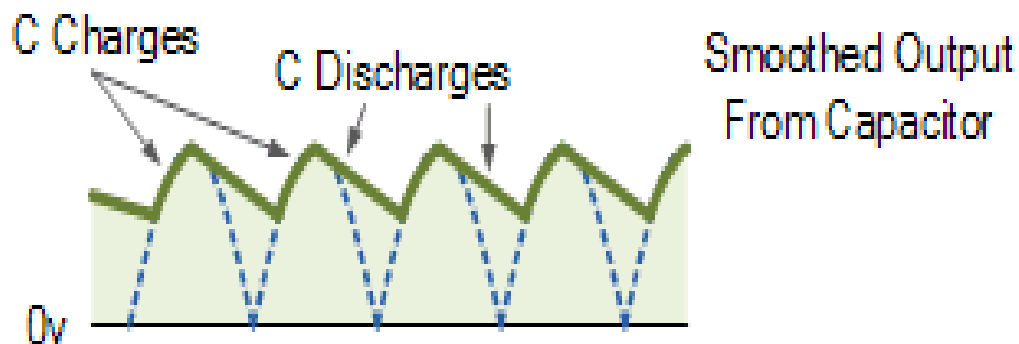
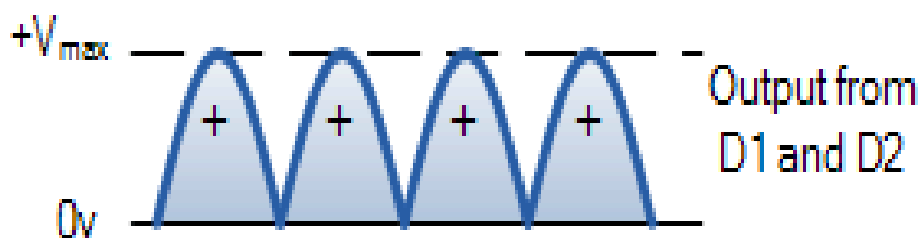
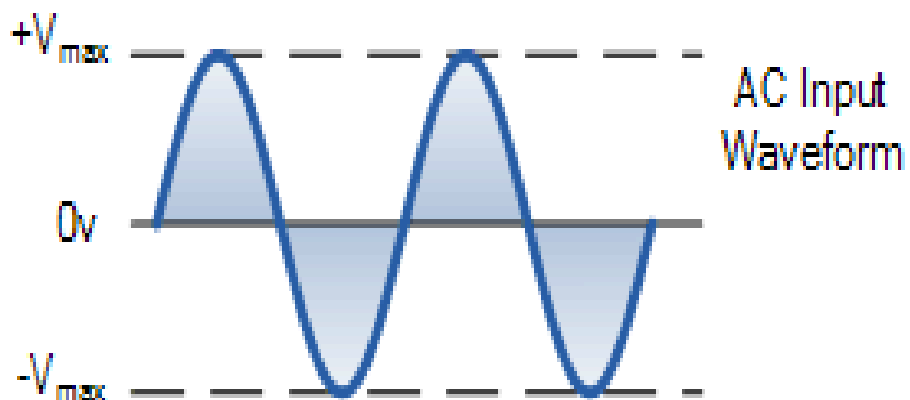
Where, $V_m = \sqrt{2}V_{rms}$, (V_{rms} =output ac voltage.)

5. Now, the Ripple factor is calculated by using the formula

$$\Gamma = \text{ac output voltage (} V_{ac} \text{) / dc output voltage (} V_{dc} \text{)}$$

6. By increasing the value of the resistance from 1 K Ω to 10K Ω , the voltage across the load (V_L) and current (I_L) flowing through the load are measured.
7. Draw a graph between load voltage (V_L) and load current (I_L) by taking V_L on X-axis and I_L on y-axis.
8. From the value of no-load voltage (V_{NL}), the % regulation is to be calculated from the theoretical calculations given below.

INPUT AND OUTPUT WAVEFORMS:



THEORETICAL CALCULATIONS FOR RIPPLE FACTOR & % REGULATION:

(a) WITHOUT FILTER:

For a Full-Wave Rectifier,

$$V_{rms} = V_m / \sqrt{2}$$

$$V_{dc} = 2V_m / \pi$$

Therefore, Ripple factor $\Gamma = \sqrt{(V_{rms} / V_{dc})^2 - 1} = \mathbf{0.482}$

$$\% \text{ regulation} = [(V_{NL} - V_{FL}) / V_{FL}] * 100$$

(b) WITH FILTER:

Ripple factor for a Full-Wave Rectifier is $\Gamma = 1 / (2\sqrt{3} fRC)$.

Where $f = 50\text{Hz}$

$C = 100\mu\text{F}$

$R = (1-10) \text{K}\Omega$

Therefore, for $1\text{K}\Omega$, Ripple factor, $\Gamma = \mathbf{0.0577}$

$$\% \text{ regulation} = [(V_{NL} - V_{FL}) / V_{FL}] * 100$$

OBSERVATIONS:

(a) WITH OUT FILTER:

$$V_{NL} = \text{_____ V}$$

S.No	Load Resistance (KΩ)	V _{ac} (v)	V _{dc} (v)	$\Gamma = V_{ac} / V_{dc}$	% Regulation

(b) *WITH FILTER*:

$$V_{NL} = \text{_____ V}$$

PRECAUTIONS:

S.No	Load Resistance (K Ω)	V _{ac} (v)	V _{dc} (v)	$\Gamma = V_{ac} / V_{dc}$	% Regulation

1. The primary and secondary sides of the transformer should be carefully identified.
2. The polarities of the diode should be carefully identified.
3. While determining the % regulation, first Full load should be applied and then it should be decremented in steps.

RESULT:

The Ripple factor and the % regulation for the Full-Wave Rectifier with and without filters are calculated.

1. The Ripple factor of Full-Wave Rectifier without filter is _____
2. The Ripple factor of Full-Wave Rectifier with filter is _____
3. The % Regulation of Full-Wave Rectifier without filter is _____
4. The % Regulation of Full-Wave Rectifier with filter is _____

VIVA QUESTIONS:

1. What is the PIV of Half wave rectifier?
2. What is the efficiency of half wave rectifier?
3. What is a rectifier?
4. What is the difference between the half wave rectifier and full wave Rectifier?
5. What is the output frequency of Bridge Rectifier?
6. What are the ripples?
7. What is the function of a filter?
8. What is TUF?
9. What is the average value of output voltage for a HWR?
10. What is the peak factor?

4. BJT CHARACTERISTICS (CE CONFIGURATION)

- AIM:** 1. To draw the input and output characteristics of transistor connected in CE Configuration
2. To find Input Resistance (R_i), Output Resistance (R_o) and Current amplification Factor (β) of the given transistor.

APPARATUS:

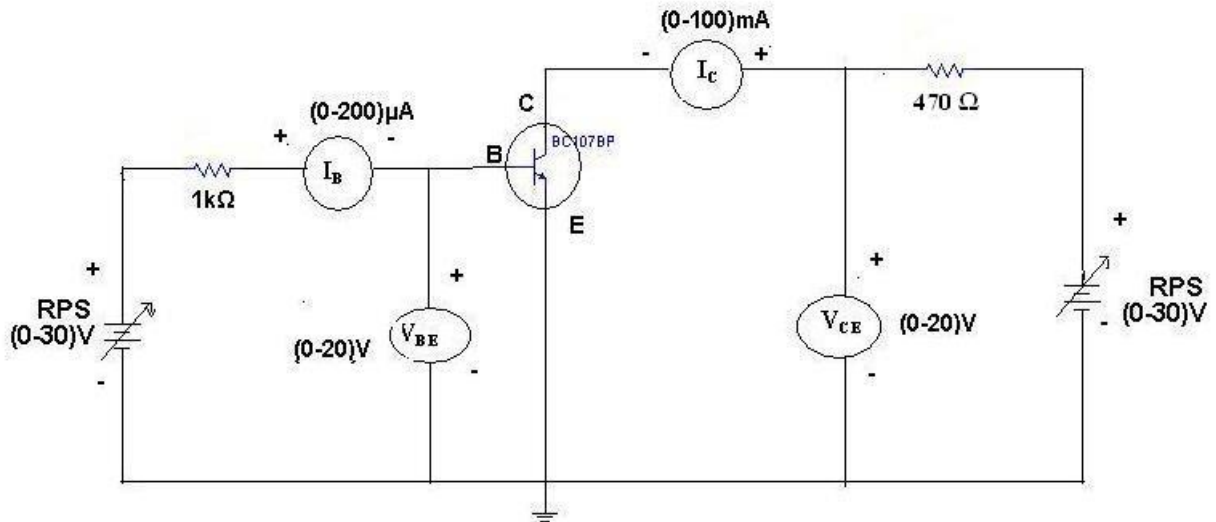
S.No	Name of the Apparatus	Range	Quantity
1	Transistor (BC-107)		1
2	Resistors	1K Ω , 470 Ω	1
3	Regulated Power Supply	(0-30)V DC	1
4	Bread Board		1
5	Digital Ammeters	(0-200) μ A/(0-200)mA	2
6	Digital Voltmeters	(0-20)V DC	2
7	Connecting Wires	As Required	

THEORY:

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and out put is taken across the collector and emitter terminals. Therefore the emitter terminal is common to both input and output.

The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement I_B increases less rapidly with V_{BE} . Therefore input resistance of CE circuit is higher than that of CB circuit.

The output characteristics are drawn between I_C and V_{CE} at constant I_B . the collector current varies with V_{CE} upto few volts only. After this the collector current becomes almost constant, and independent of V_{CE} . The value of V_{CE} up to which the collector current changes with V_{CE} is known as Knee voltage. The transistor always operated in the region above Knee voltage, I_C is always constant and is approximately equal to I_B . The current amplification factor of CE configuration is given by $\beta = \Delta I_C / \Delta I_B$

CIRCUIT DIAGRAM:**PROCEDURE:****(i) INPUT CHARACTERISTICS:**

1. Connect the circuit as per the circuit diagram.
2. For plotting the input characteristics the output voltage V_{CE} is kept constant at 1V and for different values of V_{BE} , note down the values of I_B .
3. Repeat the above step by keeping V_{CE} at 2V and 3V.
4. Tabulate all the readings.
5. Plot the graph between V_{BE} on x-axis and I_B on y-axis for constant V_{CE} .

(ii) OUTPUT CHARACTERISTICS:

1. Connect the circuit as per the circuit diagram.
2. For plotting the output characteristics the input current I_B is kept constant at $50\mu A$ and for different values of V_{CE} , note down the values of I_C .
3. Repeat the above step by keeping I_B at $75\mu A$ and $100\mu A$.
4. Tabulate the all the readings.
5. Plot the graph between V_{CE} on x-axis and I_C on y-axis for constant I_B .

OBSERVATIONS:**(i) INPUT CHARACTERISTICS:**

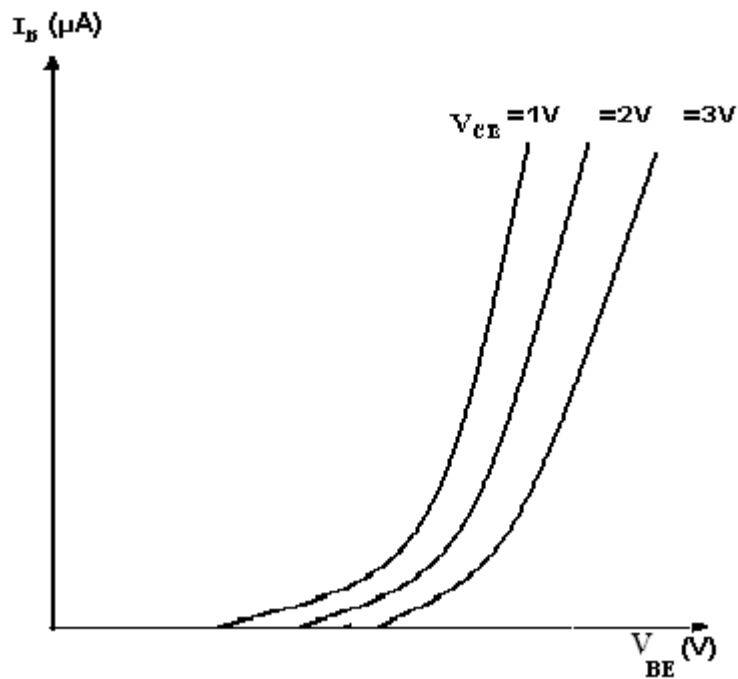
S.No	$V_{CE} = 1V$		$V_{CE} = 2V$		$V_{CE} = 3V$	
	$V_{BE} (V)$	$I_B (\mu A)$	$V_{BE} (V)$	$I_B (\mu A)$	$V_{BE} (V)$	$I_B (\mu A)$

(ii) OUTPUT CHARACTERISTICS:

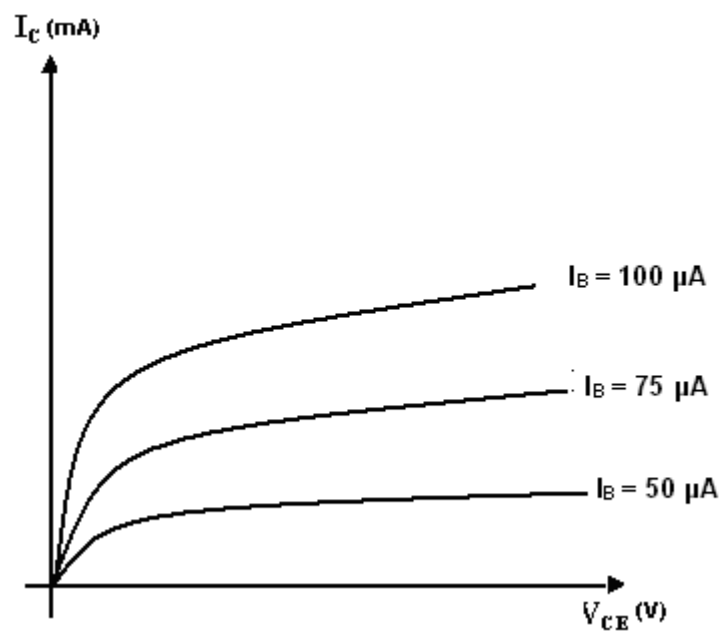
S.No	$I_B = 50 \mu A$		$I_B = 75 \mu A$		$I_B = 100 \mu A$	
	$V_{CE} (V)$	$I_C (mA)$	$V_{CE} (V)$	$I_C (mA)$	$V_{CE}(V)$	$I_C (mA)$

MODEL GRAPH:

(i) INPUT CHARACTERISTICS:



(ii) OUTPUT CHARACTERISTICS:



PRECAUTIONS:

1. While doing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base and collector terminals of the transistor.

CALCULATIONS:

1. **Input resistance:** To obtain input resistance find ΔV_{BE} and ΔI_B at constant V_{CE} on one of the input characteristics. Then

$$R_i = \Delta V_{BE} / \Delta I_B \text{ (} V_{CE} \text{ constant)}$$

2. **Output resistance:** To obtain output resistance, find ΔI_C and ΔV_{CE} at constant I_B .

$$R_o = \Delta V_{CE} / \Delta I_C \text{ (} I_B \text{ constant)}$$

3. The current amplification factor of CE configuration is given by

$$\beta = \Delta I_C / \Delta I_B$$

RESULT: The input and output characteristics of a transistor in CE configuration are drawn. The Input (R_i) and Output resistances (R_o) and β of a given transistor are calculated.

1. The Input resistance (R_i) of a given Transistor is _____
2. The Output resistance (R_o) of a given Transistor is _____
3. The Current amplification factor is _____

VIVA QUESTIONS:

1. What is the range of β for the transistor?
2. What are the input and output impedances of CE configuration?
3. Identify various regions in the output characteristics?
4. What is the relation between α and β ?
5. Define current gain in CE configuration?
6. What is the phase relation between input and output?
7. Draw diagram of CE configuration for PNP transistor?
8. What is the power gain of CE configuration?
9. What are the applications of CE configuration?

5. FET CHARACTERISTICS (CS CONFIGURATION)

- AIM:**
1. To draw the Drain and Transfer characteristics of a given FET in CS Configuration.
 2. To find the drain resistance (r_d), amplification factor (μ) and Trans-Conductance (g_m) of the given FET.

APPARATUS:

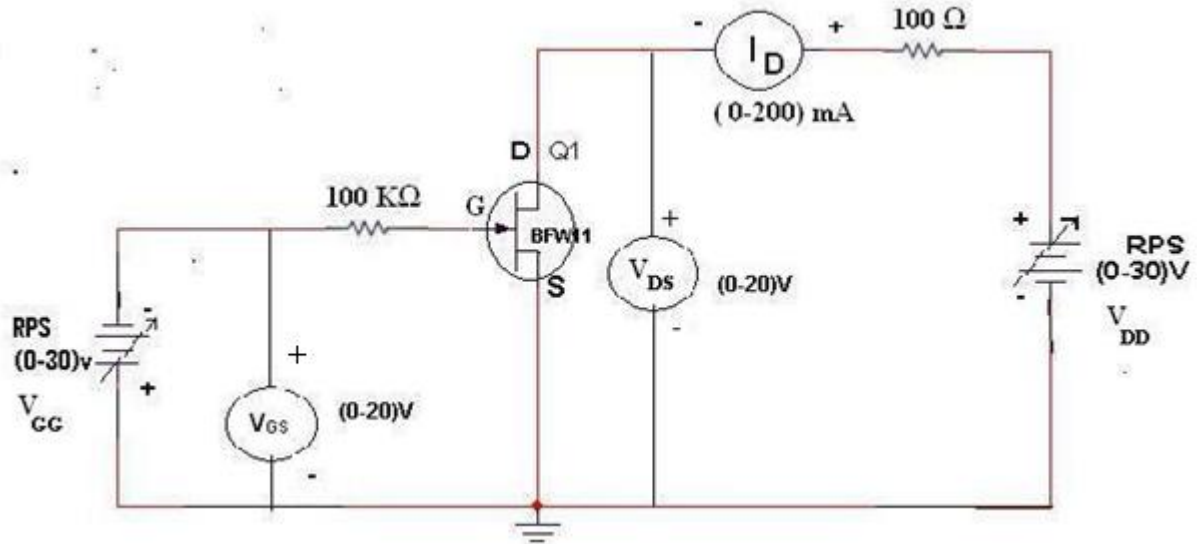
S.No	Name of the Apparatus	Range	Quantity
1	JFET (BFW-10)		1
2	Resistors	100K Ω , 100 Ω	1
3	Regulated Power Supply	(0-30)V DC	1
4	Bread Board		1
5	Digital Ammeter	(0-200)mA	1
6	Digital Voltmeter	(0-20)V DC	2
7	Connecting Wires	As Required	

THEORY:

A FET is a three terminal device, having the characteristics of high input impedance and less noise, the Gate to Source junction of the FET is always reverse biased. In response to small applied voltage from drain to source, the n-type bar acts as sample resistor, and the drain current increases linearly with V_{DS} . With increase in I_D the ohmic voltage drop between the source and the channel region reverse biases the junction and the conducting position of the channel begins to remain constant. The V_{DS} at this instant is called “pinch of voltage”.

If the gate to source voltage (V_{GS}) is applied in the direction to provide additional reverse bias, the pinch off voltage will be decreased. In amplifier application, the FET is always used in the region beyond the pinch-off.

$$I_{DS} = I_{DSS} (1 - V_{GS}/V_P)^2$$

CIRCUIT DIAGRAM:**PROCEDURE:**

1. All the connections are made as per the circuit diagram.
2. To plot the drain characteristics, keep V_{GS} constant at 0V.
3. Vary the V_{DD} and observe the values of V_{DS} and I_D .
4. Repeat the above steps 2, 3 for different values of V_{GS} at -1V and -2V.
5. All the readings are tabulated.
6. To plot the transfer characteristics, keep V_{DS} constant at 0.5V.
7. Vary V_{GG} and observe the values of V_{GS} and I_D .
8. Repeat steps 6 and 7 for different values of V_{DS} at 1V and 1.5V.
9. The readings are tabulated.
10. From drain characteristics, calculate the values of drain resistance (r_d) by using the formula

$$r_d = \Delta V_{DS} / \Delta I_D$$

11. From transfer characteristics, calculate the value of trans-conductance (g_m) by using the formula

$$g_m = \Delta I_D / \Delta V_{GS}$$

12. Amplification factor (μ) = drain resistance (r_d) x Trans-conductance (g_m)

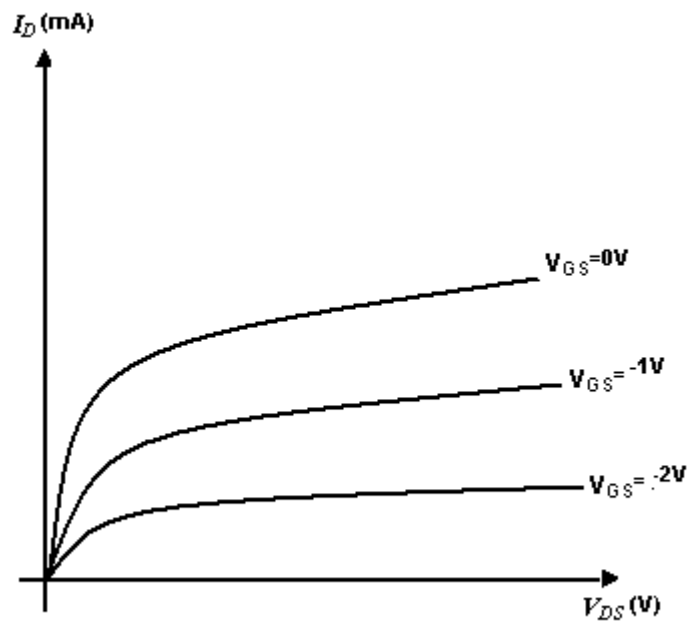
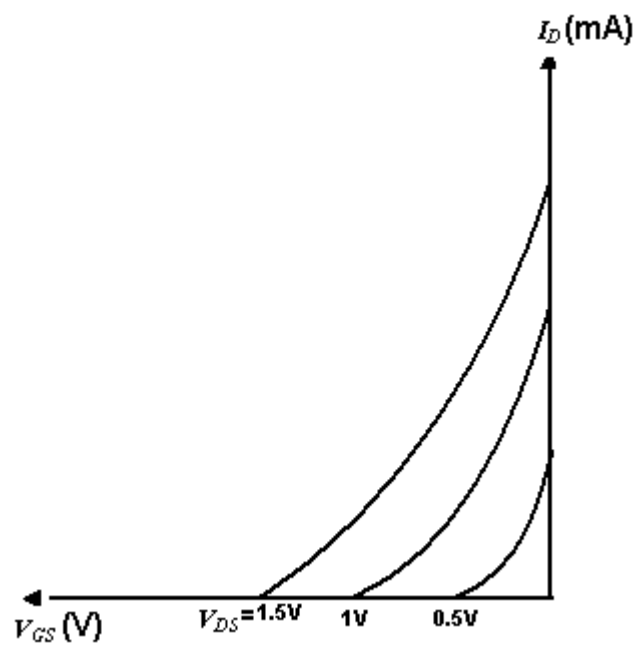
$$\mu = \Delta V_{DS} / \Delta V_{GS}$$

OBSERVATIONS:**(i) DRAIN CHARACTERISTICS:**

S.No	$V_{GS} = 0V$		$V_{GS} = -1V$		$V_{GS} = -2V$	
	V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)

(ii) TRANSFER CHARACTERISTICS:

S.No	$V_{DS} = 0.5V$		$V_{DS} = 1V$		$V_{DS} = 1.5V$	
	V_{GS} (V)	I_D (mA)	V_{GS} (V)	I_D (mA)	V_{GS} (V)	I_D (mA)

MODEL GRAPH:**(i) DRAIN CHARACTERISTICS:****(ii) TRANSFER CHARACTERISTICS:**

PRECAUTIONS:

1. While doing the experiment do not exceed the ratings of the FET. This may lead to damage the FET.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the Source, Drain and Gate terminals of the FET.

RESULT:

1. The drain and transfer characteristics of a given FET are drawn.
2. The drain resistance (r_d), amplification factor (μ) and Trans-conductance (g_m) of the given FET are calculated.
 - (i) The drain resistance (r_d) of FET is _____
 - (ii) Trans-conductance (g_m) of FET is _____
 - (iii) Amplification factor (μ) of FET is _____

VIVA QUESTIONS:

1. What are the advantages of FET?
2. Different between FET and BJT?
3. Explain different regions of V-I characteristics of FET?
4. What are the applications of FET?
5. What are the types of FET?
6. Draw the symbol of FET.
7. What are the disadvantages of FET?
8. What are the parameters of FET?

6. SCR CHARACTERISTICS

- AIM:**
1. To draw the V-I characteristics of SCR.
 2. To find the Break-over voltage (V_{BO}) and Holding current (I_H) of SCR.

APPARATUS:

S.No	Name of the Apparatus	Range	Quantity
1	SCR (TYN616)		1
2	Resistors	1K Ω , 10K Ω	1
3	Regulated Power Supply	(0-30)V DC	1
4	Bread Board		1
5	Digital Ammeter	(0-200)mA,(0-200) μ A	2
6	Digital Voltmeter	(0-20)V DC	1
7	Connecting Wires	As Required	

THEORY:

It is a four layer semiconductor device being alternate of P-type and N-type silicon. It consists of 3 junctions J_1 , J_2 , J_3 the J_1 and J_3 operate in forward direction and J_2 operates in reverse direction and three terminals called anode A, cathode K, and a gate G. The operation of SCR can be studied when the gate is open and when the gate is positive with respect to cathode. When gate is open, no voltage is applied at the gate due to reverse bias of the junction J_2 no current flows through R_2 and hence SCR is at cut off. When anode voltage is increased J_2 tends to breakdown.

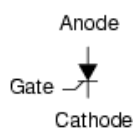
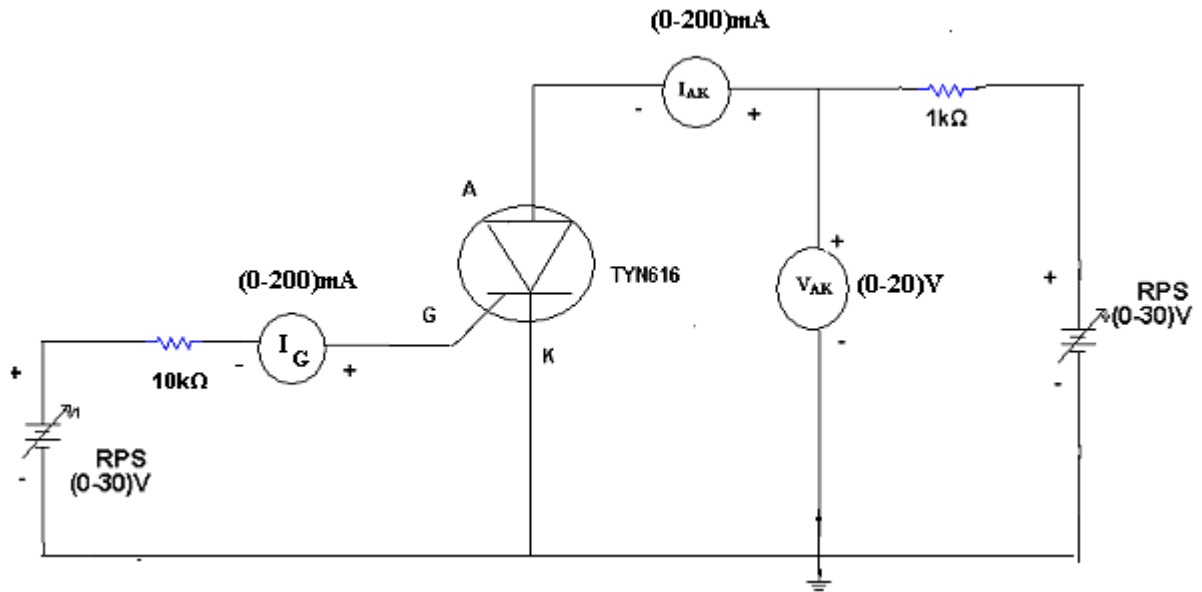


Fig.: Symbol of SCR

When the gate positive, with respect to cathode J_3 junction is forward biased and J_2 is reverse biased. Electrons from N-type material move across junction J_3 towards gate while holes from P-type material moves across junction J_3 towards cathode. So gate current starts flowing, anode current increase is in extremely small current junction J_2 break down and SCR conducts heavily. When gate is open the break over voltage is determined on the minimum forward voltage at which SCR conducts heavily. Now most of the supply voltage appears across the load resistance. The holding current is the maximum anode current gate being open, when break over occurs.

CIRCUIT DIAGRAM:

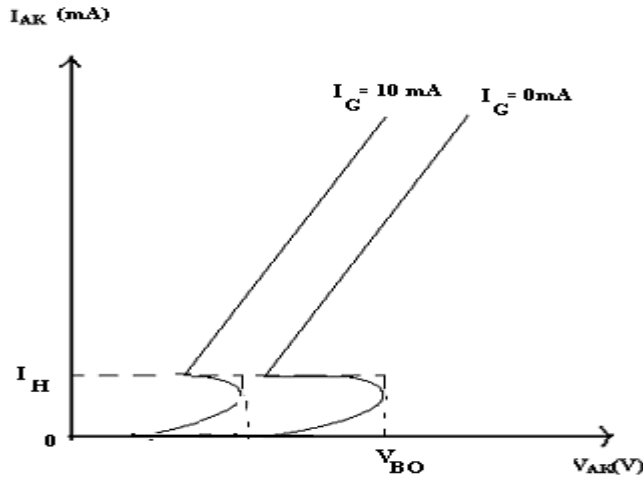


PROCEDURE:

1. All the connections are made as per the circuit diagram.
2. Keep the gate current (I_G) open i.e. $I_G = 0$ mA.
3. Vary the anode to cathode supply voltage and note down the readings of Voltage V_{AK} (V), and Current I_{AK} (μ A).
4. Now Keep the gate current (I_G) at a standard value of 10 mA i.e. $I_G = 10$ mA.
5. Again vary the anode to cathode supply voltage and note down the corresponding readings of Voltage V_{AK} (V), and Current I_{AK} (mA).
6. Plot the graph by taking V_{AK} (V) on x-axis and Current I_{AK} (mA) on y-axis.
7. Measure the Break-over voltage (V_{BO}) and Holding current (I_H) of SCR from the graph.

OBSERVATIONS:

S.No	$I_G = 0$ mA		$I_G = 10$ mA	
	V_{AK} (V)	I_{AK} (μ A)	V_{AK} (V)	I_{AK} (mA)

MODEL GRAPH:**PRECAUTIONS:**

1. While doing the experiment do not exceed the ratings of the SCR. This may lead to damage the SCR.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the Anode, Cathode and Gate terminals of the SCR.

RESULT: The V-I characteristics of SCR are drawn and the Break-over voltage (V_{BO}), Holding current (I_H) of SCR are found.

1. The Break-over voltage (V_{BO}) of SCR is _____.
2. The Holding current (I_H) of SCR is _____.

VIVA QUESTIONS:

1. What the symbol of SCR?
2. In which state SCR turns of conducting state to blocking state?
3. What are the applications of SCR?
4. What is holding current?
5. What are the important type's thyristors?
6. How many numbers of junctions are involved in SCR?
7. What is the function of gate in SCR?
8. When gate is open, what happens when anode voltage is increased?
9. What is the value of forward resistance offered by SCR?
10. What is the condition for making from conducting state to non conducting state?

7. UJT CHARACTERISTICS

- AIM:**
1. To Study and plot the Emitter characteristics of a UJT.
 2. To find the peak voltage (V_p) and valley voltage (V_v) for a given UJT.

APPARATUS:

S.No	Name of the Apparatus	Range	Quantity
1	UJT (2N2646)		1
2	Resistors	1K Ω	2
3	Regulated Power Supply	(0-30)V DC	1
4	Bread Board		1
5	Digital Ammeter	(0-200)mA	1
6	Digital Voltmeter	(0-20)V DC	2
7	Connecting Wires	As Required	

THEORY:

A Unijunction Transistor (UJT) is an electronic semiconductor device that has only one junction. The UJT Unijunction Transistor (UJT) has three terminals an emitter (E) and two bases (B1 and B2). The base is formed by lightly doped n-type bar of silicon. Two ohmic contacts B1 and B2 are attached at its ends. The emitter is of p-type and it is heavily doped. The resistance between B1 and B2, when the emitter is open-circuit is called interbase resistance. The original unijunction transistor, or UJT, is a simple device that is essentially a bar of N type semiconductor material into which P type material has been diffused somewhere along its length. The 2N2646 is the most commonly used version of the UJT.

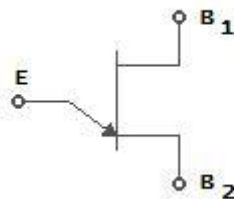
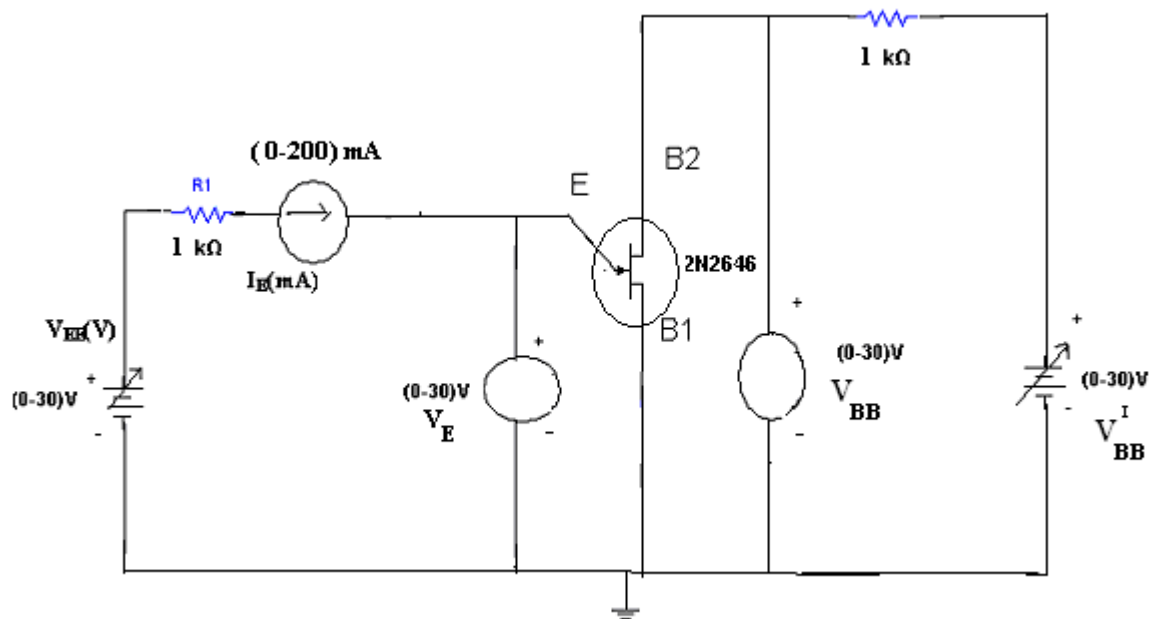


Fig: Circuit symbol of UJT

The UJT is biased with a positive voltage between the two bases. This causes a potential drop along the length of the device. When the emitter voltage is driven approximately one diode voltage above the voltage at the point where the P diffusion (emitter) is, current will begin to

flow from the emitter into the base region. Because the base region is very lightly doped, the additional current (actually charges in the base region) causes (conductivity modulation) which reduces the resistance of the portion of the base between the emitter junction and the B2 terminal. This reduction in resistance means that the emitter junction is more forward biased, and so even more current is injected. Overall, the effect is a negative resistance at the emitter terminal. This is what makes the UJT useful, especially in simple oscillator circuits. When the emitter voltage reaches V_P , the current starts to increase and the emitter voltage starts to decrease. This is represented by negative slope of the characteristics which is referred to as the negative resistance region, beyond the valley point, R_{B1} reaches minimum value and this region, V_{EB} proportional to I_E .

CIRCUIT DIAGRAM:



PROCEDURE:

1. All the connections are made as per the circuit diagram.
2. The output Base voltage (V_{BB}) is fixed at 5V by varying V_{BB}^I .
3. Varying V_{EE} gradually, note down both the Emitter current (I_E) and Emitter voltage (V_E).
4. Repeat Step 3 for $V_{BB} = 10V$.
5. Plot the graph by taking I_E (mA) on x-axis and V_E (v) on y-axis.

PRECAUTIONS:

1. While doing the experiment do not exceed the ratings of the UJT. This may lead to damage the UJT.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base-1 and base-2 terminals of the UJT.

RESULT: The Emitter characteristics of a UJT are studied and plotted. The peak voltage (V_p) and valley voltage (V_v) for a given UJT are found.

1. The peak voltage (V_p) of a UJT is _____.
2. The valley voltage (V_v) of a UJT is _____.

VIVA QUESTIONS:

1. Draw the equivalent circuit of UJT?
2. What are the applications of UJT?
3. Write the formula for the intrinsic stand off ratio?
4. What does it indicate the direction of arrow in the UJT?
5. What is the difference between FET and UJT?
6. Is UJT used as an oscillator? Why?
7. What is the Resistance between B_1 and B_2 called as?
8. What is its value of resistance between B_1 and B_2 ?
9. Draw the characteristics of UJT?

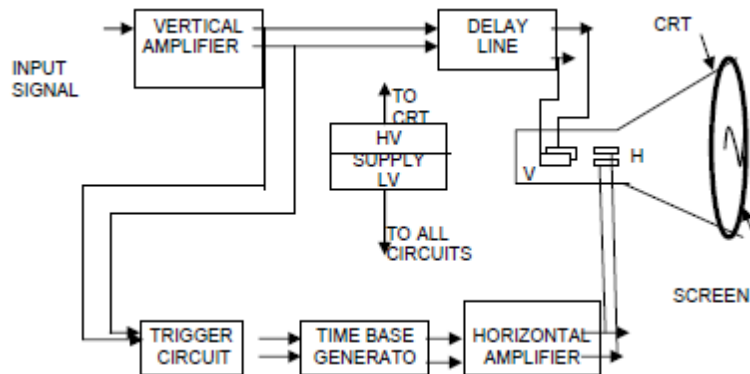
8. CRO OPERATION AND ITS MEASUREMENTS

AIM: To study the operation and applications of Cathode Ray Oscilloscope.

APPARATUS:

S.No	Name of the Apparatus	Range	Quantity
1	Resistor	1K Ω	1
2	Capacitor	0.1 μ F	1
3	CRO	(100-20M)Hz	1
4	Function generator	(100-1M)Hz	1
5	Digital Voltmeters	(0-20)V DC	1
6	Connecting Wires	As Required	

THEORY:



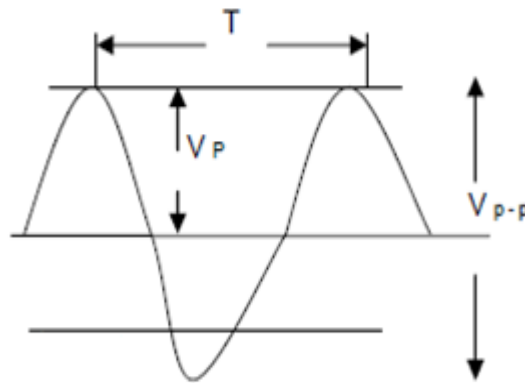
An oscilloscope is a measuring device used commonly for measurement of voltage, current, frequency, phase difference and time intervals. The heart of the oscilloscope is the cathode ray tube, which generates the electron beam, accelerates the beam to high velocity, deflects the beam to create the image, and contains the phosphor screen where the electron beam eventually becomes visible. To accomplish these tasks, various electrical signals and voltages are required. The power supply block provides the voltages required by the cathode ray tube to generate and accelerate the electron beam, as well as to supply the required operating voltages for the other circuits of the oscilloscope. Relatively high voltages are required by the cathode tubes, on the order of a few thousand volts, for acceleration, as well as a low voltage for the heater of the electron gun, which emits the electrons. Supply voltages for the other circuits are various values usually not more than few hundred volts.

The oscilloscope has a time base, which generates the correct voltage to supply the cathode ray tube to deflect this part at a constant time dependent rate. The signal to be view is fed to you vertical amplifier, which increases the potential of the input signal to a level that will

provide a usable deflection of the electron beam. To synchronize the horizontal deflection the vertical input, such that the horizontal deflection starts at the same point of the input vertical signal each time it sweeps, a synchronizing or triggering circuit is used. This circuit is the link between the vertical input and the horizontal time base.

PROCEDURE:

VOLTAGE AND TIME PERIOD MEASUREMENT:



1. Select the sine output of the signal generator, set at 1 KHz
2. Feed the signal to the vertical input of CRO.
3. Adjust level and time base to get one or two cycles of the sine signal on the oscilloscope, and Calculate the vertical scale.

4. Count the number of vertical divisions N_V on the scope and find peak-peak level.

$$V_{pp} = N_V \times (\text{Volts/Division})$$

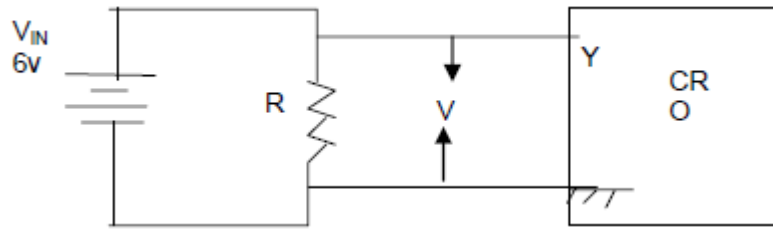
Calculate V_{rms} as $V_{pp} / 2\sqrt{2}$

5. Measure the signal with an AC milli voltmeter as well. It gives the rms value of the signal.
6. Measure the Time period 'T' of the signal by counting the number of horizontal divisions N_H covering the span of one cycle.

$$T = N_H \times (\text{Time/Division})$$

7. Calculate the frequency as $f = 1/T$.
8. Apply DC voltage from the regulated power supply and measure the DC level on the scope.

CURRENT MEASUREMENT BY A TEST RESISTOR:

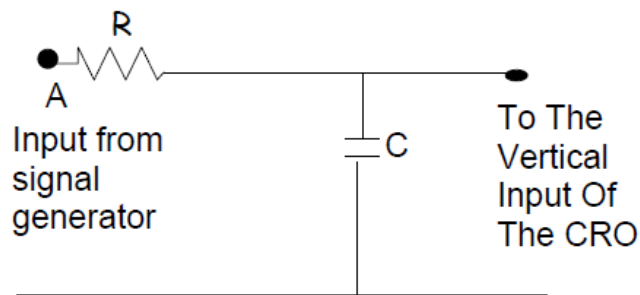


1. Connect a 1KΩ Resistor of enough wattage.
2. Measure the voltage across this resistor on the scope.
3. Calculate current as $I = V/R$.

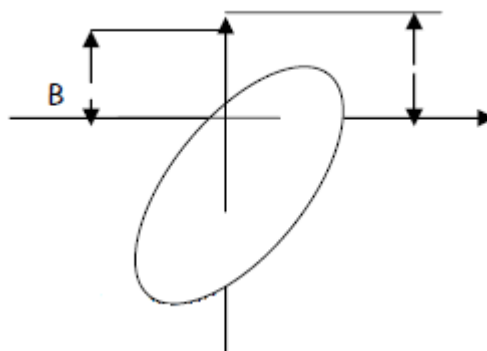
PHASE MEASUREMENT USING LISSAJOUS PATTERNS (X-Y MODE):

To Measure the phase difference of two sine waves their frequencies must be equal.

1. Connect a 1Volt peak-peak, 1 KHz sine wave signal from the function generator to the horizontal input of the CRO.
2. Connect the output of phase shift network to the vertical input as shown in figure.



3. Adjust the vertical and horizontal gains properly for good display.



4. Observe Lissajous Patterns for different combinations of R and C values.
5. Calculate the phase angle as $\text{Sine } \Phi = A/B$

A: Distance between the points where the ellipse crosses the y-axis and the origin.

B: Distance between the origin and the y – co-ordinate of the maxima of the ellipse.

6. Calculate theoretical phase difference as $\theta = \tan^{-1}(f_1/f_2)$

Where $f_2 = 1/(2\pi RC)$

f_1 = input signal frequency.

OBSERVATIONS:

1. AC VOLTAGE & FREQUENCY MEASUREMENT:

S.No	Input Signal Frequency (Hz)	CRO Reading		$V_{rms} =$ $V_{pp}/2\sqrt{2}$	Frequency $f=1/T$ (Hz)
		Peak-to-Peak amplitude (V_{pp})	Time period T (ms)		

2. DC VOLTAGE & DC CURRENT MEASUREMENT:

S.No	DC Input Voltage (V)	CRO Reading DC Voltage (Vdc) (V)	DC Current $I_{dc}=V_{dc}/R$ (A)

3. PHASE MEASUREMENT USING LISSAJOUS PATTERN:

S.No	Lissajous Pattern	Practical Phase Difference (Φ)	Theoretical Phase Difference (θ)

RESULT: The operation and applications of Cathode ray oscilloscope have been studied.

VIVA QUESTIONS:

1. How can DC current be measured?
2. Compare the triggering mode method and XY-mode method of frequency measurement?
3. Calculate the frequency for a time period of 50ms, 500ms?
4. Calculate the time period for the frequency of 500 KHz, 200 KHz?

9. BJT - CE AMPLIFIER

- AIM:**
1. To obtain the frequency response of the Common Emitter BJT Amplifier.
 2. To Measure the Voltage gain and Bandwidth of CE amplifier.

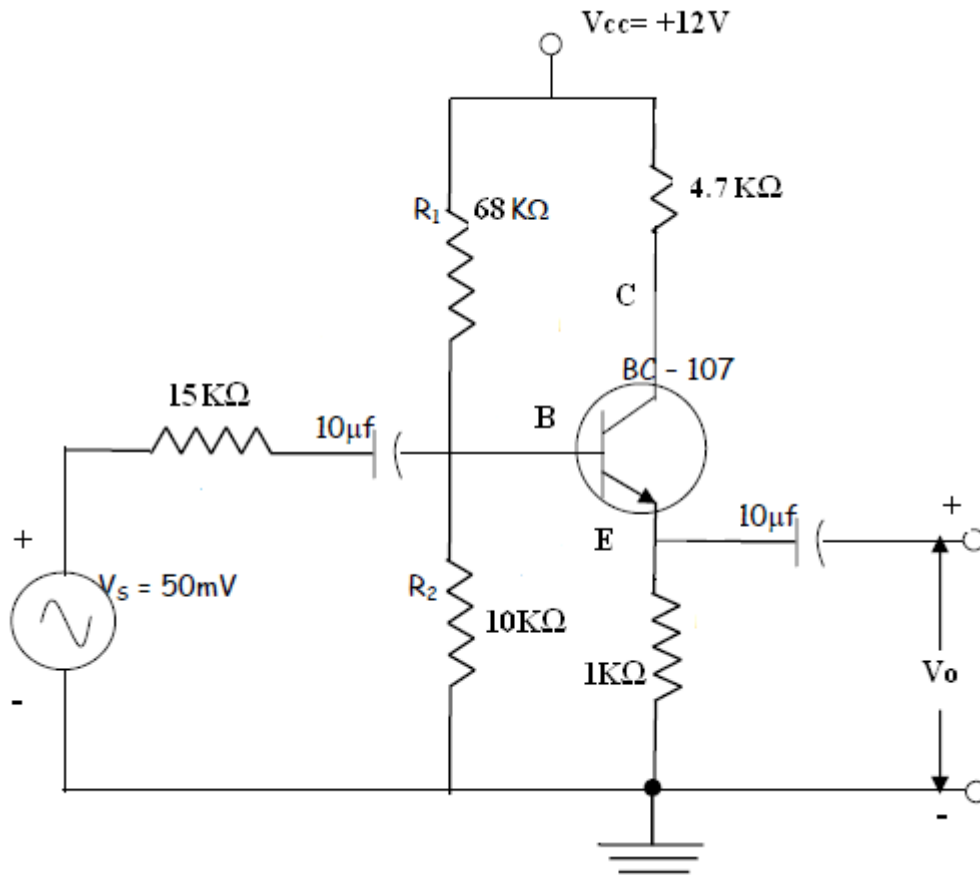
APPARATUS:

8

S.No	Name of the Apparatus	Range	Quantity
1	Transistor (BC-107)		1
2	Resistors	1K Ω , 4.7K Ω , 10K Ω , 15 K Ω , 68 K Ω	1
3	Capacitors	10 μ F 47 μ F	2 1
4	Bread Board		1
5	Regulated Power Supply	(0-30)V DC	1
6	Function Generator	(100-1M)Hz	1
7	CRO	(100-20M)Hz	1
7	Connecting Wires	As Required	

THEORY:

The CE amplifier provides high gain & wide frequency response. The emitter lead is common to both input & output circuits and is grounded. The emitter-base circuit is forward biased. The collector current is controlled by the base current rather than emitter current. The input signal is applied to base terminal of the transistor and amplifier output is taken across collector terminal. A very small change in base current produces a much larger change in collector current. When +ve half-cycle is fed to the input circuit, it opposes the forward bias of the circuit which causes the collector current to decrease, it decreases the voltage more -ve. Thus when input cycle varies through a -ve half-cycle, increases the forward bias of the circuit, which causes the collector current to increase thus the output signal is common emitter amplifier is in out of phase with the input signal.

CIRCUIT DIAGRAM:**PROCEDURE:**

1. Connect the circuit as per the circuit diagram.
2. Set Source Voltage $V_s = 50\text{mV}$ (say) at 1 KHz frequency, using function generator.
3. Keeping the input voltage constant, vary the frequency from 50Hz to 1MHz in regular steps and note down the corresponding output voltage.
4. Calculate the Voltage Gain by using the formula

$$A_v = \text{Output voltage } (V_o) / \text{Input voltage } (V_s)$$

5. Calculate the Voltage Gain in dB by using Voltage Gain $A_v (\text{dB}) = 20 \log_{10} (V_o/V_s)$.
6. Plot the Graph by taking Voltage gain (dB) on x-axis and frequency (Hz) on y-axis.
7. The Bandwidth of the amplifier is calculated from the graph using the expression,

$$\text{Bandwidth, } BW = f_2 - f_1$$

Where f_1 is lower 3-dB frequency

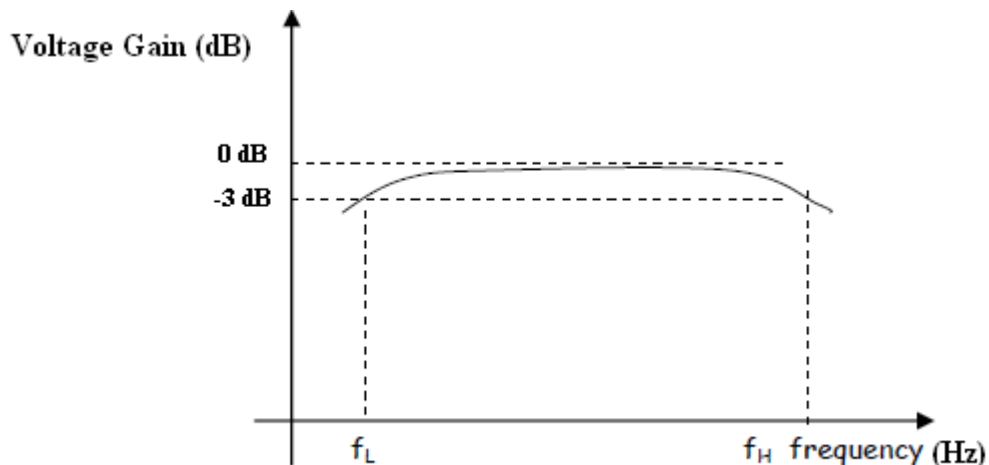
f_2 is upper 3-dB frequency

OBSERVATIONS:

$V_s = \text{_____ V}$

S.No	Input Frequency (Hz)	Output Voltage (V_o) (volts)	Voltage Gain= V_o/V_s	Voltage Gain (dB) = $20 \log_{10} (V_o/V_s)$

FREQUENCY RESPONSE:



PRECAUTIONS:

1. While doing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.
2. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.
3. Make sure while selecting the emitter, base and collector terminals of the transistor.

RESULT: The Voltage gain and Bandwidth of CE amplifier is measured and the frequency response of the CE Amplifier is obtained.

1. The Voltage gain of CE Amplifier is _____.
2. The Bandwidth of CE Amplifier is _____.

VIVA QUESTIONS:

1. What is phase difference between input and output waveforms of CE amplifier?
2. What type of biasing is used in the given circuit?
3. If the given transistor is replaced by a p-n-p, can we get output or not?
4. What is effect of emitter-bypass capacitor on frequency response?
5. What is the effect of coupling capacitor?
6. What is region of the transistor so that it is operated as an amplifier?
7. How does transistor acts as an amplifier?
8. Draw the h-parameter model of CE amplifier?
9. What type of transistor configuration is used in intermediate stages of a multistage amplifier?

10. EMITTER FOLLOWER (CC AMPLIFIER)

- AIM:**
1. To obtain the frequency response of the Common Collector BJT Amplifier.
 2. To Measure the Voltage gain and Bandwidth of CC amplifier.

APPARATUS:

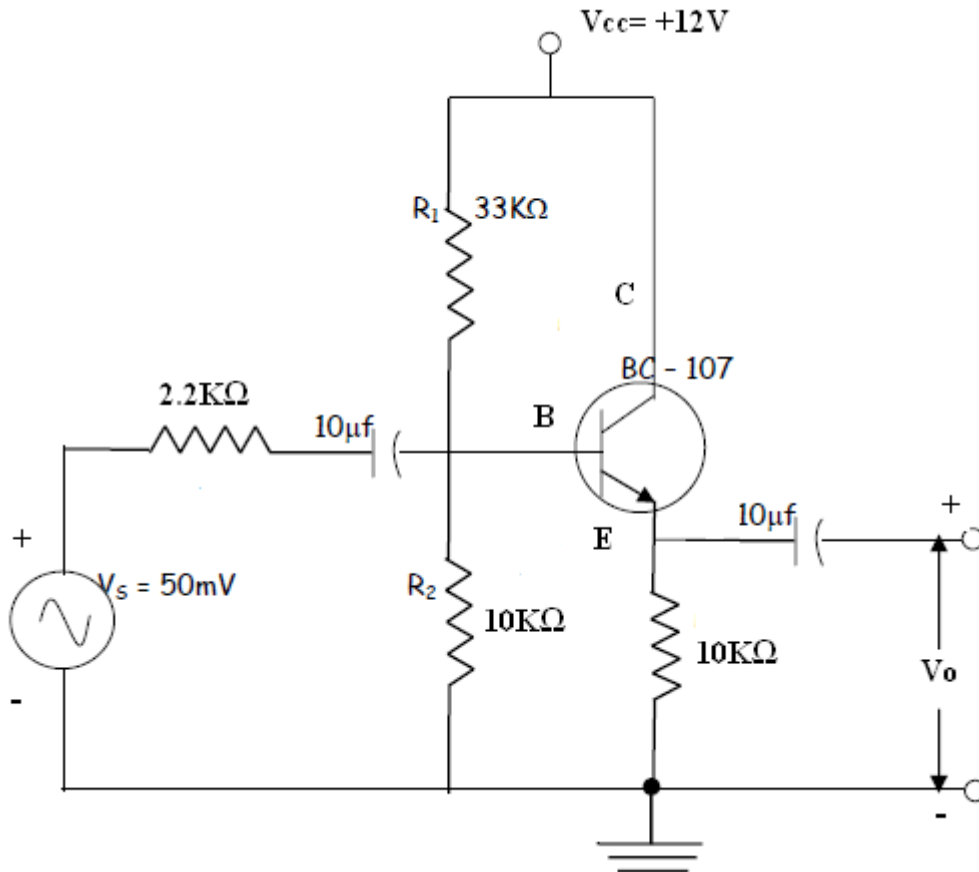
S.No	Name of the Apparatus	Range	Quantity
1	Transistor (BC-107)		1
2	Resistors	2.2K Ω , 10K Ω , 33K Ω	1
3	Capacitors	10 μ F	2
4	Bread Board		1
5	Regulated Power Supply	(0-30)V DC	1
6	Function Generator	(100-1M)Hz	1
7	CRO	(100-20M)Hz	1
7	Connecting Wires	As Required	

THEORY:

In common collector amplifier as the collector resistance is made to zero, the collector is at ac ground that is why the circuit is also called as grounded - collector amplifier or this configuration is having voltage gain close to unity and hence a change in base voltage appears as an equal change across the load at the emitter, hence the name emitter follower. In other words the emitter follows the input signal. This circuit performs the function of impedance transformation over a wide range of frequencies with voltage gain close to unity. In addition to that, the emitter follower increases the output level of the signal. Since the output voltage across the emitter load can never exceed the input voltage to base, as the emitter-base junction would become back biased. Common collector state has a low output resistance, the circuit suitable to serve as buffer or isolating amplifier or couple to a load with large current demands.

Characteristics of CC amplifier:

1. Higher current gain
2. Voltage gain is approximately unity
3. Power gain approximately equal to current gain
4. No current or voltage phase shift
5. Large input resistance
6. Small output resistance

CIRCUIT DIAGRAM:**PROCEDURE:**

1. Connect the circuit as per the circuit diagram.
2. Set Source Voltage $V_s = 50\text{mV}$ (say) at 1 KHz frequency, using function generator.
3. Keeping the input voltage constant, vary the frequency from 50Hz to 1MHz in regular steps and note down the corresponding output voltage.
4. Calculate the Voltage Gain by using the formula

$$A_v = \text{Output voltage } (V_o) / \text{Input voltage } (V_s)$$

5. Calculate the Voltage Gain in dB by using Voltage Gain $A_v(\text{dB}) = 20 \log_{10} (V_o/V_s)$.
6. Plot the Graph by taking Voltage gain (dB) on x-axis and frequency (Hz) on y-axis.
7. The Bandwidth of the amplifier is calculated from the graph using the expression,

$$\text{Bandwidth, } BW = f_2 - f_1$$

Where f_1 is lower 3-dB frequency

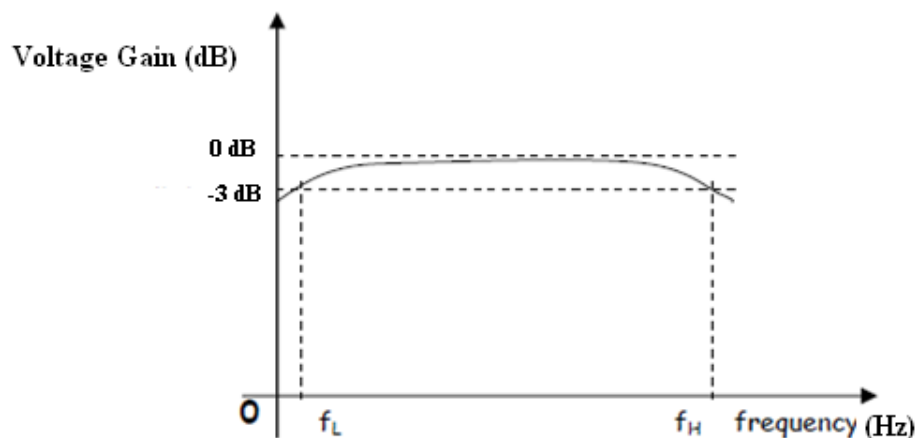
f_2 is upper 3-dB frequency

OBSERVATIONS:

$V_s = \text{_____ V}$

S.No	Input Frequency (Hz)	Output Voltage (V_o) (volts)	Voltage Gain= V_o/V_s	Voltage Gain (dB) = $20 \log_{10} (V_o/V_s)$

FREQUENCY RESPONSE:



PRECAUTIONS:

1. While doing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.
2. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.
3. Make sure while selecting the emitter, base and collector terminals of the transistor.

RESULT: The Voltage gain and Bandwidth of CC amplifier is measured and the frequency response of the CC Amplifier is obtained.

1. The Voltage gain of CC Amplifier is _____.
2. The Bandwidth of CC Amplifier is _____.

VIVA QUESTIONS:

1. Why CC amplifier is known as emitter follower?
2. Mention the applications of CC amplifier. Justify?
3. What is the phase difference between input and output signals in the case of CC amplifier?
4. Mention the characteristics of CC amplifier?
5. What is gain bandwidth product?

11. FET - CS AMPLIFIER

- AIM:** 1. To obtain the frequency response of the Common Source FET Amplifier.
2. To Measure the Voltage gain and Bandwidth of CS Amplifier.

APPARATUS:

S.No	Name of the Apparatus	Range	Quantity
1	JFET (BFW-10)		1
2	Resistors	1K Ω , 3.3K Ω , 100K Ω	1
3	Capacitors	10 μ F	3
4	Bread Board		1
5	Regulated Power Supply	(0-30)V DC	1
6	Function Generator	(100-1M)Hz	1
7	CRO	(100-20M)Hz	1
7	Connecting Wires	As Required	

THEORY:

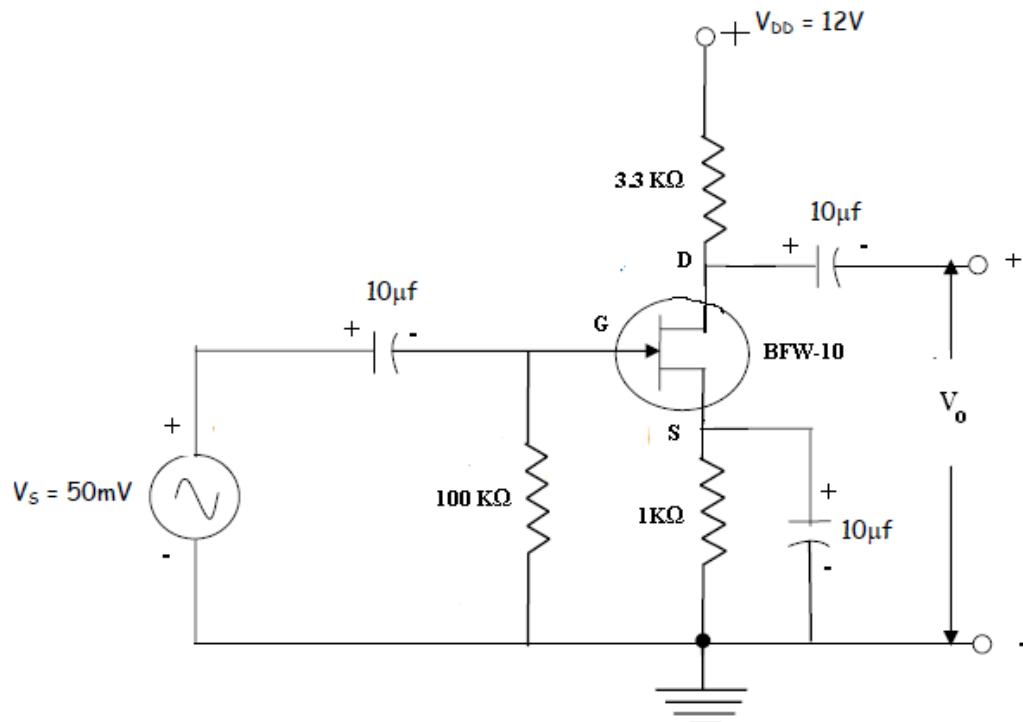
A field-effect transistor (FET) is a type of transistor commonly used for weak-signal amplification (for example, for amplifying wireless (signals)). The device can amplify analog or digital signals. It can also switch DC or function as an oscillator. In the FET, current flows along a semiconductor path called the channel. At one end of the channel, there is an electrode called the source. At the other end of the channel, there is an electrode called the drain. The physical diameter of the channel is fixed, but its effective electrical diameter can be varied by the application of a voltage to a control electrode called the gate. Field-effect transistors exist in two major classifications. These are known as the junction FET (JFET) and the metal-oxide-semiconductor FET (MOSFET). The junction FET has a channel consisting of N-type semiconductor (N-channel) or P-type semiconductor (P-channel) material; the gate is made of the opposite semiconductor type. In P-type material, electric charges are carried mainly in the form of electron deficiencies called holes. In N-type material, the charge carriers are primarily electrons. In a JFET, the junction is the boundary between the channel and the gate. Normally, this P-N junction is reverse-biased (a DC voltage is applied to it) so that no current flows between the channel and the gate. However, under some conditions there is a small current through the junction during part of the input signal cycle.

The FET has some advantages and some disadvantages relative to the bipolar transistor. Field-effect transistors are preferred for weak-signal work, for example in wireless,

communications and broadcast receivers. They are also preferred in circuits and systems requiring high impedance. The FET is not, in general, used for high-power amplification, such as is required in large wireless communications and broadcast transmitters.

Field-effect transistors are fabricated onto silicon integrated circuit (IC) chips. A single IC can contain many thousands of FETs, along with other components such as resistors, capacitors, and diodes.

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Set Source Voltage $V_s = 50\text{mV}$ (say) at 1 KHz frequency, using function generator.
3. Keeping the input voltage constant, vary the frequency from 50Hz to 1MHz in regular steps and note down the corresponding output voltage.
4. Calculate the Voltage Gain by using the formula

$$A_v = \text{Output voltage } (V_o) / \text{Input voltage } (V_s)$$

5. Calculate the Voltage Gain in dB by using Voltage Gain $A_v(\text{dB}) = 20 \log_{10} (V_o/V_s)$.
6. Plot the Graph by taking Voltage gain (dB) on x-axis and frequency (Hz) on y-axis.
7. The Bandwidth of the amplifier is calculated from the graph using the expression,

$$\text{Bandwidth, } BW = f_2 - f_1$$

Where f_1 is lower 3-dB frequency

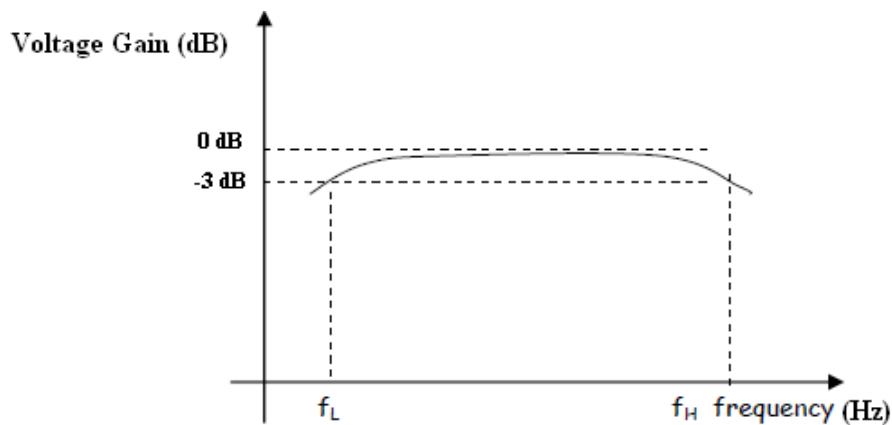
f_2 is upper 3-dB frequency

OBSERVATIONS:

$V_s = \text{_____ V}$

S.No	Input Frequency (Hz)	Output Voltage (V_o) (volts)	Voltage Gain= V_o/V_s	Voltage Gain (dB) = $20 \log_{10} (V_o/V_s)$

FREQUENCY RESPONSE:



PRECAUTIONS:

1. While doing the experiment do not exceed the ratings of the FET. This may lead to damage the FET.
2. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.
3. Make sure while selecting the source, gate and drain terminals of the FET.

RESULT: The Voltage gain and Bandwidth of CS amplifier is measured and the frequency response curve of the CS Amplifier is obtained.

1. The Voltage gain of CS Amplifier is _____.
2. The Bandwidth of CS Amplifier is _____.

VIVA QUESTIONS:

1. What are the advantages of FET amplifier over conventional transistor amplifiers?
2. Why the Voltage gain of a FET is less than a BJT?
3. Why FET is used as a buffer amplifier?
4. Why Input impedance of MOSFET is much higher than a FET?
5. Why A MOSFET can be operated with positive or negative gate voltage?