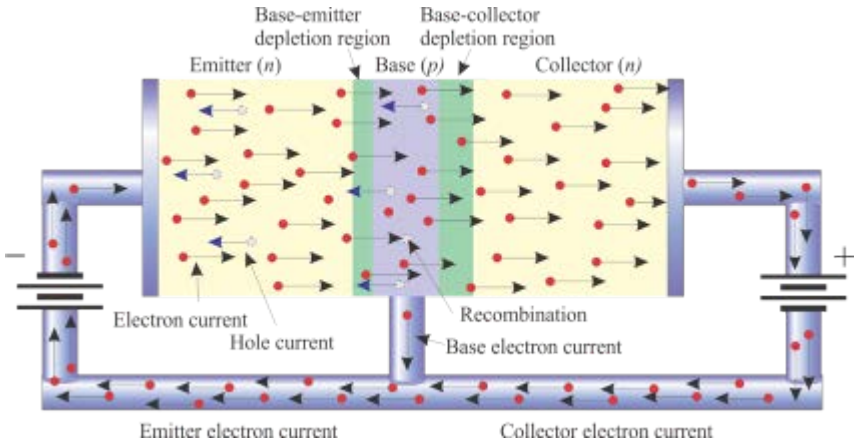
Electronic Devices

Ninth Edition

Floyd

Chapter 8

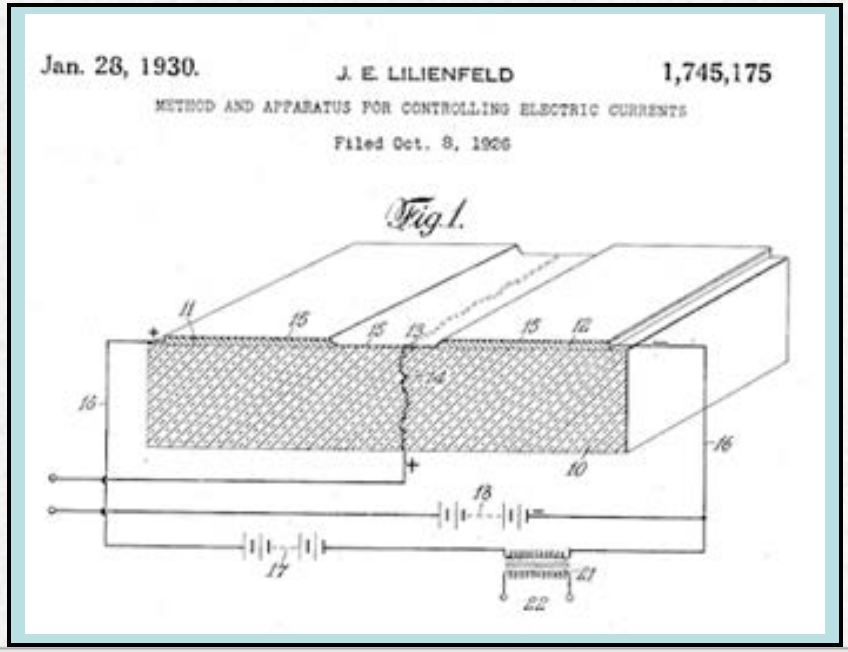


Summary

The FET

The idea for a field-effect transistor (FET) was first proposed by Julius Lilienthal, a physicist and inventor. In 1930 he was granted a U.S. patent for the device.

His ideas were later refined and developed into the FET. Materials were not available at the time to build his device. A practical FET was not constructed until the 1950's. Today FETs are the most widely used components in integrated circuits.


Jan. 28, 1930. J. E. LILIENFELD 1,745,175

METHOD AND APPARATUS FOR CONTROLLING ELECTRIC CURRENTS

Filed Oct. 8, 1926

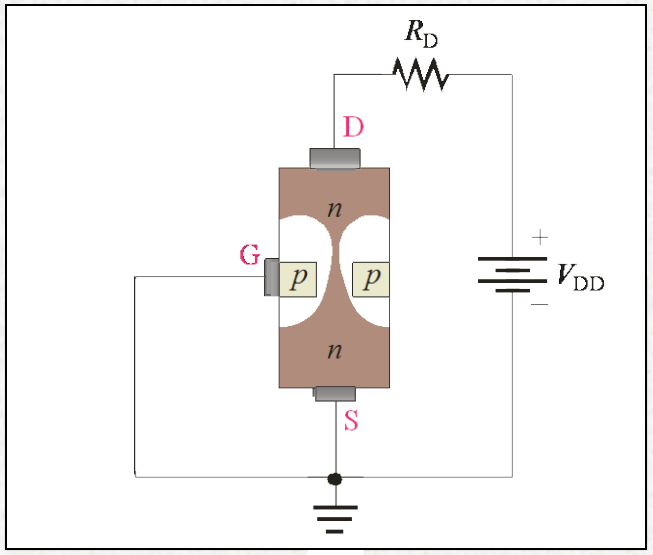
Fig 1.

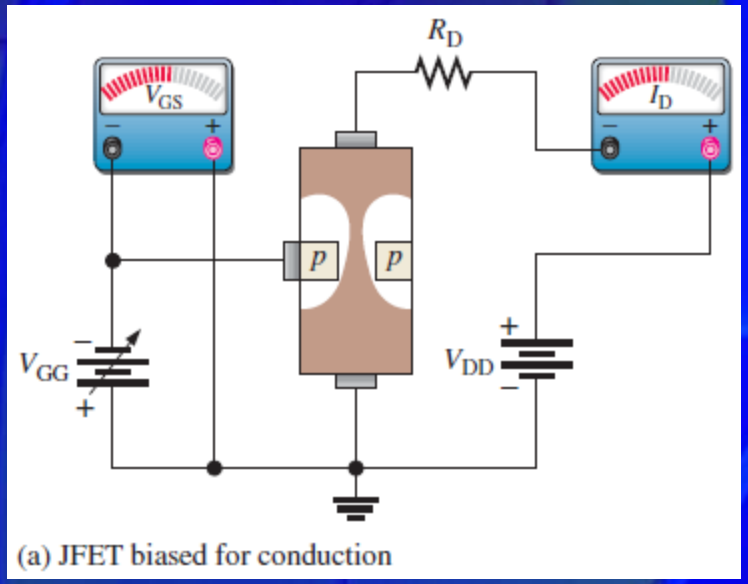
Summary

The JFET

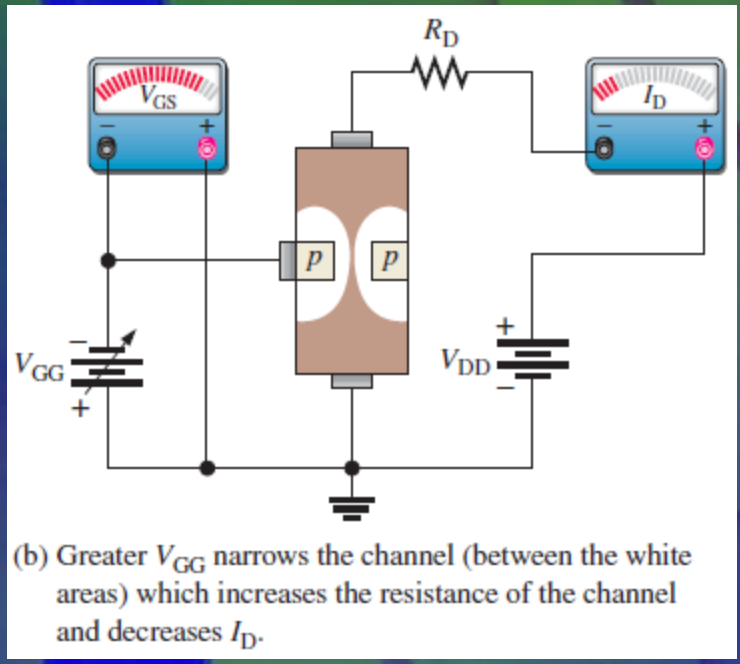
The JFET (or Junction Field Effect Transistor) is a normally ON device. For the *n*-channel device illustrated, when the drain is positive with respect to the source and there is no gate-source voltage, there is current in the channel.

When a negative gate voltage is applied to the FET, the electric field causes the channel to narrow, which in turn causes current to decrease.

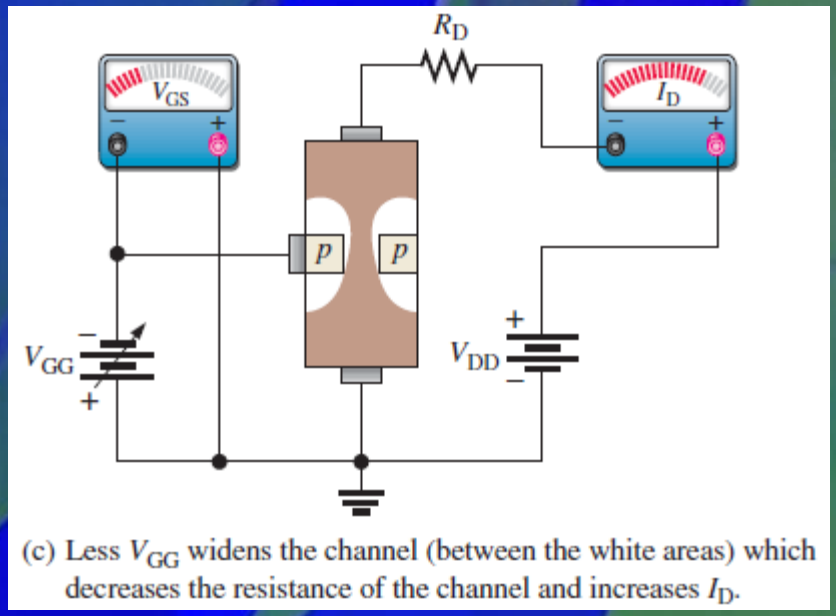




(a) JFET biased for conduction



(b) Greater V_{GG} narrows the channel (between the white areas) which increases the resistance of the channel and decreases I_D.



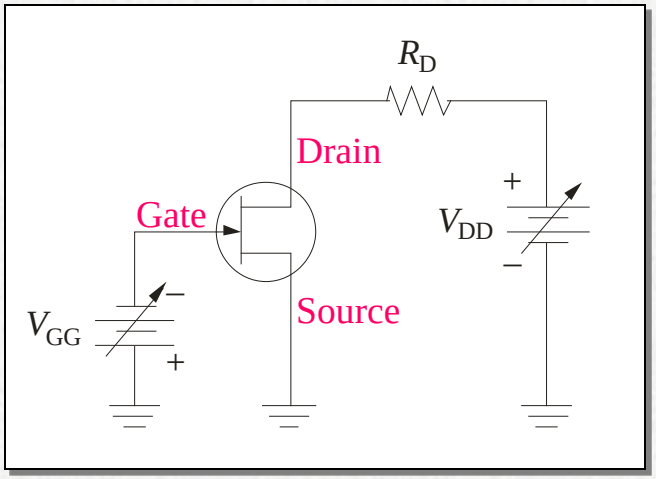
(c) Less V_{GG} widens the channel (between the white areas) which decreases the resistance of the channel and increases I_D.

Summary

The JFET

As in the base of bipolar transistors, there are two types of JFETs: *n*-channel and *p*-channel. The dc voltages are opposite polarities for each type.

The symbol for an *n*-channel JFET is shown, along with the proper polarities of the applied dc voltages. For an *n*-channel device, the gate is always operated with a negative (or zero) voltage with respect to the source.



Summary

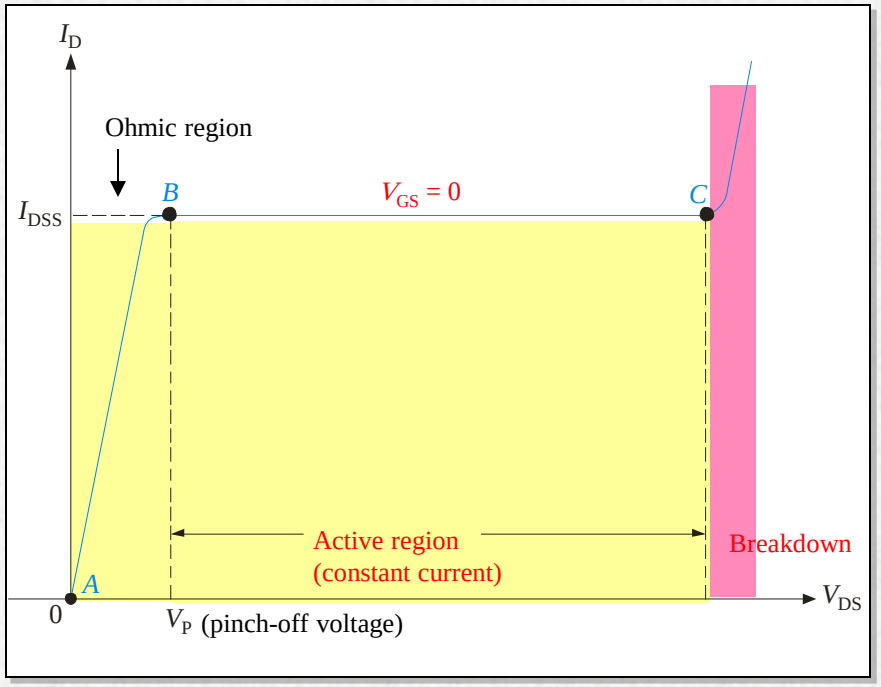
The JFET

There are three regions in the characteristic curve for a JFET as illustrated for the case when $V_{GS} = 0$ V.

Between *A* and *B* is the **Ohmic region**, where current and voltage are related by Ohm's law.

From *B* to *C* is the **active** (or *constant-current*) **region** where current is essentially independent of V_{DS}.

Beyond *C* is the **breakdown region**. Operation here can damage the FET.

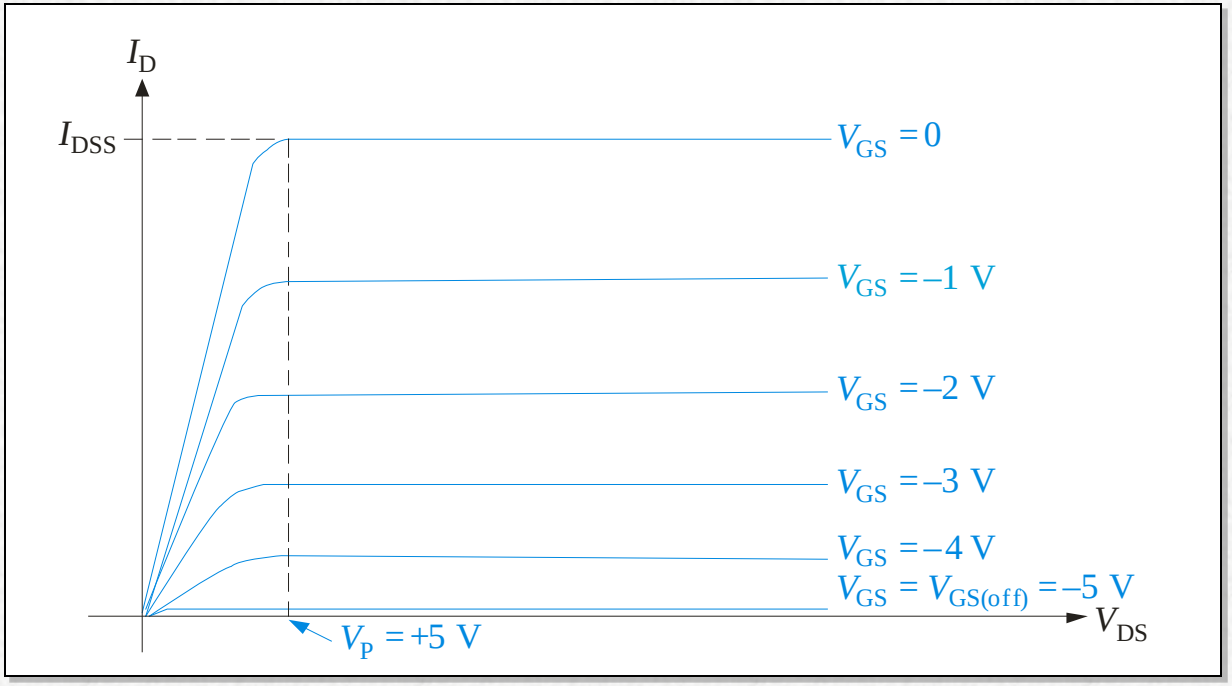


Summary

The JFET

When V_{GS} is set to different values, the relationship between V_{DS} and I_D develops a family of characteristic curves for the device.

An *n*-channel characteristic is illustrated here. Notice that V_p is positive and has the same magnitude as $V_{GS(off)}$.



Summary

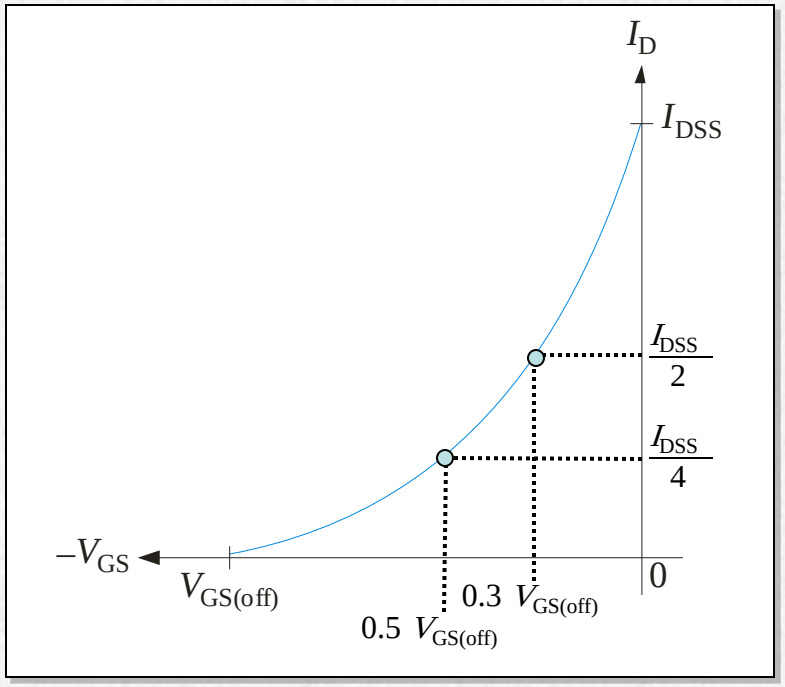
The JFET

A plot of V_{GS} to I_D is called the transfer or transconductance curve. The transfer curve is a is a plot of the output current (I_D) to the input voltage (V_{GS}).

The transfer curve is based on the equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

By substitution, you can find other points on the curve for plotting the universal curve.



Summary

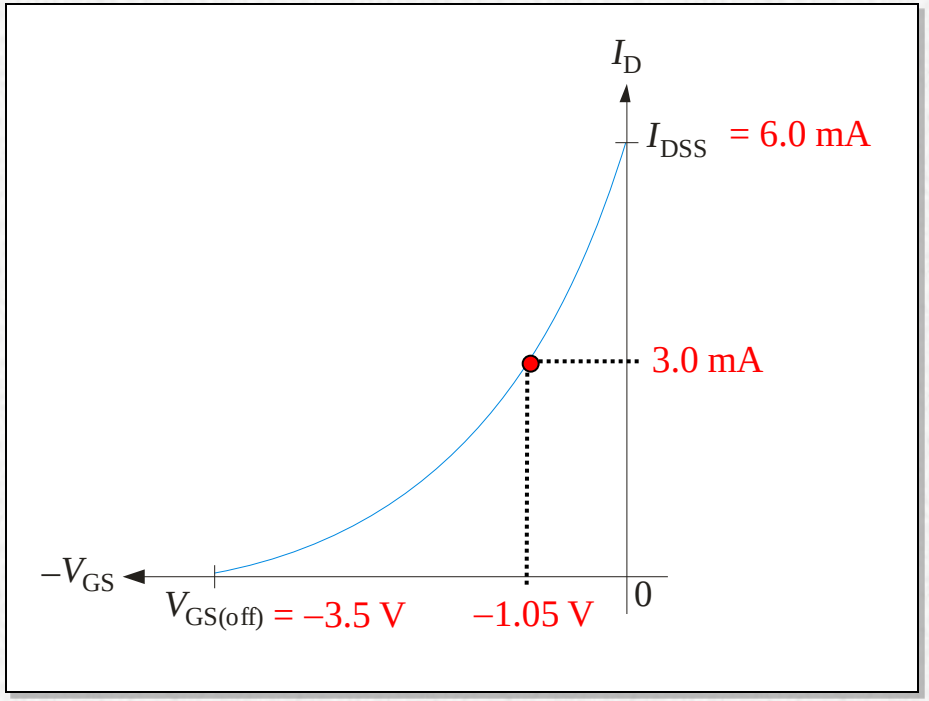
The JFET

Example:

A certain 2N5458 JFET has $I_{DSS} = 6.0$ mA and $V_{GS(off)} = -3.5$ V.

(a) Show the values of the these end points on the transfer curve.

(b) Show the point for the case when $I_D = 3.0$ mA.



Solution:

(b) When $I_D = \frac{1}{2} I_{DSS}$,
$V_{GS} = 0.3\ V_{GS(off)}$.
Therefore, $V_{GS} = -1.05$ V

Summary

The JFET

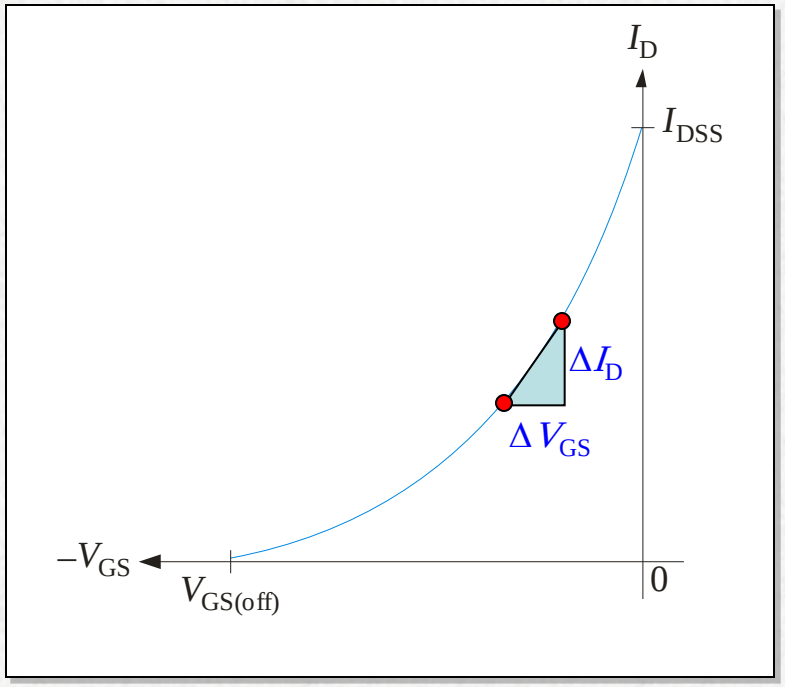
The transconductance is the ratio of a change in output current (ΔI_D) to a change in the input voltage (ΔV_{GS}).

This definition is $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}}$

The following approximate formula is useful for calculating gm if you know g_{m0}.

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$

The value of g_{m0} can be found from $g_{m0} = \dfrac{2I_{DSS}}{|V_{GS(off)}|}$



Summary

The JFET

Because the slope changes at every point along the curve, the transconductance is not constant, but depends on where it is measured.

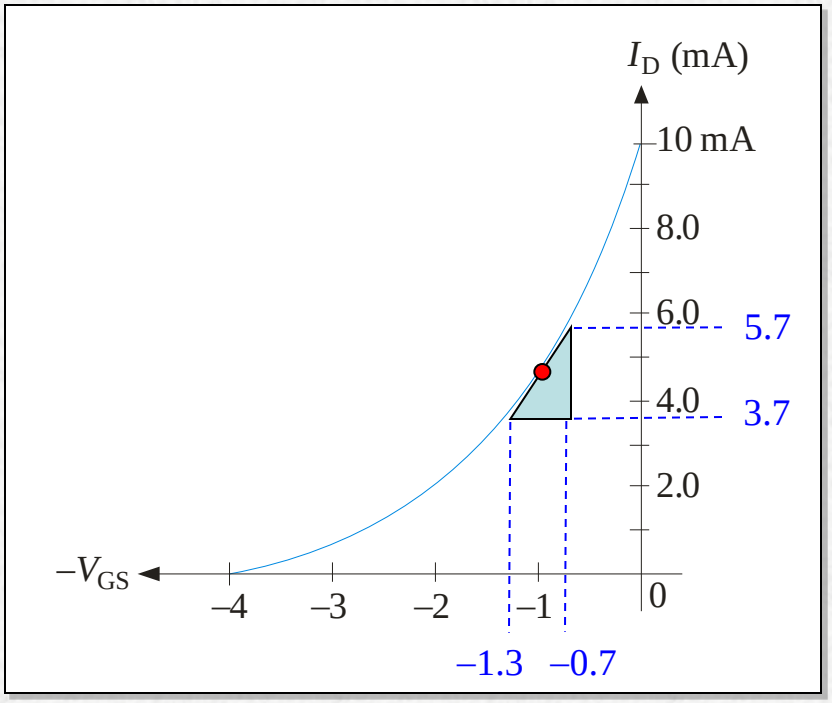
Example:

What is the transconductance for the JFET at the point shown?

Solution:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{5.7\text{ mA} - 3.7\text{ mA}}{-0.7\text{ V} - (-1.3\text{ V})}$$

$$= \frac{2.0\text{ mA}}{0.6\text{ V}} = 3.33\text{ mS}$$



Electrical Characteristics

$T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	$I_G = 10\ \mu A$, $V_{DS} = 0$		- 25			V
I_{GSS}	Gate Reverse Current	$V_{GS} = -15$ V, $V_{DS} = 0$				- 1.0	nA
		$V_{GS} = -15$ V, $V_{DS} = 0$, $T_A = 100°C$				- 200	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15$ V, $I_D = 10$ nA	5457	- 0.5		- 6.0	V
			5458	- 1.0		- 7.0	V
			5459	- 2.0		- 8.0	V
V_{GS}	Gate-Source Voltage	$V_{DS} = 15$ V, $I_D = 100\ \mu A$	5457		- 2.5		V
		$V_{DS} = 15$ V, $I_D = 200\ \mu A$	5458		- 3.5		V
		$V_{DS} = 15$ V, $I_D = 400\ \mu A$	5459		- 4.5		V
ON CHARACTERISTICS							
I_{DSS}	Zero-Gate Voltage Drain Current*	$V_{DS} = 15$ V, $V_{GS} = 0$	5457	1.0	3.0	5.0	mA
			5458	2.0	6.0	9.0	mA
			5459	4.0	9.0	16	mA
SMALL SIGNAL CHARACTERISTICS							
g_{fs}	Forward Transfer Conductance*	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 kHz					
			5457	1000		5000	µmhos
			5458	1500		5500	µmhos
			5459	2000		6000	µmhos
g_{os}	Output Conductance*	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 kHz			10	50	µmhos
C_{iss}	Input Capacitance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 MHz			4.5	7.0	pF
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 MHz			1.5	3.0	pF
NF	Noise Figure	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 kHz, $R_G = 1.0$ megohm, BW = 1.0 Hz				3.0	dB

*Pulse Test: Pulse Width ≤ 300 ms, Duty Cycle ≤ 2%

Summary

JFET Input Resistance

The input resistance of a JFET is given by: $R_{IN} = \left| \frac{V_{GS}}{I_{GSS}} \right|$

where I_{GSS} is the current into the reverse biased gate.

JFETs have very high input resistance, but it drops when the temperature increases.

Example:

Compare the input resistance of a 2N5485 at 25 °C and at 100 °C. The specification sheet shows that for $V_{GS} = -20$ V, $I_{GSS} - 1$ nA at 25 °C and 0.2 μA at 100 °C.

Solution:

At 25 °C, $R_{IN} = \left| \frac{V_{GS}}{I_{GSS}} \right| = \left| \frac{20 \text{ V}}{1 \text{ nA}} \right| = 20 \text{ G}\Omega!$

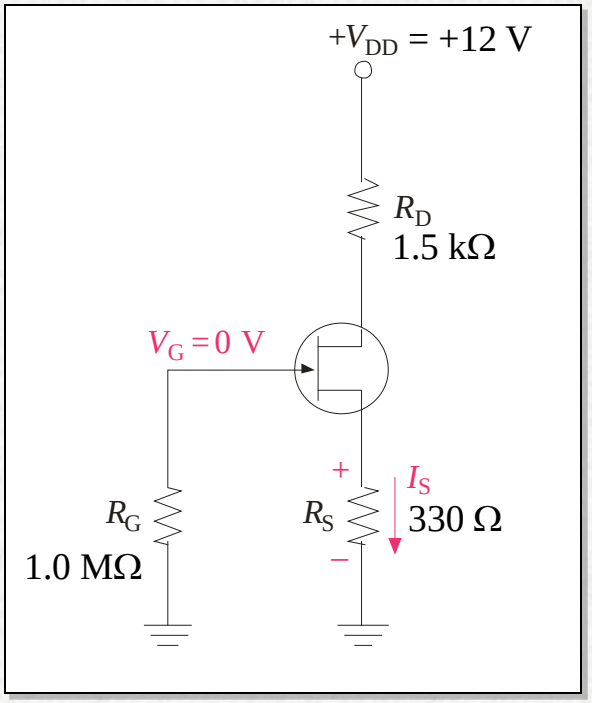
At 100 °C, $R_{IN} = \left| \frac{V_{GS}}{I_{GSS}} \right| = \left| \frac{20 \text{ V}}{0.2 \text{ μA}} \right| = 100 \text{ M}\Omega$

Summary

JFET Biasing

Self-bias is simple and effective, so it is the most common biasing method for JFETs. With self bias, the gate is essentially at 0 V.

An *n*-channel JFET is illustrated. The current in R_S develops the necessary reverse bias that forces the gate to be less than the source.



Example:

Assume the resistors are as shown and the drain current is 3.0 mA. What is V_{GS}?

Solution:

$V_G = 0$ V; $V_S = (3.0 \text{ mA})(330\ \Omega) = 0.99$ V

$V_{GS} = 0 - 0.99 \text{ V} = -0.99$ V

Summary

JFET Biasing

You can use the transfer curve to obtain a reasonable value for the source resistor in a self-biased circuit.

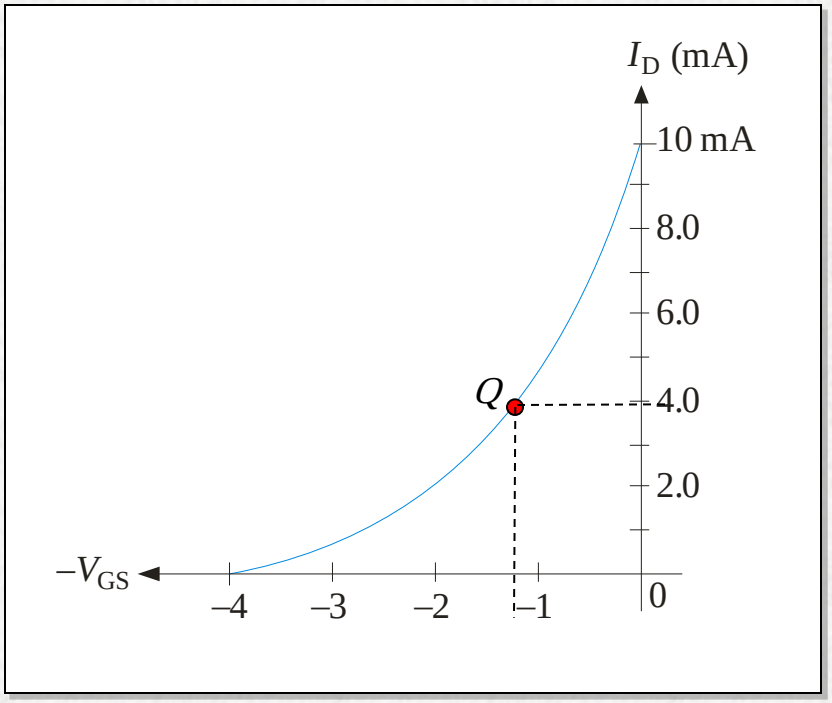
Example:

What value of R_S should you use to set the Q point as shown?

Solution:

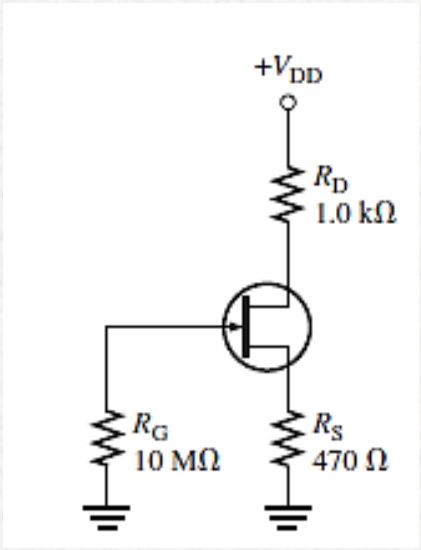
The Q point is approximately at $I_D = 4.0$ mA and $V_{GS} = -1.25$ V.

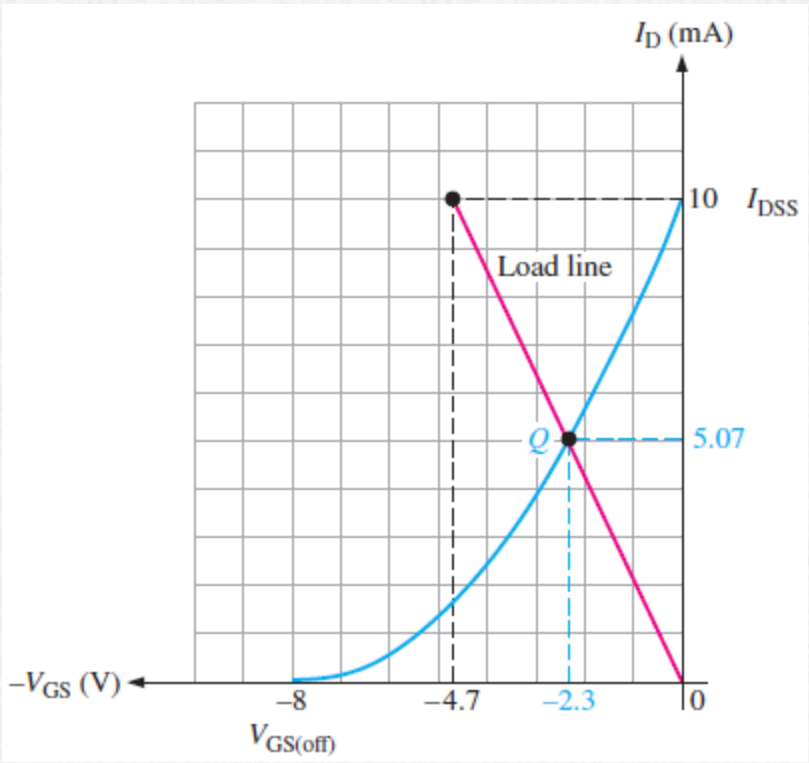
$$R_S = \left|\frac{V_{GS}}{I_D}\right| = \frac{1.25\text{ V}}{3.0\text{ mA}} = 375\ \Omega$$



Summary

Graphical Analysis of a Self-Biased JFET





First, calculate V_{GS} when I_D is zero.

$$V_{GS} = -I_D R_S = (0)(470\ \Omega) = 0\ \text{V}$$

Next, calculate V_{GS} when $I_D = I_{DSS}$.

$$V_{GS} = -I_D R_S = -(10\ \text{mA})(470\ \Omega) = -4.7\ \text{V}$$

Q-point of the circuit as shown, where $I_D = 5.07$ mA and $V_{GS} = -2.3$ V.

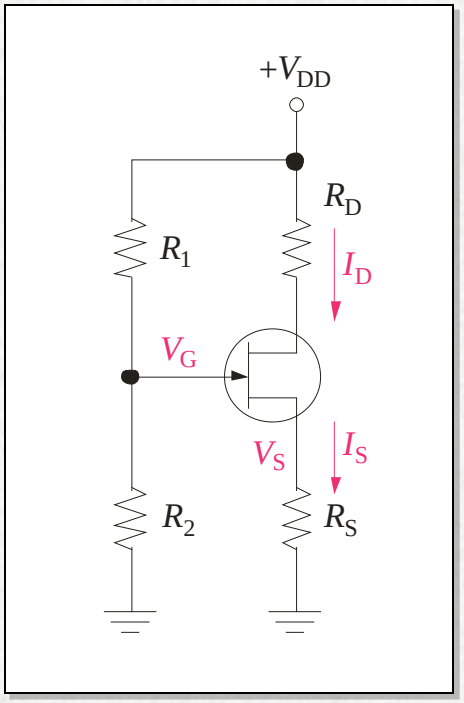
Summary

JFET Biasing

Voltage-divider biasing is a combination of a voltage-divider and a source resistor to keep the source more positive than the gate.

V_G is set by the voltage-divider and is independent of V_S. V_S must be larger than V_G in order to maintain the gate at a negative voltage with respect to the source.

Voltage-divider bias helps stabilize the bias for variations between transistors.



Summary

JFET Biasing

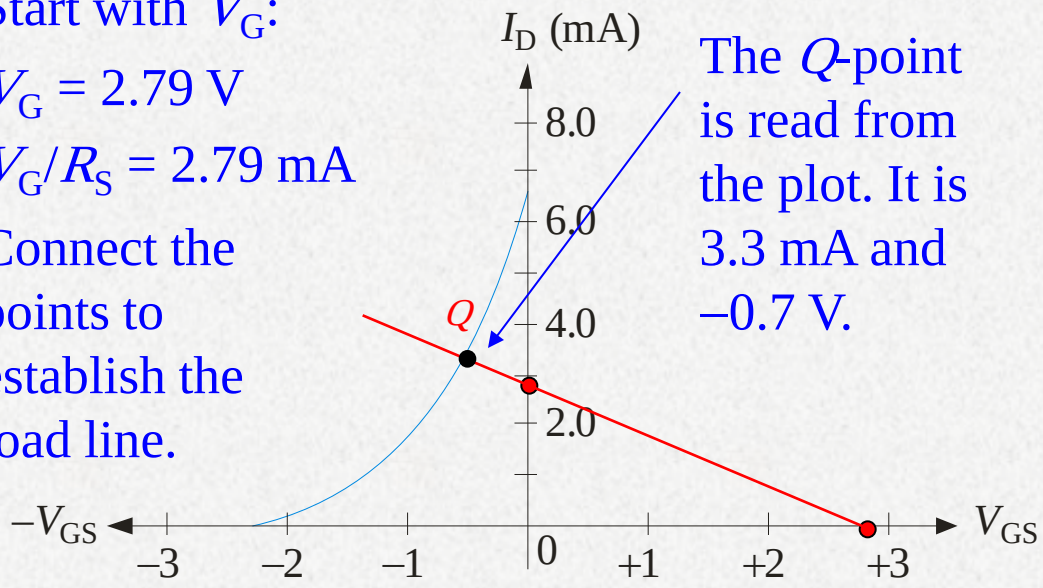
A graphical analysis of voltage-divider biasing is illustrated. A typical transconductance curve for the 2N5485 is shown with I_{DSS} = 6.5 mA and $V_{GS(off)}$ = –2.2 V.

Start with V_G:

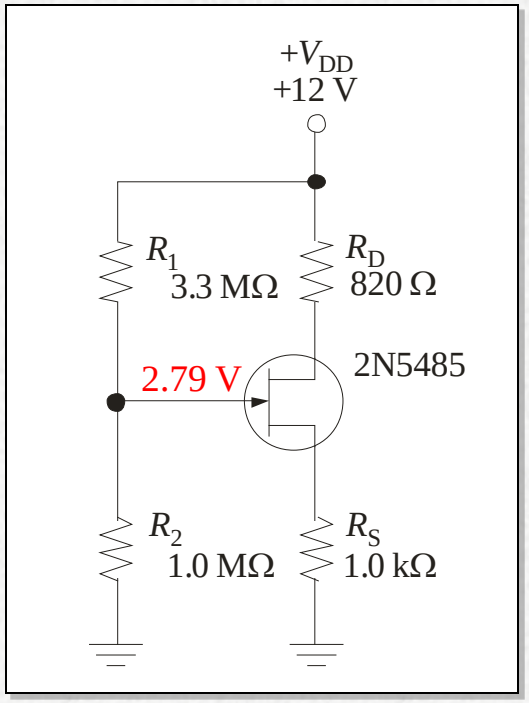
V_G = 2.79 V

V_G/R_S = 2.79 mA

Connect the points to establish the load line.

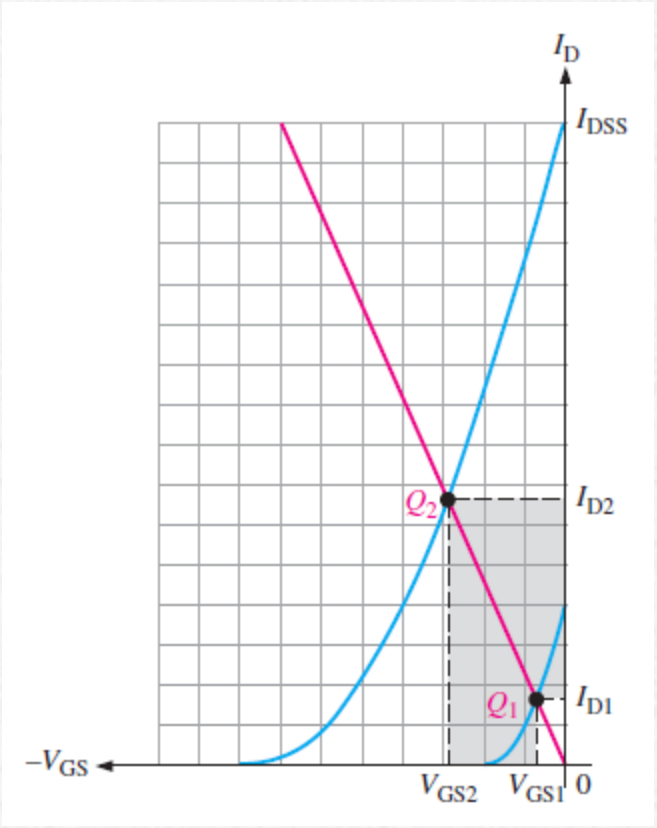


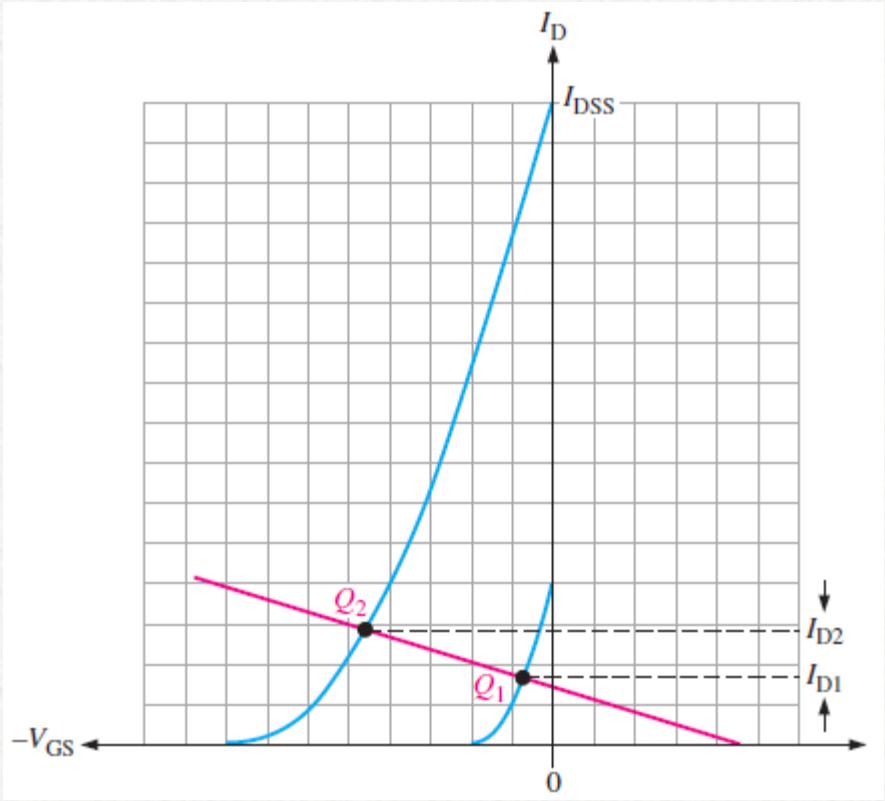
The *Q*-point is read from the plot. It is 3.3 mA and –0.7 V.



Summary

Q-Point Stability





Summary

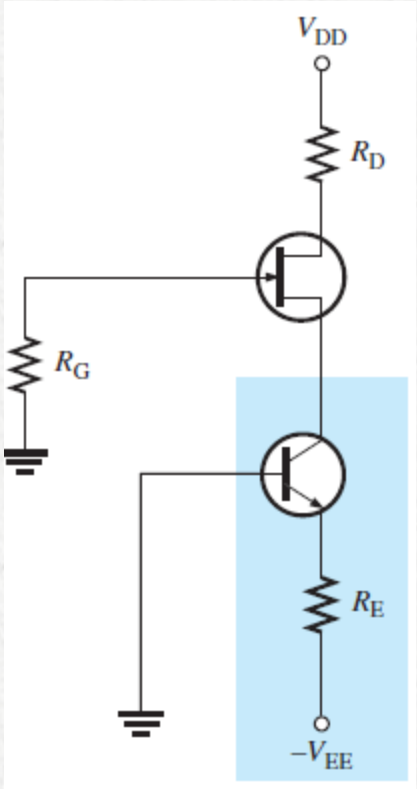
Current-Source Bias

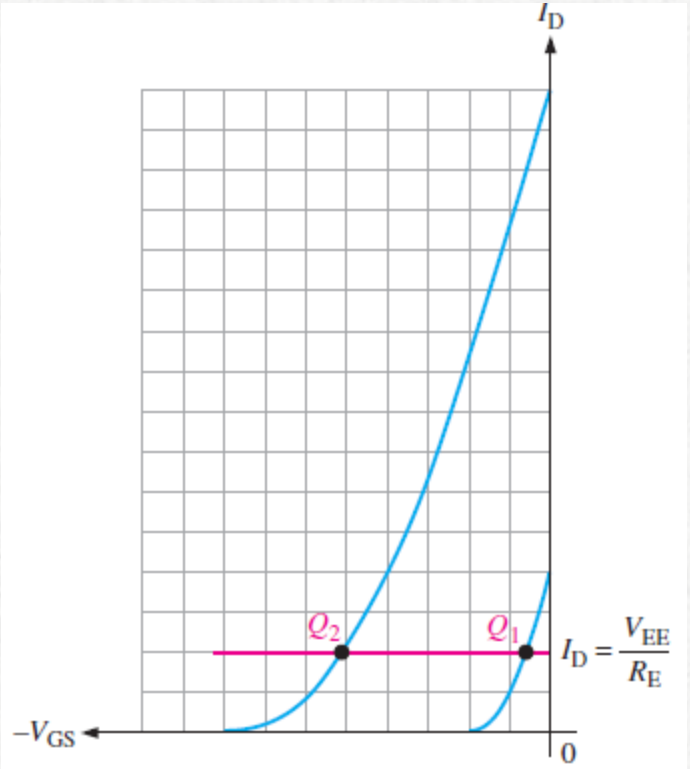
if $V_{EE} \gg V_{BE}$

$$I_E = \frac{V_{EE} - V_{BE}}{R_E} \cong \frac{V_{EE}}{R_E}$$

Since $I_E \cong I_D$

$$I_D \cong \frac{V_{EE}}{R_E}$$



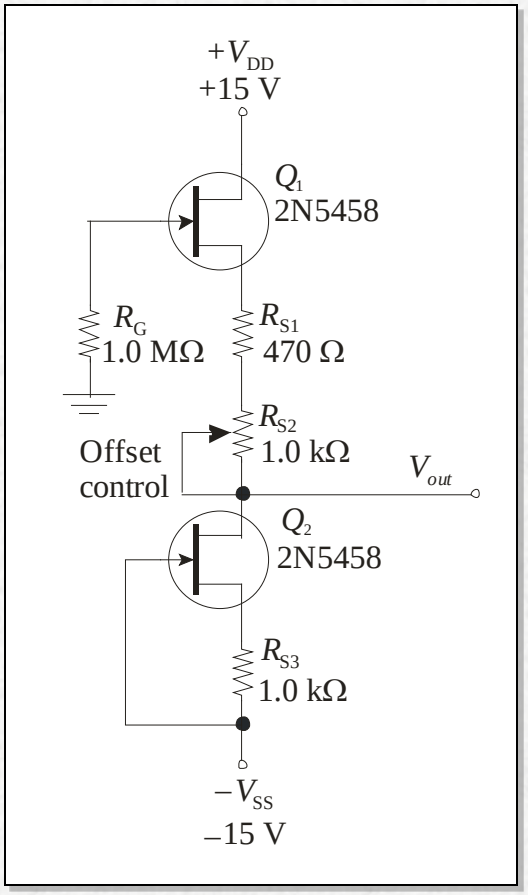


Summary

JFET Biasing

An even more stable form of bias is current-source bias. The current-source can be either a BJT or another FET. With current-source biasing, the drain current is essentially independent of V_{GS}.

In this circuit Q_2 serves as a current source for Q_1. An advantage to this particular circuit is that the output can be adjusted (using R_{S2}) for 0 V DC.

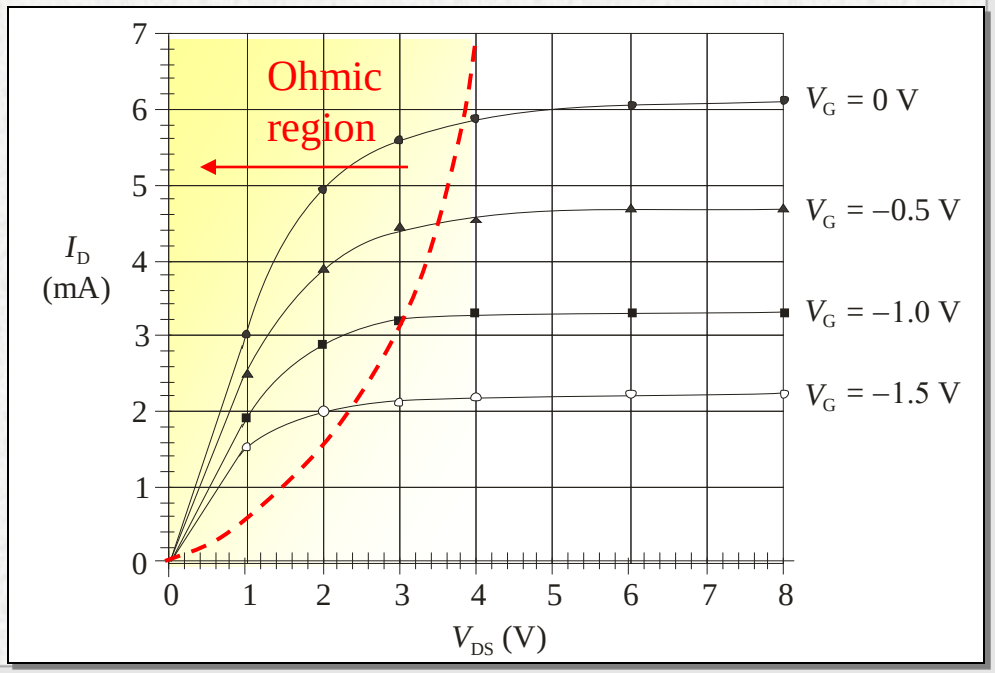


Summary

JFET Ohmic Region

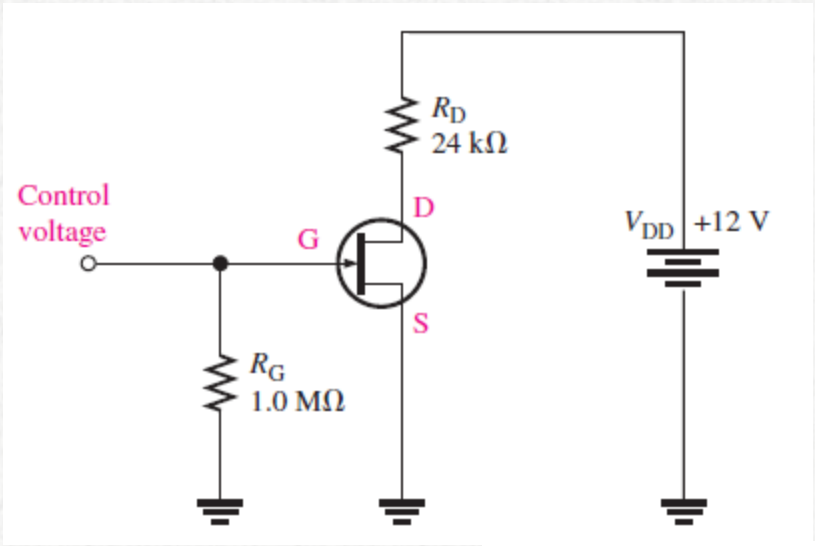
As described before, the ohmic region is between the origin and the active region. A JFET operated in this region can act as a variable resistor.

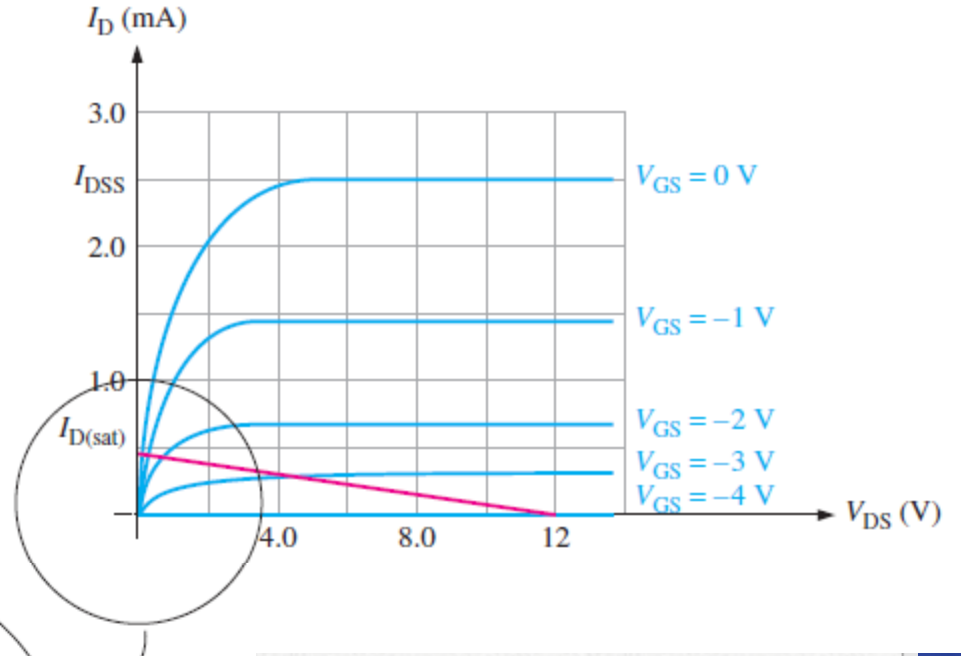
Data from an actual FET is shown. The slopes (which represent conductance) of successive V_{GS} lines are different in the ohmic region. This difference is exploited for use as a voltage controlled resistance.

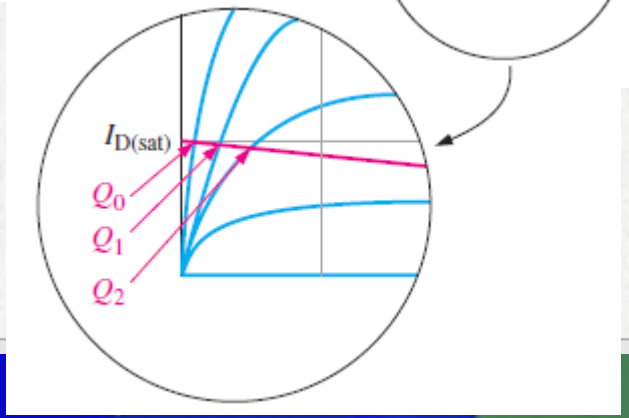


Summary

JFET Ohmic Region



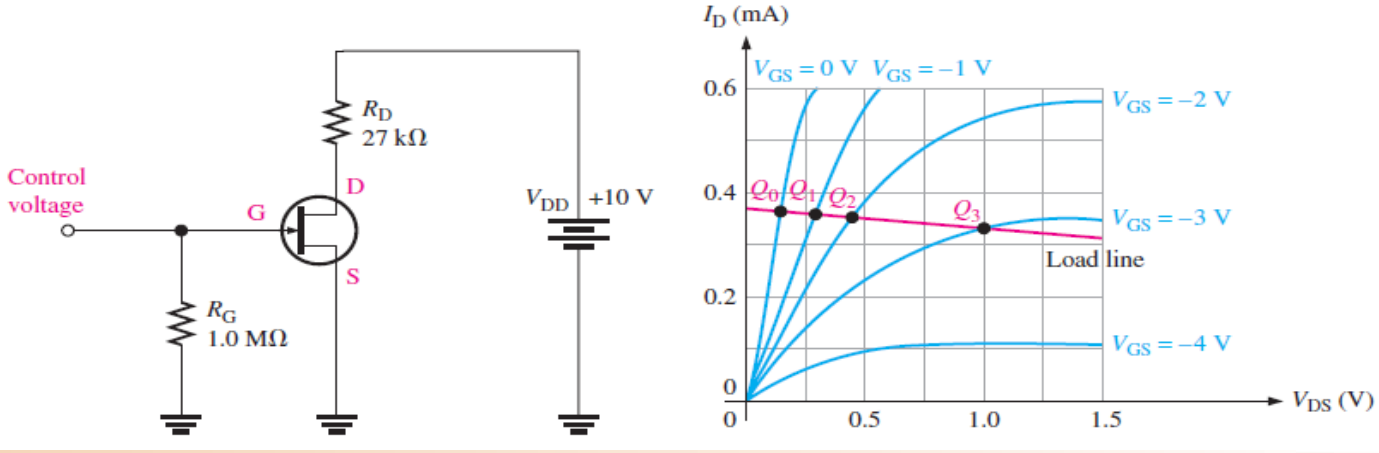




$$I_{D(sat)} = \frac{V_{DD}}{R_D}$$

EXAMPLE 8–14

An *n*-channel JFET is biased in the ohmic region as shown in Figure 8–32. The graph shows an expanded section of the load line in the ohmic region. As V_{GS} is



varied from 0 V to −3 V as indicated, assume that the graph shows the following Q-point values:

Q_0: $I_D = 0.360$ mA, $V_{DS} = 0.13$ V
Q_1: $I_D = 0.355$ mA, $V_{DS} = 0.27$ V
Q_2: $I_D = 0.350$ mA, $V_{DS} = 0.42$ V
Q_3: $I_D = 0.33$ mA, $V_{DS} = 0.97$ V

Determine the range of R_{DS} as V_{GS} is varied from 0 V to −3 V.

Solution

$$Q_0: R_{DS} = \frac{V_{DS}}{I_D} = \frac{0.13\text{ V}}{0.360\text{ mA}} = 361\ \Omega$$

$$Q_1: R_{DS} = \frac{V_{DS}}{I_D} = \frac{0.27\text{ V}}{0.355\text{ mA}} = 760\ \Omega$$

$$Q_2: R_{DS} = \frac{V_{DS}}{I_D} = \frac{0.42\text{ V}}{0.27\text{ mA}} = 1.2\text{ k}\Omega$$

$$Q_3: R_{DS} = \frac{V_{DS}}{I_D} = \frac{0.6\text{ V}}{0.26\text{ mA}} = 2.9\text{ k}\Omega$$

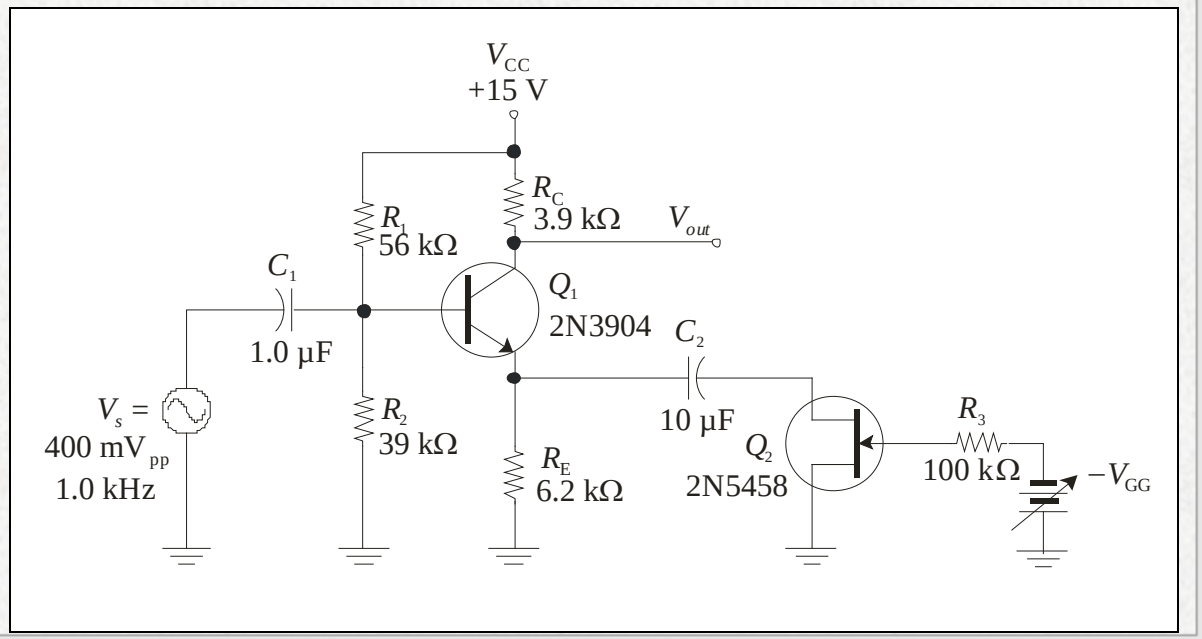
When V_{GS} is varied from 0 V to −3 V, **R_{DS} changes from 361 Ω to 2.9 kΩ.**

Summary

JFET Ohmic Region

Here is a circuit in which the JFET is used as a variable resistor. Notice that that the drain is connected through a capacitor, which means the JFET's *Q*-point is at the origin.

The gain of the BJT depends on the dc voltage setting of V_{GG}.

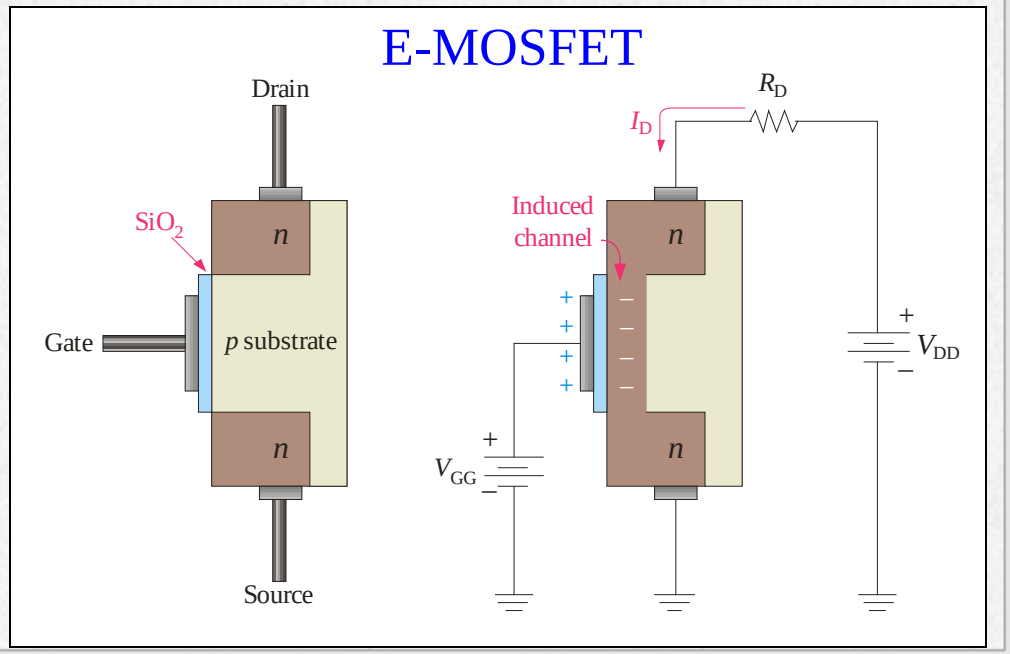


Summary

The MOSFET

The metal oxide semiconductor FET uses an insulated gate to isolate the gate from the channel. Two types are the enhancement mode (E-MOSFET) and the depletion mode (D-MOSFET).

An E-MOSFET has no channel until it is induced by a voltage applied to the gate, so it operates only in enhancement mode. An *n*-channel type is illustrated here; a positive gate voltage induces the channel.



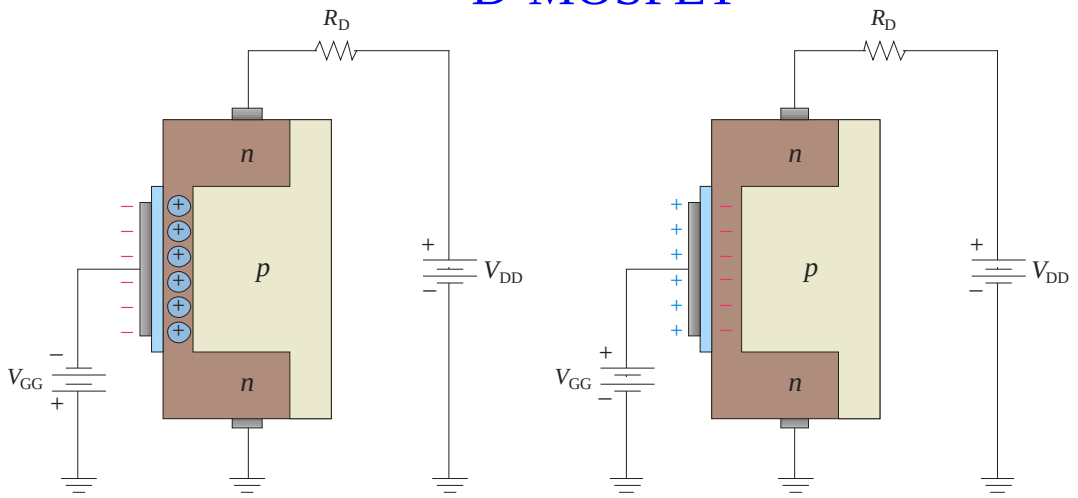
Summary

The MOSFET

The D-MOSFET has a channel that can is controlled by the gate voltage. For an *n*-channel type, a negative voltage depletes the channel; and a positive voltage enhances the channel.

A D-MOSFET can operate in either mode, depending on the gate voltage.

D-MOSFET



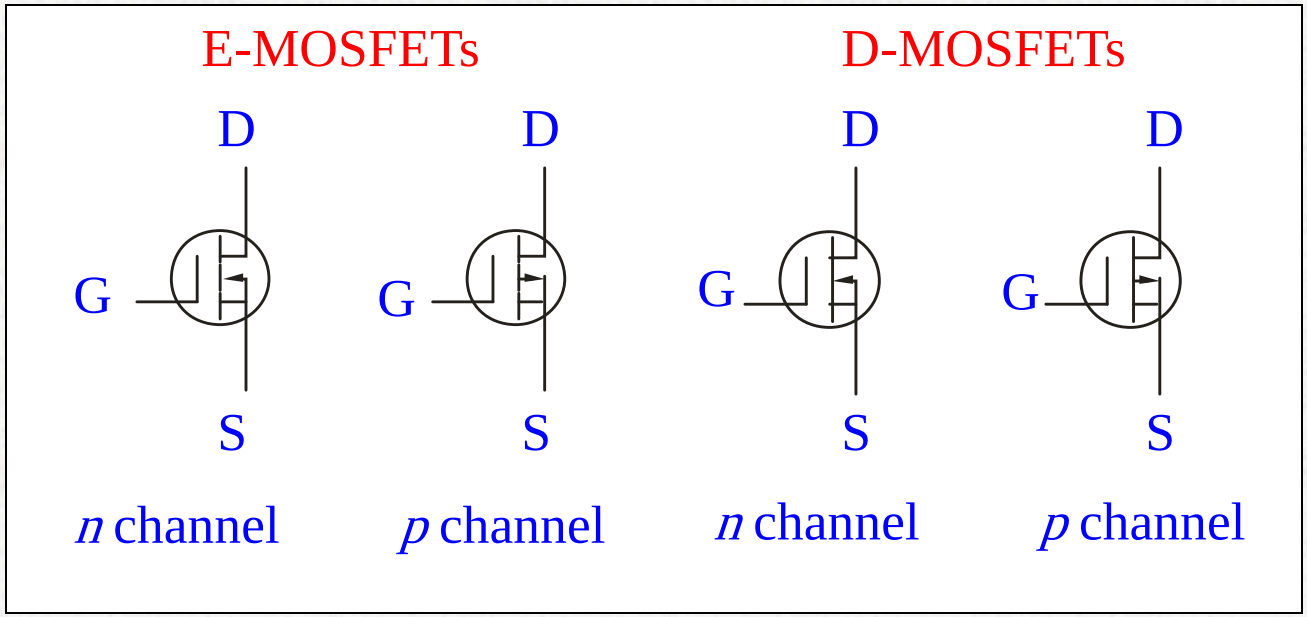
operating in D-mode

operating in E-mode

Summary

The MOSFET

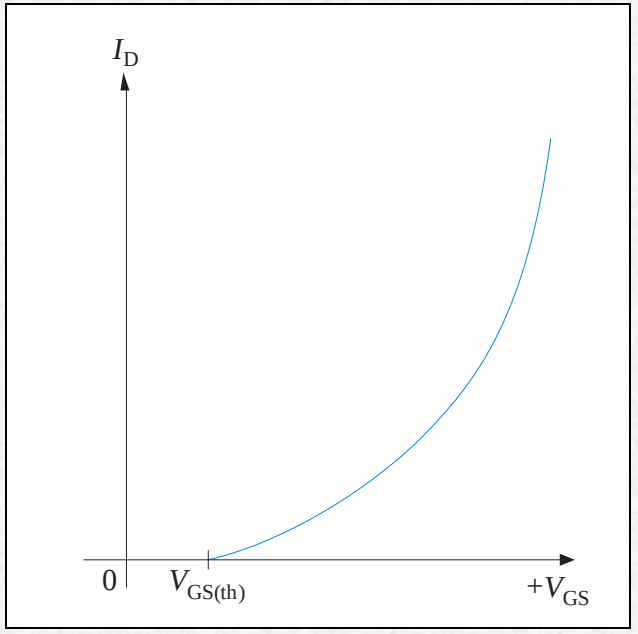
MOSFET symbols are shown. Notice the broken line representing the E-MOSFET that has an induced channel. The *n* channel has an inward pointing arrow.



Summary

The MOSFET

The transfer curve for a MOSFET is has the same parabolic shape as the JFET but the position is shifted along the *x*-axis. The transfer curve for an *n*-channel E-MOSFET is entirely in the first quadrant as shown.



The curve starts at $V_{GS(th)}$, which is a nonzero voltage that is required to have channel conduction. The equation for the drain current is

$$I_D = K\left(V_{GS} - V_{GS(th)}\right)^2$$

EXAMPLE 8–16

The datasheet (see www.fairchild.com) for a 2N7002 E-MOSFET gives $I_{D(on)} = 500$ mA (minimum) at $V_{GS} = 10$ V and $V_{GS(th)} = 1$ V. Determine the drain current for $V_{GS} = 5$ V.

Solution First, solve for K using Equation 8–4.

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{500\text{ mA}}{(10\text{ V} - 1\text{ V})^2} = \frac{500\text{ mA}}{81\text{ V}^2} = 6.17\text{ mA/V}^2$$

Next, using the value of K, calculate I_D for $V_{GS} = 5$ V.

$$I_D = K(V_{GS} - V_{GS(th)})^2 = (6.17\text{ mA/V}^2)(5\text{ V} - 1\text{ V})^2 = \mathbf{98.7\text{ mA}}$$

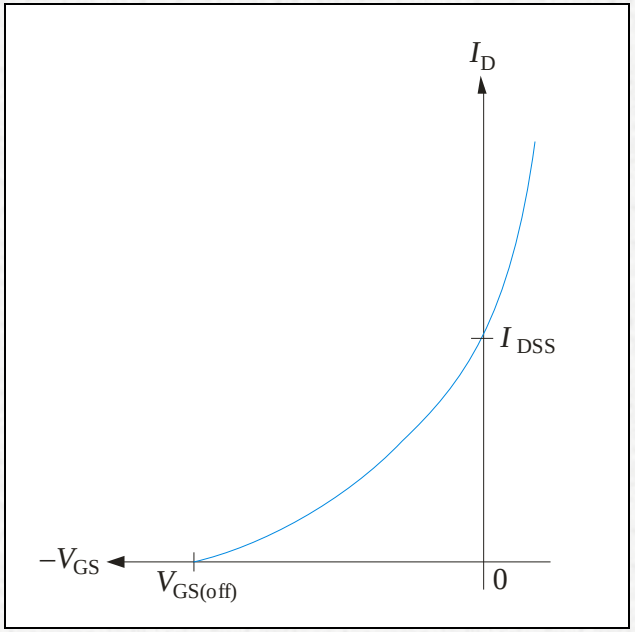
Summary

The MOSFET

Recall that the D-MOSFET can be operated in either mode. For the *n*-channel device illustrated, operation to the left of the *y*-axis means it is in depletion mode; operation to the right means is in enhancement mode.

As with the JFET, I_D is zero at $V_{GS(off)}$. When VGS is 0, the drain current is IDSS, which for this device is *not* the maximum current. The equation for drain current is

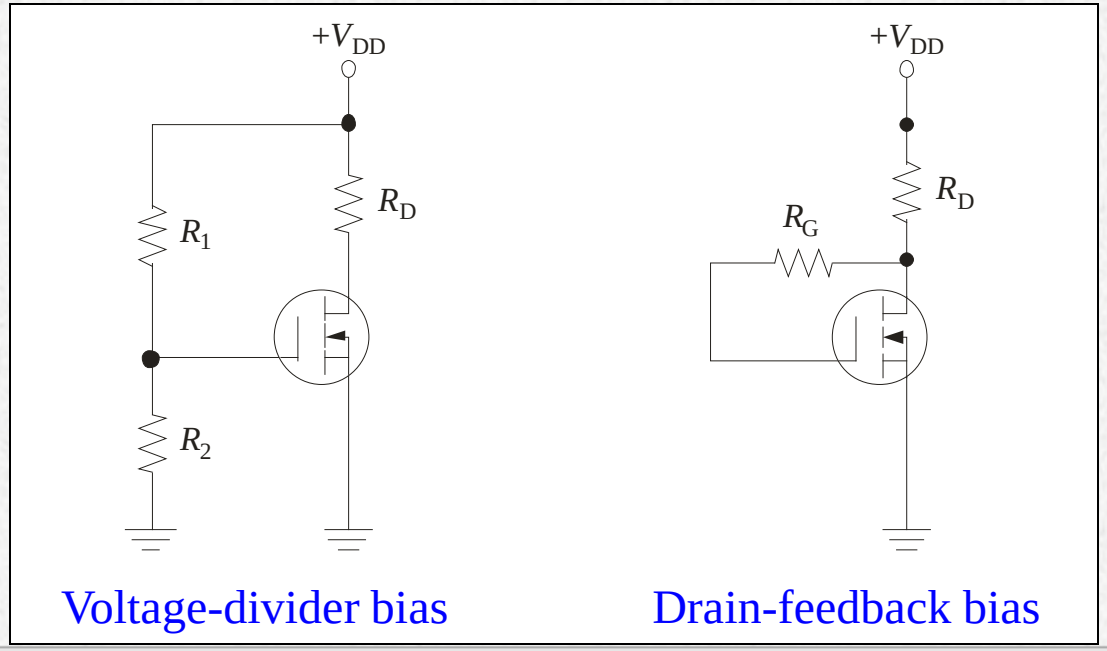
$$I_D \cong I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2$$



Summary

MOSFET Biasing

E-MOSFETs can be biased using bias methods like the BJT methods studied earlier. Voltage-divider bias and drain-feedback bias are illustrated for *n*-channel devices.



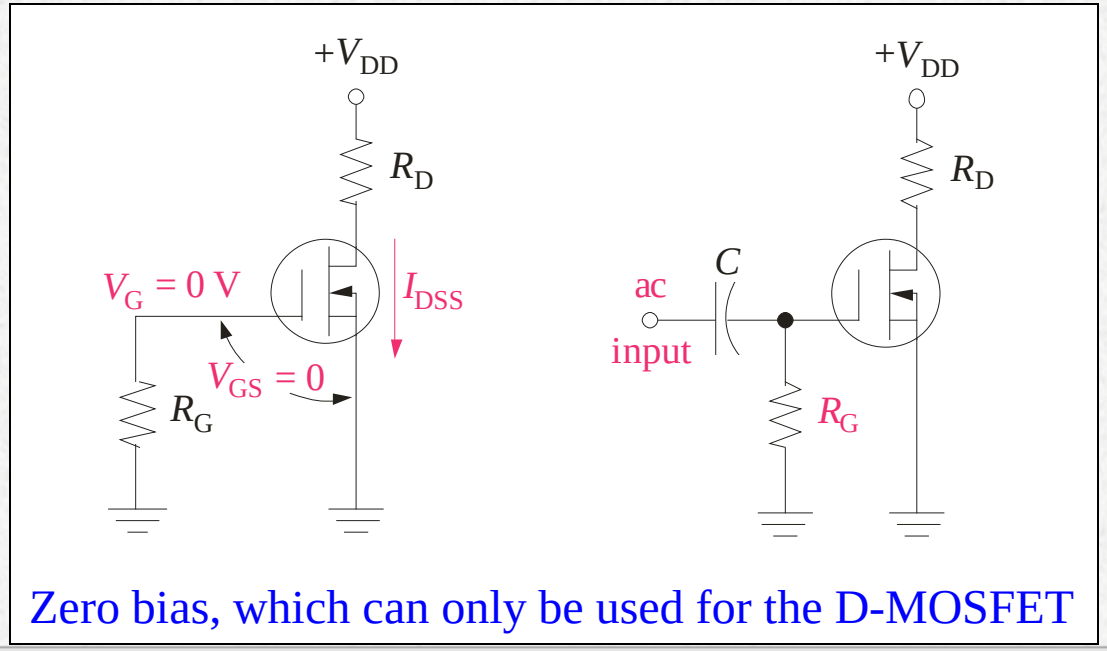
Voltage-divider bias

Drain-feedback bias

Summary

MOSFET Biasing

The simplest way to bias a D-MOSFET is with zero bias. This works because the device can operate in either depletion or enhancement mode, so the gate can go above or below 0 V.

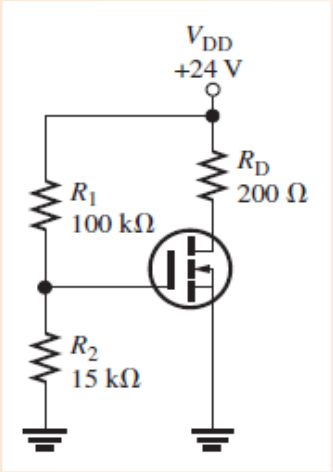


Zero bias, which can only be used for the D-MOSFET

EXAMPLE 8–18

Determine V_{GS} and V_{DS} for the E-MOSFET circuit in Figure 8–47. Assume this particular MOSFET has minimum values of $I_{D(on)} = 200\ \text{mA}$ at $V_{GS} = 4\ \text{V}$ and $V_{GS(th)} = 2\ \text{V}$.

▶ FIGURE 8–47



Solution For the E-MOSFET in Figure 8–47, the gate-to-source voltage is

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} = \left(\frac{15\ \text{k}\Omega}{115\ \text{k}\Omega}\right)24\ \text{V} = \mathbf{3.13\ V}$$

To determine V_{DS}, first find K using the minimum value of $I_{D(on)}$ and the specified voltage values.

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{200\ \text{mA}}{(4\ \text{V} - 2\ \text{V})^2} = \frac{200\ \text{mA}}{4\ \text{V}^2} = 50\ \text{mA/V}^2$$

Now calculate I_D for $V_{GS} = 3.13\ \text{V}$.

$$I_D = K(V_{GS} - V_{GS(th)})^2 = (50\ \text{mA/V}^2)(3.13\ \text{V} - 2\ \text{V})^2$$
$$= (50\ \text{mA/V}^2)(1.13\ \text{V})^2 = 63.8\ \text{mA}$$

Finally, calculate V_{DS}.

$$V_{DS} = V_{DD} - I_D R_D = 24\ \text{V} - (63.8\ \text{mA})(200\ \Omega) = \mathbf{11.2\ V}$$

Selected Key Terms

JFET Junction field-effect transistor; one of two major types of field-effect transistors.

Drain One of three terminals of a FET analogous to the collector of a BJT.

Source One of three terminals of a FET analogous to the emitter of a BJT.

Gate One of three terminals of a FET analogous to the base of a BJT.

Selected Key Terms

Transconductance (g_m)	The ratio of a change in drain current to a change in gate-to-source voltage in a FET.
MOSFET	Metal oxide semiconductor field effect transistor; one of two major types of FETs; sometimes called IGFET.
Depeletion	In a MOSFET, the process of removing or depleting the channel of charge carriers and thus decreasing the channel conductivity.
Enhancement	In a MOSFET, the process of creating a channel or increasing the conductivity of the channel by the addition of charge carriers.

Quiz

1. If an *n*-channel JFET has a positive drain voltage and the gate-source voltage is zero, the drain current will be

a. zero

b. I_{DSS}

c. I_{GSS}

d. none of the above

Quiz

2. For a JFET, two voltages with the same magnitude but opposite signs are

a. V_D and V_p

b. V_D and V_S

c. $V_{GS(th)}$ and V_{cutoff}

d. V_p and $V_{GS(off)}$

Quiz

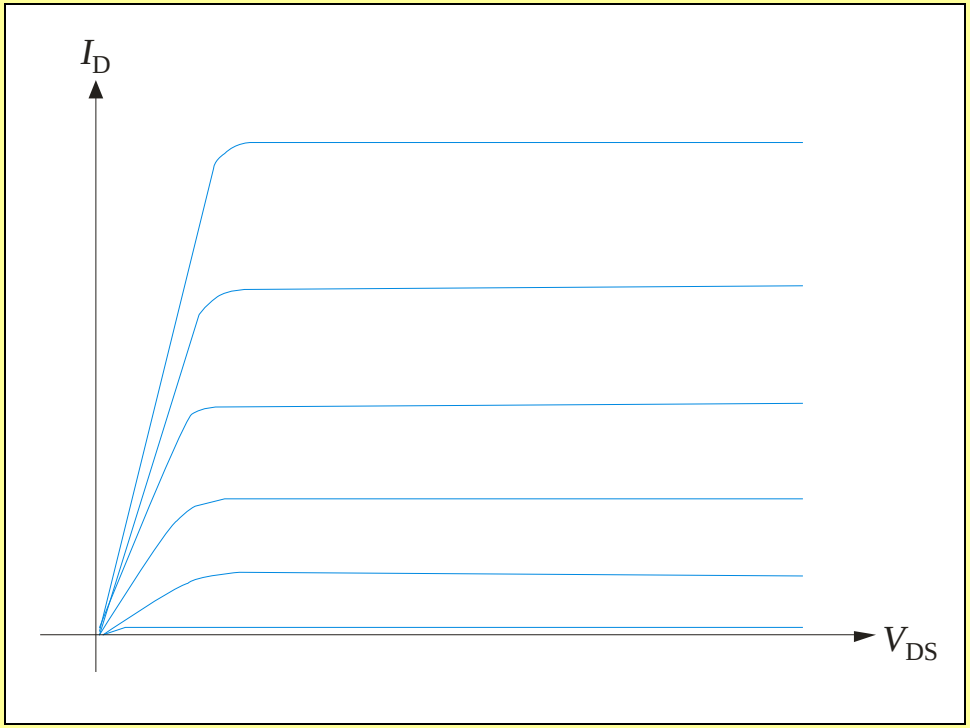
3. A set of characteristic curves for a JFET are shown. The blue lines represent different values of

a. V_{DS}

b. V_{GS}

c. V_S

d. V_{th}



Quiz

4. *Transconductance* can be expressed as

a. $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}}$

b. $g_m = \dfrac{\Delta I_G}{\Delta V_{DS}}$

c. $g_m = \dfrac{\Delta I_D}{\Delta V_{DS}}$

d. $g_m = \dfrac{\Delta I_G}{\Delta V_{GS}}$

Quiz

5. JFETs *cannot* be biased using

a. self bias

b. voltage-divider bias

c. zero bias

d. current-source bias

Quiz

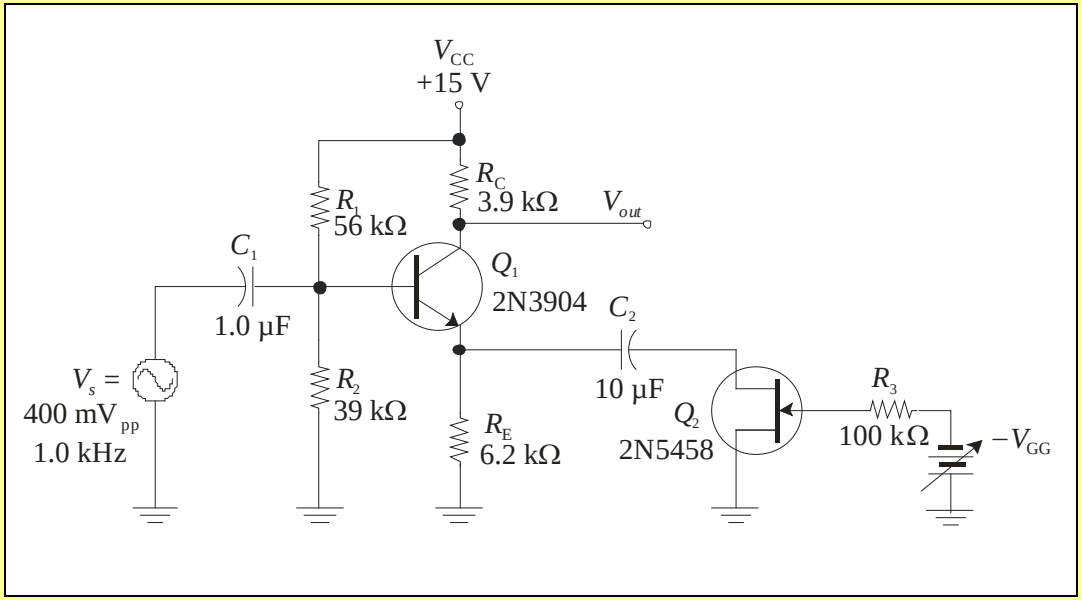
6. The JFET operating point in the circuit shown is

a. at the origin

b. at I_{sat}

c. at V_{CC}

d. undefined



Quiz

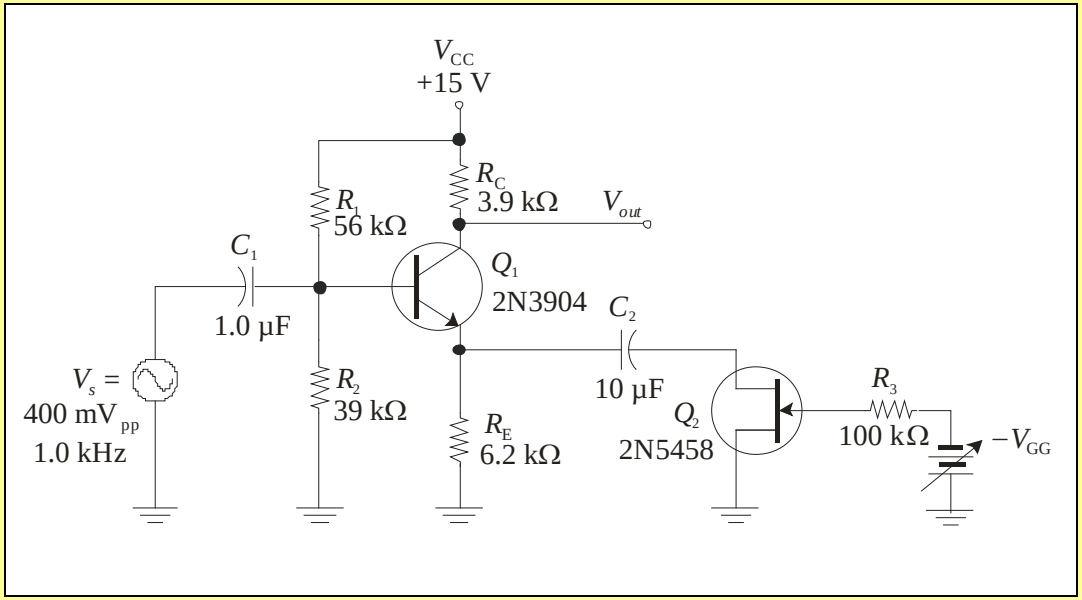
7. The JFET in this circuit acts like a(n)

a. voltage source

b. amplifier

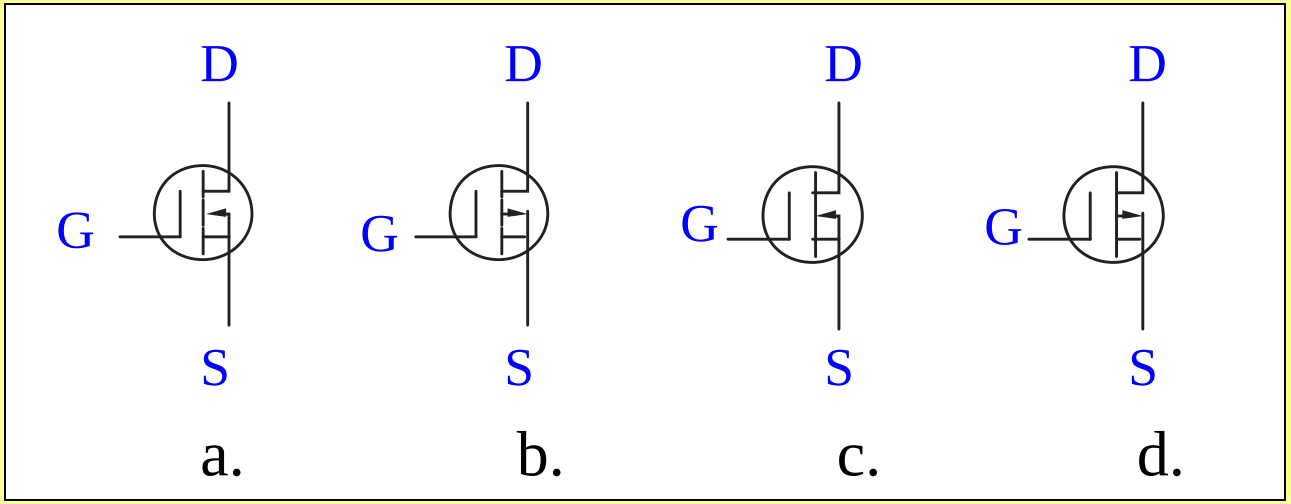
c. capacitor

d. resistor



Quiz

8. The symbol for a *p*-channel E-MOSFET is



Quiz

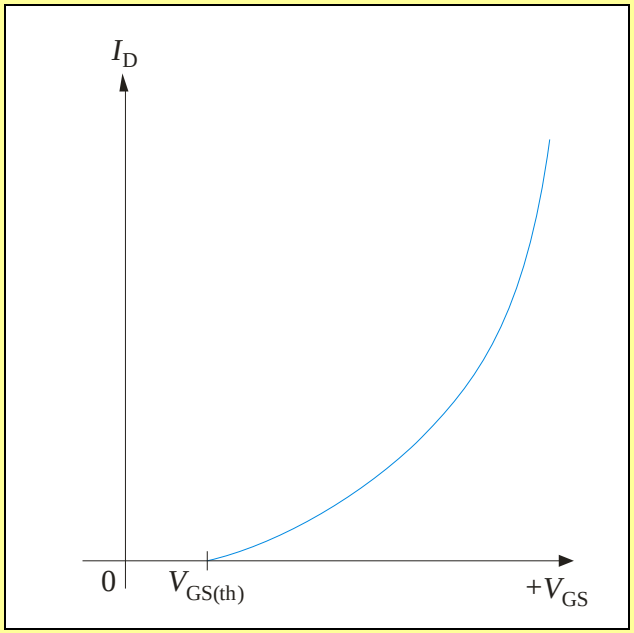
9. The transfer curve shown is for an *n*-channel

a. E-MOSFET

b. D-MOSFET

c. JFET

d. all of the above



Quiz

10. A type of FET that can use the same bias method as a BJT is a(n)

a. E-MOSFET

b. D-MOSFET

c. JFET

d. all of the above

Quiz

Answers:

1. b	6. a
2. d	7. d
3. b	8. b
4. a	9. a
5. c	10. a