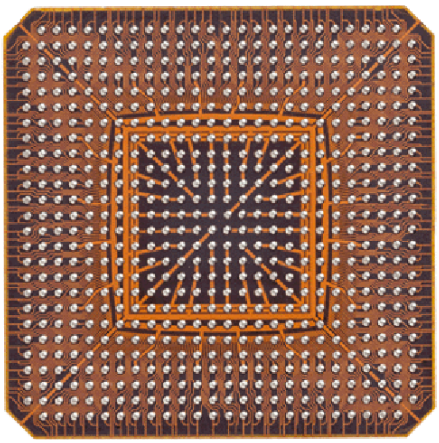


# Electronic Packaging Technologies

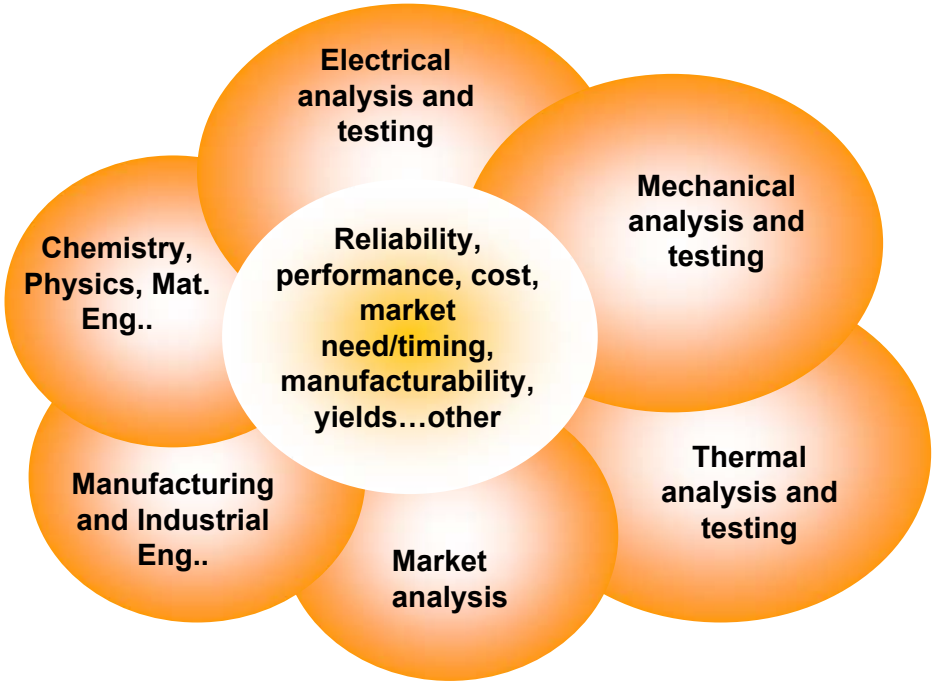
Sergio Lopez-Buedo, Eduardo Boemo
Universidad Autonoma de Madrid
e-mail: sergio.lopez-buedo@uam.es



## Introduction to Electronic Packaging

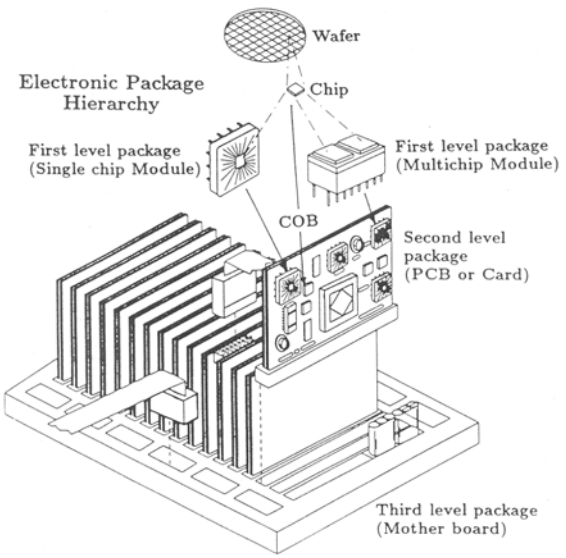
- **Electronic Packaging** is a multi-disciplinary subject
  - Mechanical, Electrical and Industrial Engineering, Chemistry, Physics and even Marketing
- **Electronic Packaging:** Housing and interconnection of integrated circuits to form electronic systems
- **Electronic Packaging** must provide
  - Circuit support and protection
  - Heat dissipation
  - Signal distribution
  - Manufacturability and serviceability
  - Power distribution

# Issues in Electronic Packaging



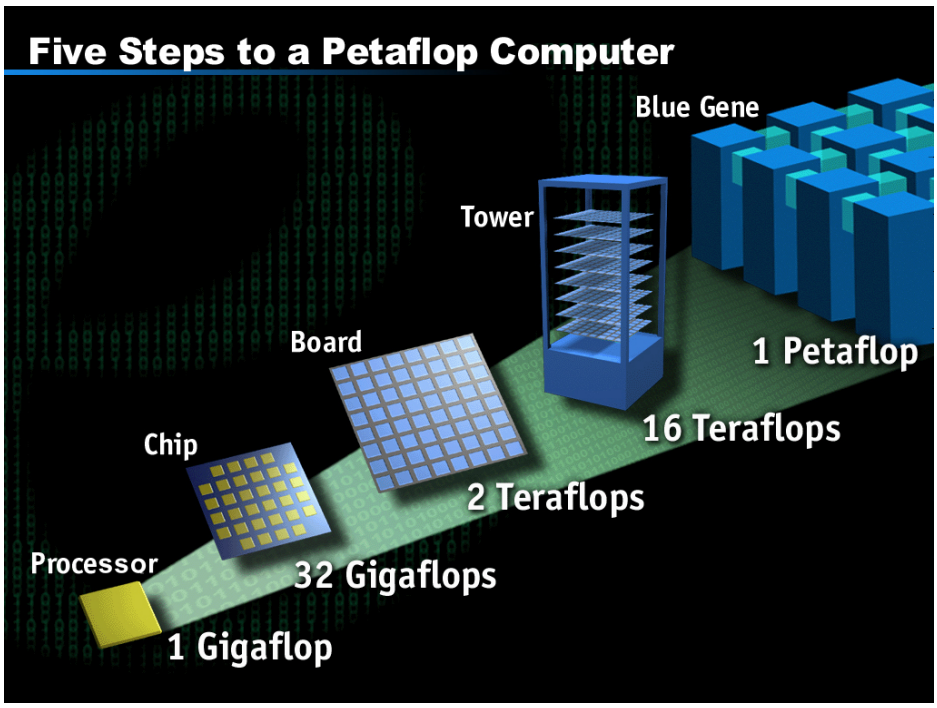



# Hierarchy of Interconnection Levels



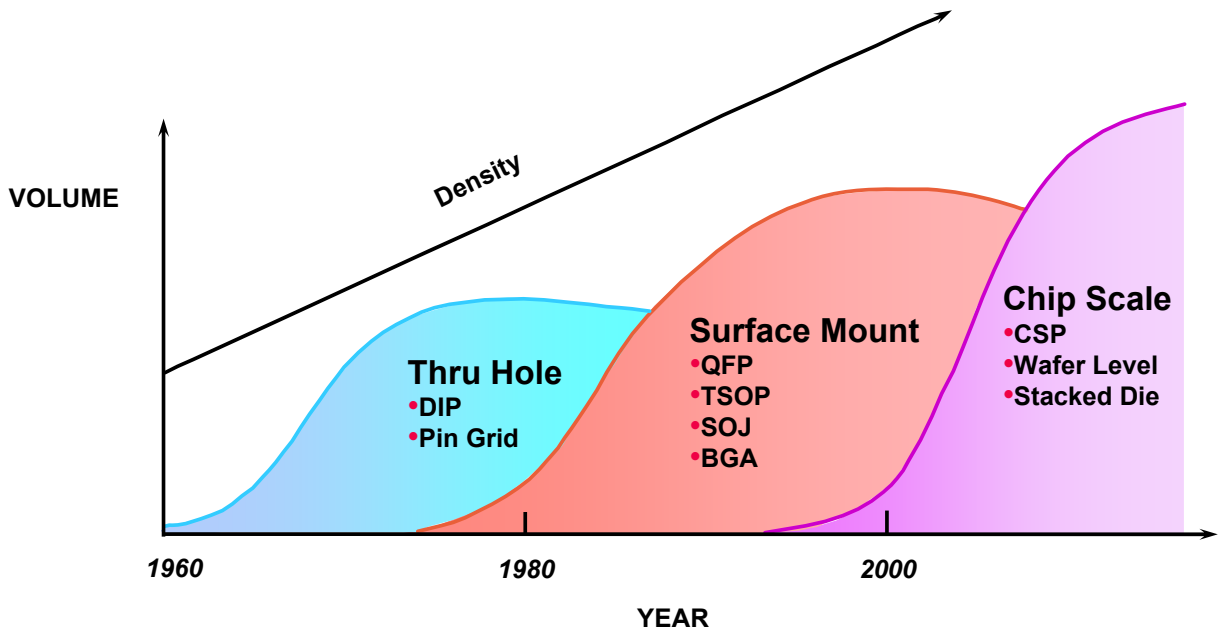

- Level 0
  - Gate-to-gate interconnections on the silicon die
- Level 1
  - Connections from the chip to its package
- Level 2
  - PCB, from component to component or to external connector
- Level 3
  - Connections between PCBs, including backplanes or motherboards
- Level 4
  - Connections between subassemblies, for example a rack
- Level 5
  - Connections between physically separate systems, using for example an Ethernet LAN

# Blue Gene: Example of Connection Hierarchy

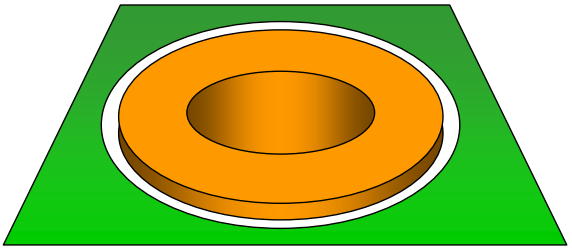


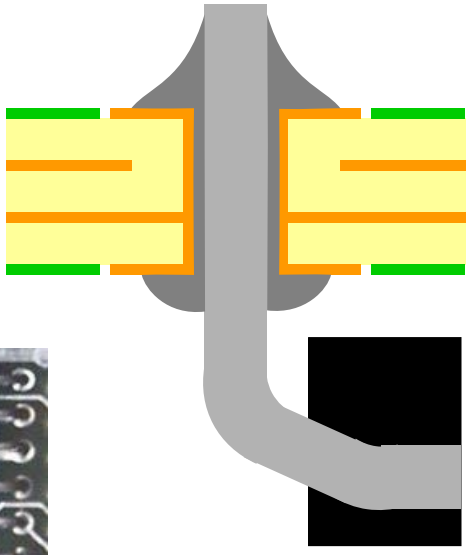


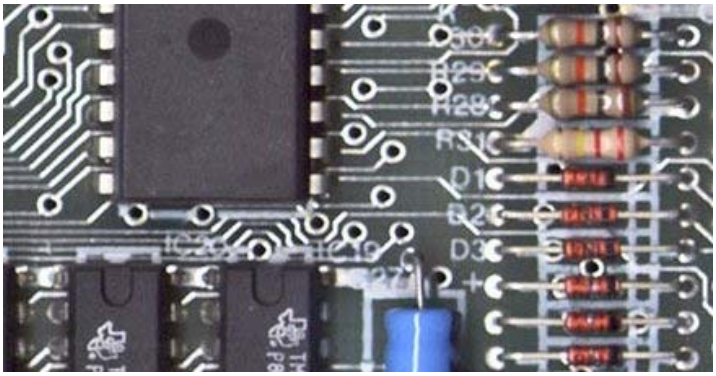

# The Three Breakthroughs in Chip Packaging Technology



# Through (Thru) Hole Mounting





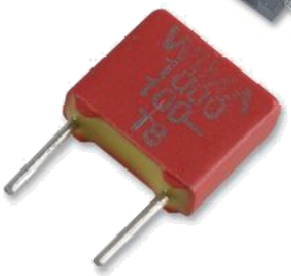


Sinclair ZX48 motherboard
(Manufactured 1984)

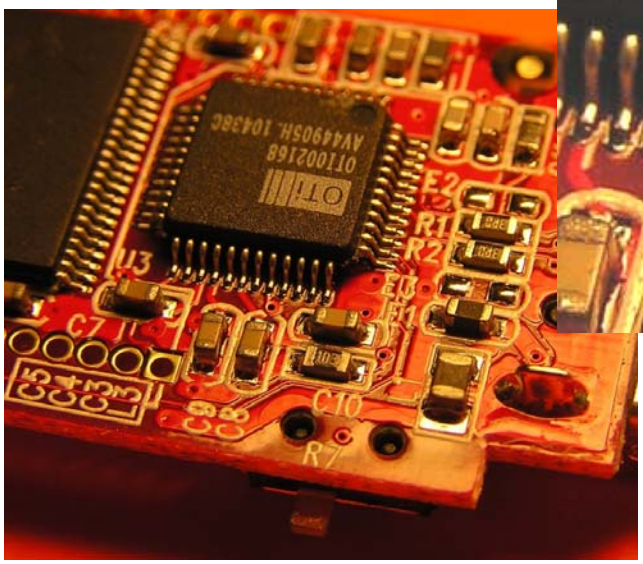


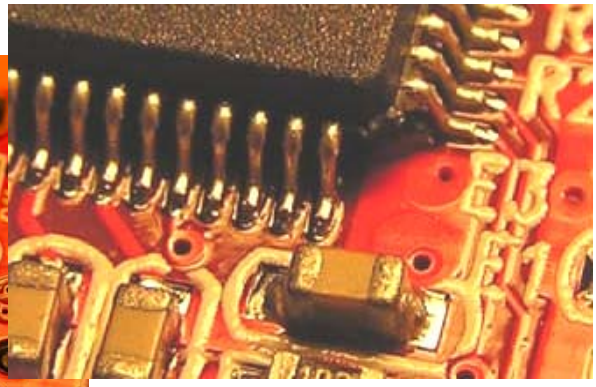
# Through-Hole Benefits and Drawbacks

- The pins of the components go through the previously drilled PCB holes
- Benefits
  - Easy to solder, either automatically (wave) or by hand
  - Easy to desolder and test
  - Implement interconnections between upper and lower layers (vias) in non-plated hole technologies
- Drawbacks
  - Signals must necessarily go through all PCB layers
  - Low density due to minimum pin diameter and only one-sided mounting

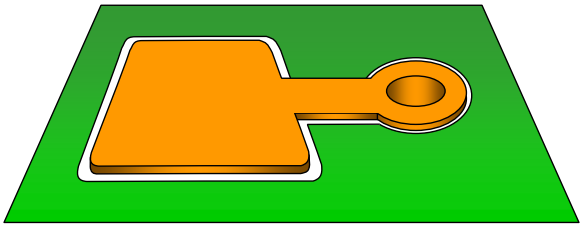


# Surface-Mount Technology (SMD)





USB Flash drive (Manufactured 2004)



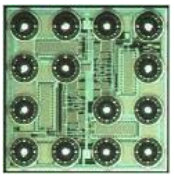


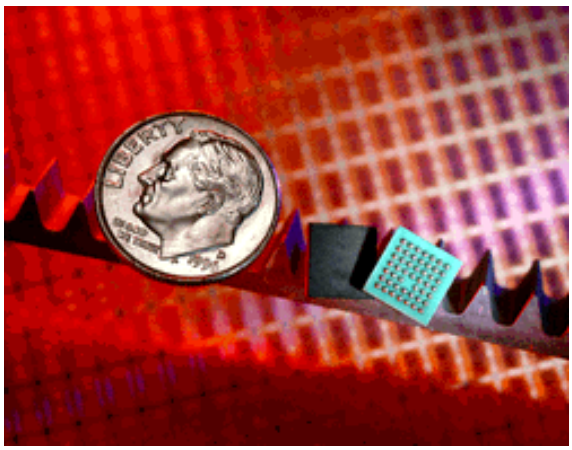
# SMD Benefits and Drawbacks

- The pins of the devices are mounted directly onto the surface of the PCB
- Benefits
  - Much higher density: pins can be thinner, devices can be mounted on both sides of the PCB, components do not block signals in inner layers
  - Higher degree in the automation of the mounting process
  - Less parasitic inductance and capacitance
  - Reduced costs (½ to ¼) and size (¼ to one tenth)
- Drawbacks
  - Poor manual solderability and reparability
  - Reliability issues due to thermal/mechanical stress during soldering and operation (different thermal expansion coefficients)
  - Classic verification procedures no longer valid

# Chip Scale Packages (CSP)

- **Chip Scale Package,** or **CSP,** based on IPC/JEDEC J-STD-012 definition, is a single-die, direct surface mountable package with an area of no more than 1.2 times the original die area





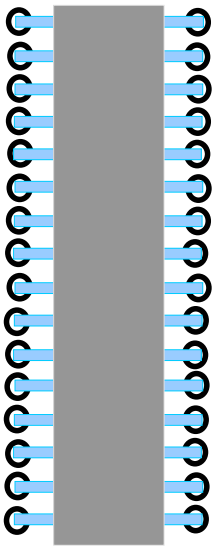


# CSP Benefits and Drawbacks

- CSP is not a new mounting technology, is an evolution of SMD
- The passive components surrounding the chips must also be miniaturized (resistors, decoupling capacitors)
- Benefits
  - CSP is the only way to achieve pervasive and ubiquitous computing
  - Further improvement in high-speed performance
- Drawbacks
  - Difficulty of PCB fabrication and mounting due to minute pin pitches (0.5 mm)
  - Long-term reliability not studied
  - Not serviceable

# Three Packaging Technologies: Summary

Through Hole → Surface Mount → CSP / WLP



**DIP**

- 100 mil pitch
- Limited by through hole spacing

**TSOP**

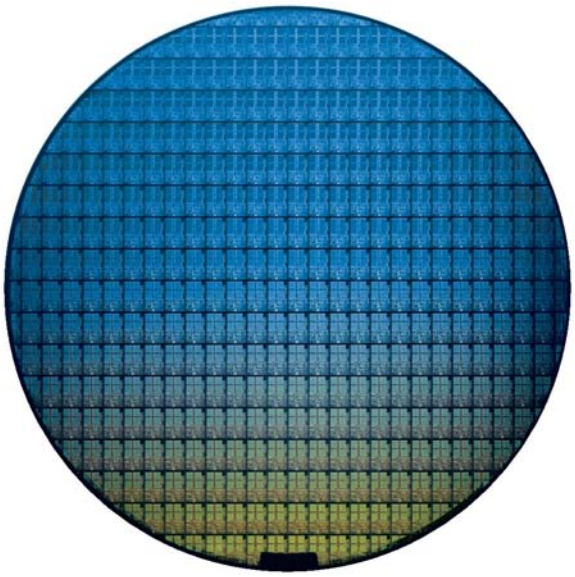
- 25 mil pitch
- Limited by perimeter leads

**CSP/WLP**

- Area array 0.8 mm to 0.5 mm
- Limited by substrate wiring

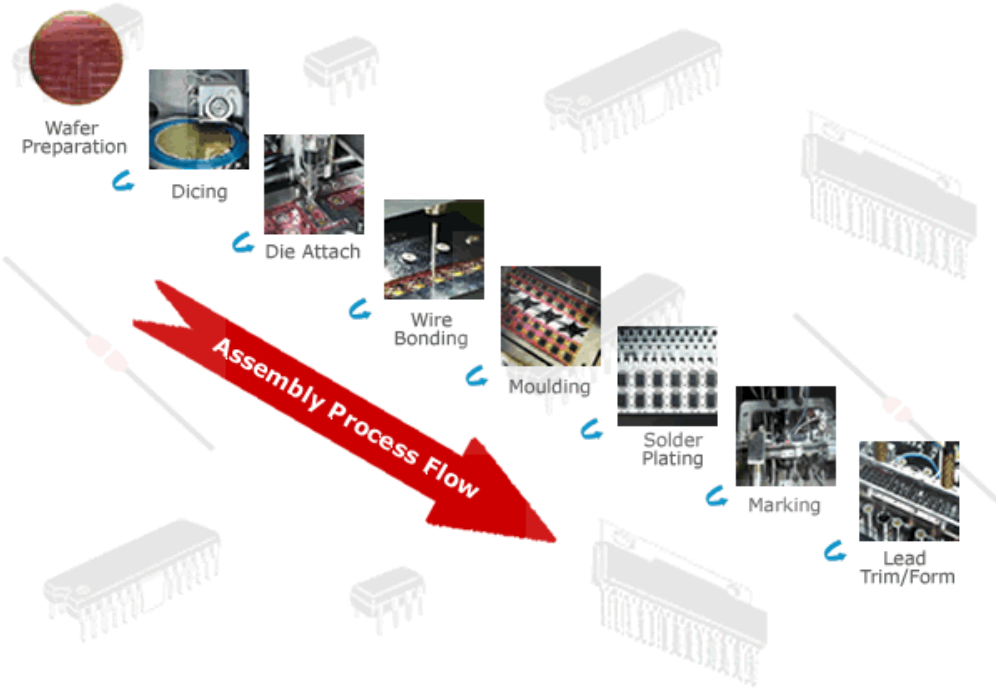


# First Step of Packaging: The Silicon Wafer



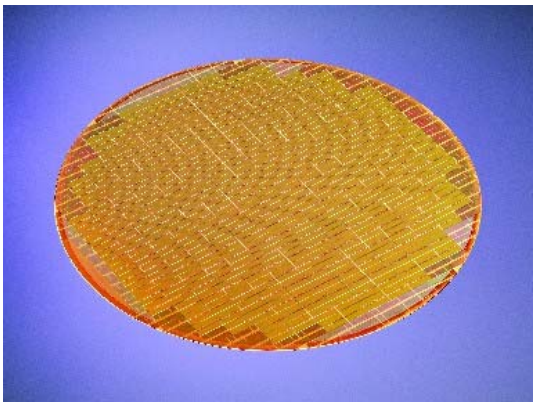
- The problem: How do I know that the chip is going to work before packaging it?
- Solution: Test it. But this is not easy to achieve…
  - Probing pads 150 μm away
  - Area array pads
  - Powering the chip
  - Removing the heat it generates
  - Testing it in a reasonable time
- Only a limited testing (if any) is usually performed, full testing is done after packaging

# A Typical Low-Density SMD Process from Silicon Wafer to Package





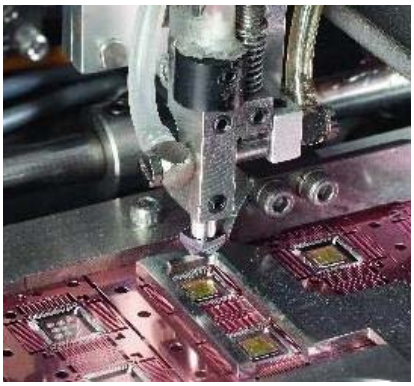

# Wafer Preparation and Dicing



Wafers are mounted on a laminating tape that adheres to the back of the wafer. It holds the wafer throughout the dicing and the die attaching process.

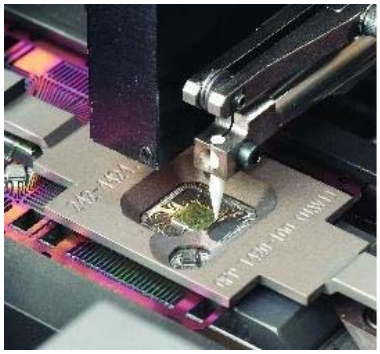
The die-sawing machine using a diamond saw blade saws the wafer into the individual die/pellet on the adhesive backing tape. Deionized water and CO2 bubbles are dispensed on the wafer to remove silicon dust/debris besides lubricating and cooling down the blade

# Die Attach and Wire Bonding



The die attach machine will pick up the die and deposit it on the frame. It may utilize the wafer mapping method to pick up only good die. For most processes, die attach materials like gold or lead-tin based solder wires or silver epoxy paste potting on the frame are required prior to die bonding process.

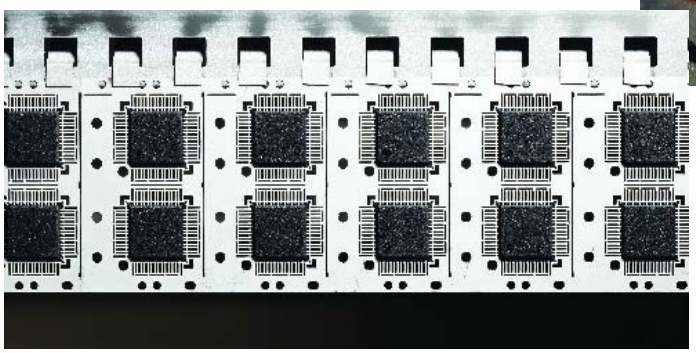
Either Au or Al wires are used depending on application. Bonded one at a time, the wire is fed through a ceramic capillary. With a good combination of temperature and ultrasonic energy, a good metalized wire bond is formed.





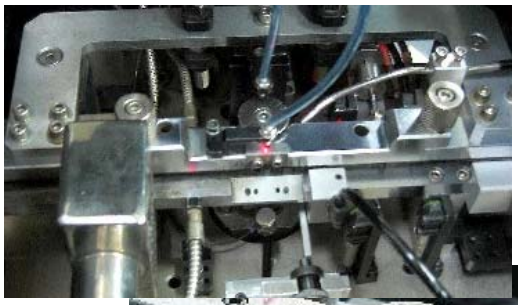
# Moulding and Solder Plating

The moulding process aims to encapsulate the whole wire bonded die against exposure to contamination and other physical damages. The lead frames that hold the dies are placed in individual cavities which are filled with liquid resin.

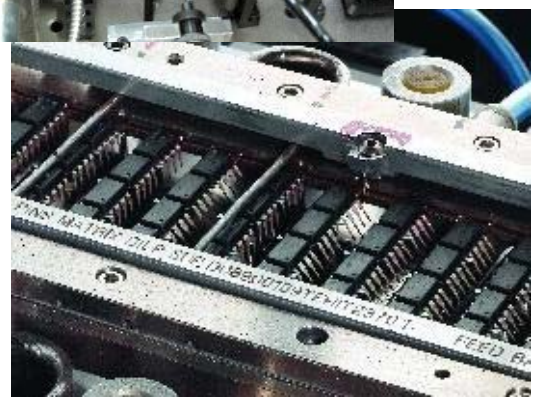


This step provides a layer of Tin Lead solder on the lead frame for making easier the PCB assembly process. Lead free finishing with Tin Bismuth plating or Tin Copper dipping can also be used.

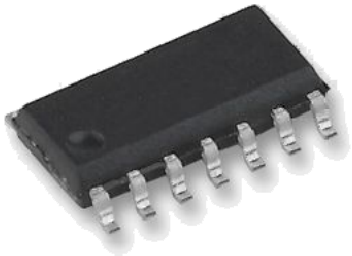
# Marking and Lead Trim/Form



Marking is the coding process that writes customer's corporate and product identification code on a packaged device. It commonly uses a laser-based machine



The final process is to trim away the leads of the packaged device from the frame strip. The leads are cut and formed mechanically to the specified shape

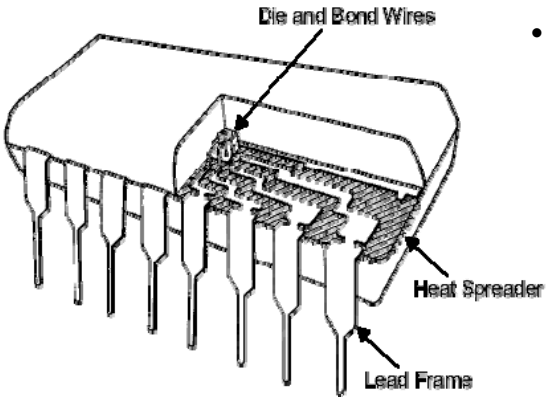




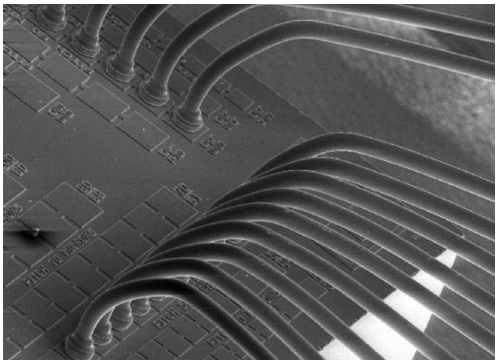
# Chip Attachment to the Package Substrate

- The die attachment compound should provide
  - Electrical grounding
  - Thermal dissipation
- There are three alternatives
  - *Soft Solder Die Attach:* This process uses a solder material to bond the die to the lead frame. The solder is introduced as a wire preform and melted onto the hot lead frame surface as a liquid solder dot.
  - *Epoxy Die Attach:* Epoxy die attach is the most commonly used process. Usually silver-loaded polymers are used, but the term generally encompasses the use of other adhesives, such as polyimide- or silicone-based materials.
  - *Metal-filled glasses:* Less used because the high temperatures needed, but have been used in ceramic packages
- Points to pay attention to: Different CTEs, fatigue, creeps

# Chip-Package Connection: Wire Bonding



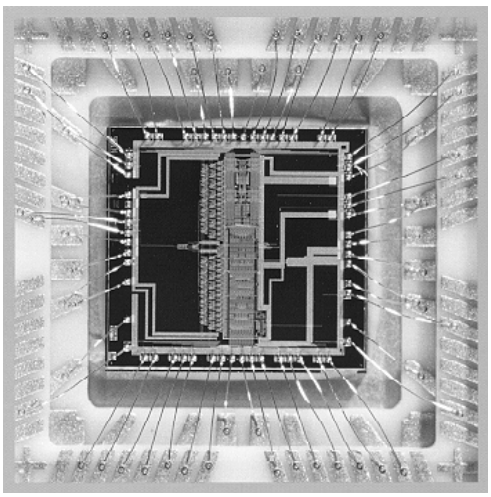

- Connections are made from the chip to the pad frame via thin wires
  - Typically 100x100 μm metal pads on 200 μm pitch
  - Mechanical bonding of one pin at a time (sequential)



- The wires are made of low resistivity alloys or doped metals
  - Gold and aluminum
  - Also copper and silver
  - Typically 25 μm diameter for logic devices

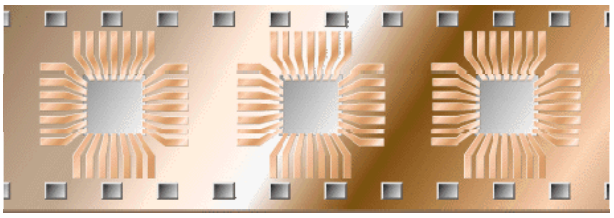


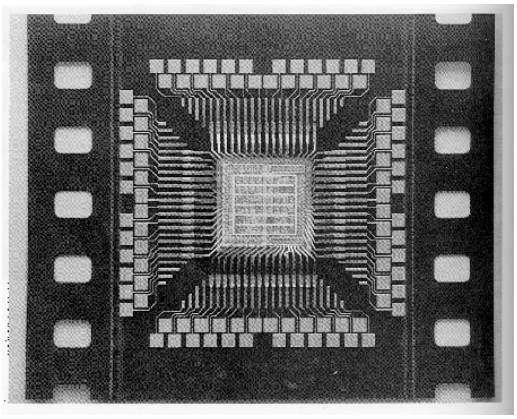
# Drawbacks of Wire Bonding



- Slow process
  - One pin at a time
  - Speeds from 4 to 10 wires per second
- Pads are limited to the chip periphery
  - Low pad density and reduced pad pitch
  - Up to approx 500 pads
- Electrical limitations
  - High inductance (~1nH) of wires (~10nH plus pins)
  - Crosstalk between adjacent wires

# Chip-Package Connection: TAB

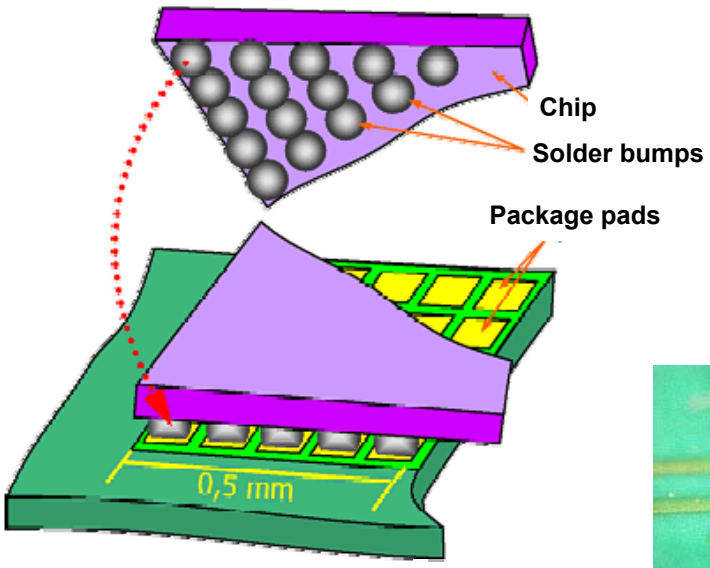




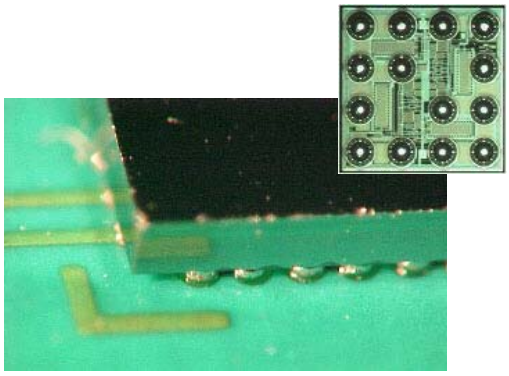
- Tape automated bonding
  - The interconnections are patterned on a multilayer polymer tape.
  - The tape is positioned above the `bare die' so that the metal tracks (on the polymer tape) correspond to the bonding sites on the die
- Advantages over wire bonding
  - Smaller and closer pads: higher density, up to 850 pins
  - Better electrical characteristics
  - Faster procedure but more expensive machinery



# Chip-Package Connection: Flip-Chip




The chip is “soldered” to the package substrate using the solder balls “bumps” that have been grown over the die pads



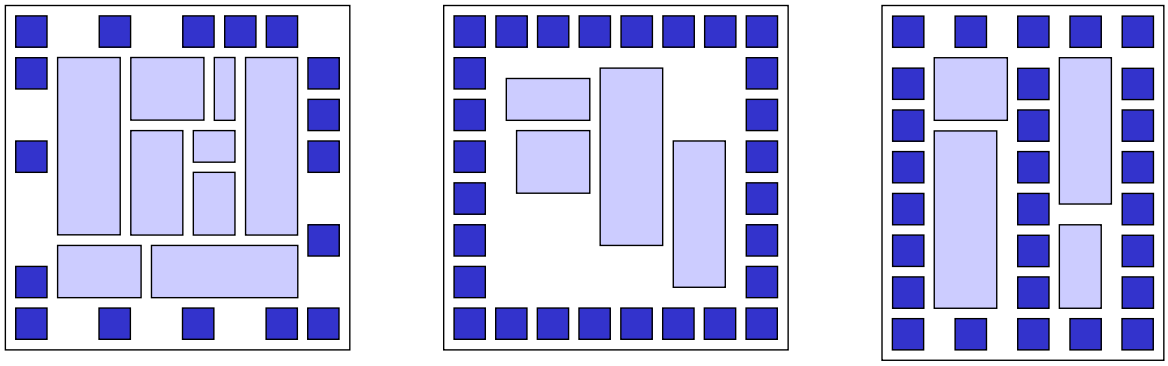
Controlled Collapse Chip Connection, C4

# Flip-Chip Advantages and Drawbacks

- Flip-chip is currently the preferred process for high-end integrated circuits
  - High frequency of operation, small size and/or many I/O pins
- Many advantages:
  - Improved density: pad pitch and size is not better than in wire bonding, but I/O pads can be distributed all over the die, not just in the borders
  - Reduced inductance (~0.1 nH) due to the elimination of wires and better power/ground behavior
  - Faster process, all the pads are soldered at the same time
- Some drawbacks
  - Alignment is critical (and blind), although there is some tolerance due to its self-alignment property
  - Mechanical stress due to different thermal expansion coefficients of the silicon and the package substrate



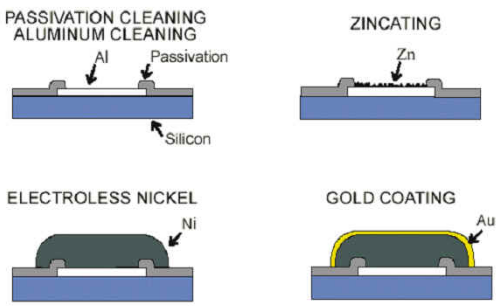
# Flip-Chip: No Longer Pad-Limited Chips



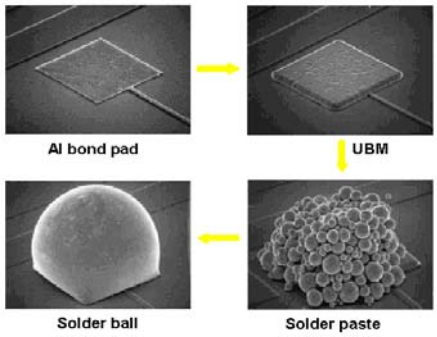
Core-Limited Pad-Limited Area-Array Pads

# Flip-Chip: Growing the Solder Bumps

- There are many techniques, for example:




*Plated bumping removes the oxide layer on the Al bond pad through wet chemical cleaning processes. Electroless nickel plating is then employed to cover the Al bond pad with a nickel layer to the desired plating thickness, forming the foundation of the bump. An immersion gold layer is then added over the nickel bump for protection.*

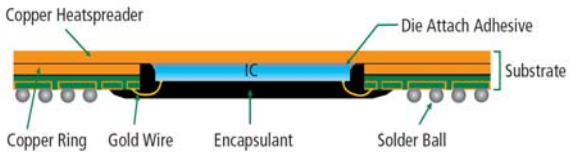


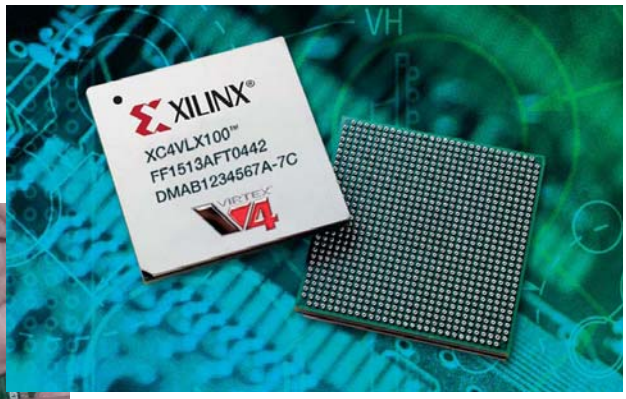

*Adhesive bumping is a flip-chip bumping process that stencils electrically conductive adhesive over an underbump metallization placed over the bond pad. The stenciled adhesive serves as the bump after it has been cured.*

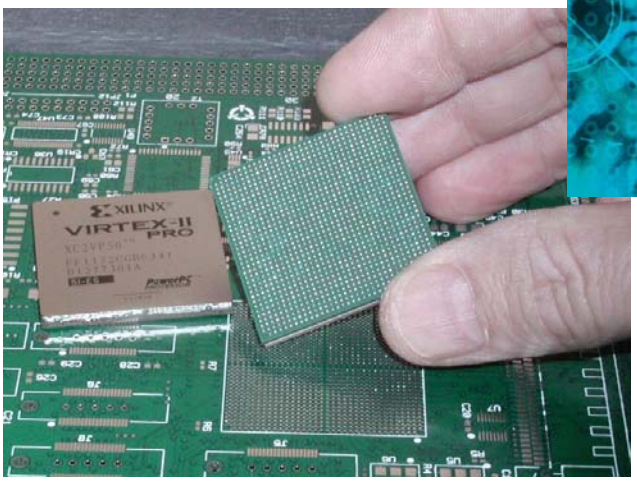
- A bump is typically 70-100 μm high, and 100-125 μm in diameter.
- Current materials for the bumps are: SnPb Eutectic (63%Sn, 37%Pb), high lead (95%Pb, 5%Sn) or lead-free (97.5%Pb, 2.5%Ag) compositions

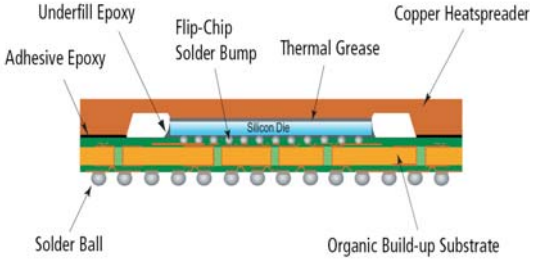


# Flip-Chip Concept at the Board Level: BGA Packages

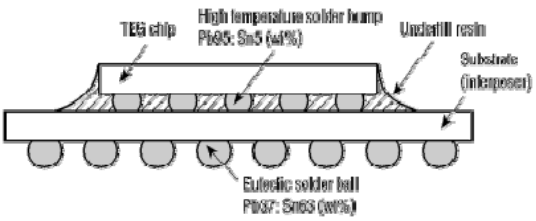


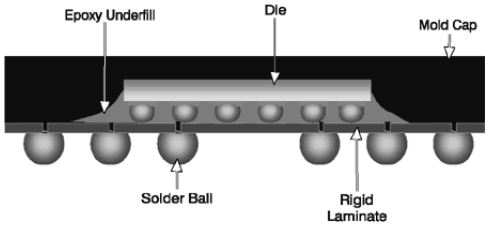



# Flip-Chip: Direct Access to Silicon View or Using a Lid/Overmold



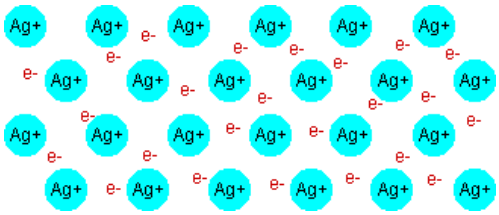



# Materials Used in Electronic Packaging

| Material | Application |
|---|---|
| Semiconductors | Si, GaAs |
| Metals | Solders for interconnects (Sn-Pb, Sn-Ag; gold wirebonds; copper leadframes (Kovar, CuBe, Alloy 42); copper traces in substrates; tungsten, molybdenum traces in co-fired ceramics; Ag, Au, Pd for thin/thick films on ceramics; and nickel diffusion barrier metallizations. |
| Ceramics | $Al_2O_3$ substrates modified with BaO, $SiO_2$, CuO,etc.; SiN dielectrics; diamond heat sinks. |
| Polymers | Epoxies (overmold); filled epoxies (overmold); silica-filled anhydride resin (underfills); conductive adhesives (die bonding, interconnects); laminated epoxy/glass substrates; polyimide dielectric; benzoyclobutene; silicones; and photosensitive polymers for photomasks. |
| Glasses | $SiO_2$ fibers for optoelectronics; silicate glasses for sealing; borosilicate glass substrates; and glass fibers for epoxy/glass substrates (F4-4). |

# Metals

- In a metal, the outer electrons are shared among all the atoms in the solid

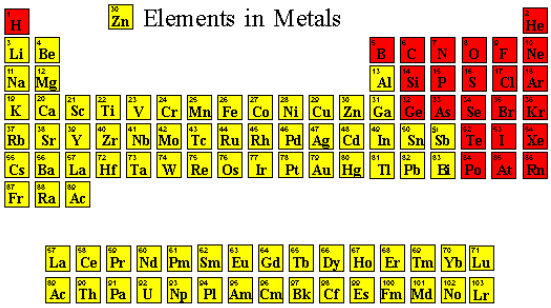



- Each atom gives up its outer electrons and becomes slightly positively charged
  - The negatively charged electrons hold the metal atoms together
  - Since the electrons are free to move, they lead to good thermal and electrical conductivity
- It is impossible to see through metals, since these valence electrons absorb any photons of light which reach the metal.
  - No photons pass through



# Metal Alloys

- Alloys are compounds consisting of more than one metal
  - Adding other metals can affect the density, strength, fracture toughness, plastic deformation, electrical conductivity and environmental degradation
- Unlike pure metals, many alloys do not have a single melting point.
  - Instead, they have a melting range in which the material is a mixture of solid and liquid phases.
  - Alloys can be designed with a single melting point, and these are called eutectic mixtures
  - Example: 63%Sn, 37%Pb



# Properties of Metals and Metal Alloys

- At least good, but usually excellent thermal and electrical conductivities
- Relatively high densities, especially compared to polymers
  - Materials with high densities often contain atoms with high atomic numbers, such as gold
  - However, some metals such as aluminum or magnesium have low densities, and are used in applications that require other metallic properties but low weight
- Fracture Toughness
  - Ability to avoid fracture, especially when a flaw is introduced
- Plastic deformation



# Lead Poisoning

- Saturnism, plumbism or painter's colic
- Neurological problems
  - reduced IQ, nausea, abdominal pain, irritability, insomnia, excess lethargy or hyperactivity, headache and, in extreme cases, seizure and coma
- Gastrointestinal problems
  - constipation, diarrhea, abdominal pain, vomiting, poor appetite, weight loss
- Other associated affects are anemia, kidney problems, and reproductive problems
  - Lead toxicity often causes the formation of bluish line along the gums, which is known as the "Burtons's line "
- Elimination of lead: RoHS EU directives (Restriction of Hazardous Substances)

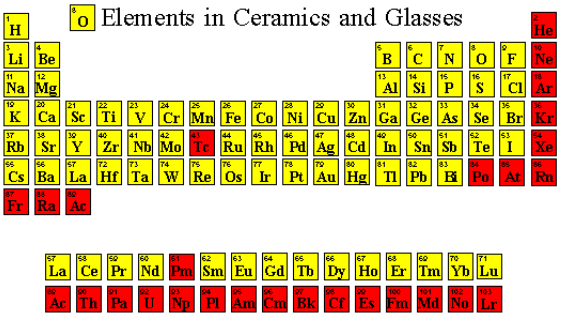
# RoHS Directive

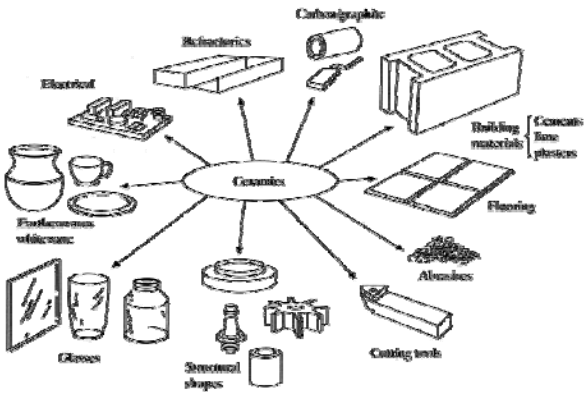
- "Directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment"
  - 2002/95/EC, took effect July 1st, 2006
- Forbidden substances:
  - Lead
  - Mercury
  - Cadmium
  - Hexavalent chromium ($Cr^{6+}$)
  - Polybrominated biphenyls (PBB)
  - Polybrominated diphenyl ether (PBDE)
- The maximum permitted concentrations are 0.1% or 1000 ppm (except for cadmium, which is limited to 0.01% or 100 ppm) by weight of homogeneous material:
  - Limits do not apply to the weight of the finished product
  - But to any single substance that could be separated mechanically



# Ceramics

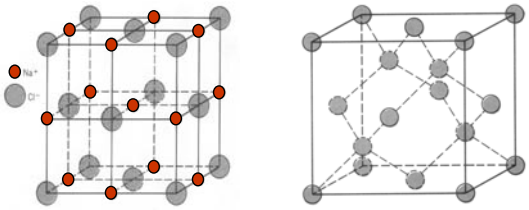
- **Ceramics:** Often broadly defined as any inorganic nonmetallic material. Examples of such materials can be anything from NaCl (table salt) to clay (a complex silicate).
  - Metallic plus nonmetallic elements joined together by ionic and/or covalent bonds
  - Crystalline, polycrystalline or amorphous. The last one is sometimes treated as a different category, glasses
- **Glasses:** An inorganic nonmetallic amorphous material (does not have a crystalline structure). Examples of glasses range from bottles to the extremely high purity silica glass in optical fibers.

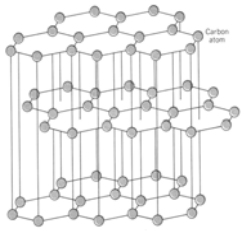


# Properties of Ceramics and Glasses

- High melting temperature
- Low density
- High strength and Hardness
- Water resistance
- Corrosion resistance
- Many ceramics are good electrical and thermal insulators
  - Graphite: electrical and thermal conductor
- Low to null ductility
- Low fracture toughness
- Some ceramics have special properties:
  - Magnetic materials
  - Piezoelectric materials
  - Superconductors at very low temperatures

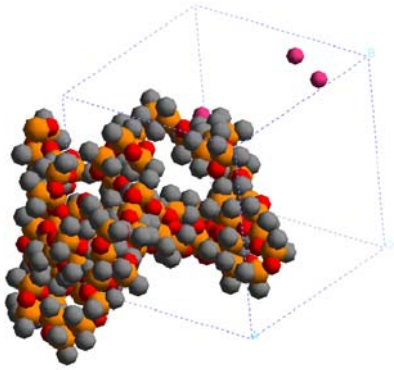


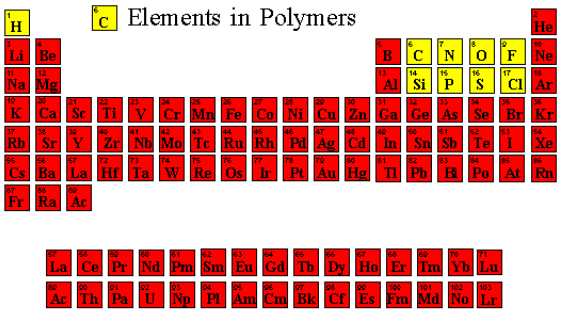




# Plastics: Polymers

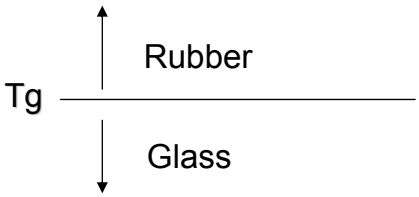
- Poly-mer = “several-parts”
  - Typically organic materials
  - But could be inorganic like silicones
  - Offer poor protection levels
  - But they are cost effective
- Electrical characteristics
  - High resistivity (insulator)
  - Low dielectric constant (<4)
- Thermal characteristics
  - Bad thermal conductivity
  - Low coefficient of thermal expansion (CTE) for T<Tg
  - Thermal stability up to 300 ºC for some compounds
- Good mechanical properties
- High water and solvent absorption
- Good adhesion

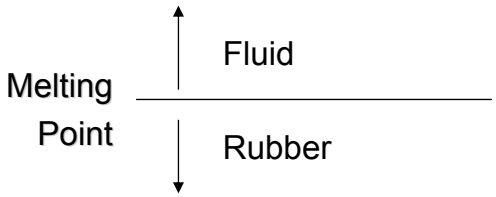




# Glass Transition and Melting Point

- Glass transition temperature $T_g$ :




- Melting point: Temperature of fusion
- Glass and melting points of a polymer will determine which applications it will be suitable for
  - Many industrially important polymers have glass transition temperatures near the boiling point of water, and they are most useful for room temperature applications
  - Some specially engineered polymers can withstand temperatures as high as 300 ºC



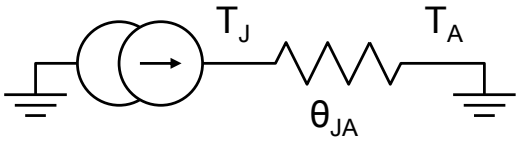
# Characteristics of a Package

- Thermal performance
  - Ability to dissipate the heat generated by the IC
- Signal integrity
  - To ensure that the package parasitic inductances and capacitances do not distort the I/O signals
- Power distribution
  - The package must be able to supply enough current for the IC to work, and it must be also capable of handling the highest current peaks
- Manufacturability
  - The best package is useless if it cannot be soldered. It should not require excessive handling precautions
- Testability
  - To check if all pins have been correctly soldered. It is also about its prototyping capabilities
- Reliability
  - The package must provide a good long-term reliability even in the harshest environments

*All this features should be achieved at a reasonable COST*

# Thermal Behavior of a Package

- For modeling the thermal behavior of a package, a comparison to this circuit is used:



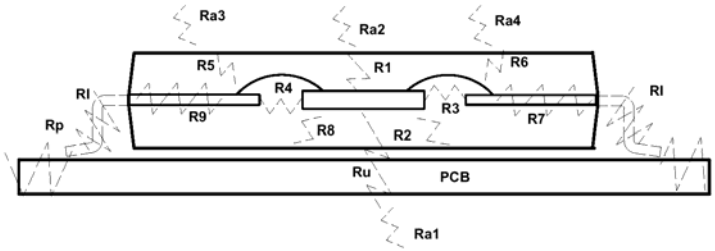

  - Where the intensity is the power dissipated, the thermal resistance means the ability of the package to remove the heat, and the voltage relates to the temperatures
  - This model just says that the increase in the junction temperature respect to the ambient one is proportional to the power dissipated and the thermal characteristics of the package

$$T_J = T_A + \theta_{JA} P_D$$



# Thermal Resistances

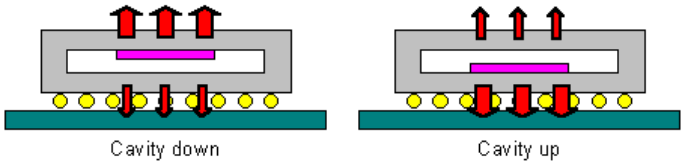
- The thermal model of a package can be very complex:



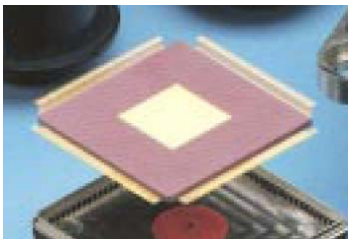

- Moreover, it may have a heat sink over it, or a forced flux of air, etc.. So the thermal resistance is often splitted into resistance from junction-to-case and from case-to-ambient:

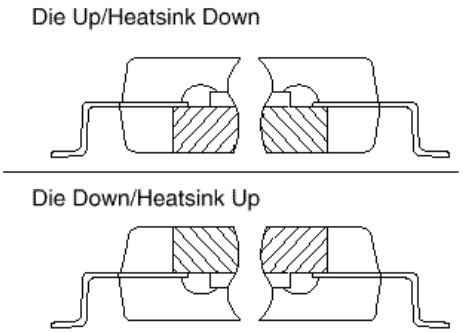
$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

# Some Thermal Aspects in Package Desing

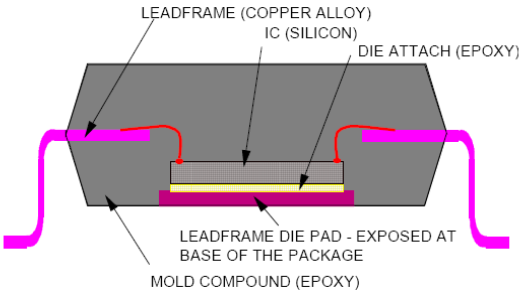



Cavity-Up or Cavity-Down packages



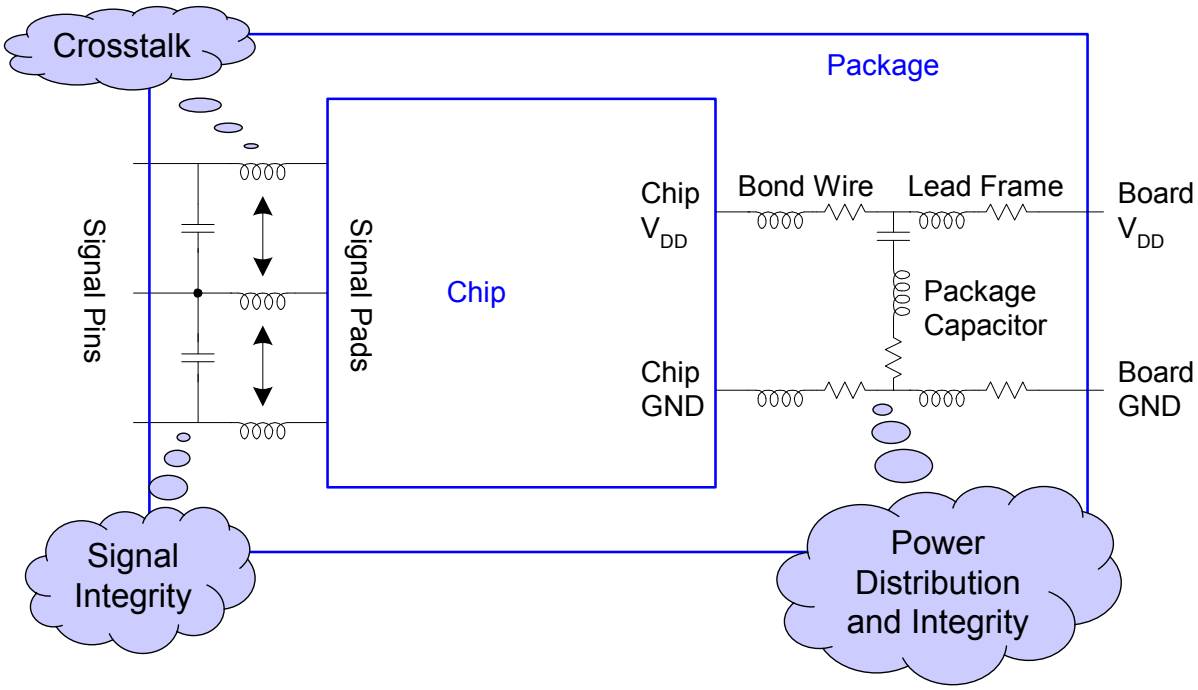



Thermally enhanced packages (TI)

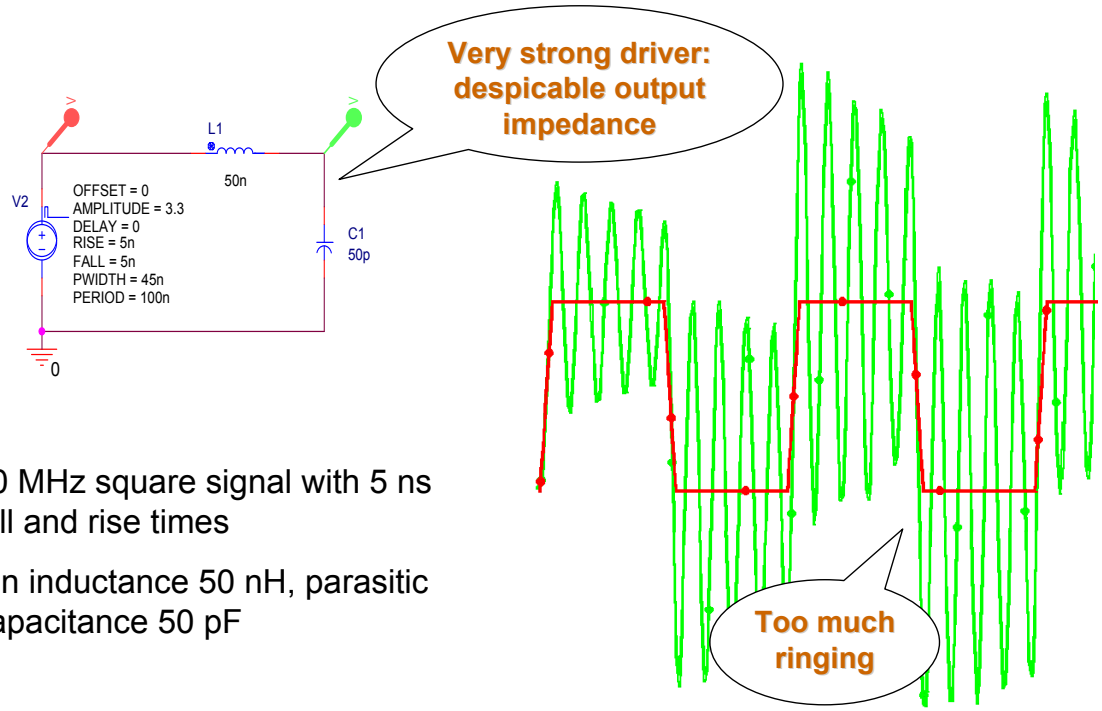





# Electrical Model of the Package



# Spice Simulation: Strong Driver

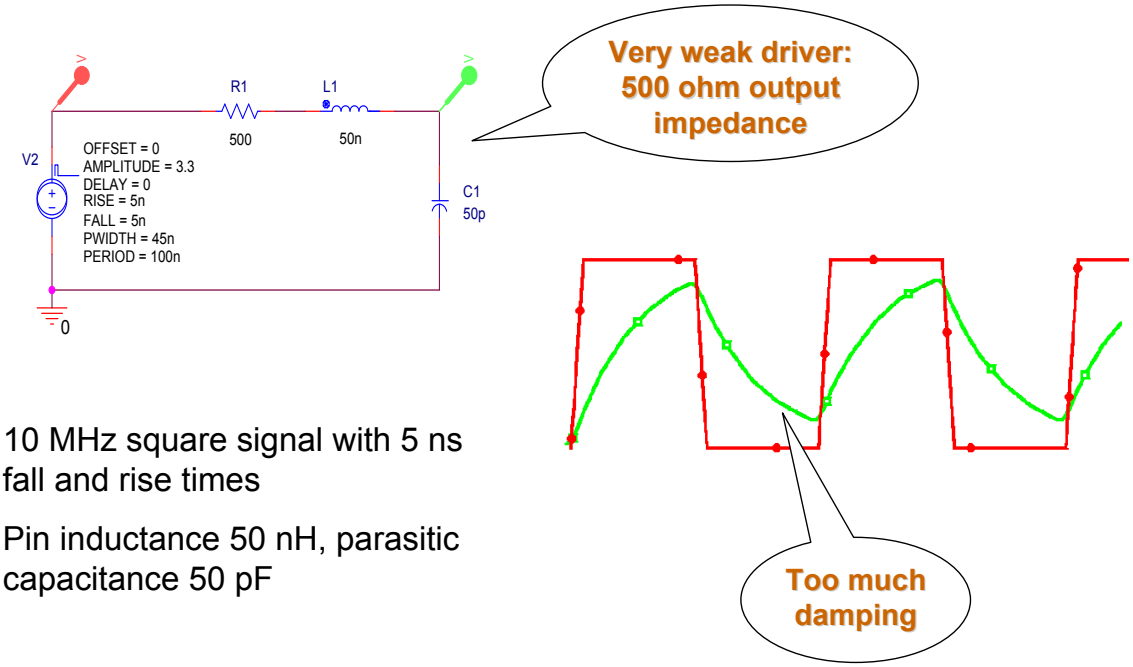



10 MHz square signal with 5 ns fall and rise times

Pin inductance 50 nH, parasitic capacitance 50 pF



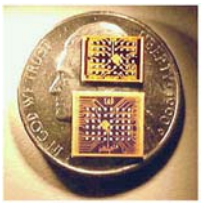
# Spice Simulation: Weak Driver

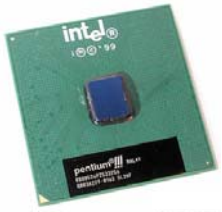


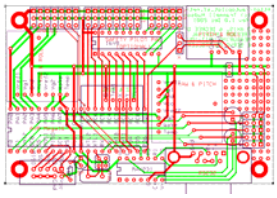

10 MHz square signal with 5 ns fall and rise times

Pin inductance 50 nH, parasitic capacitance 50 pF

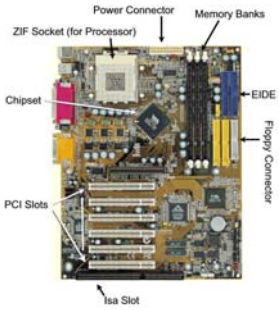
# Parasitic Capacitance as Function of the Interconnection Level

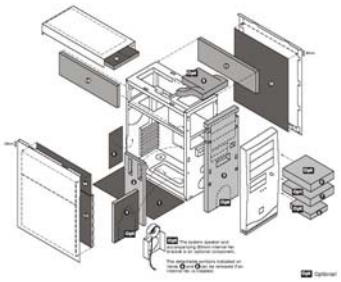


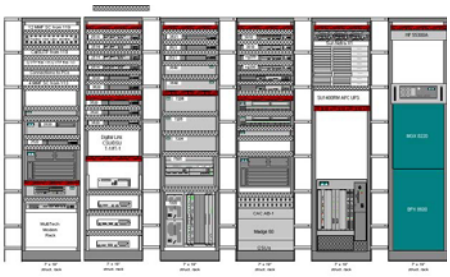


C ~ 10 x f Farads → C ~ pFarads → C ~ 10 x pFarads



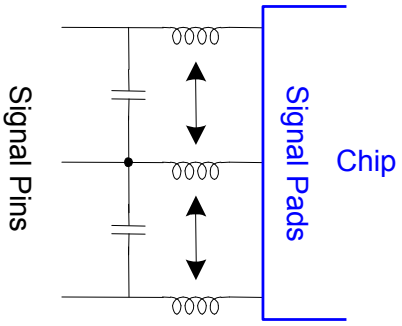


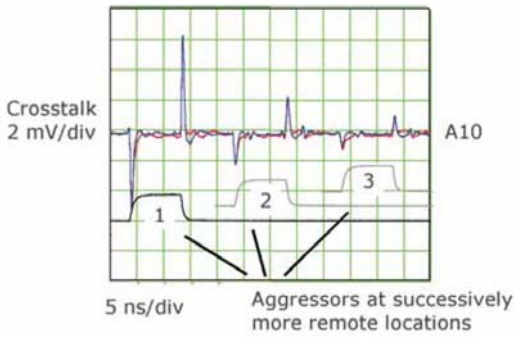
C ~ 10 x pFarads → C ~ 100 x pFarads



# Crosstalk

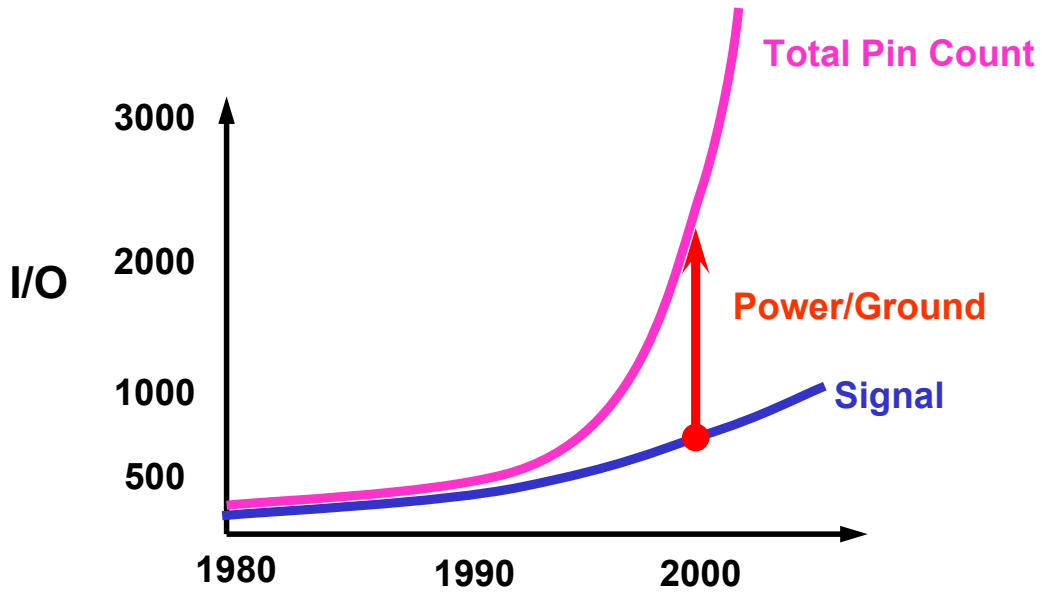
- Crosstalk occurs when a line or pin (aggressor) induces some voltage changes in other line or pin (victim) via their mutual capacitance or inductance




- This two parameters depend on the geometry of the package, and the mutual inductance also on the proximity of a ground pin or plane (length of ground loops)

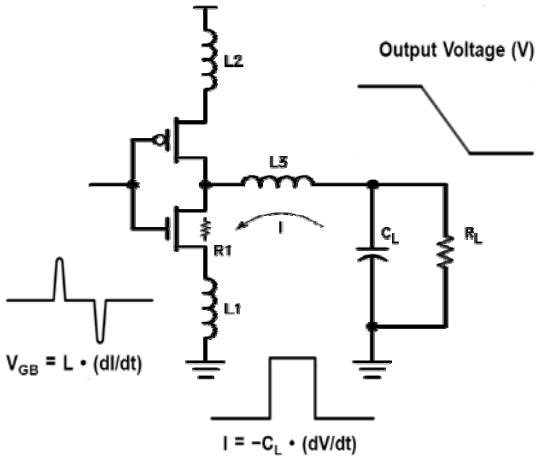
# Power Integrity and Distribution

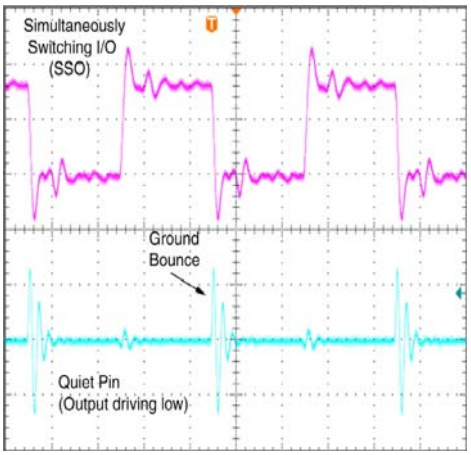



**The PWR/GND pins are no longer despicable in comparison to the I/Os**



# Ground Bounce

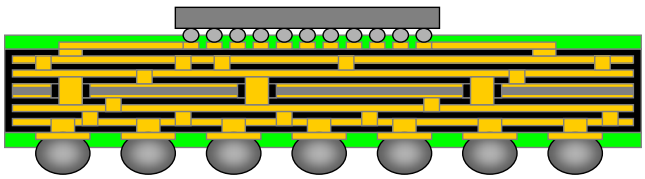



- When many I/O simultaneously switch from 1 to 0, a sudden current surge goes through the GND leads parasitic inductance, causing the chip ground to "bounce"
- A similar phenomenon happens to Vcc, "Vcc Sag", but historically has been less worrying because the increased voltage margin for ones (in 5V TTL, '0' goes from 0 to 0.8 volts, but a '1' is anything between 2.0 and 5.0 volts)

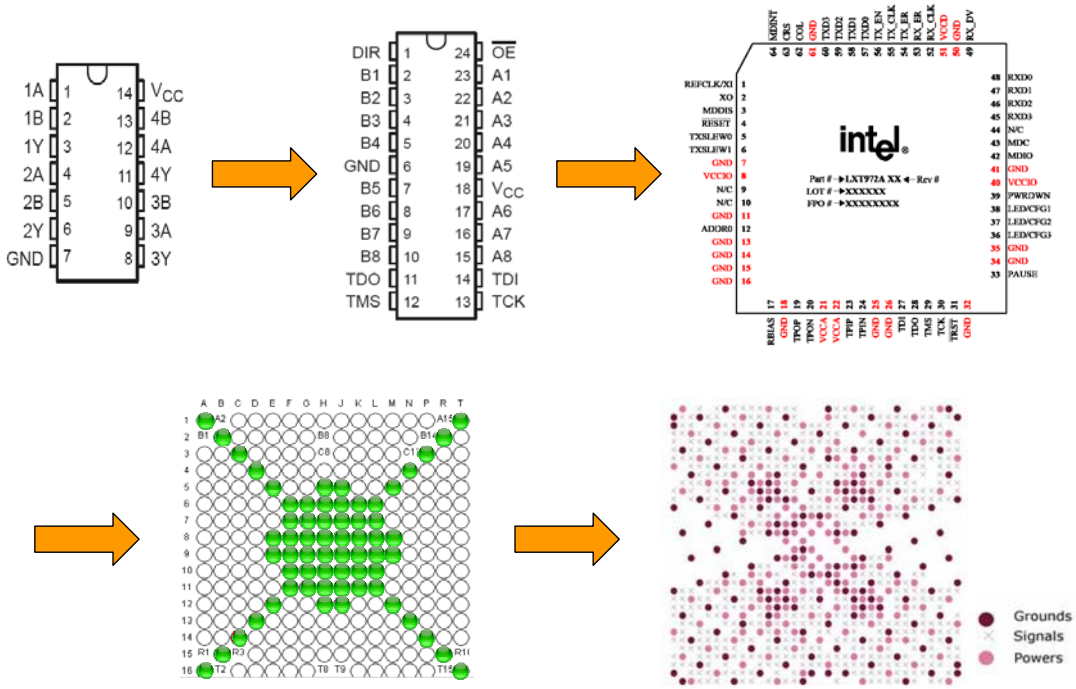
# Power/Ground Count

- There are many reasons for the recent increase in the number of PWR/GND pins
  - To reduce the parasitic resistance so that the power consumption requirements of the IC are fulfilled (several Amps)
  - To reduce the parasitic inductance in order to eliminate the ground bounce and Vcc sag problems
  - To ensure that there is a ground pin close to each I/O pin so that the ground loops are minimized and so the crosstalk
- High-end devices, at the package level, currently have a 8-1-1 I/O-Power-Ground relationship
  - Using flip-chip, the number of PWR/GND pairs at chip level is much higher, because there are many bumps connected to the power and ground planes created in the package substrate





# Evolution in Power/Ground Layout



# Manufacturability

- PCB requirements
  - Minimum size of the tracks and pads
  - Pin pitch: The higher, the easiest
  - For the same number of I/Os, BGAs have much higher pitches
- Solderability
  - BGAs self-alignment versus conventional SMD “self-misalignment”
- Handling precautions
  - Plastic packages tend to absorb moisture that may cause the package to crack during soldering
- Bottom line: Always keep in contact to your PCB manufacturing and mounting partner

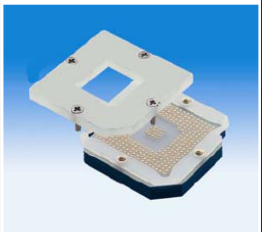
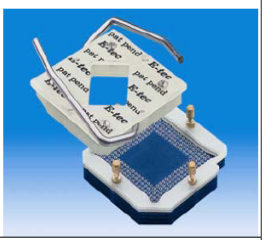
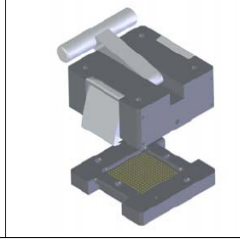
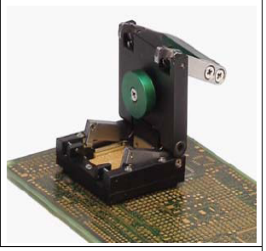
BGA256 vs QFP160



# Testability

- While BGAs are good in almost every field
  - Electrical and thermal performance
  - Solderability
- Their verification capabilities are very poor
  - No access to I/O signals, no way to view the pads to assess the quality of the soldering
  - Automated verification approaches are needed
  - X-Ray inspection may also be needed to ensure the quality of the soldering process, or special optic-fiber cameras
- Fine-pitch + BGAs = Is prototyping over?
  - Fortunately, there are companies who build sockets for almost everything

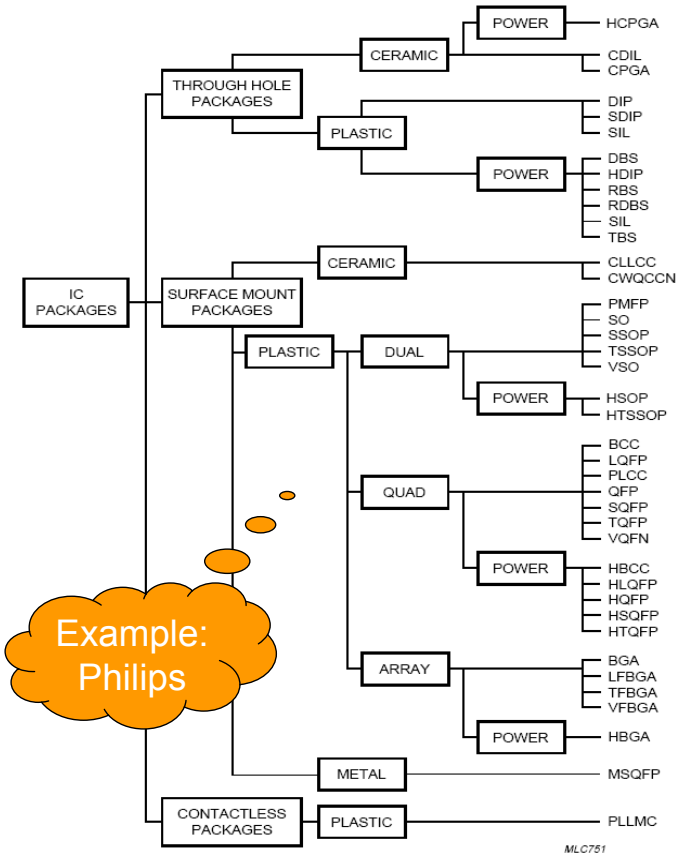
# Example: Emulation Technology

| "Knob lock" for multiple insertions and extractions of chips, for example in test and burn-in | "Screw lock" for prototypes and pre-production | "ZIF (lever) lock" for pre-production and volume productions |
|---|---|---|
| |  |  |
| "Quick lock" for test purposes (socket up to 80 pins) | "Quick lock" for test purposes (socket as of 81 pins) | "Grip lock" for test purposes |
| |  |  |
| Other socket styles: Please contact ET's for other socket styles or custom specials | | |



# Reliability

- Plastic packages are best suited for controlled environments
  - For example, low moisture and applications not requiring long-term storage or extreme temperature cycling
- Ceramic packages offer the best performance in terms of thermal characteristics, moisture absorption and endurance in harsh environments
  - Moisture permeability is orders of magnitude better than in plastics
  - Moisture is the most important cause of corrosion
- Qualification tests impart varying extent of stresses on the packages
  - The purpose is to accelerate any potential failure mechanism, which may occur during actual operation
  - Temperature cycling, high-pressure and high moisture, etc…
  - The manufacturer provides reliability data based on these tests
- Fabrication process certification
  - QML, MIL-PRF-38535



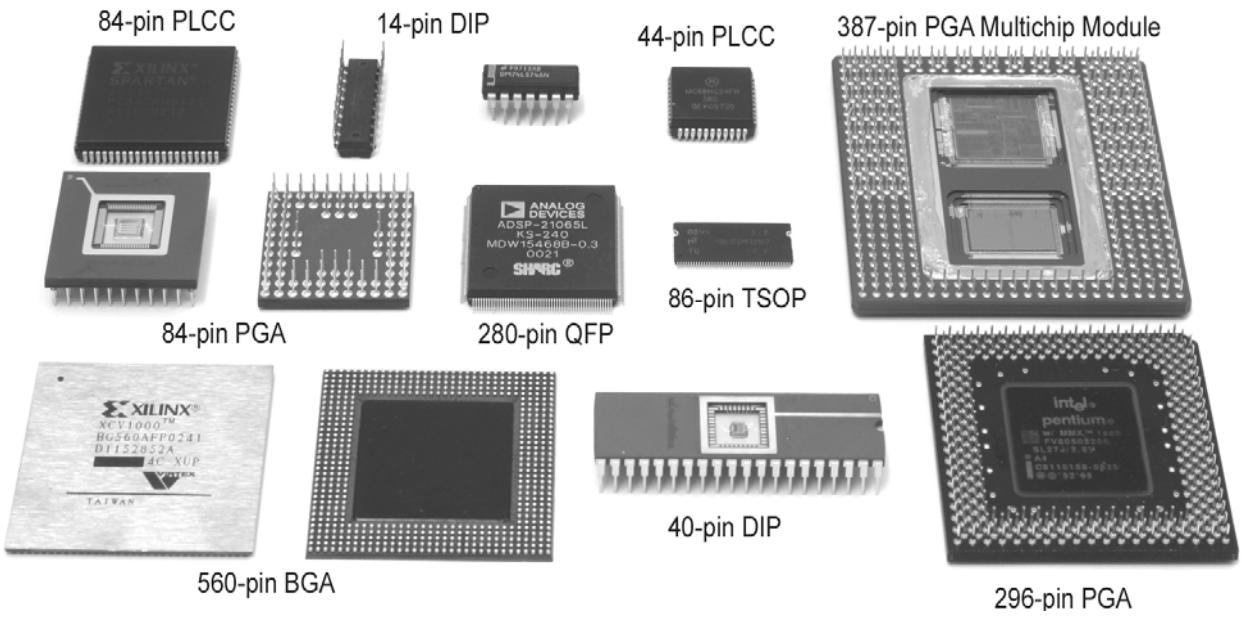

Example: Philips

# Package Types

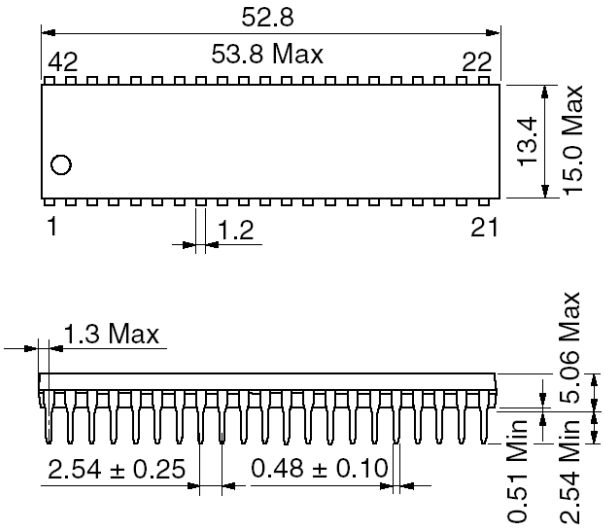
- The basic types are shared among manufacturers
- But each manufacturer has its own nomenclature for the variants
  - Acronym salad
- Fundamental types for ICs
  - DIP, PGA
  - CLCC
  - SOP, PLCC, QFP
  - BGA
- Specific types for discrete and passive components

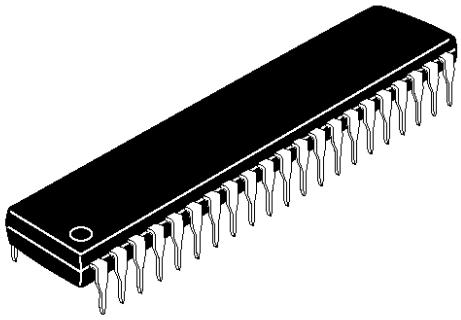


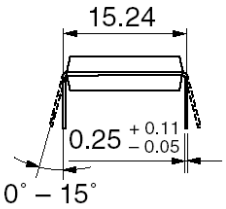
# Example of IC Packages



# DIP: Dual In-Line Package

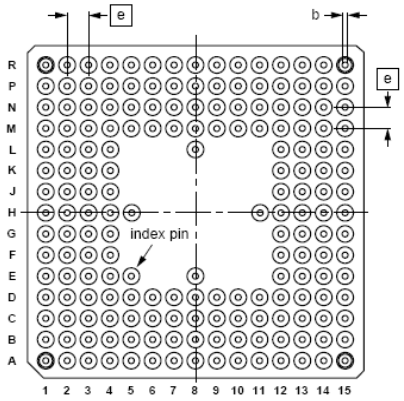


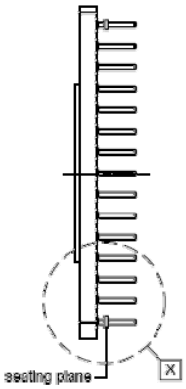







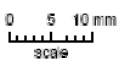

# PGA: Pin Grid Array



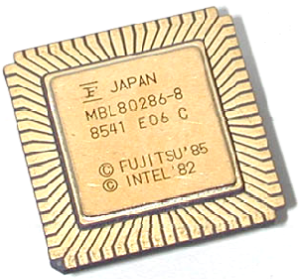



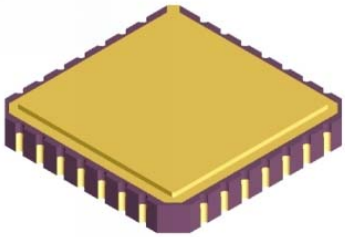

DIMENSIONS (mm dimensions are derived from the original inch dimensions)

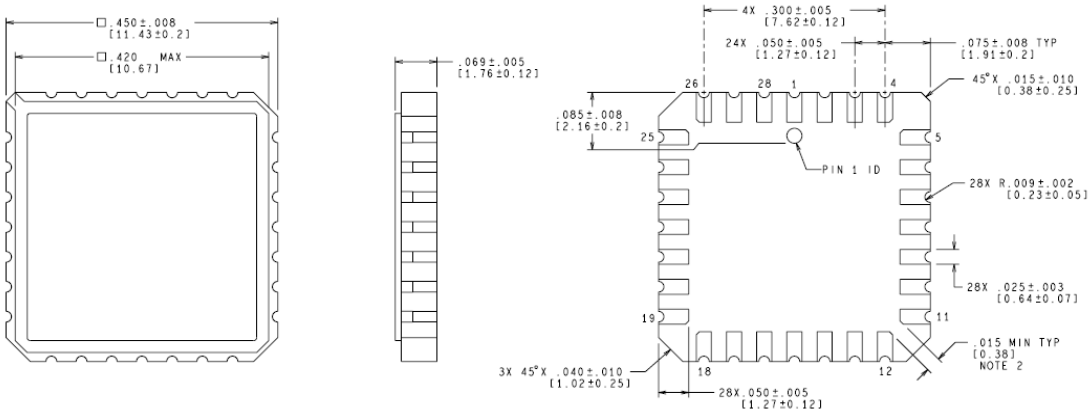
| UNIT | $A_1$ | $A_2$ | b | D | $D_1$ | E | $E_1$ | e | L |
|---|---|---|---|---|---|---|---|---|---|
| mm | 1.40<br>1.14 | 3.23<br>2.59 | 0.51<br>0.41 | 40.41<br>39.60 | 21.34<br>19.05 | 40.41<br>39.60 | 21.34<br>19.05 | 2.54 | 3.43<br>3.17 |



# CLCC: Ceramic LeadLess Chip Carrier

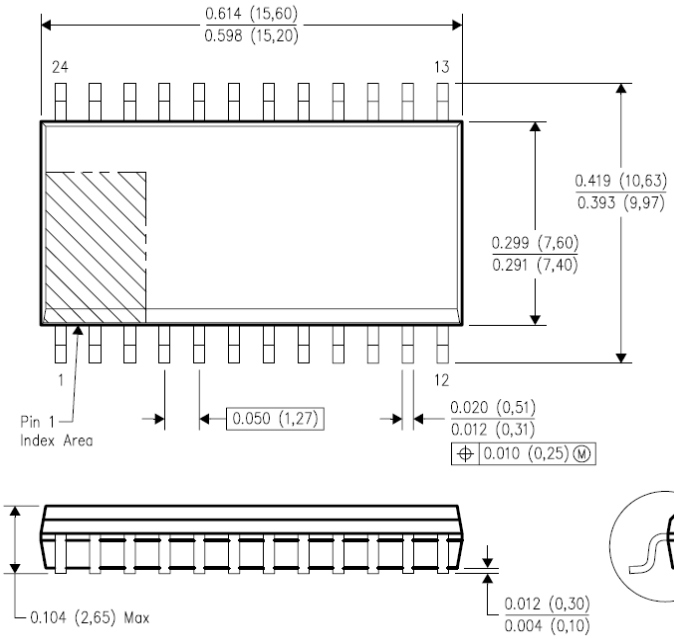


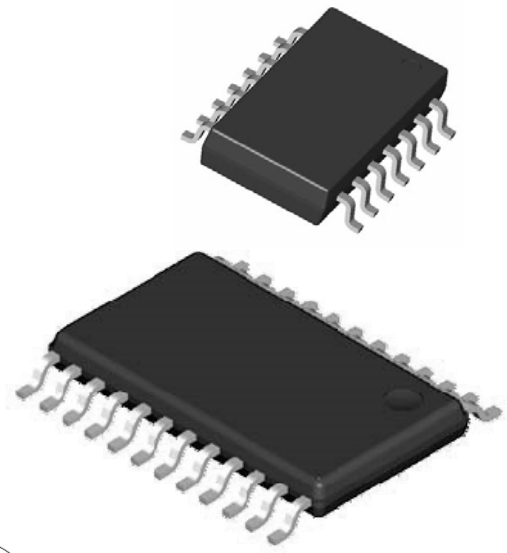





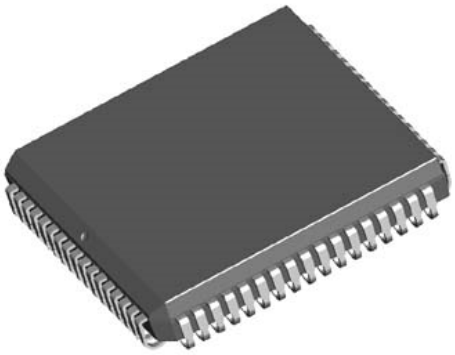


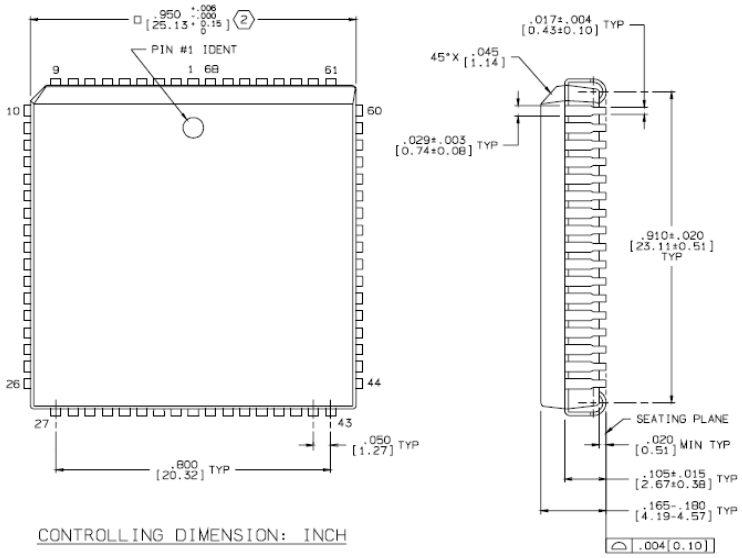

# SOP: Small Outline Package



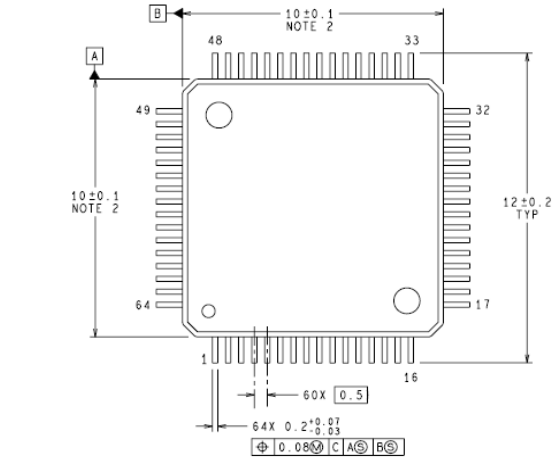
# PLCC: Plastic Leadless Chip Carrier

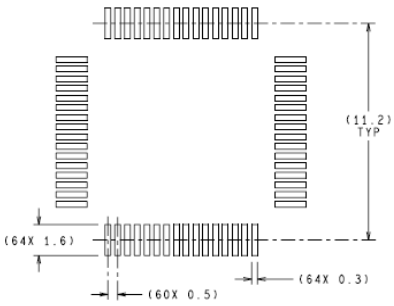




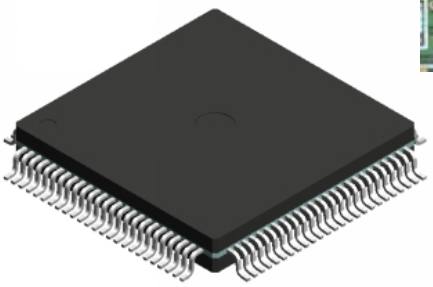



# QFP: Quad Flat Pack

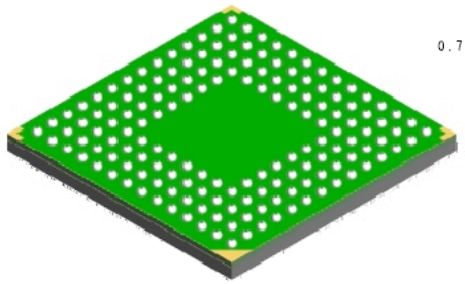


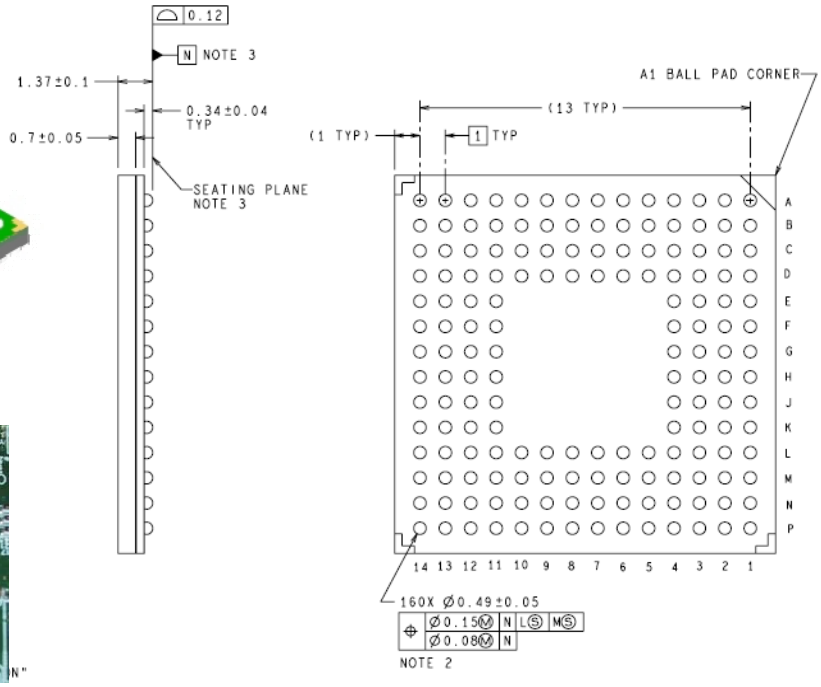



LAND PATTERN RECOMMENDATION



# BGA: Ball Grid Array



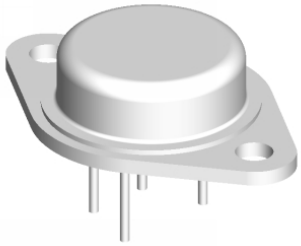





# Reduced Pin Count Devices

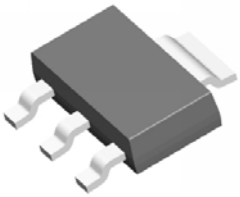
TO-92

TO-220



TO-3

SOT-23 (TO-236)



SOT-223 (TO-261)

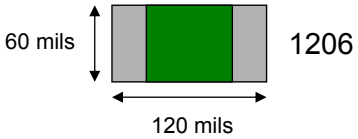
TO-263

# Passive Components

- Through hole
  - Axial

  - Radial

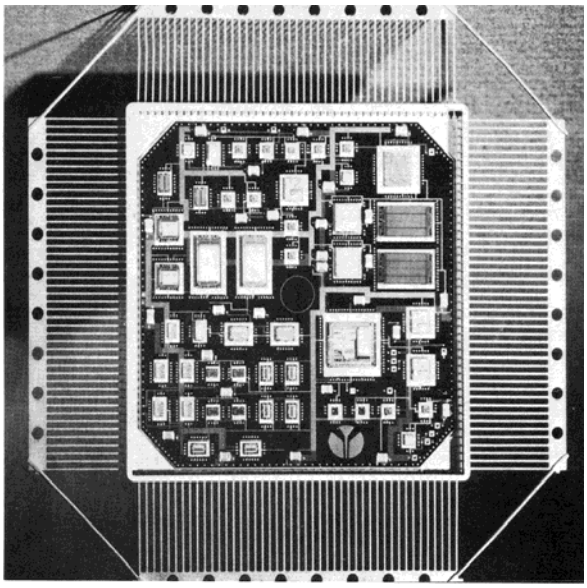
- Surface Mount (SMD)
  - 1206, 0805, 0603, 0402 (in x 100)



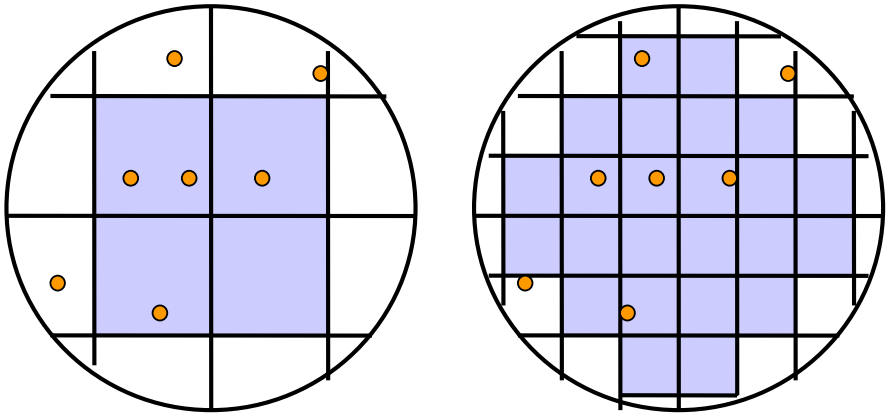
  - Case A: 3216, Case B: 3528, Case C: 6032 (mm x 10)

# Advanced Packaging: Multi-Chip-Modules (MCMs)

- Increase integration level of system (smaller size)
- Decrease loading of external signals: Higher performance
- No packaging of individual chips
- Problems with known good die:
  - Single chip fault coverage: 95%
  - MCM yield with 10 chips: $(0.95)^{10} = 60\%$
- Problems with cooling
- Expensive



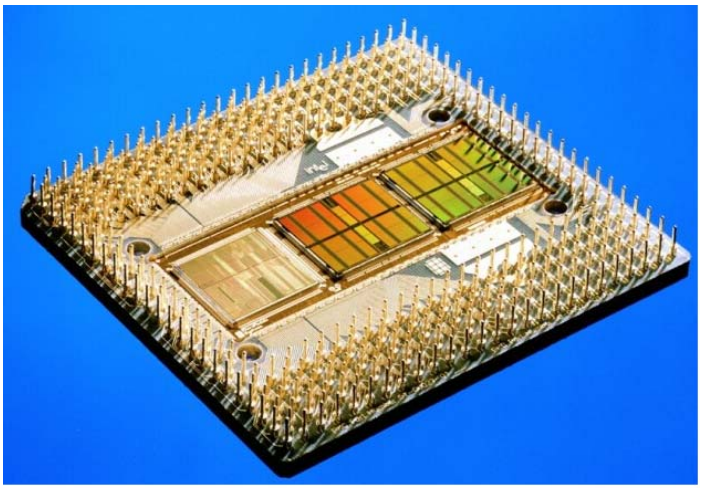
# Yield



die cost is $f$(die area)$^4$

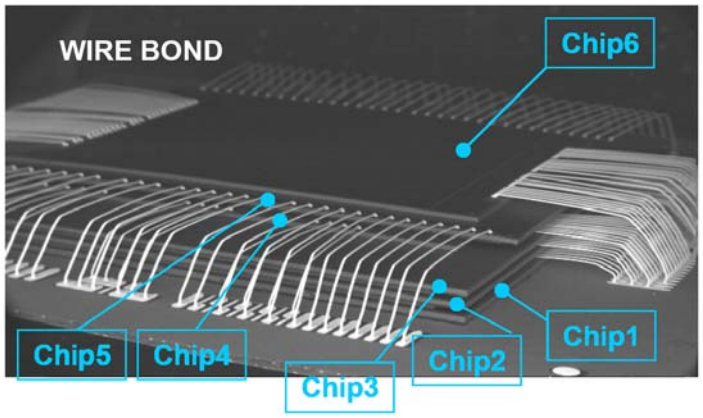


# Pentium Pro: Example of Commercial MCM

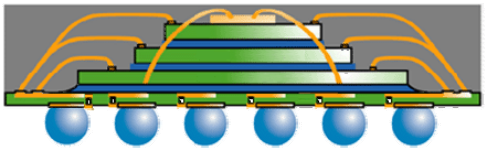


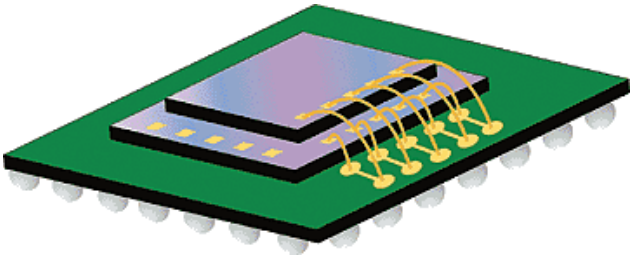
CPU plus separated, on-package, level-2 caches

# Chip Stacked Packages



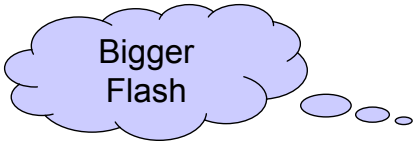

- Currently based on wire bonding, but there is research on flip-chip
- Used for example in memory devices for mobile applications (Flash + SRAM)

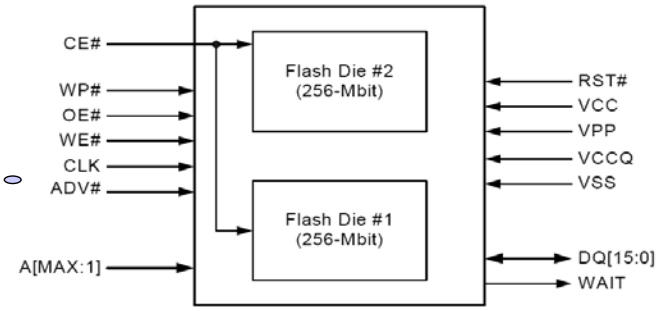


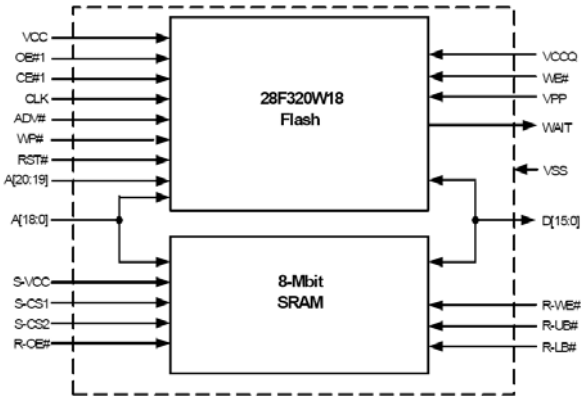


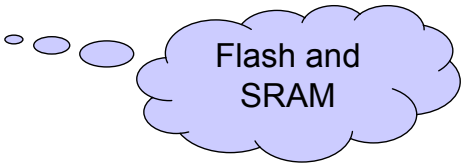


# Examples of Chip Stacked Packages: Intel

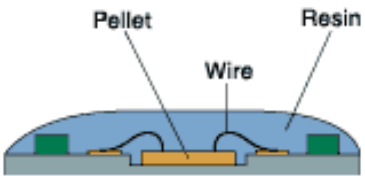


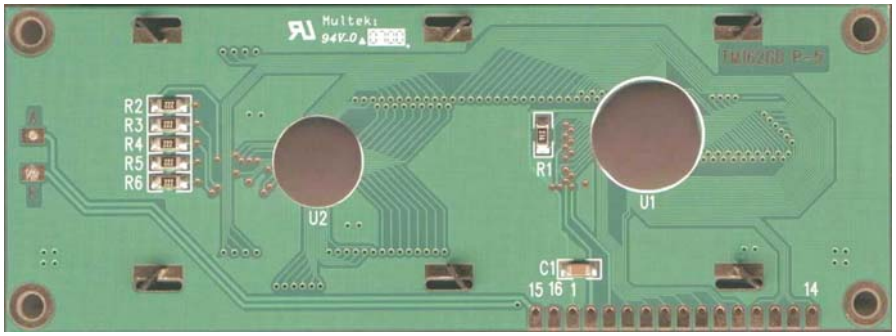



# But Are Packages Really Necessary? Chip-On-Board Mounting (COB)




- Chips are directly mounted over the PCB, using a wire bonding technique very similar to the one used in packaging
- Drawbacks
  - Obtaining Known-Good-Dies (KGD)
  - Component Storage






# Sources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- Renesas Semiconductor Assembly Service
- Frear, Materials Issues in Area-Array Microelectronic Packaging
- Harris & Bushnell, Packages and Power, Rutgers University
- The Nordic Electronics Packaging Guideline
- Brown, Advanced Electronic Packaging: With Emphasis on MCMs

- Additional sources for Images: Xilinx, IBM, Bill Bertram (Wikipedia), Farnell, John Fader (Wikipedia), Philips, Maxim, Intel, Fraunhofer Institute, SMART Group, Hochschule Heilbronn, DRS Test & Energy Management, cpu-world.com, hardwarezone.com, Amkor, TI, coolingzone.com, NASA Office of Logic Design, Altera, Fairchild, Emulation Technology, National Semiconductor, OKI Semiconductor, ASE Malaysia, Pro Systems China, Toshiba