Electronics

Bipolar Junction Transistors

Chapter 3- Bipolar Junction Transistors (BJT)

On December 23, 1947, however, the electronics industry was to experience the advent of a completely new direction of interest and development. It was on the afternoon of this day that Dr. S. William Shockley, Walter H. Brattain, and John Bardeen demonstrated the amplifying action of the first transistor at the Bell Telephone Laboratories. The advantages of this three-terminal solid-state device were immediately obvious:

(a) It was smaller and lightweight;
(b) It had no heater requirement or heater loss;
(c) It had a rugged construction;
(d) It was more efficient since less power was absorbed by the device itself; and lower operating voltages were possible.

The transistor is a three-layer semiconductor device consisting of either two n - and one p -type layers of material or two p and one n type layers of material. The former is called an npn transistor, and the latter is called a pnp transistor. Both are shown in Fig.3.1 with the proper dc biasing. The dc biasing is necessary to establish the proper region of operation for ac amplification. The emitter layer is heavily doped, with the base and collector only lightly doped. The lower doping levels decrease the conductivity (increase the resistance) of this material by limiting the number of "free" carriers. For the biasing shown in Fig.3.1 the terminals have been indicated by the capital letters E for emitter , C for collector , and B for base. The abbreviation BJT, from bipolar junction transistor is often applied to this three-terminal device. The term bipolar reflects the fact that holes and electrons participate in the injection process into the oppositely polarized material. If only one carrier is employed (electron or hole), it is considered a unipolar device.

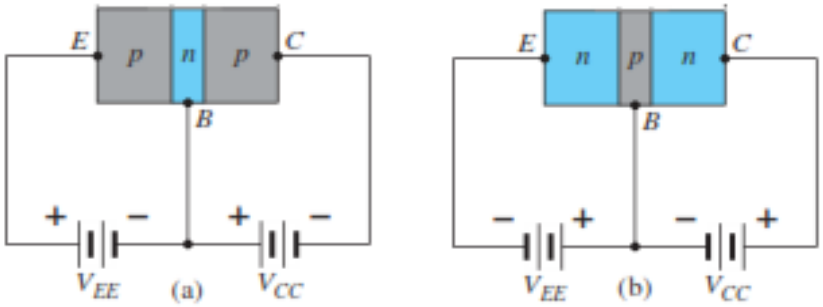


FIG. 3.1: Types of transistors: (a) pnp; (b) npn

Transistor Operation

The basic operation of the transistor will now be described using the pnp transistor of Fig. 3.1a. The operation of the npn transistor is exactly the same if the roles played by the electron and hole are interchanged. In Fig. 3.2(a) the pnp transistor has been redrawn without the base to collector bias. Note the similarities between this situation and that of the forward-biased diode in Chapter2. The

depletion region has been reduced in width due to the applied bias, resulting in a heavy flow of majority carriers from the p to the n type material.

Let us now remove the base-to-emitter bias of the pnp transistor of Fig. 3.1(a) as shown in Fig. 3.2(b). Consider the similarities between this situation and that of the reverse-biased diode. Recall that the flow of majority carriers is zero, resulting in only a minority-carrier flow, as indicated in Fig. 3.2(b). In summary, therefore: **One p–n junction of a transistor is reverse-biased, whereas the other is forward-biased.**

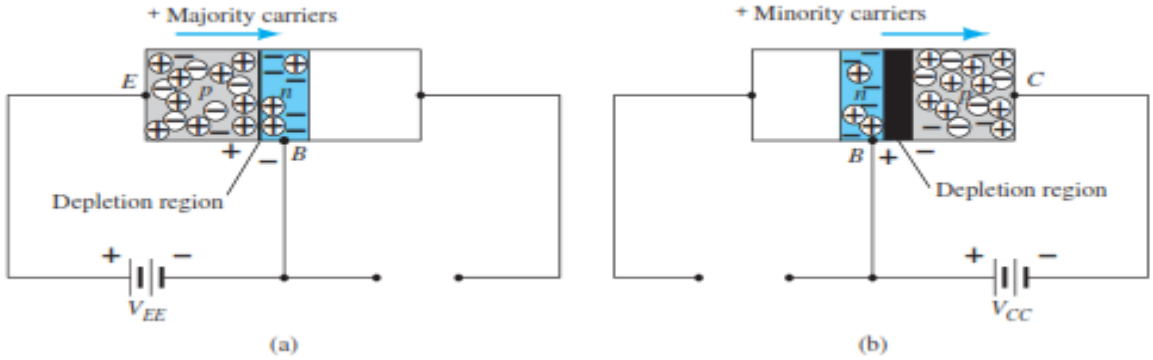


FIG. 3.2: Biasing a transistor: (a) forward-bias; (b) reverse-bias.

In Fig. 3.3 both biasing potentials have been applied to a pnp transistor, with the resulting majority- and minority-carrier flows indicated. Note in Fig. 3.3, the widths of the depletion regions, indicating clearly which junction is forward-biased and which is reverse-biased. As indicated in Fig. 3.3, a large number of majority carriers will diffuse across the forward biased p–n junction into the n-type material. The question then is whether these carriers will contribute directly to the base current I or pass directly into the p -type material. Since the sandwiched n -type material is very thin and has a low conductivity a very small number of these carriers will take this path of high resistance to the base terminal. The magnitude of the base current is typically on the order of microamperes, as compared to mille amperes for the emitter and collector currents. The larger number of these majority carriers will diffuse across the reverse-biased junction into the p -type material connected to the collector terminal as indicated in Fig. 3.2.

The reason for the relative ease with which the majority carriers can cross the reverse-biased junction is easily understood if we consider that for the reverse-biased diode the injected majority carriers will appear as minority carriers in the n type material. In other words, there has been an injection of minority carriers into the n-type base region material. Combining this with the fact that all the minority carriers in the depletion region will cross the reverse-biased junction of a diode accounts for the flow indicated in Fig 3. 2.

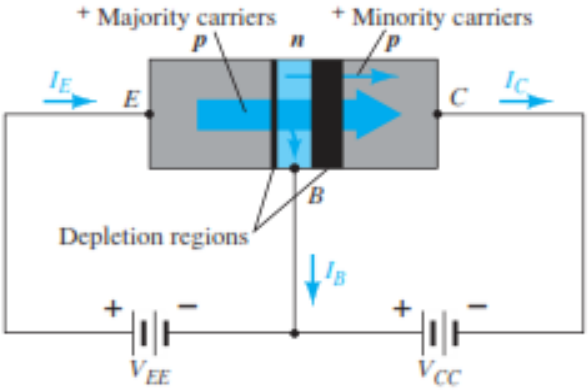


FIG. 3.2: Majority and minority carrier flow of a pnp transistor.

Applying Kirchhoff's current law to the transistor of Fig.3.2 as if it were a single node, we obtain: $\mathbf{I_E = I_C + I_B}$, and find that the emitter current is the sum of the collector and base currents. The collector current, however, comprises two components, the majority and the minority carriers as indicated in Fig. 3.2. The minority current component is called the leakage current and is given the symbol I_{CO} (I_C current with emitter terminal Open). The collector current, therefore, is determined in total by:

$\mathbf{IC = I_{C\ majority} + I_{CO\ minority}}$

For general-purpose transistors, I_C is measured in milliamperes and I_{CO} is measured in microamperes or Nano amperes. I_{CO}, like I_s for a reverse-biased diode, is temperature sensitive and must be examined carefully when applications of wide temperature ranges are considered. It can severely affect the stability of a system at high temperature if not considered properly. Improvements in construction techniques have resulted in significantly lower levels of I_{CO}, to the point where its effect can often be ignored.

Common-Base Configuration

The common-base terminology is derived from the fact that the base is common to both the input and output sides of the configuration as shown in figure 3.3. In addition, the base is usually the terminal closest to, or at, ground potential. Throughout this text all current directions will refer to conventional (hole) flow rather than electron flow. The result is that the arrows in all electronic symbols have a direction defined by this convention. **The arrow in the graphic symbol defines the direction of emitter current (conventional flow) through the device.**

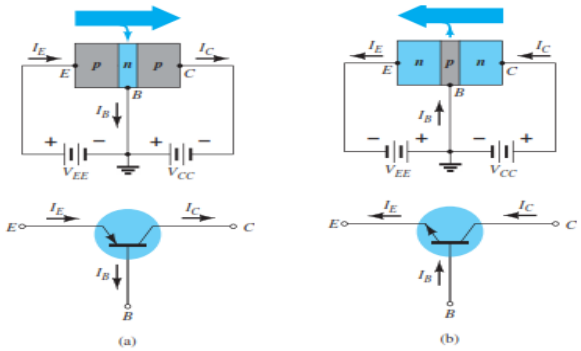


FIG. 3.3: Notation and symbols used with the common-base configuration: (a) pnp transistor; (b) npn transistor.

To fully describe the behavior of a three-terminal device such as the common-base (CB) amplifiers requires two sets of characteristics one for the driving point or input parameters and the other for the output side. The input set for the common-base amplifier as shown in Fig. 3.4 relates an input current (I_E) to an input voltage (V_{BE}) for various levels of output voltage (V_{CB}).

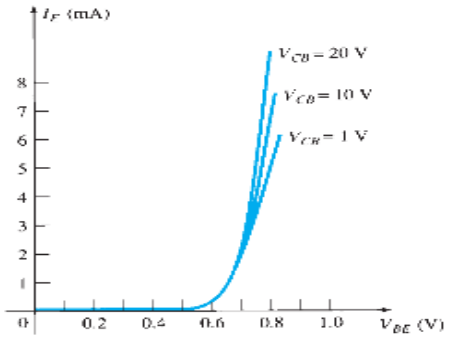


FIG. 3.4: Input or driving point characteristics for a common-base silicon transistor amplifier.

The output set relates an output current (I_C) to an output voltage (V_{BE}) for various levels of input current (I_E) as shown in Fig. 3.5. The output or collector set of characteristics has three basic regions of interest, as indicated in Fig. 3.5: the active, cutoff, and saturation regions.

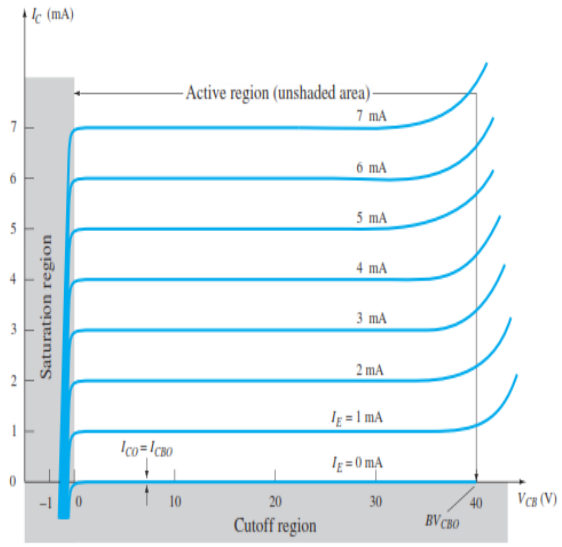


FIG. 3.5: Output or collector characteristics for a common-base transistor amplifier.

The active region is the region normally employed for linear (undistorted) amplifiers. In particular: **In the active region the base–emitter junction is forward-biased, whereas the collector–base junction is reverse-biased.**

The active region is defined by the biasing arrangements given before. At the lower end of the active region the emitter current (I_E) is zero, and the collector current is simply that due to the reverse saturation current I_{CbO}, as indicated in Fig. 3.6. The current I_{CBO} is so small (microamperes) in magnitude compared to the vertical scale of I_C (milliamperes) that it appears on virtually the same horizontal line as: $I_C = 0$. The circuit conditions that exist when $I_E = 0$ for the common-base configuration are shown in Fig. 3.6.

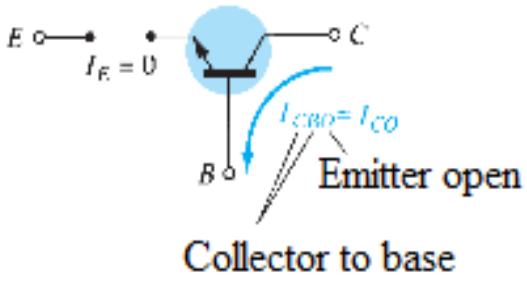


FIG. 3.6: Reverse saturation current.

The notation most frequently used for I_{CBO} on data and specification sheets is, as indicated in Fig.3.6, I_{CBO} (Collector to base current with the emitter leg is open). The level of I_{CBO} for general purpose transistors in the low and mid power ranges is usually so low, that its effect can be ignored, keep in mind that I_{CBO}, like I_s, for the diode (both reverse leakage currents) is temperature sensitive. At higher temperatures the effect of I_{CBO} may become an important factor since it increases so rapidly with temperature. Note in Fig. 3.5 that as the emitter current increases above zero, the collector current increases to a magnitude essentially equal to that of the emitter current as determined by the basic transistor-current relations. Note also the almost negligible effect of V_{CB} on the collector current for the active region. The curves clearly indicate that a first approximation to the relationship between I_E and I_C in the active region is given by:

$$\mathbf{I_C = I_E}$$

As inferred by its name, the **cutoff region** is defined as that region where the collector current is 0 A, as revealed on Fig. 3.6. In addition: **In the cutoff region the base–emitter and collector–base junctions of a transistor are both reverse-biased.**

The saturation region is defined as that region of the characteristics to the left of V_{CB}= 0V.The horizontal scale in this region was expanded to clearly show the dramatic change in characteristics in this region. Note the exponential increase in collector current as the voltage V_{CB} increases toward 0V. **In the saturation region the base–emitter and collector–base junctions are forward-biased.** The input characteristics of Fig. 3.5 reveal that the change due to changes in V_{CB} can be ignored and the characteristics drawn as shown in Fig. 3.7. For the analysis to follow the equivalent model, that is, once a transistor is in the "on" state, the base-to-emitter voltage will be assumed to be the following**: V_{BE} = 0.7 V.**

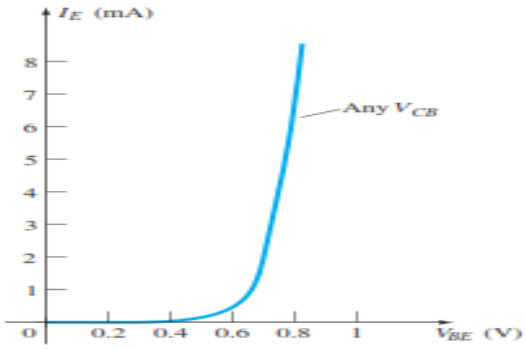


FIG. 3.7: The equivalent model to be employed for the base-to-emitter region of an amplifier in the dc mode.

Alpha (α): DC Mode: In the dc mode the levels of I_C and I_E due to the majority carriers are related by a quantity called alpha (α) and defined by the following equation:

$\alpha_{dc} = I_C/I_E$ where I_C and I_E are the levels of current at the point of operation. Even though the characteristics given before would suggest that α= 1, for practical devices alpha typically extends from 0.90 to 0.998, with most values approaching the high end of the range. Since alpha is defined solely for the majority carriers, thus:

$I_C = \alpha I_E + I_{CBO}$

When I_E = 0mA, I_C is therefore equal to I_{CBO}, but as mentioned earlier, the level of I_{CBO} is usually very small, that when I_E= 0 mA, I_C also appears to be 0 mA.

AC Mode: For ac situations where the point of operation moves on the characteristic curve, an ac alpha is defined by:

$$\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=\text{constant}}$$

The ac alpha is formally called the common base, short circuit, amplification factor, specifies that a relatively small change in collector current is divided by the corresponding change in emitter current with the collector to base voltage held constant. For most situations the magnitudes of α_{ac} and α_{dc} are quite close, permitting the use of the magnitude of one for the other.

Biasing

The proper biasing of the common-base configuration in the active region can be determined quickly using the approximation: $I_C \approx I_E$ and assuming for the moment that $I_B \approx 0\mu A$. The result is the configuration of Fig. 3.8 for the pnp transistor. The arrow of the symbol defines the direction of conventional flow for $I_C \approx I_E$. The dc supplies are then inserted with a polarity that will support the resulting current direction. For the npn transistor the polarities will be reversed.

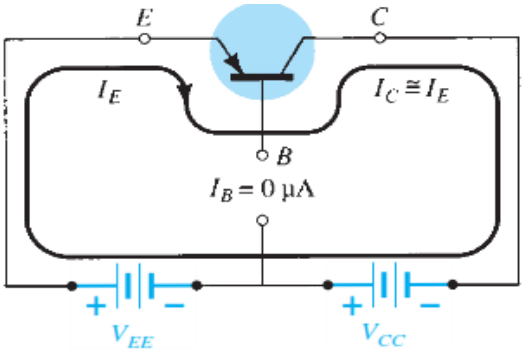


FIG. 3.8: The proper biasing for a common base pnp transistor in the active region.

Breakdown Region:

As the applied voltage V_{CB} increases there is a point where the curves take a dramatic upswing in Fig. 3.5. This is due primarily to an avalanche effect similar to that described for the diode, when the reverse-bias voltage reached the breakdown region. As stated earlier the base-to-collector junction is reversed biased in the active region, but there is a point where too large a reverse-bias voltage will lead to the avalanche effect. The result is a large increase in current for small increases in the base-to-collector voltage. The largest permissible base-to-collector voltage is labeled BV_{CBO} as shown in Fig. 3.5. It is

also referred to as $V_{(BR)CBO}$. Note in each of the above notations the use of the uppercase letter O to represent that the emitter leg is in the open state (not connected). It is important to remember when taking note of this data point that this limitation is only for the common-base configuration. You will find in the common-emitter configuration that this limiting voltage is quite a bit less.

Common-Emitter Configuration

The most frequently encountered transistor configuration appears in Fig. 3.9 for the pnp and npn transistors. It is called the common-emitter configuration because the emitter is common to both the input and output terminals (in this case common to both the base and collector terminals). Two sets of characteristics are again necessary to describe fully the behavior of the common emitter configuration: one for the input or base emitter circuit and one for the output or collector emitter circuit. Both are shown in Fig. 3.9.

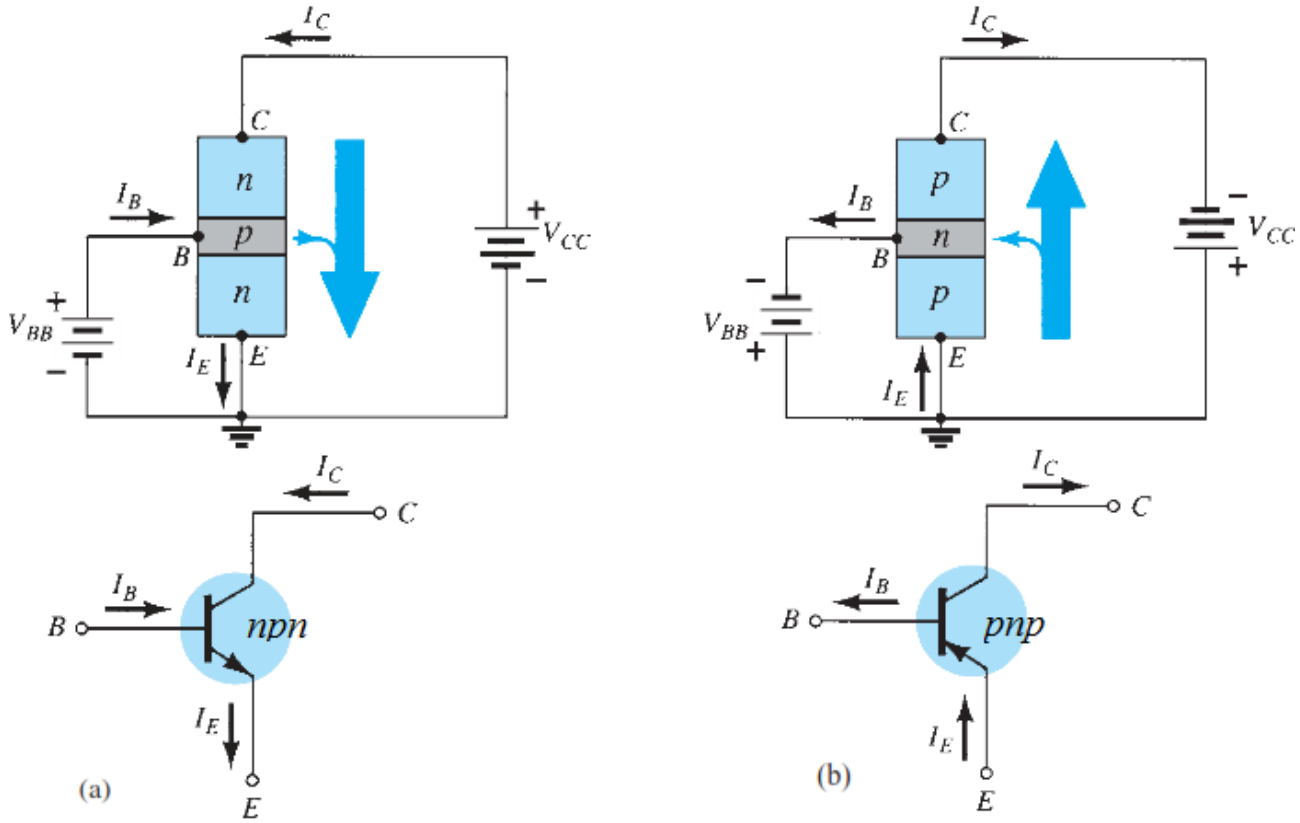


FIG. 3.9: Notation and symbols used with the common-emitter configuration: (a) npn transistor; (b) pnp transistor.

The emitter, collector, and base currents are shown in their actual conventional current direction. Even though the transistor configuration has changed, the current relations developed earlier for the common-base configuration are still applicable. For the common-emitter configuration the output characteristics are a plot of the output current (I_C) versus output voltage (V_{CE}) for a range of values of input current (I_B). The input characteristics are a plot of the input current (I_B) versus the input voltage (V_{BE}) for a range of values of output voltage (V_{CE})as shown in Fig 3.10. The curves of I_B are not as horizontal as those obtained for IE in the common-base configuration, indicating that the collector to emitter voltage will influence the magnitude of the collector current.

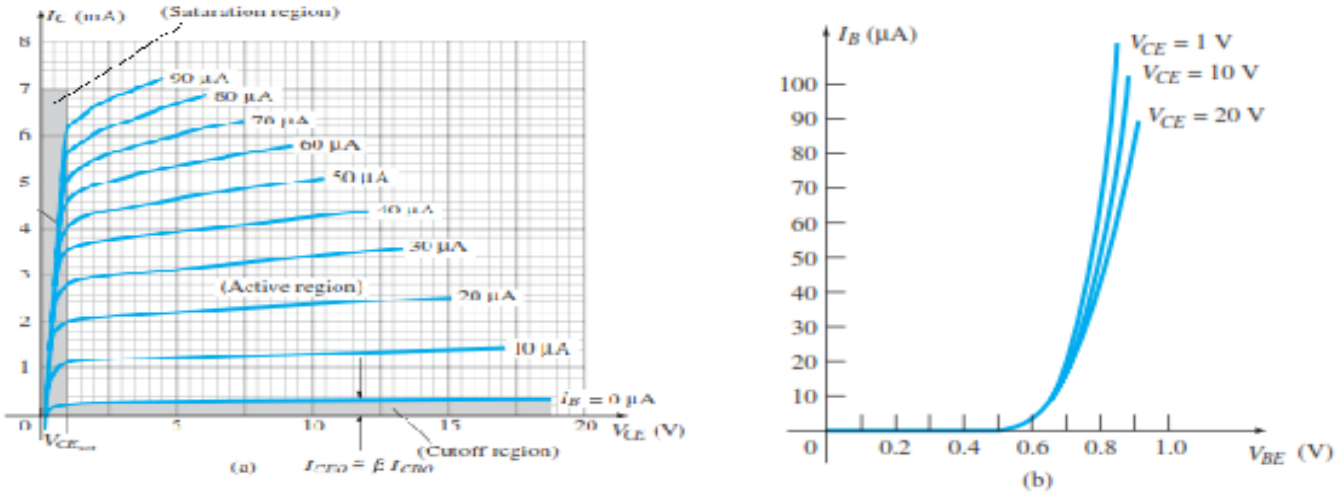


FIG. 3.10: Characteristics of a silicon transistor in the common-emitter configuration: (a) collector characteristics; (b) base characteristics.

The active region for the common-emitter configuration is that portion of the upper right quadrant that has the greatest linearity, that is, that region in which the curves for I_B are nearly straight and equally spaced. This region exists to the right of the vertical dashed line at V_{CEsat} and above the curve for I_B equal to zero. The region to the left of V_{CEsat} is called the saturation region. **In the active region of a common emitter amplifier, the base emitter junction is forward biased, whereas the collector base junction is reverse biased.** The active region of the common emitter configuration can be employed for voltage, current, or power amplification.

The cutoff region for the common emitter configuration is not as well defined as for the common-base configuration. Note on the collector characteristics of Fig. 3.10 that I_C is not equal to zero when I_B is zero. The reason for this difference in collector characteristics can be derived from:

$\mathbf{I_C = \alpha I_E + I_{CBO}}$

$\mathbf{I_C = \alpha (I_C + I_B) + I_{CBO}}$

$\mathbf{I_C = [\alpha I_B/1 - \alpha] + [I_{CBO}/ 1 - \alpha]}$

For future reference, the collector current defined by the condition $I_B = 0$ μA will be assigned the notation indicated by the following equation:

$$I_{CEO} = \left.\frac{I_{CBO}}{1 - \alpha}\right|_{I_B = 0\,\mu A}$$

In Fig. 3.10, the conditions surrounding this newly defined current are demonstrated with its assigned reference direction. **For linear (least distortion) amplification purposes, cutoff for the common-emitter configuration will be defined by** $I_C = I_{CEO}$.

Beta (β)

DC Mode: In the dc mode the levels of I_C and I_B are related by a quantity called beta and defined by the following equation: $\mathbf{\beta_{dc} = I_C/I_B}$, where I_C and I_B are determined at a particular operating point on the characteristics. For practical devices the level of β typically ranges from about 50 to over 400, with most in the midrange. As for α, the parameter β reveals the relative magnitude of one current with respect to the other. For a device with a β of 200, the collector current is 200 times the magnitude of the base current.

AC Mode: For ac situations an ac beta is defined as follows:

$\beta_{ac} = \Delta I_C / \Delta I_B \mid V_{CE=constant}$.

The formal name for βac is common-emitter, forward-current amplification factor. A relationship can be developed between β and α using the basic relationships introduced thus far. Using

$I_B = I_C/\beta$, $I_E = I_C/\alpha$ an $I_E = I_C + I_B$, we have:

$I_C/\alpha = I_C + I_C/\beta$ so that:

$$\alpha = \frac{\beta}{\beta + 1}$$ and $$\beta = \frac{\alpha}{1 - \alpha}$$ and $$I_E = (\beta + 1)I_B$$

Biasing

The proper biasing of a common-emitter amplifier can be determined in a manner similar to that introduced for the common-base configuration. Let us assume that we are presented with an npn transistor. The first step is to indicate the direction of I_E as established by the arrow in the transistor symbol. Next, the other currents are introduced, keeping in mind Kirchhoff's current law relationship: $I_C + I_B = I_E$.

That is, both I_C and I_B must enter the transistor structure. Finally, the supplies are introduced with polarities that will support the resulting directions of I_B in Fig. 3.11 to complete the picture. The same approach can be applied to pnp transistors. If the transistor of Fig. 3.11 was a pnp transistor, all the currents and polarities would be reversed.

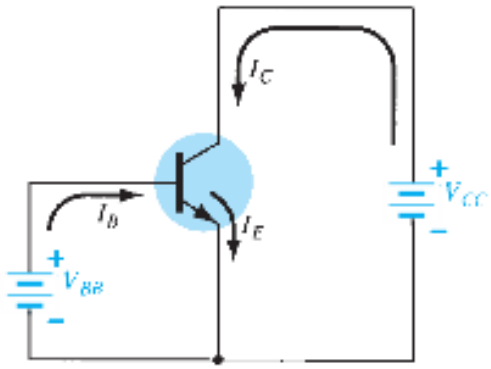


FIG. 3.11: Determining the proper biasing arrangement for a common-emitter npn transistor configuration.

Common-Collector Configuration

The third and final transistor configuration is the common-collector configuration, shown in Fig. 3.12 (a). The proper current directions and voltage notation is given in (b). The common-collector configuration is used primarily for impedance-matching purposes since it has a high input impedance and low output impedance, opposite to that of the common-base and common emitter configurations. A common-collector circuit configuration is provided in Fig. 3.12 (c) with the load resistor connected from emitter to ground. Note that the collector is tied to ground even though the transistor is connected in a manner similar to the common-emitter configuration. For all practical purposes, the output characteristics of the common-collector configuration are the same as for the common-emitter configuration. For the common-collector configuration the output characteristics are a plot of I_E versus V_{CE} for a range of values of I_B. The input current, therefore, is the same for both the common emitter and common-collector characteristics. The horizontal voltage axis for the common collector configuration is obtained by simply changing the sign of the collector to emitter voltage of the common-emitter characteristics. Finally, there is an almost unnoticeable change in

the vertical scale of I_C of the common-emitter characteristics if I_E is replaced by I_C for the common-collector characteristics (since $\alpha \sim 1$). For the input circuit of the common-collector configuration the common-emitter base characteristics are sufficient for obtaining the required information.

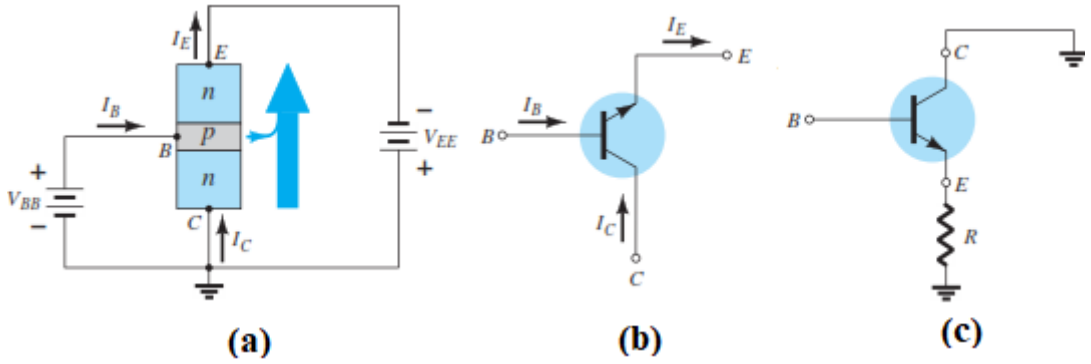


FIG. 3.12: (a) Notation and symbols used with the common-collector configuration, transistor; (b) npn transistor. (c) Common-collector configuration used for impedance matching purposes.

Analysis or design of a transistor amplifier

The analysis or design of a transistor amplifier requires knowledge of both the dc and the ac response of the system. The transistor can raise the level of the applied ac input without the assistance of an external energy source. In actuality, **any increase in ac voltage, current, or power is the result of a transfer of energy from the applied dc supplies.**

The analysis or design of any electronic amplifier therefore has two components: a dc and an ac portion. However, one must keep in mind that during the design or synthesis stage the choice of parameters for the required dc levels will affect the ac response, and vice versa. The dc level of operation of a transistor is controlled by a number of factors, including the range of possible operating points on the device characteristics. Once the desired dc current and voltage levels have been defined, a network must be constructed that will establish the desired operating point.

Use of the following important basic relationships for a transistor:

$V_{BE} \cong 0.7\,\text{V}$ $\quad I_E = (\beta + 1)I_B \cong I_C$ $\quad I_C = \beta I_B$

Operating Point

For transistor amplifiers the resulting dc current and voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal. Because the operating point is a fixed point on the characteristics, it is also called the quiescent point (abbreviated Q point). By definition quiescent means quiet, still, inactive. Fig. 3.13 shows a general output device characteristic with four operating points indicated. The biasing circuit can be designed to set the device operation at any of these points or others within the active region. The maximum ratings are indicated on the characteristics of Fig. 3.13, by a horizontal line for the maximum collector current I_{Cmax} and a vertical line at the maximum collector-to-emitter voltage V_{CEmax}. The maximum power constraint is defined by the curve P_{Cmax} in the same figure. At the lower end of the scales are the cutoff region, defined by $I_B \leq 0$ mA, and the saturation region, defined by $V_{CE} \leq V_{CEsat}$

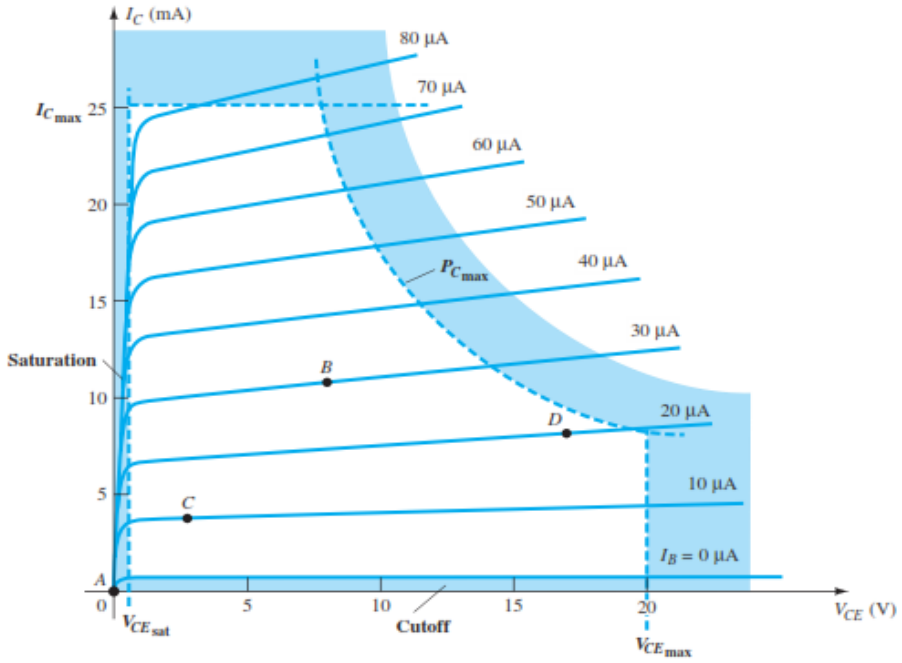


FIG. 3.13: Various operating points within the limits of operation of a transistor.

1. If no bias was used, the device would initially be completely off, resulting in a Q point at A namely, zero current through the device (and zero voltage across it). Because it is necessary to bias a device so that it can respond to the entire range of an input signal, point A would not be suitable.
2. For point B, if a signal is applied to the circuit, the device will vary in current and voltage from the operating point, allowing the device to react to (and possibly amplify) both the positive and negative excursions of the input signal. If the input signal is properly chosen, the voltage and current of the device will vary, but not enough to drive the device into cutoff or saturation.
3. Point C would allow some positive and negative variation of the output signal, but the peak-to-peak value would be limited by the proximity of V_{CE}= 0 V and I_C= 0 mA. Operating at point C also raises some concern about the nonlinearities introduced by the fact that the spacing between I_C curves is rapidly changing in this region.
4. Point D sets the device operating point near the maximum voltage and power level. The output voltage swing in the positive direction is thus limited if the maximum voltage is not to be exceeded.
5. In general, it is preferable to operate where the gain of the device is fairly constant (or linear) to ensure that the amplification over the entire swing of input signal is the same. Point B is a region of more linear spacing and therefore more linear operation, therefore seems the largest possible voltage and current swing.

Having selected and biased the BJT at a desired operating point, we must also take the effect of **temperature** into account. Temperature causes the device parameters such as the transistor current gain (β_{ac}) and the transistor leakage current (I_{CEO}) to change. Higher temperatures result in increased leakage currents in the device, thereby changing the operating condition set by the biasing network. The result is that the network design must also provide a degree of temperature stability so that temperature changes result in minimum changes in the operating point.

- **For the BJT to be biased in its linear or active operating region the following must be true:**

1. The base emitter junction must be forward-biased (p-region voltage more positive), with a resulting forward-bias voltage of about 0.6 V to 0.7 V.

2. The base collector junction must be reverse-biased (n-region more positive), with the reverse-bias voltage being any value within the maximum limits of the device.

- **For the Cutoff-region operation: Base emitter junction reverse-biased and Base collector junction reverse biased.**
- **For the Saturation region operation: Base emitter junction forward biased and Base collector junction forward biased.**

<u>Biasing Types</u>

First: Fixed-Bias Configuration

The fixed bias circuit of Fig. 3.14(a) is the simplest transistor dc bias configuration. Even though the network employs an npn transistor, the equations and calculations apply equally well to a pnp transistor configuration merely by changing all current directions and voltage polarities. The current directions of Fig. 3.14(a) are the actual current directions, and the voltages are defined by the standard double-subscript notation. For the dc analysis the network can be isolated from the indicated ac levels by replacing the capacitors with an open-circuit equivalent because the reactance of a capacitor is a function of the applied frequency.

For dc, f = 0 Hz, and $X_C = 1/2\pi fC = 1/2\pi\ (0)\ C = \infty\ \Omega$.

In addition, the dc supply V_{CC} can be separated into two supplies (for analysis purposes only) as shown in Fig. 3.14(b) to permit a separation of input and output circuits. It also reduces the linkage between the two to the base current I_B

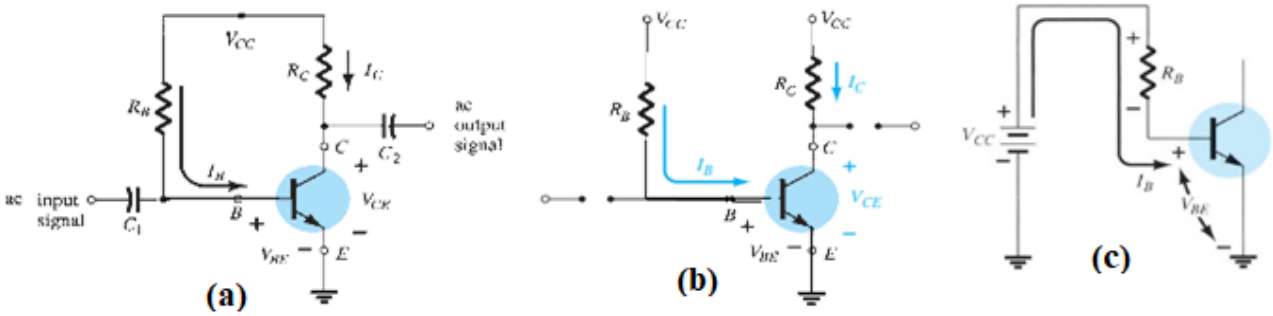


FIG. 3.14(a): Fixed-bias circuit (b) DC equivalent of Fig. (a). (c) The base emitter circuit loop

Consider first the base emitter circuit loop of Fig. 3.14(c). Writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain:

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Solving the equation for the current I_B results in the following:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Because the supply voltage V_{CC} and the base emitter voltage V_{BE} are constants, the selection of a base resistor R_B sets the level of base current for the operating point.

The collector emitter section of the network appears in Fig. 3.16, with the indicated direction of current I_C and the resulting polarity across R_C. The magnitude of the collector current is related directly to I_B through:

$$I_C = \beta I_B$$

It is interesting to note that because the base current is controlled by the level of R_B and I_C is related to I_B by a constant β, the magnitude of I_C is not a function of the resistance R_C. However, as we shall see, the level of R_C will determine the magnitude of V_{CE}, which is an important parameter.

Applying Kirchhoff's voltage law in the clockwise direction around the indicated closed loop results in the following:

V_{CE}+ $I_C R_C$ - V_{CC} = 0,

and $V_{CE} = V_{CC} - I_C R_C$

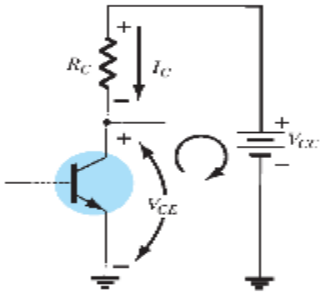


FIG. 3.16: Collector emitter loop

Example 3.1 Determine the following for the fixed-bias configuration of Fig. 3.17: I_{BQ}, I_{CQ}, V_{CEQ}, V_B, V_C and V_{BC}, Determine the saturation level for the network

Solution:

a. $I_{B_Q} = \dfrac{V_{CC} - V_{BE}}{R_B} = \dfrac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$

$I_{C_Q} = \beta I_{BQ} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\text{ mA}}$

b. $V_{CE_Q} = V_{CC} - I_C R_C = 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega)$
$= \mathbf{6.83\text{ V}}$

c. $V_B = V_{BE} = \mathbf{0.7\text{ V}}$
$V_C = V_{CE} = \mathbf{6.83\text{ V}}$

d. Using double-subscript notation yields
$V_{BC} = V_B - V_C = 0.7\text{ V} - 6.83\text{ V} = \mathbf{-6.13\text{ V}}$

The negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.

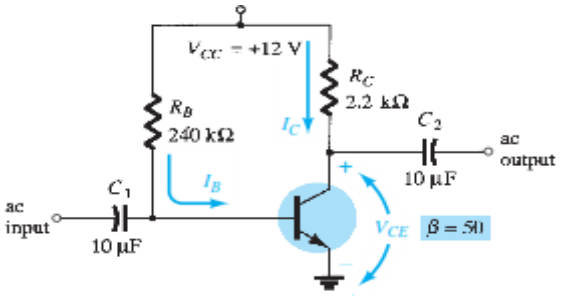


FIG. 3.17: DC fixed-bias circuit for example.

e. $I_{C_{sat}} = \dfrac{V_{CC}}{R_C} = \dfrac{12\text{ V}}{2.2\text{ k}\Omega} = \mathbf{5.45\text{ mA}}$

Second: Emitter Bias Configuration

The dc bias network of Fig. 3.18(a) contains an emitter resistor to improve the stability level over that of the fixed-bias configuration. The analysis will be performed by first examining the base emitter loop and then using the results to investigate the collector emitter loop. The dc equivalent appears in Fig 3.18(b) with a separation of the source to create an input and output section.

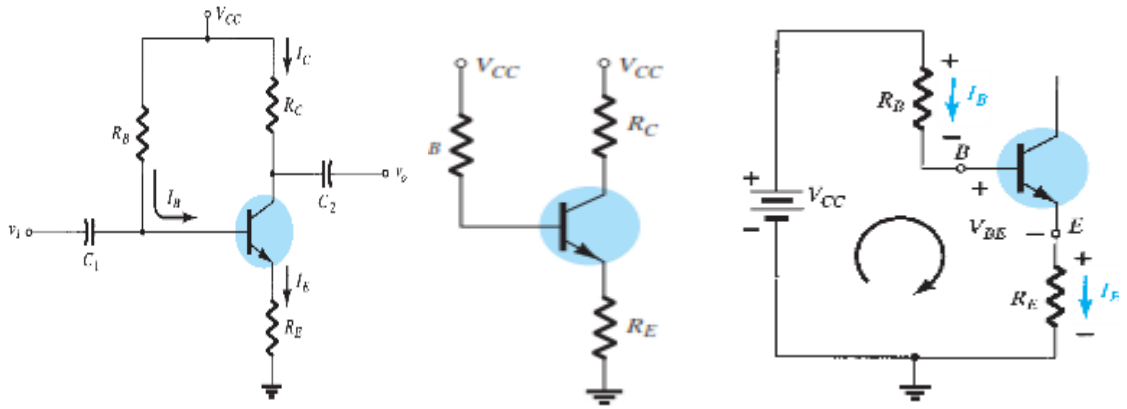
The base emitter loop of the network can be redrawn as shown in Fig. 3.18(c). Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction results in the following equation:

+V_{CC}- $I_B R_B$- V_{BE}- $I_E R_E$ = 0

But: **$I_E = (\beta + 1)\, I_B$,** Thus

$$V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$



(a) (b) (c)

FIG. 3.18: (a) BJT bias circuit with emitter resistor. (b) DC equivalent. (c) Base emitter loop.

There is an interesting result that can be derived from the above Eq. if the equation is used to sketch a series network that would result in the same equation. Such is the case for the network of Fig. 3.19(a). Note that aside from the base emitter voltage VBE, the resistor R_E is reflected back to the input base circuit by a factor (β + 1). In other words, the emitter resistor, which is part of the collector–emitter loop, "appears as" (β + 1) R_E in the base emitter loop. Because β is typically 50 or more, the emitter resistor appears to be a great deal larger in the base circuit. In general, therefore, for the configuration of Fig. 3.19(b):

$$R_i = (\beta + 1)R_E$$

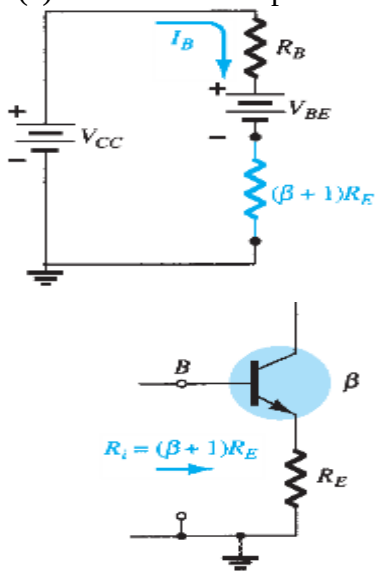


FIG. 3.19(a): Network derived from Eq. above. (b) Reflected impedance level of R_E.

The collector emitter loop appears in Fig. 3.19(c). Writing Kirchhoff's voltage law for the indicated loop in the clockwise direction results in:

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting $I_E \sim I_C$ and grouping terms gives

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

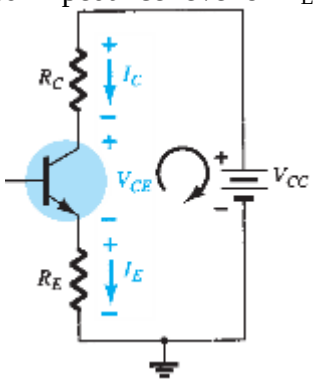


Fig. 3.19(c): Collector emitter loop.

Example 3.2: For the emitter-bias network of Fig. 3.20, determine: **I_B, (b) I_C, (c) V_{CE}, (d) V_C, (e) V_E, (f) V_B, (g) V_{BC}.** Determine the saturation current for the network.

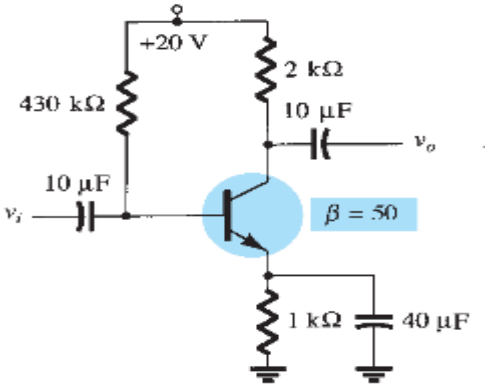


Fig 3.2: Example

Solution:

a. $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\text{ k}\Omega + (51)(1\text{ k}\Omega)}$$

$$= \frac{19.3\text{ V}}{481\text{ k}\Omega} = \mathbf{40.1\ \mu A}$$

b. $I_C = \beta I_B = (50)(40.1\ \mu\text{A}) \cong \mathbf{2.01\ mA}$

$V_{CE} = V_{CC} - I_C(R_C + R_E)$

$= 20\text{V} - (2.01\text{ mA})(2\text{ k}\Omega + 1\text{ k}\Omega)$

$= 20\text{ V} - 6.03\text{ V} = \mathbf{13.97\ V}$

d. $V_C = V_{CC} - I_C R_C = 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega)$

$= 20\text{ V} - 4.02\text{ V} = \mathbf{15.98\ V}$

e. $V_E = V_C - V_{CE} = 15.98\text{ V} - 13.97\text{ V} = \mathbf{2.01\ V}$

or $V_E = I_E R_E \cong I_C R_E = (2.01\text{ mA})(1\text{ k}\Omega) = \mathbf{2.01V}$

f. $V_B = V_{BE} + V_E = 0.7\text{ V} + 2.01\text{ V} = \mathbf{2.71\ V}$

g. $V_{BC} = V_B - V_C = 2.71\text{ V} - 15.98\text{ V}$

$= \mathbf{-13.27\ V}$ (reverse-biased as required)

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E} = \frac{20\text{ V}}{2\text{ k}\Omega + 1\text{ k}\Omega} = \frac{20\text{ V}}{3\text{ k}\Omega} = \mathbf{6.67\ mA}$$

which is about three times the level of I_{CQ}

Third: Voltage-Divider Bias Configuration

In the previous bias configurations the bias current I_{CQ} and voltage V_{CEQ} were a function of the current gain β of the transistor. However, because β is temperature sensitive, especially for silicon transistors, and the actual value of β is usually not well defined, it would be desirable to develop a bias circuit that is independent of, the transistor beta. The voltage divider bias configuration is shown in Fig. 3.21(a). If the circuit parameters are properly chosen, the resulting levels of I_{CQ} and V_{CEQ} can be almost totally independent of beta. For the dc analysis thep0tential divider network can be redrawn as shown in Fig. 3.21(b). The input side of the network can then be redrawn as shown in Fig. 3.21(c) for the dc analysis.

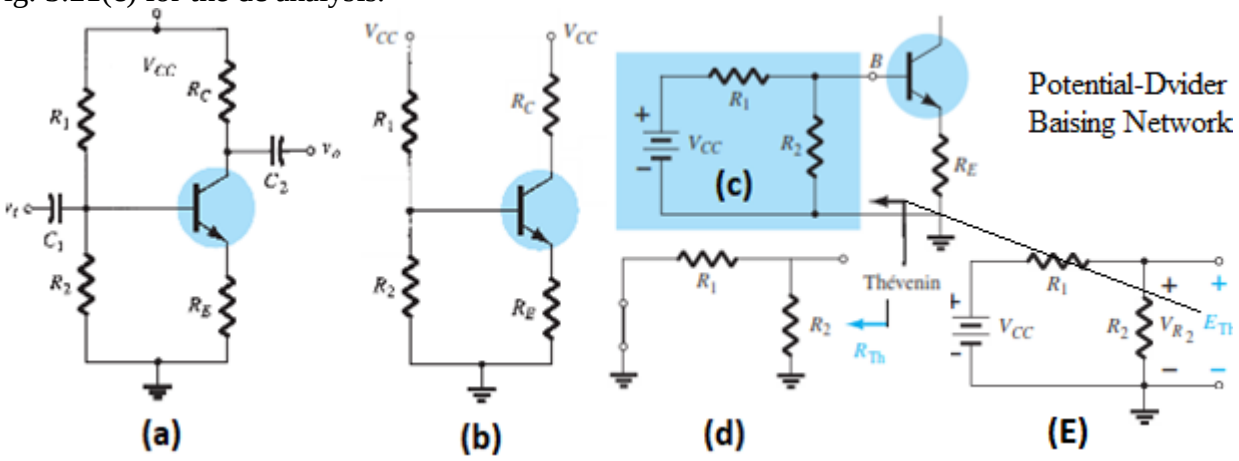


FIG. 3.21: (a) Voltage-divider bias configuration. (b) DC components of the voltage- divider configuration (c) Redrawing the input side of the network (d) Determining R_{Th} (e) Determining E_{Th}.

The Thévenin equivalent network for the network to the left of the base terminal can then be found in the following manner:

R_{Th}: The voltage source is replaced by a short-circuit equivalent as shown in Fig. 3.21(d): E_{th}: The voltage source V_{CC} is returned to the network and the open-circuit Thévenin voltage

of Fig. 3.21(e) determined as follows:
Applying the voltage-divider rule gives

$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$R_{Th} = R_1 \| R_2$$

The Thévenin network is then redrawn as shown in Fig. 3.22, and I_{BQ} can be determined by first applying Kirchhoff's voltage law in the clockwise direction for the loop indicated:

$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

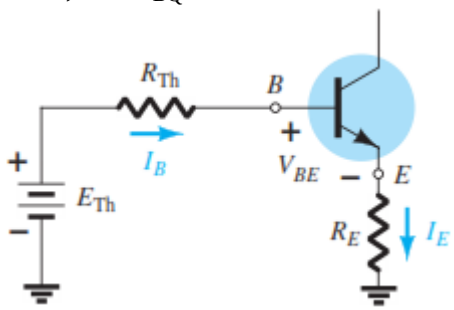


FIG. 3.22: Inserting the Thévenin equivalent circuit

Example 3.3: Determine the dc bias voltage V_{CE} and the current I_C for the voltage divider configuration of Fig.3.23. Determine the saturation current for the network.

Solution:

$$R_{Th} = R_1 \| R_2 = \frac{(39\,\text{k}\Omega)(3.9\,\text{k}\Omega)}{39\,\text{k}\Omega + 3.9\,\text{k}\Omega} = 3.55\,\text{k}\Omega$$

$$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(3.9\,\text{k}\Omega)(22\,\text{V})}{39\,\text{k}\Omega + 3.9\,\text{k}\Omega} = 2\,\text{V}$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} = \frac{2\,\text{V} - 0.7\,\text{V}}{3.55\,\text{k}\Omega + (101)(1.5\,\text{k}\Omega)} = \frac{1.3\,\text{V}}{3.55\,\text{k}\Omega + 151.5\,\text{k}\Omega} = 8.38\,\mu\text{A}$$

$$I_C = \beta I_B = (100)(8.38\,\mu\text{A}) = \mathbf{0.84\,mA}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E) = 22\,\text{V} - (0.84\,\text{mA})(10\,\text{k}\Omega + 1.5\,\text{k}\Omega) = 22\,\text{V} - 9.66\,\text{V} = \mathbf{12.34\,V}$$

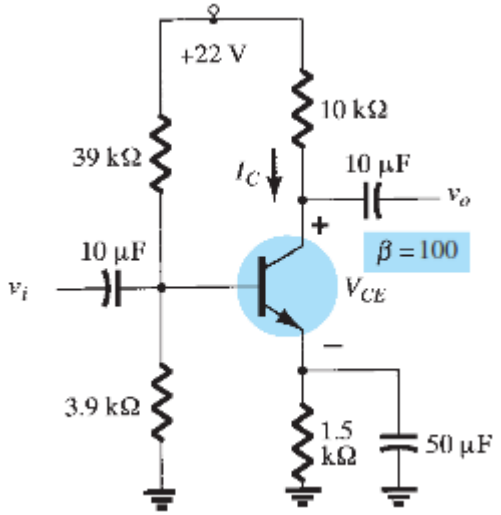


Fig 3.23: Example, voltage divider biasing.

Forth: Collector Feedback Bias Configuration

An improved level of stability can also be obtained by introducing a feedback path from collector to base as shown in Fig. 3.24(a). Although the Q -point is not totally independent of beta (even under approximate conditions), the sensitivity to changes in beta or temperature variations is normally less than encountered for the fixed-bias or emitter-biased configurations. The analysis will again be performed by first analyzing the base emitter loop, with the results then applied to the collector emitter loop. Figure 3.24(b), shows the base emitter loop for the voltage feedback configuration. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in:

$$V_{CC} - I_C' R_C - I_B R_F - V_{BE} - I_E R_E = 0$$

It is important to note that the current through R_C is not I_C, but I_C" (where I_C" = I_C + I_B). However, the level of I_C and I_C" far exceeds the usual level of I_B, and the approximation I_C' ~ I_C is normally employed. Substituting I_C"~ I_C = β*I_B and I_E= I_C, results in

$$V_{CC} - \beta I_B R_C - I_B R_F - V_{BE} - \beta I_B R_E = 0$$

$$V_{CC} - V_{BE} - \beta I_B(R_C + R_E) - I_B R_F = 0$$

Giving,

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$$

In general, the equation for I_B has the following format, which can be compared with the result for the fixed-bias and emitter-bias configurations.

$$I_B = \frac{V'}{R_F + \beta R'} \quad \text{Because } I_C = \beta I_B$$

$$I_{C_Q} = \frac{\beta V'}{R_F + \beta R'} = \frac{V'}{\frac{R_F}{\beta} + R'} \cong \frac{V'}{R'} \quad \text{In general, } R' >> \frac{R_F}{\beta}$$

The result is an equation absent of β, which would be very stable for variations in β. Because R' is typically larger for the voltage-feedback configuration than for the emitter bias configuration, the sensitivity to variations in beta is less.

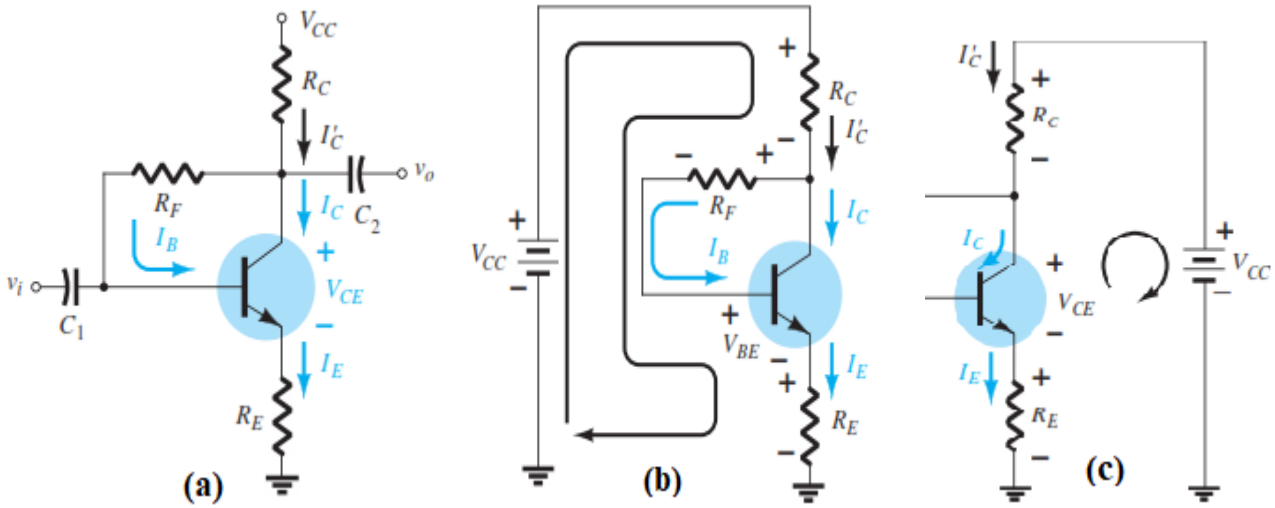


FIG. 3.24: (a) DC bias circuit with voltage feedback. (b) Base emitter loop for the network. (c) Collector emitter loop for the network.

The collector emitter loop for the network is provided in Fig.3.24 (c). Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction results in:

$$I_E R_E + V_{CE} + I_C' R_C - V_{CC} = 0$$

Because $I_C' \cong I_C$ and $I_E \cong I_C$, we have

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Example 3.4: Determine the quiescent levels of I_{CQ} and V_{CEQ} for the network of Fig. 3.25.
Solution:

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$$
$$= \frac{10\text{ V} - 0.7\text{ V}}{250\text{ k}\Omega + (90)(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)}$$
$$= \frac{9.3\text{ V}}{250\text{ k}\Omega + 531\text{ k}\Omega} = 11.91\ \mu\text{A}$$
$$I_{C_Q} = \beta I_B = (90)(11.91\ \mu\text{A}) = \mathbf{1.07\ mA}$$
$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$
$$= 10\text{ V} - (1.07\text{ mA})(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)$$
$$= 10\text{ V} - 6.31\text{ V} = \mathbf{3.69\ V}$$

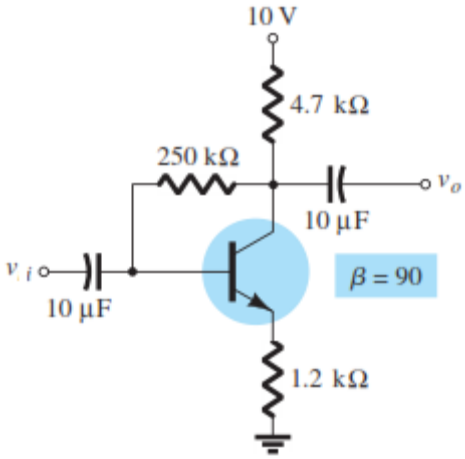


Fig 3.25: Example

Example 3.5: Repeat the previous Example using a beta of 135 (50% greater).
Solution:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$
$$= \frac{10\text{ V} - 0.7\text{ V}}{250\text{ k}\Omega + (135)(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)}$$
$$= \frac{9.3\text{ V}}{250\text{ k}\Omega + 796.5\text{ k}\Omega} = 8.89\ \mu\text{A}$$

$$I_{C_Q} = \beta I_B = (135)(8.89\ \mu\text{A}) = \mathbf{1.2\ mA}$$
$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$
$$= 10\text{ V} - (1.2\text{ mA})(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)$$
$$= 10\text{ V} - 7.08\text{ V} = \mathbf{2.92\ V}$$

Discussion: Even though the level of β increased 50%, the level of I_{CQ} only increased 12.1%, whereas the level of V_{CEQ} decreased about 20.9%. If the network were a fixed-bias design, a 50% increase in β would have resulted in a 50% increase in I_{CQ} and a dramatic change in the location of the Q -point.

Common Collector (Emitter-Follower) Configuration

The previous sections introduced configurations in which the output voltage is typically taken off the collector terminal of the BJT. This section will examine a configuration where the output is taken off the emitter terminal as shown in Fig. 3.26 (a). The dc equivalent of the network appears in Fig. 3.26(b). Applying Kirchhoff's voltage rule to the input circuit will result in:

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0 \quad \text{and using } I_E = (\beta + 1)I_B$$
$$I_B R_B + (\beta + 1)I_B R_E = V_{EE} - V_{BE} \quad \text{so that} \quad \boxed{I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}}$$

For the output network, an application of Kirchhoff's voltage law will result in

$$-V_{CE} - I_E R_E + V_{EE} = 0$$

and $$\boxed{V_{CE} = V_{EE} - I_E R_E}$$

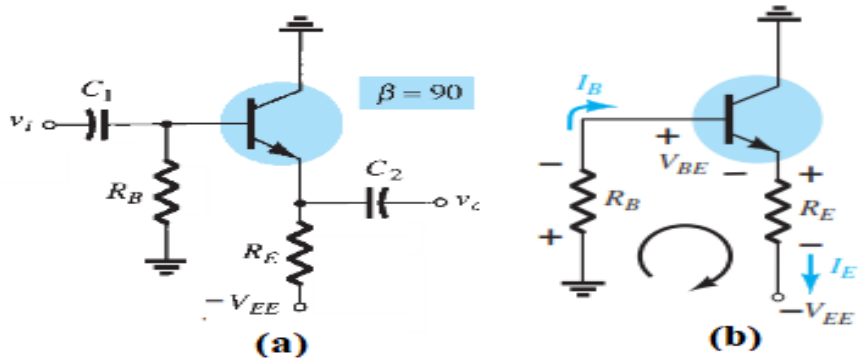


FIG. 3.26: (a) Common collector (emitter-follower) configuration. (b) DC equivalent circuit.

Example 3.6: Determine V_{CEQ} and I_{EQ} for the common collector (emitter-follower) configuration, suppose: R_B = 240K, R_E = 2K, V_{EE} = -20V.

Solution:

$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$= \frac{20\,\text{V} - 0.7\,\text{V}}{240\,\text{k}\Omega + (90 + 1)2\,\text{k}\Omega} = 45.73\,\mu\text{A}$$

$$V_{CE_Q} = V_{EE} - I_E R_E = V_{EE} - (\beta + 1)I_B R_E$$

$$= 20\,\text{V} - (90 + 1)(45.73\,\mu\text{A})(2\,\text{k}\Omega) = \mathbf{11.68\,V}$$

$$I_{E_Q} = (\beta + 1)I_B = (91)(45.73\,\mu\text{A}) = 4.16\,\text{mA}$$

Common-Base Configuration

The common-base configuration is unique in that the applied signal is connected to the emitter terminal and the base is at, or just above, ground potential. It is a fairly popular configuration because in the ac domain it has a very low input impedance, high output impedance, and good gain.

A typical common-base configuration appears in Fig. 3.27(a). Note that two supplies are used in this configuration and the base is the common terminal between the input emitter terminal and output collector terminal. The dc equivalent of the input side appears in Fig. 3.27(b). Applying Kirchhoff's voltage law will result in:

$$-V_{EE} + I_E R_E + V_{BE} = 0$$

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

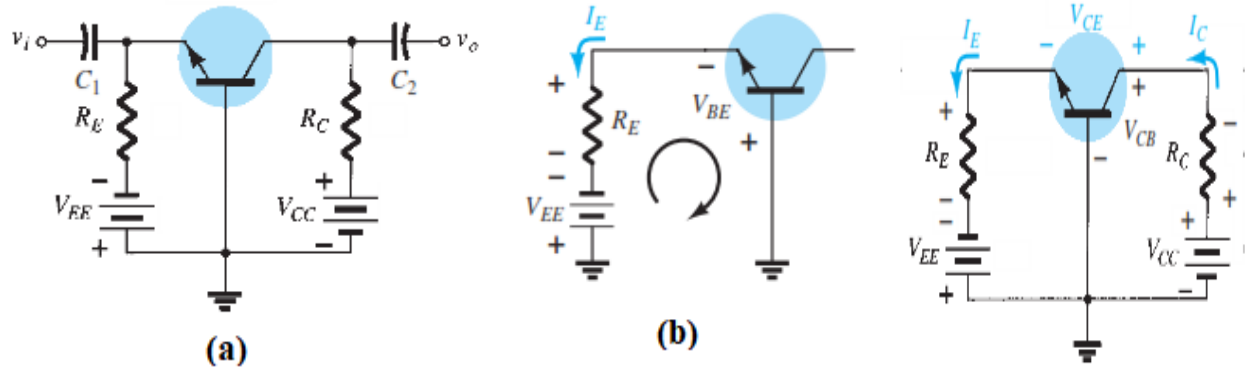


Fig. 3. 27: (a) Common-base configuration. (b) Input dc equivalent. (c) Determining V_{CE} and V_{CB}.

Applying Kirchhoff's voltage law to the entire outside perimeter of the network appears in Fig. 3.27(c) will result in:

$$-V_{EE} + I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} = V_{EE} + V_{CC} - I_E R_E - I_C R_C$$

$$I_E \cong I_C$$

$$\boxed{V_{CE} = V_{EE} + V_{CC} - I_E(R_C + R_E)}$$

$$V_{CB} + I_C R_C - V_{CC} = 0$$

$$V_{CB} = V_{CC} - I_C R_C$$

$$I_C \cong I_E$$

$$\boxed{V_{CB} = V_{CC} - I_C R_C}$$

Example 3.7: Determine the currents I_E and I_B and the voltages V_{CE} and V_{CB} for the common-base configuration given in fig 3.27(a), suppose $R_E = 1.2K$, $R_C = 2.4K$, $V_{EE} = 4V$, $V_{CC} = 10V$ and $\beta = 60$.

Solution:

$$I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{4\text{ V} - 0.7\text{ V}}{1.2\text{ k}\Omega} = \mathbf{2.75\text{ mA}}$$

$$I_B = \frac{I_E}{\beta + 1} = \frac{2.75\text{ mA}}{60 + 1} = \frac{2.75\text{ mA}}{61} = \mathbf{45.08\ \mu A}$$

$$V_{CE} = V_{EE} + V_{CC} - I_E(R_C + R_E)$$
$$= 4\text{ V} + 10\text{ V} - (2.75\text{ mA})(2.4\text{ k}\Omega + 1.2\text{ k}\Omega)$$
$$= 14\text{ V} - (2.75\text{ mA})(3.6\text{ k}\Omega) = \mathbf{4.1\text{ V}}$$

$$V_{CB} = V_{CC} - I_C R_C = V_{CC} - \beta I_B R_C$$
$$= 10\text{ V} - (60)(45.08\ \mu\text{A})(24\text{ k}\Omega) = \mathbf{3.51\text{ V}}$$

Amplification in the ac Domain

It was demonstrated previous sections that the transistor can be employed as an amplifying device. That is, the output sinusoidal signal is greater than the input sinusoidal signal, or, stated another way, the output ac power is greater than the input ac power. The question then arises as to how the ac power output can be greater than the input ac power. Conservation of energy dictates that over time the total power output, Po , of a system cannot be greater than its power input, Pi, and that the efficiency defined by: η = Po/Pi cannot be greater than 1. The factor missing from the discussion above that permits an ac power output greater than the input ac power is the applied dc power. It is the principal contributor to the total output power even though part of it is dissipated by the device and resistive elements. In other words, there is an exchange of dc power to the ac domain that permits establishing a higher output ac power.

In general, therefore, proper amplification design requires that the dc and ac components be sensitive to each other's requirements and limitations. However, it is extremely helpful to realize that: The superposition theorem is applicable for the analysis and design of the dc and ac components of a BJT network, permitting the separation of the analysis of the dc and ac responses of the system. In other words, one can make a complete dc analysis of a system before considering the ac response. Once the dc analysis is complete, the ac response can be determined using a completely ac analysis.

The key to transistor small-signal analysis is the use of the equivalent circuits (models). A model is a combination of circuit elements, properly chosen, that best approximates the actual behavior of a semiconductor device under specific operating conditions. Once the ac equivalent circuit is determined, the schematic symbol for the device can be replaced by this equivalent circuit and the basic methods of circuit analysis applied to determine the desired quantities of the network. Throughout the course the $\mathbf{r_e}$ model is the model of choice. In an effort to demonstrate the effect

that the ac equivalent circuit will have on the analysis to follow, consider the circuit of Fig. 3. 28(a). Let us assume for the moment that the small-signal ac equivalent circuit for the transistor has already been determined. All the dc supplies can be replaced by a zero-potential equivalent (short circuit) because they determine only the dc (quiescent level) of the output voltage and not the magnitude of the swing of the ac output. This is clearly demonstrated by Fig. 3. 28(b). The dc levels were simply important for determining the proper Q -point of operation.

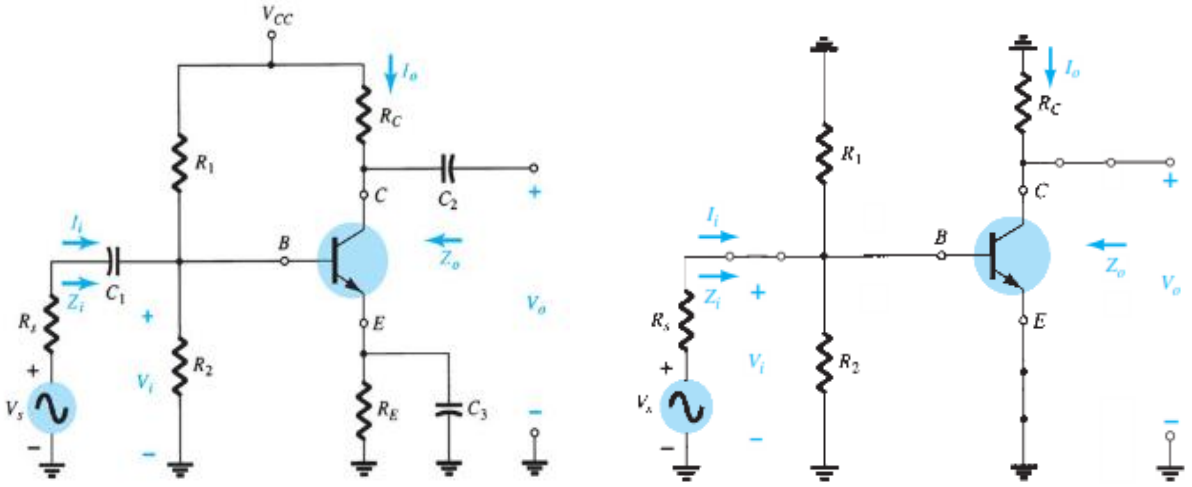


FIG. 3.28: (a) Transistor circuit under examination in this introductory discussion. (b) The network of Fig. (a), following removal of the dc supply and insertion of the short-circuit equivalent for the capacitors.

Once determined, the dc levels can be ignored in the ac analysis of the network. In addition, the coupling capacitor C_1 and C_2 and bypass capacitor C_3 were chosen to have a very small reactance at the frequency of application. Therefore, they, too, may for all practical purposes be replaced by a low-resistance path or a short circuit. Note that this will result in the "shorting out" of the dc biasing resistor R_E. Recall that capacitors assume an "open-circuit" equivalent under dc steady-state conditions, permitting isolation between stages for the dc levels and quiescent conditions. It is important as you progress through the modifications of the network to define the ac equivalent that the parameters of interest such as Z_i, Z_o, I_i and I_o as defined by Fig. 3.29(a) be carried through properly. The input impedance is defined from base to ground, the input current as the base current of the transistor, the output voltage as the voltage from collector to ground, and the output current as the current through the load resistor R_C.

FIG. 3.29 (a): Defining the important parameters of any system, (b) Demonstrating the reason for the defined directions and polarities.

The defined polarities for the input and output voltages are also as appearing. If V_O has the opposite polarity, the minus sign must be applied. Note that Z_i is the impedance "looking into" the system, whereas Z_o is the impedance "looking back into" the system from the output side. By choosing the defined directions for the currents and voltages as appearing in Fig. 3.29(a), both the input impedance and output impedance are defined as having positive values. For example, in Fig.

3.29 (b), the input and output impedances for a particular system are both resistive. For the direction of Ii and Io the resulting voltage across the resistive elements will have the same polarity as V_i and Vo, respectively. If Io had been defined as the opposite direction in Fig. 3.29(a), a minus sign would have to be applied. For each case $Z_i=V_i/I_i$ and $Z_o= V_o/I_o$ with positive results if they all have the defined directions and polarity of Fig 3.29. If the output current of an actual system has a direction opposite to that of Fig. 3.29, a minus sign must be applied to the result because V_o must be defined.

If we establish a common ground and rearrange the elements of Fig. 3.29, R_1 and R_2 will be in parallel, and R_C will appear from collector to emitter as shown in Fig. 3.30. Because the components of the transistor equivalent circuit appearing in Fig. 3.30 employ familiar components such as resistors and independent controlled sources, analysis techniques such as superposition, Thévenin's theorem, and so on, can be applied to determine the desired quantities.

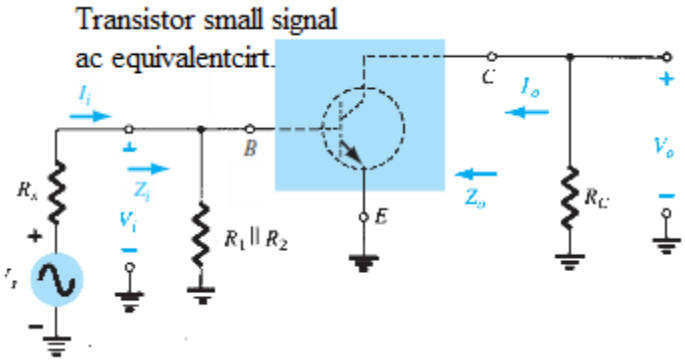


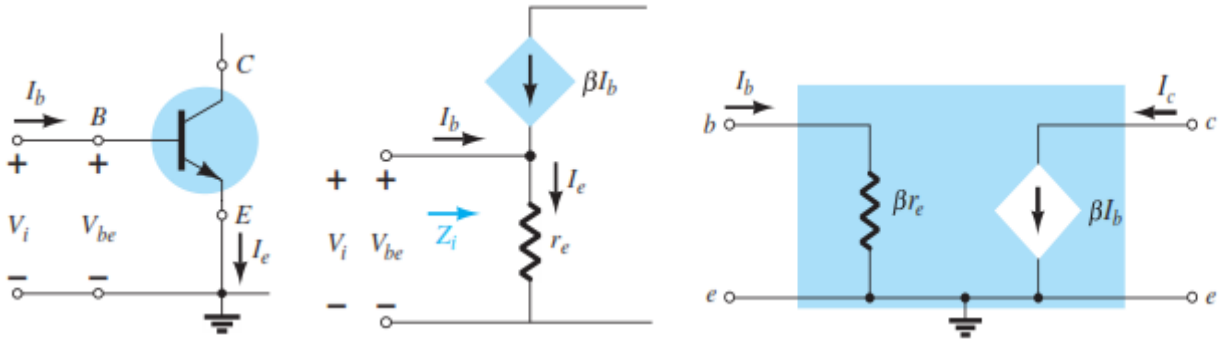
FIG. 3.30: Circuit of Fig. 3.29, redrawn for small-signal ac analysis.

The r_e Transistor Model

r_e model for the CE, CB, and CC BJT transistor configurations will now be introduced with a short description of why each is a good approximation to the actual behavior of a BJT transistor.

Common-Emitter Configuration

The equivalent circuit for the common-emitter configuration will be constructed using the device characteristics and a number of approximations. Starting with the input side, we find the applied voltage V_i is equal to the voltage V_{be} with the input current being the base current I_b as shown in Fig. 3.31(a). For the equivalent circuit, therefore, the input side is simply a single diode with a current Ie. It can be improved by first replacing the diode by its equivalent resistance as determined by the level of I_E as: $\mathbf{r_e = 26\ mV / I_E}$. However, we must now add a component to the network that will establish the current Ie using the output characteristics. Drawing the collector characteristics to have a constant β, the common-emitter configuration has been established in Fig. 3.31(b).



(a) (b) (c)

FIG. 3.31: (a) finding the input equivalent circuit for a BJT transistor. (b) BJT equivalent circuit. (c) Improved BJT equivalent circuit.

Now, for the input side, and solving for V_{be}:

$$Z_i = \frac{V_i}{I_b} = \frac{V_{be}}{I_b}$$

$$V_{be} = I_e r_e = (I_c + I_b) r_e$$

$$= (\beta I_b + I_b) r_e = (\beta + 1) I_b r_e$$

$$Z_i = \frac{V_{be}}{I_b} = \frac{(\beta + 1) I_b r_e}{I_b}$$

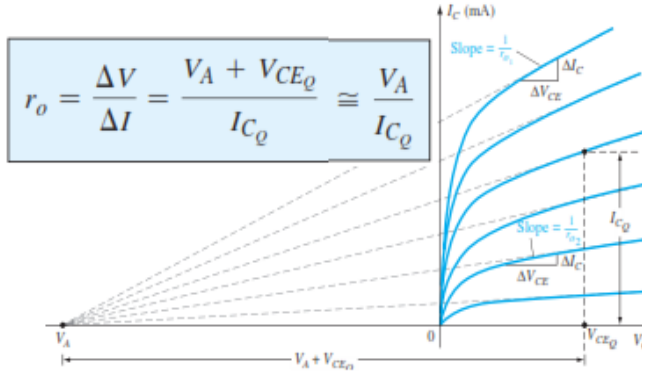
$$\boxed{Z_i = (\beta + 1) r_e \cong \beta r_e}$$

The result is that the impedance seen "looking into" the base of the network is a resistor equal to beta times the value of re , as shown in Fig. 3.31(c). The collector output current is still linked to the input current by beta as shown in the same figure.

Early Voltage

We now have a good representation for the input circuit, but aside from the collector output current being defined by the level of β and I_B, we do not have a good representation for the output impedance of the device. In general, it is desirable to have large output impedances to avoid loading down the next stage of a design. If the slope of the curves that defines the output impedance of the device is extended until they reach the horizontal axis, as shown in Fig. 3.32, that they will all intersect at a voltage called the Early voltage. For a particular collector and base current, the output impedance can be found using the following equation:

$$r_o = \frac{\Delta V}{\Delta I} = \frac{V_A + V_{CE_Q}}{I_{C_Q}} \cong \frac{V_A}{I_{C_Q}}$$



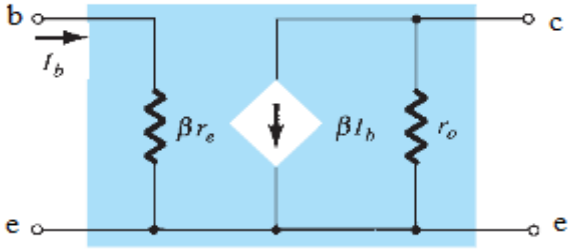


FIG. 3.32: (a) defining the Early voltage and the output impedance of a transistor. (b) $\mathbf{r_e}$ model for the common-emitter transistor configuration including effects of $\mathbf{r_o}$.

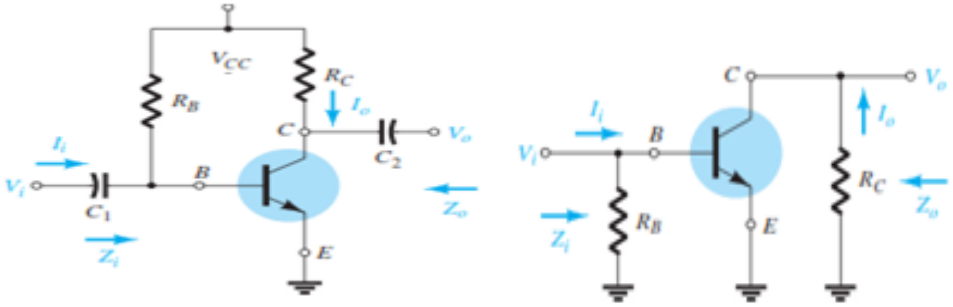
Typically, however, the Early voltage is sufficiently large compared with the applied collector-to-emitter voltage to permit the above approximation. Clearly, since V_A is a fixed voltage, the larger the collector current, the less the output impedance. In any event, an output impedance can now be defined that will appear as a resistor in parallel with the output as shown in the equivalent circuit of Fig. 3.32(b).

Common Emitter Bias Configuration

First: Common Emitter Fixed-Bias Configuration

The transistor models just introduced will now be used to perform a small signal ac analysis of a number of standard transistor network configurations. The networks analyzed represent the majority of those appearing in practice. Modifications of the standard configurations will be relatively easy to examine. The effect of output impedance is examined for completeness. The first configuration to be analyzed in detail is the common emitter fixed-bias network of Fig. 3.33(a). Note that the input signal V_i is applied to the base of the transistor, whereas the output V_o is off the collector. In addition, recognize that the input current I_i is not the base current, but the source current, and the output current I_o is the collector current. The small signal ac analysis begins by removing the dc

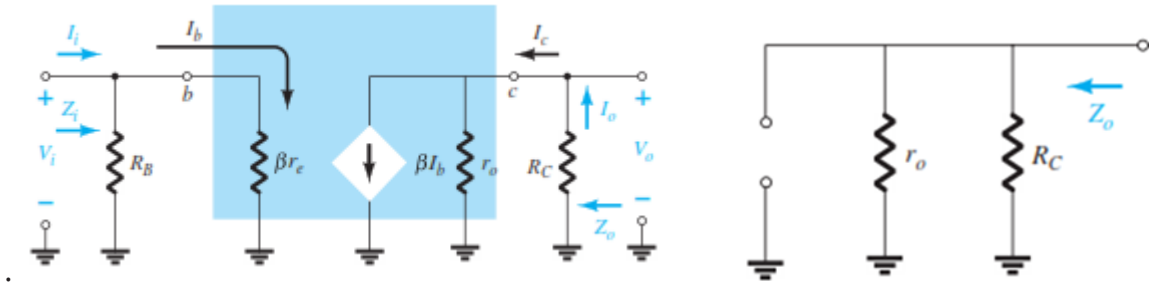
effects of V_{CC} and replacing the dc blocking capacitors C_1 and C_2 by short-circuit equivalents, resulting in the network of Fig. 3.33(b). Note that the common ground of the dc supply and the transistor emitter terminal permit the relocation of R_B and R_C in parallel with the input and output sections of the transistor, respectively. In addition, note the placement of the important network parameters Z_i, Z_o, I_i, and I_o on the redrawn network.



(a) (b)

FIG. 3.33(a): Common emitter fixed bias configuration. (b) Network of Fig (a) following the removal of the effects of V_{CC}, C_1, and C_2.

Substituting the r_e model for the common emitter configuration of Fig. 3.33 results the network of Fig. 3.34 (a).



(a) (b)

FIG. 3.34(a) Substituting the re model into the network of Fig.3.33. (b) Determining Zo for the network of Fig. 3.34(a).

The next step is to determine β, re, and ro. The magnitude of β and ro are typically obtained from a specification sheet or by direct measurement using a curve tracer or transistor testing instrument. The value of re must be determined from a dc analysis of the system. Assuming that β, re, and ro have been determined will result in the following equations for the important two port characteristics of the system.

$$Z_i = R_B \| \beta r_e \quad \text{ohms}$$

For the majority of situations R_B is greater than βre by more than a factor of 10, permitting the following approximation:

$$Z_i \cong \beta r_e \quad \text{ohms} \qquad R_B \geq 10\beta r_e$$

Recall that the output impedance of any system is defined as the impedance Z_o determined when $V_i = 0$. When $V_i = 0$, $I_i = I_b = 0$, resulting in an open circuit equivalence for the current source. The result is the configuration of Fig. 3.34 (b). We have

$$Z_o = R_C \| r_o \quad \text{ohms}$$

If $r_o \geq 10R_C$, the approximation $R_C \| r_o = R_C$ is frequently applied, and

$$Z_o \cong R_C \qquad r_o \geq 10R_C$$

Av: The resistors r_o and R_C are in parallel, and

$$V_o = -\beta I_b (R_C \| r_o)$$

$$I_b = \frac{V_i}{\beta r_e}$$

$$V_o = -\beta \left(\frac{V_i}{\beta r_e}\right)(R_C \| r_o)$$

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{(R_C \| r_o)}{r_e}}$$

If $r_o \geq 10R_C$, the approximation $R_C \| r_o = R_C$ is frequently applied, and

$$\boxed{A_v = -\frac{R_C}{r_e}} \quad r_o \geq 10R_C$$

Example: For the network of Fig.3.33, determine: 1.r_e, 2. Z_i, Z_o, and A_v (with $r_o = \infty$). 3. Repeat parts (2) including r_o = 50 kΩ, and compare results. Suppose R_B =470 kΩ, R_C = 3kΩ and β =100.

Solution: 1. DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{470\text{ k}\Omega} = 24.04\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (101)(24.04\ \mu\text{A}) = 2.428\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.428\text{ mA}} = \mathbf{10.71\ \Omega}$$

2. $\beta r_e = (100)(10.71\ \Omega) = 1.071\text{ k}\Omega$

$$Z_i = R_B \| \beta r_e = 470\text{ k}\Omega \| 1.071\text{ k}\Omega = \mathbf{1.07\ k\Omega}$$

$$Z_o = R_C = \mathbf{3\ k\Omega}$$

$$A_v = -\frac{R_C}{r_e} = -\frac{3\text{ k}\Omega}{10.71\ \Omega} = \mathbf{-280.11}$$

3. $Z_o = r_o \| R_C = 50\text{ k}\Omega \| 3\text{ k}\Omega = \mathbf{2.83\ k\Omega}$ vs. 3 kΩ

$$A_v = -\frac{r_o \| R_C}{r_e} = \frac{2.83\text{ k}\Omega}{10.71\ \Omega} = \mathbf{-264.24}\text{ vs.} -280.11$$

<u>Second: Voltage Divider Bias</u>

The next configuration to be analyzed is the voltage divider bias network of Fig 3.35(a).Recall that the name of the configuration is a result of the voltage divider bias at the input side to determine the dc level of V_B. Substituting the re equivalent circuit results in the network of Fig 3.35(b). Note the absence of R_E due to the low impedance shorting effect of the bypass capacitor, C_E. That is, at the frequency (or frequencies) of operation, the reactance of the capacitor is so small compared to R_E that it is treated as a short circuit across R_E. When V_{CC} is set to zero, it places one end of R_1 and R_C at ground potential. In addition, note that R_1 and R_2 remain part of the input circuit, whereas R_C is part of the output circuit.

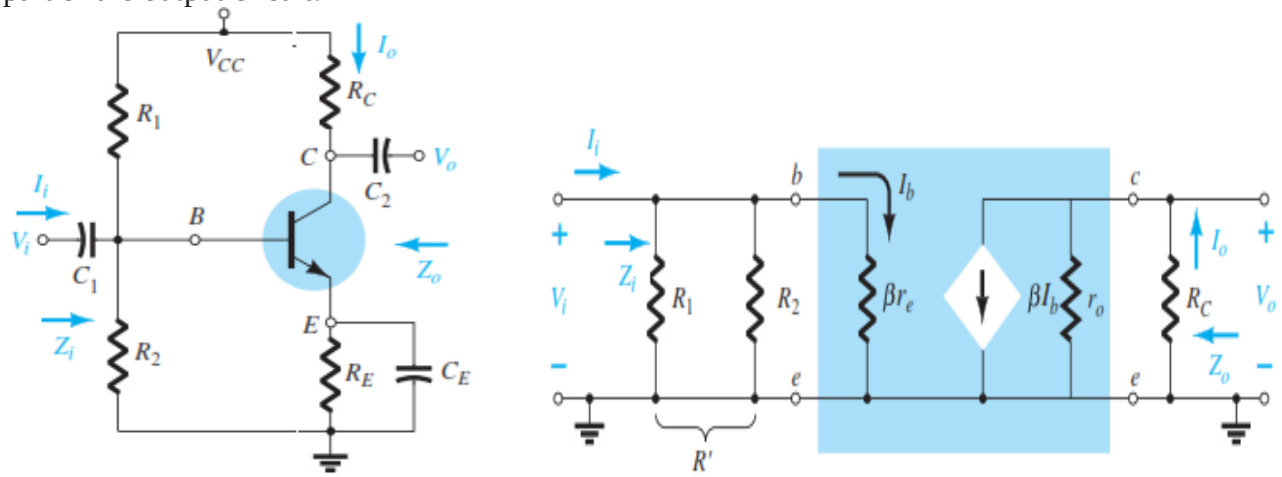


FIG 3.35; (a): Voltage divider bias configuration. (b) Substituting the re equivalent circuit into the ac equivalent network of (a).

The parallel combination of $R_1$and R_2 is defined by:

$$R' = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$ And

$$Z_i = R' \| \beta r_e$$ And $$Z_o = R_C \| r_o$$ And

$$Z_o \cong R_C \quad r_o \geq 10R_C$$

$$V_o = -(\beta I_b)(R_C \| r_o) \text{ And } I_b = \frac{V_i}{\beta r_e}$$

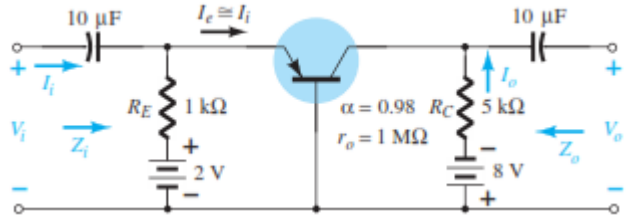
$$V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_C \| r_o)$$

$$A_v = \frac{V_o}{V_i} = \frac{-R_C \| r_o}{r_e}$$

$$A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e} \quad r_o \geq 10R_C$$

Av:

Example: For the voltage divider bias network of figure 3.35, determine, 1. r_e, 2. Z_i, Z_o, and A_v (with $r_o = \infty$), Repeat 2 (with $r_o = 50$ kΩ). Suppose $V_{CC} = 22$V, $R_1 = 56$ kΩ, $R_2 = 8.2$ kΩ, $R_C = 6.8$ kΩ, $R_E = 1.5$ kΩ and $\beta = 90$.



Solution:

1. DC: Testing $\beta R_E > 10R_2$,

$(90)(1.5\text{ k}\Omega) > 10(8.2\text{ k}\Omega)$

$135\text{ k}\Omega > 82\text{ k}\Omega$ (*satisfied*)

Using the approximate approach,

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{(8.2\text{ k}\Omega)(22\text{ V})}{56\text{ k}\Omega + 8.2\text{ k}\Omega} = 2.81\text{ V}$$

$$V_E = V_B - V_{BE} = 2.81\text{ V} - 0.7\text{ V} = 2.11\text{ V}$$

$$I_E = \frac{V_E}{R_E} = \frac{2.11\text{ V}}{1.5\text{ k}\Omega} = 1.41\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{1.41\text{ mA}} = \mathbf{18.44\ \Omega}$$

2. $$R' = R_1 \| R_2 = (56\text{ k}\Omega) \| (8.2\text{ k}\Omega) = 7.15\text{ k}\Omega$$

$$Z_i = R' \| \beta r_e = 7.15\text{ k}\Omega \| (90)(18.44\ \Omega)$$

$$= 7.15\text{ k}\Omega \| 1.66\text{ k}\Omega = \mathbf{1.35\ k\Omega}$$

$$Z_o = R_C = \mathbf{6.8\ k\Omega}$$

$$A_v = -\frac{R_C}{r_e} = -\frac{6.8\text{ k}\Omega}{18.44\ \Omega} = \mathbf{-368.76}$$

3. $Z_i = \mathbf{1.35\ k\Omega}$

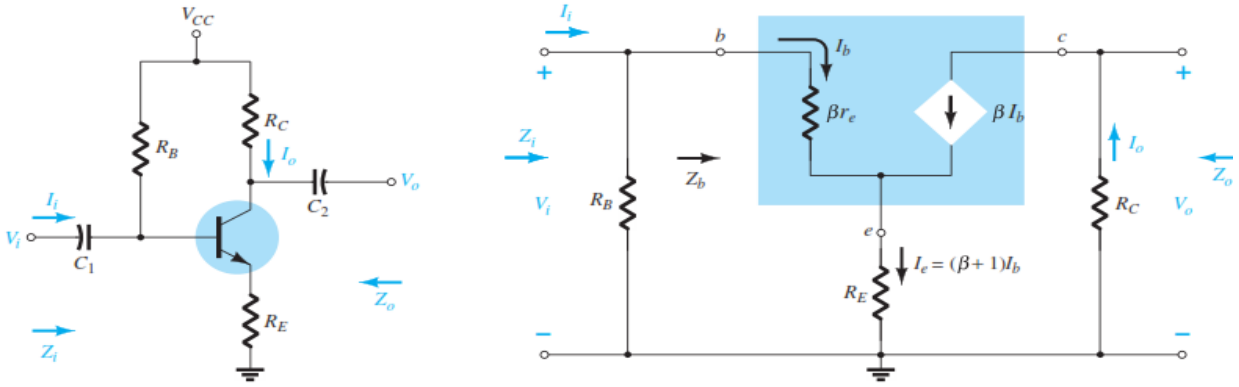
$$Z_o = R_C \| r_o = 6.8\text{ k}\Omega \| 50\text{ k}\Omega = \mathbf{5.98\ k\Omega}$$

$$A_v = -\frac{R_C \| r_o}{r_e} = -\frac{5.98\text{ k}\Omega}{18.44\ \Omega} = \mathbf{-324.3}$$

Third: Emitter Resistance Bias Configuration

The networks examined in this section include an emitter resistor that may or may not be bypassed in the ac domain. We first consider the unbypassed situation and then modify the resulting equations for the bypassed configuration.

Unbypassed: The most fundamental of unbypassed configurations appears in Fig. 3.36(a). The re equivalent model is substituted in Fig. 3.36(b), but note the absence of the resistance r_o. The effect of ro is to make the analysis a great deal more complicated, and considering the fact that in most situations its effect can be ignored, it will not be included in the present analysis.



(a) (b)

FIG. 3.36: (a) Emitter resistance bias configuration. (b) Substituting the r_e equivalent circuit into the ac equivalent network of Fig. (a).

Applying Kirchhoff's voltage law to the input side results in:

$$V_i = I_b\beta r_e + I_e R_E \quad \textbf{And} \quad V_i = I_b\beta r_e + (\beta + I)I_b R_E$$

looking into the network to the right of R_B is

$$Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta + 1)R_E$$

$$\boxed{Z_b = \beta r_e + (\beta + 1)R_E}$$

the approximate equation is

$$\boxed{Z_b \cong \beta(r_e + R_E)}$$

Eq. can be further reduced to

$$\boxed{Z_b \cong \beta R_E}$$

$$\boxed{Z_i = R_B \| Z_b}$$

With V_i set to zero, $I_b = 0$,

$$\boxed{Z_o = R_C}$$

A_v : $\quad I_b = \dfrac{V_i}{Z_b}$

$$V_o = -I_o R_C = -\beta I_b R_C = -\beta\left(\frac{V_i}{Z_b}\right)R_C$$

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{\beta R_C}{Z_b}}$$

Substituting $Z_b \cong \beta(r_e + R_E)$ gives

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e + R_E}}$$

and for the approximation $Z_b \cong \beta R_E$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{R_E}}$$

Note the absence of β from the equation for Av demonstrating independence in variation of β.

Effect of r_o

The equations appearing below will clearly reveal the additional complexity resulting from including ro in the analysis. Note in each case, however, that when certain conditions are met, the equations return to the form just derived.

$$\boxed{Z_b = \beta r_e + \left[\frac{(\beta + 1) + R_C/r_o}{1 + (R_C + R_E)/r_o}\right]R_E}$$

And

$$\boxed{Z_b \cong \beta(r_e + R_E)} \qquad r_o \geq 10(R_C + R_E)$$

$$Z_o = R_C \| \left[r_o + \frac{\beta(r_o + r_e)}{1 + \frac{\beta r_e}{R_E}} \right]$$

And $\boxed{Z_o \cong R_C}$ Any level of r_o

$$A_v = \frac{V_o}{V_i} = \frac{-\frac{\beta R_C}{Z_b}\left[1 + \frac{r_e}{r_o}\right] + \frac{R_C}{r_o}}{1 + \frac{R_C}{r_o}}$$

And $\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b}}$ $r_o \geq 10R_C$

Bypassed: If R_E of Fig. 3.34 is bypassed by an emitter capacitor C_E, the complete re equivalent model can be substituted, resulting in the same equivalent network as Fig. 3.35. Equations are therefore applicable.

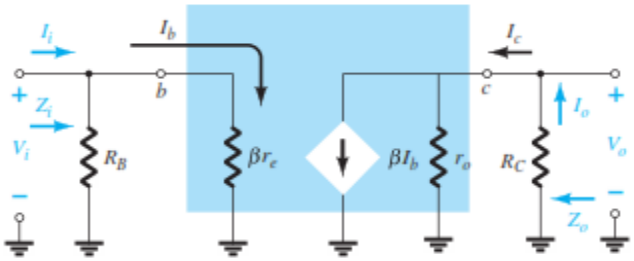


Figure 3.35: RE is bypassed

Example: For the network of Fig. 3.37: (1) without CE (unbypassed), determine: r_e, Z_i, Z_o, and A_v. (2) Repeat the analysis of part (1) with CE in place.

Solution: (1) DC analysis:

$$\text{DC:} \quad I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{470\text{ k}\Omega + (121)0.56\text{ k}\Omega} = 35.89\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (121)(35.89\ \mu\text{A}) = 4.34\text{ mA} \quad \text{and} \quad r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{4.34\text{ mA}} = \mathbf{5.99\ \Omega}$$

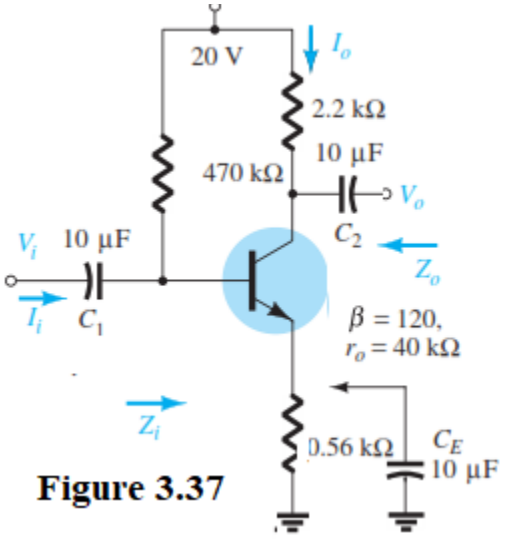


Figure 3.37

Testing the condition $r_o \geq 10(R_C + R_E)$

$40\text{ k}\Omega \geq 10(2.2\text{ k}\Omega + 0.56\text{ k}\Omega)$

$40\text{ k}\Omega \geq 10(2.76\text{ k}\Omega) = 27.6\text{ k}\Omega$ (*satisfied*)

Therefore,

$$Z_b \cong \beta(r_e + R_E) = 120(5.99\ \Omega + 560\ \Omega) = 67.92\text{ k}\Omega$$

and $Z_i = R_B \| Z_b = 470\text{ k}\Omega \| 67.92\text{ k}\Omega = \mathbf{59.34\ k\Omega}$

$Z_o = R_C = \mathbf{2.2\ k\Omega}$

$r_o \geq 10R_C$ is satisfied. Therefore,

$$A_v = \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b} = -\frac{(120)(2.2\text{ k}\Omega)}{67.92\text{ k}\Omega} = \mathbf{-3.89}$$

compared to -3.93 using Eq. $A_v \cong -R_C/R_E$.

(2) The dc analysis is the same, and $r_e = 5.99\ \Omega$. R_E is "shorted out" by C_E for the ac analysis. Therefore,

$$Z_i = R_B \| Z_b = R_B \| \beta r_e = 470\text{ k}\Omega \| (120)(5.99\ \Omega) = 470\text{ k}\Omega \| 718.8\ \Omega \cong \mathbf{717.70\ \Omega}$$

$$Z_o = R_C = \mathbf{2.2\ k\Omega} \quad \textbf{And} \quad A_v = -\frac{R_C}{r_e} = -\frac{2.2\text{ k}\Omega}{5.99\ \Omega} = \mathbf{-367.28}\ \text{(a significant increase)}$$

Emitter Follower Configuration

When the output is taken from the emitter terminal of the transistor as shown in Fig. 3.38 (a), the network is referred to as an emitter-follower. The output voltage is always slightly less than the input signal due to the drop from base to emitter, but the approximation $A_v \cong 1$ is usually a good one. Unlike the collector voltage, the emitter voltage is in phase with the signal V_i. The fact that V_o "follows" the magnitude of V_i with an in-phase relationship accounts for the terminology emitter follower. The emitter-follower configuration is frequently used for impedance matching purposes. It presents high impedance at the input and low impedance at the output, which is the direct opposite of the standard fixed bias configuration. The resulting effect is much the same as that obtained with a transformer, where a load is matched to the source impedance for maximum power transfer through the system. Equivalent circuit into the network of emitter follower results in the network of Fig. 3.38 (b).

The input impedance is determined in the same manner as described in the preceding section:

$$Z_i = R_B \| Z_b$$ With $$Z_b = \beta r_e + (\beta + 1)R_E$$ Or $$Z_b \cong \beta(r_e + R_E)$$ And $$Z_b \cong \beta R_E \quad R_E \gg r_e$$

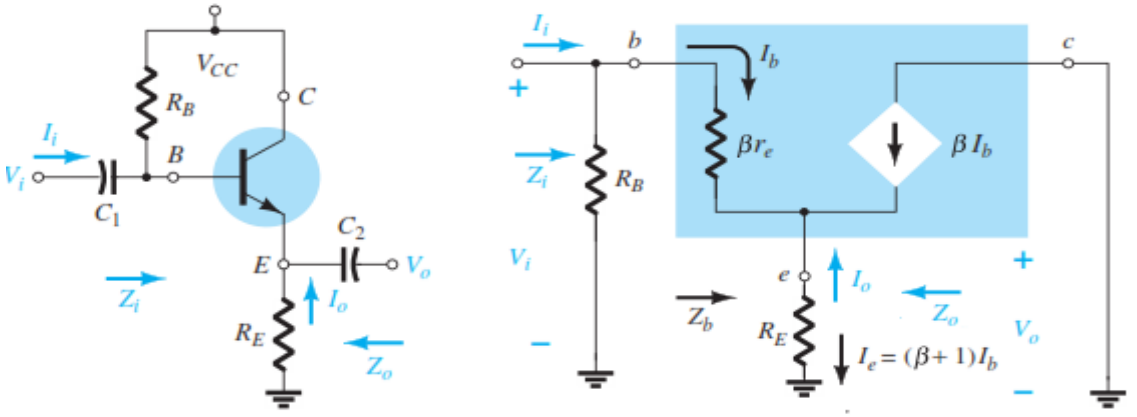


FIG. 3.38: (a) Emitter follower configuration. (b) Substituting the re equivalent circuit into the ac equivalent network of Fig. 3.38 (a).

Z_o: The output impedance is best described by first writing the equation for the current I_b, $I_b = V_i/Z_b$, and then multiplying by $(\beta + 1)$ to establish I_e. That is,

$$I_e = (\beta + 1)I_b = (\beta + 1)\frac{V_i}{Z_b}$$

$$I_e = \frac{(\beta + 1)V_i}{\beta r_e + (\beta + 1)R_E}$$

$$I_e = \frac{V_i}{[\beta r_e/(\beta + 1)] + R_E}$$

$$(\beta + 1) \cong \beta \quad \text{and}$$

$$\frac{\beta r_e}{\beta + 1} \cong \frac{\beta r_e}{\beta} = r_e$$

$$I_e \cong \frac{V_i}{r_e + R_E}$$

If we now construct the network defined by the above Equation, the configuration of Fig. 3.39 is result. To determine Z_o, V_i is set to zero and:

$$Z_o = R_E \| r_e$$

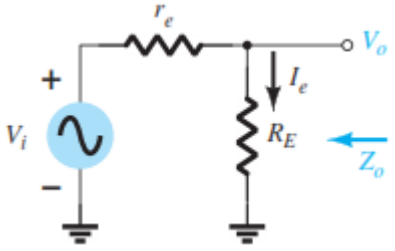


FIG. 3.39: Defining the output impedance for the emitter follower configuration

A_v: Figure 3.39 can be used to determine the voltage gain through an application of the voltage-divider rule:

$$V_o = \frac{R_E V_i}{R_E + r_e}$$

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e}}$$

Because R_E is usually much greater than r_e, $R_E + r_e \cong R_E$ and

$$\boxed{A_v = \frac{V_o}{V_i} \cong 1}$$

Example: For the emitter follower network of Fig 3.40, determine: (1) r_e. (2) Z_i, Z_o, and A_v. (3) Repeat part 2 with $r_o = 25\ k\Omega$.

Solution:

$$\textbf{(1)}\ I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{12\ V - 0.7\ V}{220\ k\Omega + (101)3.3\ k\Omega} = 20.42\ \mu A$$

$$I_E = (\beta + 1)I_B = (101)(20.42\ \mu A) = 2.062\ mA \text{ and } r_e = \frac{26\ mV}{I_E} = \frac{26\ mV}{2.062\ mA} = \mathbf{12.61\ \Omega}$$

$$\textbf{(2)}\ Z_b = \beta r_e + (\beta + 1)R_E = (100)(12.61\ \Omega) + (101)(3.3\ k\Omega) = 334.56\ k\Omega \cong \beta R_E$$

$$Z_i = R_B \| Z_b = 220\ k\Omega \| 334.56\ k\Omega = \mathbf{132.72\ k\Omega}$$

$$Z_o = R_E \| r_e = 3.3\ k\Omega \| 12.61\ \Omega = \mathbf{12.56\ \Omega} \cong r_e$$

$$A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e} = \frac{3.3\ k\Omega}{3.3\ k\Omega + 12.61\ \Omega} = \mathbf{0.996 \cong 1}$$

(3) Checking the condition $r_o \geq 10R_E$, we have: $25\ k\Omega \geq 10(3.3\ k\Omega) = 33\ k\Omega$, which is not satisfied. Therefore,

$$Z_b = \beta r_e + \frac{(\beta + 1)R_E}{1 + \frac{R_E}{r_o}} = (100)(12.61\ \Omega) + \frac{(100 + 1)3.3\ k\Omega}{1 + \frac{3.3\ k\Omega}{25\ k\Omega}} = 295.7\ k\Omega$$

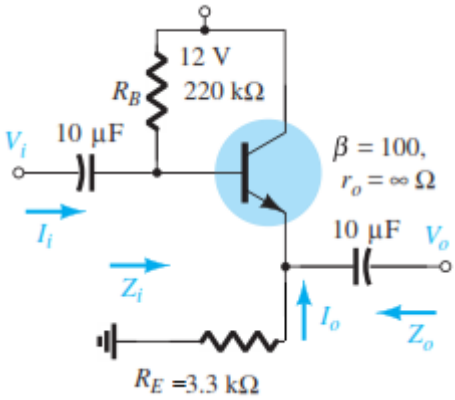
$$Z_i = R_B \| Z_b = 220\ k\Omega \| 295.7\ k\Omega$$

$$= \mathbf{126.15\ k\Omega} \text{ vs. } 132.72\ k\Omega \text{ obtained earlier}$$

$$Z_o = R_E \| r_e = \mathbf{12.56\ \Omega} \quad \text{as obtained earlier}$$

$$A_v = \frac{(\beta + 1)R_E / Z_b}{\left[1 + \frac{R_E}{r_o}\right]}$$

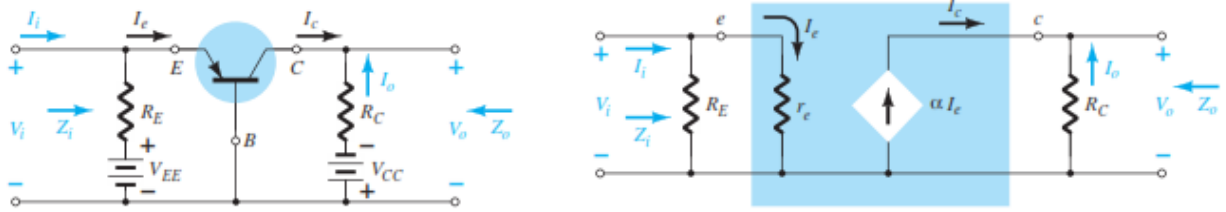
$$= \frac{(100 + 1)(3.3\ k\Omega)/295.7\ k\Omega}{\left[1 + \frac{3.3\ k\Omega}{25\ k\Omega}\right]} = \mathbf{0.996 \cong 1}$$



Common-Base Configuration

The common-base configuration is characterized as having a relatively low input and high output impedance and a current gain less than 1. The voltage gain, however, can be quite large. The

standard configuration appears in Fig. 3.40 (a), with the common base $\mathbf{r_e}$ equivalent model substituted in Fig. 3.40 (b). The transistor output impedance $\mathbf{r_o}$ is not included for the common-base configuration because it is in the MΩ range and can be ignored in parallel with the resistor R_C.



(a) (b)

FIG. 3.40 (a): Common-base configuration. (b) Substituting the $\mathbf{r_e}$ equivalent circuit into the ac equivalent network Fig. (a) .

$$Z_i = R_E \| r_e \qquad Z_o = R_C$$

$$V_o = -I_o R_C = -(-I_c)R_C = \alpha I_e R_C$$

$$I_e = \frac{V_i}{r_e} \quad \text{and} \quad V_o = \alpha\left(\frac{V_i}{r_e}\right)R_C$$

$$A_v = \frac{V_o}{V_i} = \frac{\alpha R_C}{r_e} \cong \frac{R_C}{r_e}$$

Assuming that $R_E \gg r_e$ yields

$$I_e = I_i \quad \text{and} \quad I_o = -\alpha I_e = -\alpha I_i$$

$$A_i = \frac{I_o}{I_i} = -\alpha \cong -1$$

The fact that A_v is a positive number shows that V_o and V_i are inphase for the common-base configuration. Also ro is typically in the MΩ range and sufficiently larger than the parallel resistance R_C to permit the approximation $r_o \| R_C \sim R_C$.

Example: For the network of Fig. 3.33, determine: re, Z_i, Z_o, A_v and A_i. Suppose R_E = 1K, R_C = 5K, α= 0.98, V_{EE}=2V and V_{CC} = 8V.

Solution:

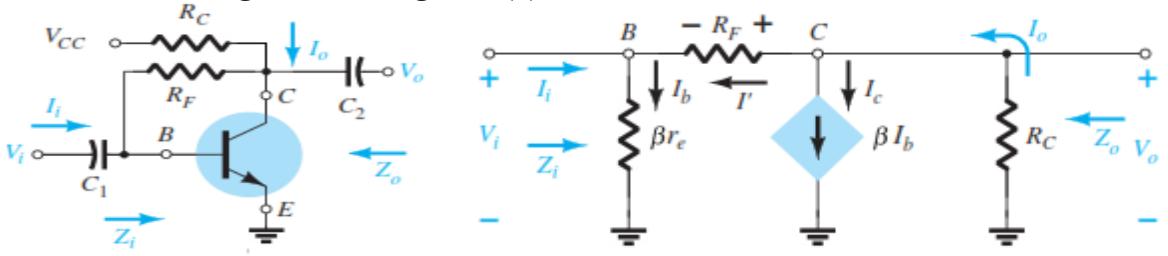
$$I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{2\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = 1.3\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{1.3\text{ mA}} = \mathbf{20\ \Omega}$$

$$Z_i = R_E \| r_e = 1\text{ k}\Omega \| 20\ \Omega$$
$$= \mathbf{19.61\ \Omega} \cong r_e$$
$$Z_o = R_C = \mathbf{5\ k\Omega}$$
$$A_v \cong \frac{R_C}{r_e} = \frac{5\text{ k}\Omega}{20\ \Omega} = \mathbf{250}$$
$$A_i = \mathbf{-0.98} \cong -1$$

Collector Feedback Configuration

The collector feedback network of Fig. 3.41 (a) employs a feedback path from collector to base to increase the stability of the system. Substituting the equivalent circuit and redrawing the network results in the configuration of Fig. 3.41(b).



(a) (b)

FIG. 3.41: (a) collector feedback configuration, (b) Substituting the $\mathbf{r_e}$ equivalent circuit into the ac equivalent network of Fig (a).

$$I_o = I' + \beta I_b \quad \text{and} \quad I' = \frac{V_o - V_i}{R_F} \quad \text{and} \quad V_o = -I_o R_C = -(I' + \beta I_b)R_C \quad \text{and} \quad V_i = I_b \beta r_e$$

$$\text{Thus} \quad I' = -\frac{(I' + \beta I_b)R_C - I_b \beta r_e}{R_F} = -\frac{I' R_C}{R_F} - \frac{\beta I_b R_C}{R_F} - \frac{I_b \beta r_e}{R_F} = -\beta I_b \frac{(R_C + r_e)}{R_C + R_F}$$

$$\text{Now } Z_i = \frac{V_i}{I_i}: \quad \text{And} \quad I_i = I_b - I' = I_b + \beta I_b \frac{(R_C + r_e)}{R_C + R_F} \quad \text{Thus} \quad I_i = I_b\left(1 + \beta \frac{(R_C + r_e)}{R_C + R_F}\right)$$

Substituting for Z_i leaves

$$Z_i = \frac{V_i}{I_i} = \frac{I_b \beta r_e}{I_b\left(1 + \beta \dfrac{(R_C + r_e)}{R_C + R_F}\right)} = \frac{\beta r_e}{1 + \beta \dfrac{(R_C + r_e)}{R_C + R_F}} \quad \text{Since } R_C \gg r_e$$

$$Z_i = \frac{\beta r_e}{1 + \dfrac{\beta R_C}{R_C + R_F}} \quad \text{Finaly} \quad \boxed{Z_i = \frac{r_e}{\dfrac{1}{\beta} + \dfrac{R_C}{R_C + R_F}}}$$

Zo: If we set V_i to zero as required to define Zo, the network will appear as shown in Fig. 3.42. The effect of $\boldsymbol{\beta r_e}$ is removed, and R_F appears in parallel with R_C, and

$$\boxed{Z_o \cong R_C \| R_F}$$

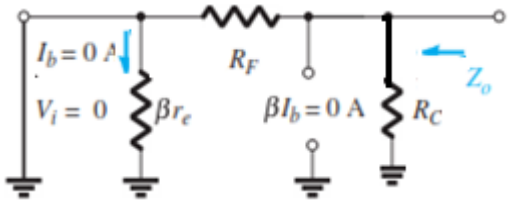


Fig. 3.42: Defining Zo for the collector feedback configuration.

Av: ----------

$$V_o = -I_o R_C = -(I' + \beta I_b)R_C$$

$$= -\left(-\beta I_b \frac{(R_C + r_e)}{R_C + R_F} + \beta I_b\right)R_C$$

$$V_o = -\beta I_b\left(1 - \frac{(R_C + r_e}{R_C + R_F}\right)R_C$$

$$A_v = \frac{V_o}{V_i} = \frac{-\beta I_b\left(1 - \dfrac{(R_C + r_e)}{R_C + R_F}\right)R_C}{\beta r_e I_b}$$

$$A_v = -\left(1 - \frac{R_C}{R_C + R_F}\right)\frac{R_C}{r_e}$$

$$A_v = -\frac{(R_C + R_F - R_C)R_C}{R_C + R_F \quad r_e}$$

$$\boxed{A_v = -\left(\frac{R_F}{R_C + R_F}\right)\frac{R_C}{r_e}}$$

For $R_F \gg R_C$ $\quad \boxed{A_v \cong -\dfrac{R_C}{r_e}}$

The negative sign of A_v indicates a 180° phase shift between V_o and V_i

Effect of R_L And R_S

All the parameters determined in the last few sections have been for an unloaded amplifier with the input voltage connected directly to a terminal of the transistor. In this section the effect of applying a load (R_L) to the output terminal and the effect of using a source with an internal resistance (R_S) will be investigated. The network of Fig. 3.36(a) is typical of those investigated in the previous section. Because a resistive load was not attached to the output terminal, the gain is commonly referred to as the **no-load gain** and given the following notation (A_{vNL}). In Fig. 3.36 (b) a load has been added in the form of a resistor R_L, which will change the overall gain of the system. This loaded gain is typically given the following notation (A_{vL}). In Fig. 3.36 (c) both a load and a source resistance have been introduced, which will have an additional effect on the gain of the system. The resulting gain is typically given the following notation (A_{vS}).

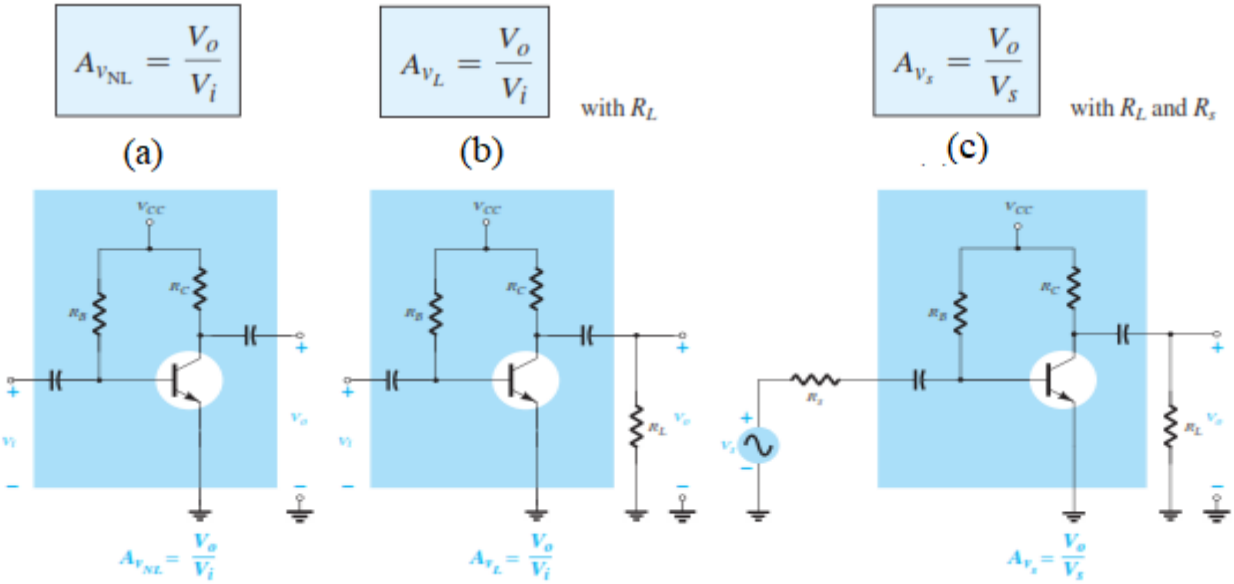


FIG. 3.36: Amplifier configurations: (a) unloaded; (b) loaded with (R_L); (c) loaded with a source resistance (R_L & R_S).

The analysis to follow will show that:

1. The loaded voltage gain of an amplifier is always less than the no-load gain.
2. The gain obtained with a source resistance in place will always be less than that obtained under loaded or unloaded conditions due to the drop in applied voltage across the source resistance.
3. In total, therefore, the highest gain is obtained under no-load conditions and the lowest gain with a source impedance and load in place. That is, for the same configuration:

   $A_{VNL} > A_{VL} > A_{VS}$.
4. For a particular design, the larger the level of R_L, the greater is the level of ac gain. In other words, the larger the load resistance, the closer it is to an open-circuit approximation that would result in the higher no-load gain.
5. For a particular amplifier, the smaller the internal resistance of the signal source, the greater is the overall gain. In other words, the closer the source resistance is to a short-circuit approximation, the greater is the gain because the effect of R_S will essentially be eliminated.
6. For any network, such as those shown in Fig. 3.36 that have coupling capacitors, the source and load resistance do not affect the dc biasing levels.

For the **fixed-bias transistor amplifier**, substituting the $\mathbf{r_e}$ equivalent circuit for the transistor and removing the dc parameters results in the configuration of Fig 3.37.

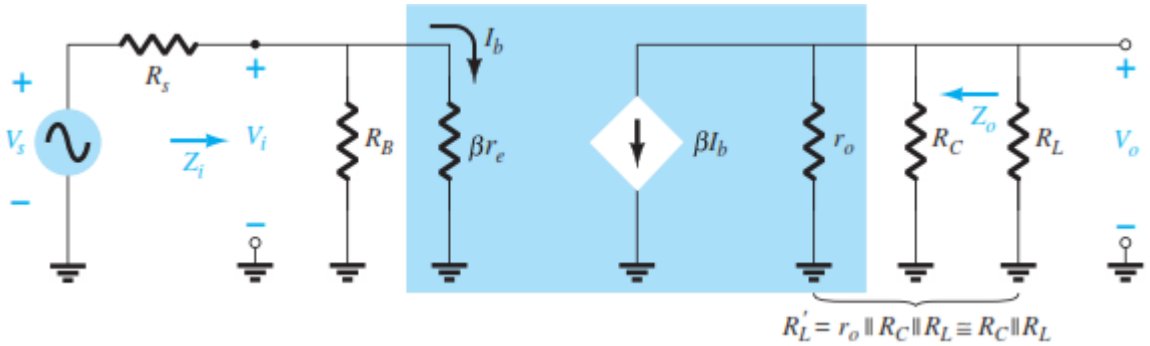


FIG. 3.37: the ac equivalent network for the network of Fig. 3.36(c).

The parallel combination of

$$R'_L = r_o \| R_C \| R_L \cong R_C \| R_L$$

$$V_o = -\beta I_b R'_L = -\beta I_b (R_C \| R_L)$$

$$I_b = \frac{V_i}{\beta r_e}$$

$$V_o = -\beta \left(\frac{V_i}{\beta r_e} \right) (R_C \| R_L)$$

$$\boxed{A_{v_L} = \frac{V_o}{V_i} = -\frac{R_C \| R_L}{r_e}}$$

The input impedance is $\boxed{Z_i = R_B \| \beta r_e}$

nd the output impedance is $\boxed{Z_o = R_C \| r_o}$

ıe overall gain from signal source V_s to output voltage V_o

$$V_i = \frac{Z_i V_s}{Z_i + R_s} \quad \& \quad \frac{V_i}{V_s} = \frac{Z_i}{Z_i + R_s}$$

$$v_s = \frac{V_o}{V_s} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_s} = A_{v_L} \frac{Z_i}{Z_i + R_s}$$

$$\boxed{A_{v_S} = \frac{Z_i}{Z_i + R_s} A_{v_L}}$$

Example: Using the parameter values for the fixed-bias configuration of Fig 3.38, with an applied load of 4.7 kΩ and a source resistance of 0.3 kΩ, determine the following and compare to the no-load values: A_{VL}, A_{VS}, Z_i and Z_o.

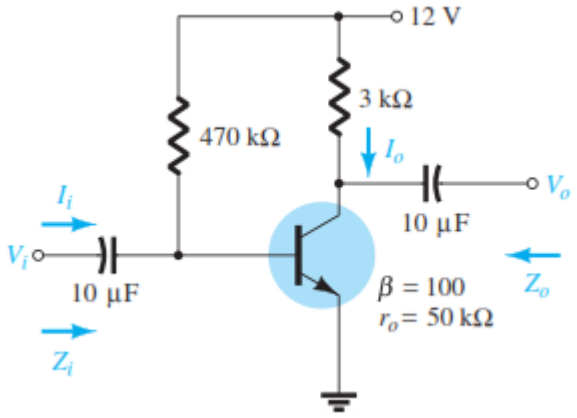


Figure 3.38: Fixed bias configuration.

DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{470\text{ k}\Omega} = 24.04\ \mu\text{A}$$

$$I_E = (\beta + 1) I_B = (101)(24.04\ \mu\text{A}) = 2.428\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.428\text{ mA}} = \mathbf{10.71\ \Omega}$$

$$\beta r_e = (100)(10.71\ \Omega) = 1.071\text{ k}\Omega$$

$$Z_i = R_B \| \beta r_e = 470\text{ k}\Omega \| 1.071\text{ k}\Omega = \mathbf{1.07\text{ k}\Omega}$$

$$Z_o = R_C = \mathbf{3\text{ k}\Omega}$$

$$A_{vNL} = -\frac{R_C}{r_e} = -\frac{3\text{ k}\Omega}{10.71\ \Omega} = \mathbf{-280.11}$$

$$A_{v_L} = -\frac{R_C \| R_L}{r_e} = -\frac{3\,\text{k}\Omega \| 4.7\,\text{k}\Omega}{10.71\,\Omega} = -\frac{1.831\,\text{k}\Omega}{10.71\,\Omega} = \mathbf{-170.98}$$

Which is significantly less than the no-load gain of -280.11.

$$A_{v_s} = \frac{Z_i}{Z_i + R_s} A_{v_L} = \frac{1.07\,\text{k}\Omega}{1.07\,\text{k}\Omega + 0.3\,\text{k}\Omega}(-170.98) = \mathbf{-133.54}$$

Which again is significantly less than A_{vNL} or A_{vL}.

From DC analysis:

$Z_i = \mathbf{1.07\,k\Omega}$

$Z_o = R_C = \mathbf{3\,k\Omega}$

For the **voltage-divider configuration** of Fig. 3.39(a) with an applied load and series source resistor the ac equivalent network is as shown in Fig 3.39(b). First note the strong similarities with fixed-bias transistor amplifier, the only difference being the parallel connection of R_1 and R_2 instead of just R_B. Everything else is exactly the same. The following equations result for the important parameters of the configuration:

$$A_{v_L} = \frac{V_o}{V_i} = -\frac{R_C \| R_L}{r_e}$$

$$Z_i = R_1 \| R_2 \| \beta r_e$$

$$Z_o = R_C \| r_o$$

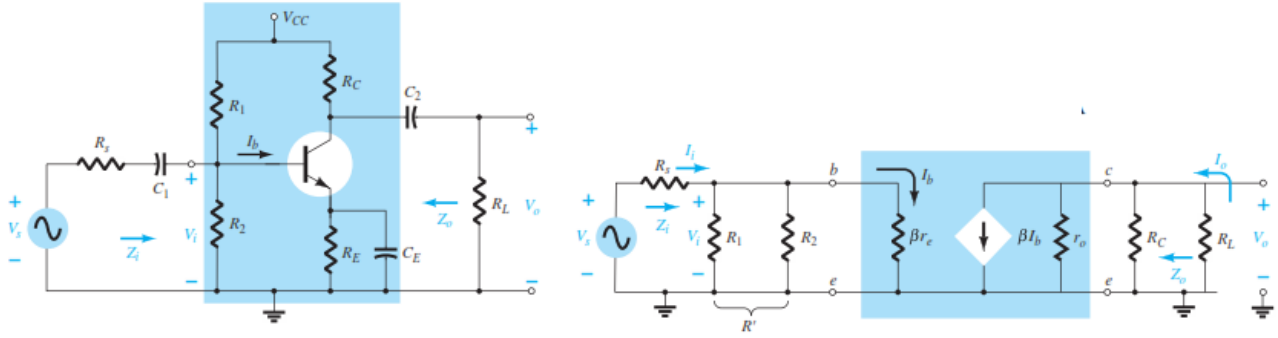


FIG. 3.39(a): Voltage-divider bias configuration with R_s and R_L. (b) Substituting the re equivalent circuit into the ac equivalent network of voltage-divider bias configuration.

For the **emitter-follower configuration** of Fig. 3.40 (a), the small-signal ac equivalent network is as shown in Fig. 3.40 (b). The only difference between this configuration and the unloaded configuration is the parallel combination of RE and RL and the addition of the source resistor R_s. The equations for the quantities of interest can therefore be determined by simply replacing R_E by $R_E \| R_L$ wherever R_E appears. That is,

$$A_{v_L} = \frac{V_o}{V_i} = \frac{R_E \| R_L}{R_E \| R_L + r_e}$$

$$Z_i = R_B \| Z_b$$

$$Z_b \cong \beta(R_E \| R_L)$$

$$Z_o \cong r_e$$

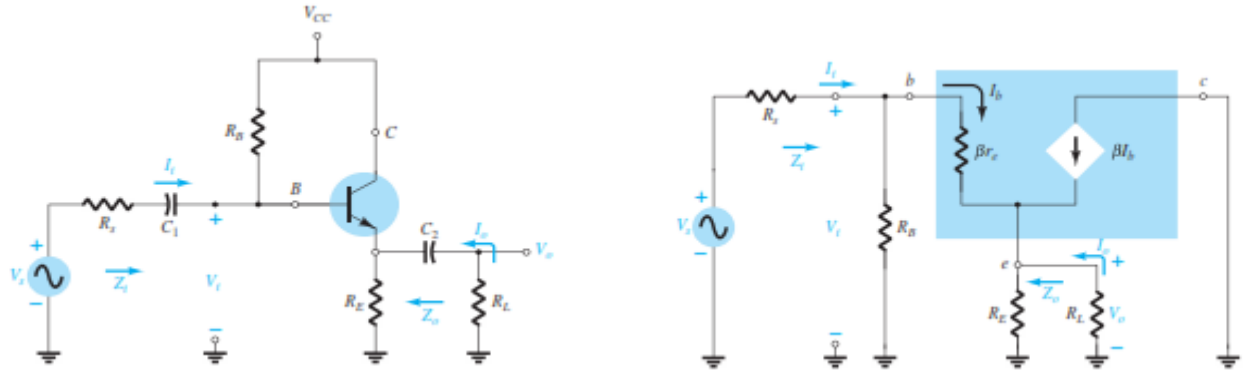


FIG. 3.40 (a): Emitter follower configuration with R_s and R_L. (b) Substituting the re equivalent circuit into the ac equivalent network of Fig. (a).

Determining the Current Gain

For each transistor configuration, the current gain can be determined directly from the voltage gain, the defined load, and the input impedance. The derivation of the equation linking the voltage and current gains can be derived using the two-port configuration of Fig. 3.41.

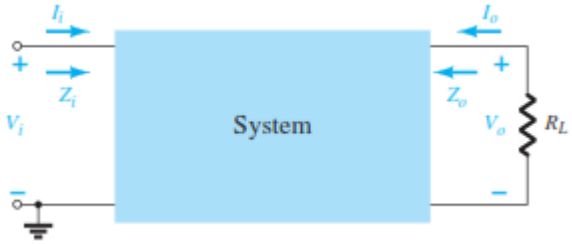


FIG. 3.41: determining the current gain using the voltage gain.

The current gain is defined by: $\mathbf{A_i = I_o / I_i}$. Applying Ohm's law to the input and output circuits results in: $\mathbf{I_i = V_i / Z_i}$ **and** $\mathbf{I_o = - V_o / R_.}$

The minus sign associated with the output equation is simply there to indicate that the polarity of the output voltage is determined by an output current having the opposite direction. By definition, the input and output currents have a direction entering the two-port configuration. Substituting the results in;

$$A_{i_L} = \frac{I_o}{I_i} = \frac{-\frac{V_o}{R_L}}{\frac{V_i}{Z_i}} = -\frac{V_o}{V_i}\cdot\frac{Z_i}{R_L}$$

$$\boxed{A_{i_L} = -A_{v_L}\frac{Z_i}{R_L}}$$

To demonstrate the validity of the above Eq. Consider the fixed bias configuration in previous example, Fig 3.42, using the results:

$Z_i = \mathbf{1.07\,k\Omega}, Z_o = R_C = \mathbf{3\,k\Omega}$

& $A_{v_L} = \mathbf{-170.98}$

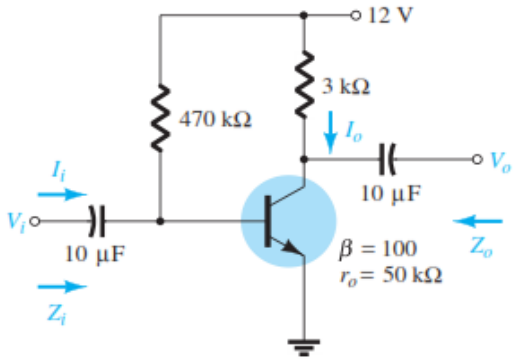


Fig. 3.42: Fixed bias configuration

$$I_i = \frac{V_i}{Z_i} = \frac{V_i}{\mathbf{1.07\ k\Omega}} \text{ and } I_o = -\frac{V_o}{R_L} = -\frac{V_o}{\mathbf{3\ k\Omega}}$$

$$A_{i_L} = \frac{I_o}{I_i} = \frac{\left(-\frac{V_o}{\mathbf{3\ k\Omega}}\right)}{\frac{V_i}{\mathbf{1.07\ k\Omega}}} = -\left(\frac{V_o}{V_i}\right)\left(\frac{\mathbf{1.07\ k\Omega}}{\mathbf{3\ k\Omega}}\right)$$

$$A_{i_L} = -(\mathbf{-170.98})\left(\frac{\mathbf{1.07\ k\Omega}}{\mathbf{3\ k\Omega}}\right) = \mathbf{61}$$

$$A_{i_L} = -A_{v_L}\frac{Z_i}{R_L} = -(\mathbf{-170.98})\left(\frac{\mathbf{1.07\ k\Omega}}{\mathbf{3\ k\Omega}}\right) = \mathbf{61}$$

As a second example, consider the common-base bias configuration. In this case the voltage gain is: $\mathbf{A_{vL} \approx R_C / r_e}$ and $\mathbf{Z_i = R_E \parallel r_e \sim r_e}$, with RL defined as RC due to the location of Io. The result is the following:

$$A_{i_L} = -A_{v_L}\frac{Z_i}{R_L} = \left(-\frac{R_C}{r_e}\right)\left(\frac{r_e}{R_C}\right) \cong -1$$

Which agrees with the solution of that section because Ic~ Ie. Note, in this case, that the output current has the opposite direction to that appearing in the networks of that section due to the minus sign.

Example: Determine A_{vL} and A_{vs} for the network of previous Example showed that A_{vNL} = -280, Zi = 1.07 kΩ and Zo = 3 kΩ. Suppose, RL = 4.7 kΩ and Rs= 0.3 kΩ.

Solution:

$$A_{v_L} = \frac{R_L}{R_L + R_o}A_{v_{NL}}$$

$$= \frac{4.7\ \text{k}\Omega}{4.7\ \text{k}\Omega + 3\ \text{k}\Omega}(-280.11) = \mathbf{-170.98}$$

$$A_{v_s} = \frac{R_i}{R_i + R_s}\cdot\frac{R_L}{R_L + R_o}A_{v_{NL}}$$

$$= \frac{1.07\ \text{k}\Omega}{1.07\ \text{k}\Omega + 0.3\ \text{k}\Omega}\cdot\frac{4.7\ \text{k}\Omega}{4.7\ \text{k}\Omega + 3\ \text{k}\Omega}(-280.11)$$

$$= (0.781)(0.610)(-280.11) = \mathbf{-133.45}$$