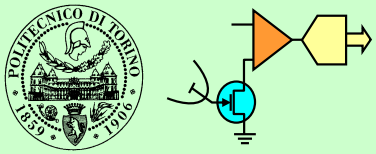
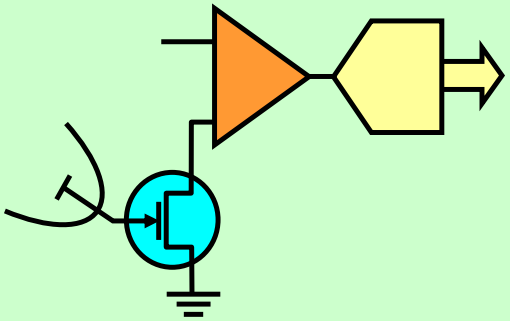


Politecnico di Torino - ICT School

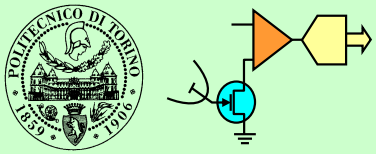
Analog and Telecommunication Electronics

A1 – MOS and Bipolar transistor

- » MOS structure and characteristic
- » BJT structure and characteristic
- » Large signal models
- » Small signal model



AY 2015-16

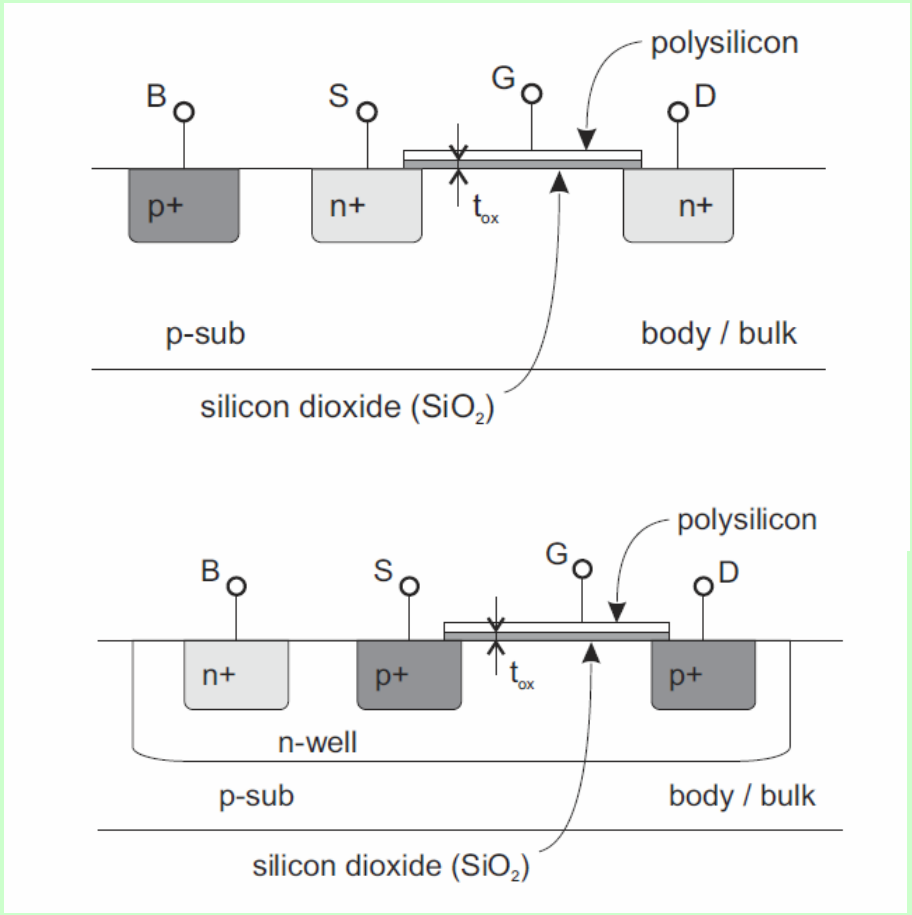


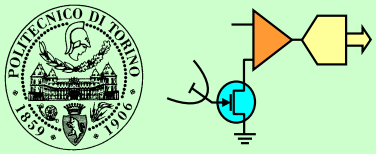
Lesson A1: MOS and BJT devices

- A refresh lesson!
- MOS and BJT structures and characteristic
  - Comparison of structure, parameters, models
  - Emphasis on similarities
- Operating regions
- Large signal models
- Small signal model
- Difference MOS/BJT
  - Some drawings from:
    - » F. Fiori: Introduction to CMOS Analog Circuits.
    - » F. Bonani: High speed Electron Devices slides

Structure of N- and P-MOS devices

- N-MOS
- P-MOS



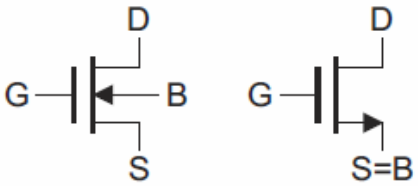


Symbols fom MOS devices

- Correspondence with BJT: S→E; G→B; D→C
- Current flowing in arrow direction

- N-MOS: (npn BJT)

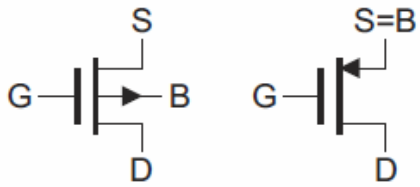
n-channel



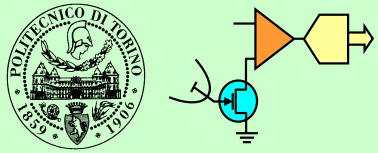
used when bulk terminal is connected to the source (common bulk)

- P-MOS: (pnp BJT)

p-channel



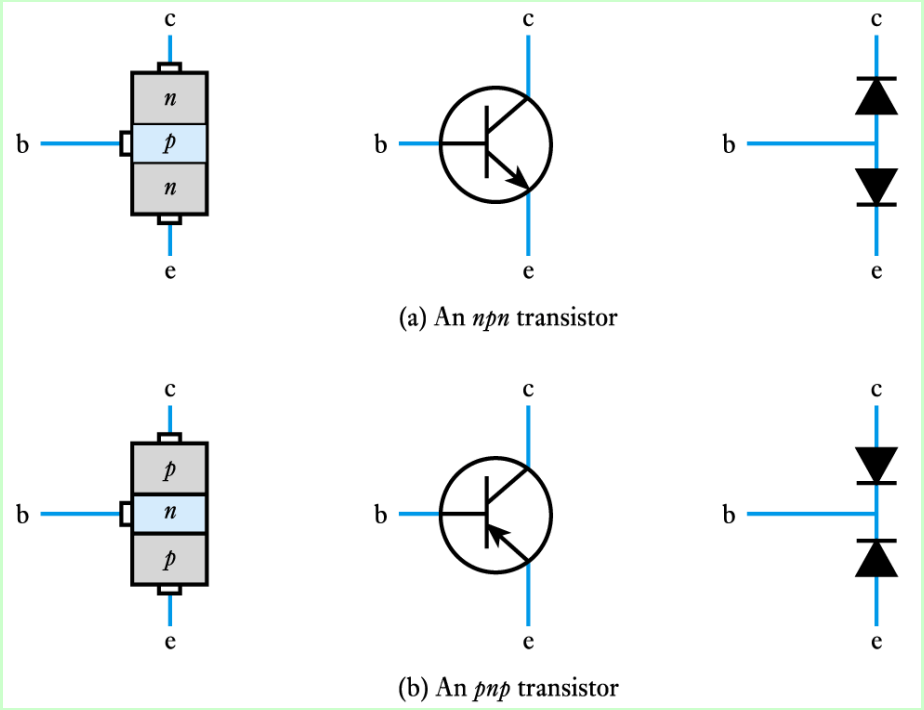
used when bulk terminal (n-well) is connected to the source



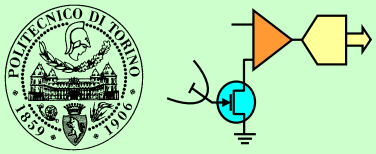
Structure of NPN and PNP devices

- NPN
(N-MOS)

- PNP
(P-MOS)



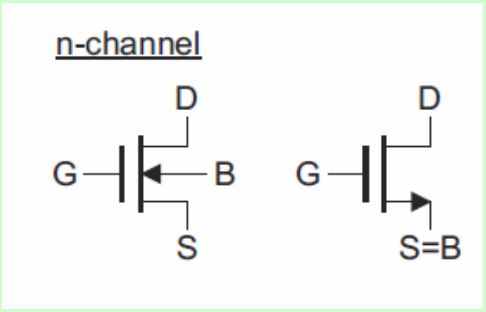
– (real devices use mostly planar structures)

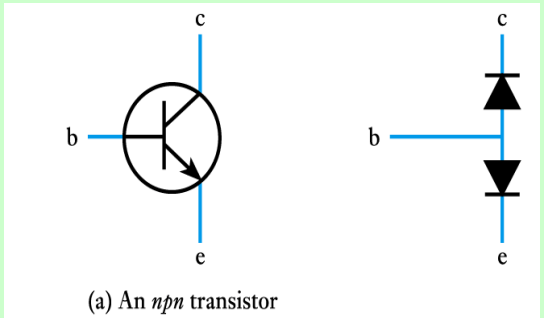


Correspondence MOS/BJT devices

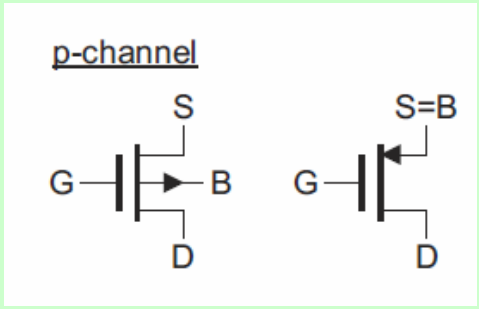
- S→E; G→B; D→C
- Current can flow in arrow direction

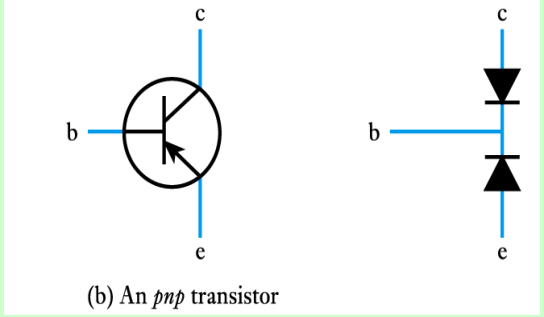
- N-MOS
  npn BJT





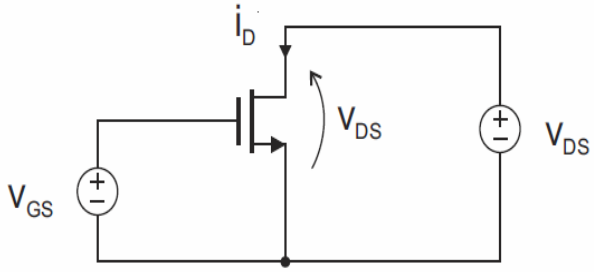
- P-MOS:
  pnp BJT

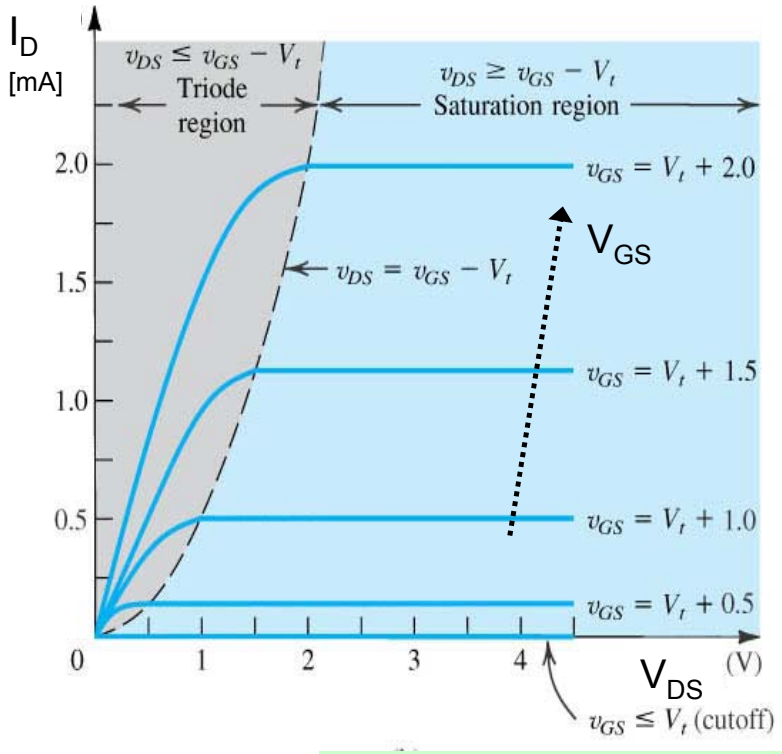




MOS output characteristics

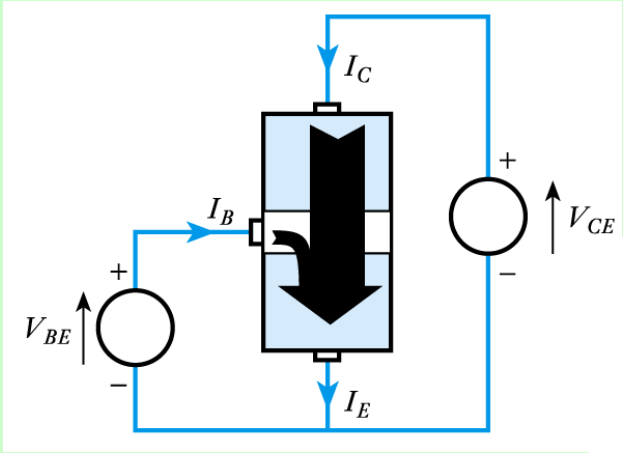
- Operating regions
  - Triode →Low V_{DS}
  - Saturation → Const. Id ("active" region in BJT)
  - (cutoff)

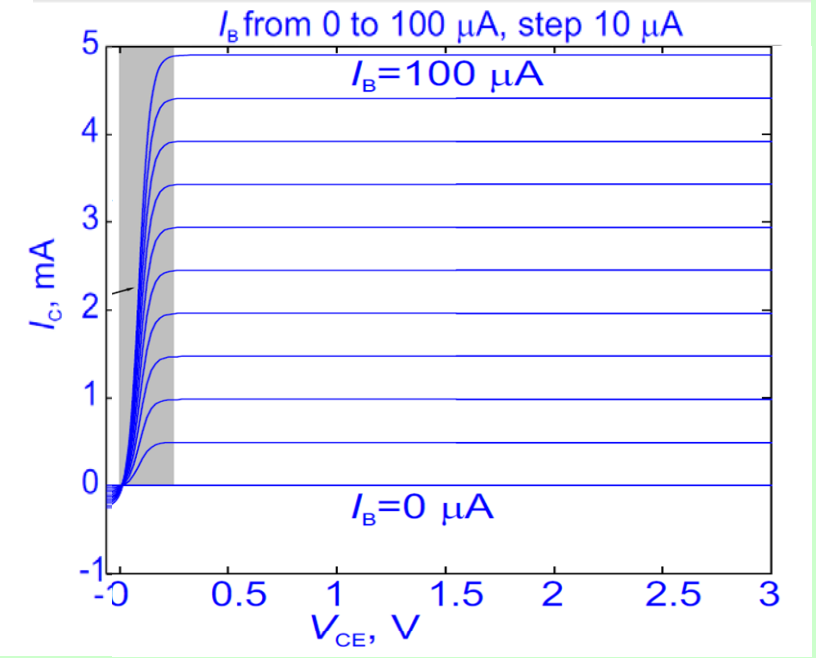




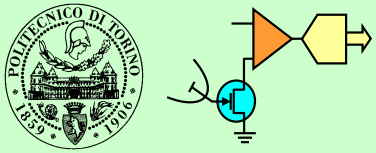
$$i_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left[2(v_{GS} - V_{TH})v_{DS} - v_{DS}^2\right]$$

BJT output characteristic



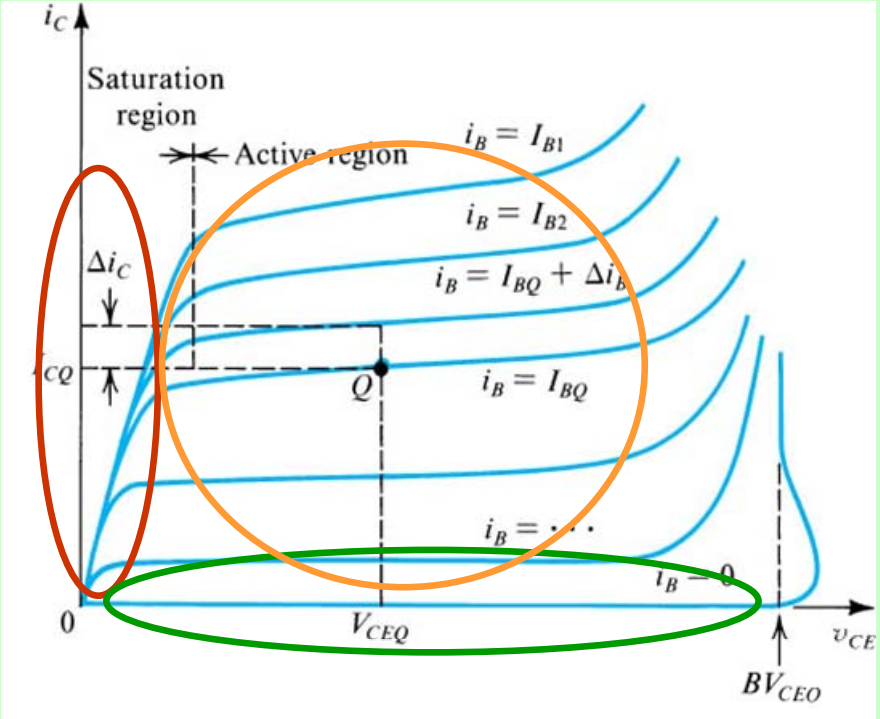


- Operating regions
  - Saturation → Low V_{CE}
  - Active → Constant Ic
  - (cutoff)



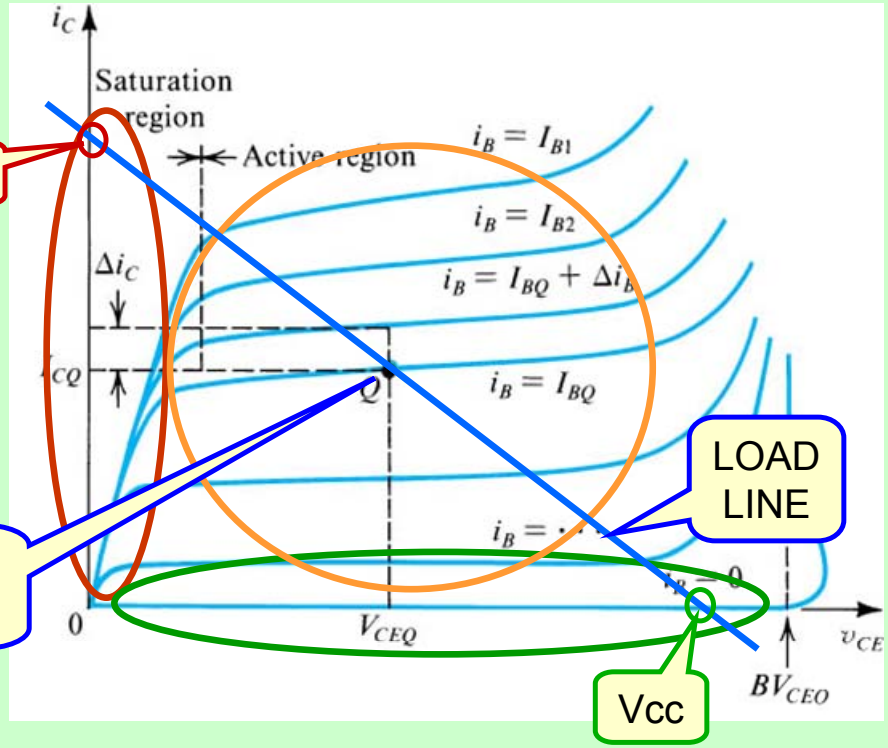
Switch or amplifier?

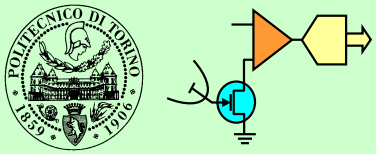
- Use as amplifier
  - BJT: Active region
    MOS: Saturation
- Switch ON
  - BJT: Saturation
    MOS: Resistive
- Switch OFF
  - Cutoff



Operation in a circuit

- A LOAD LINE models the external circuit
- Operating points must be on load line AND on device I(V)

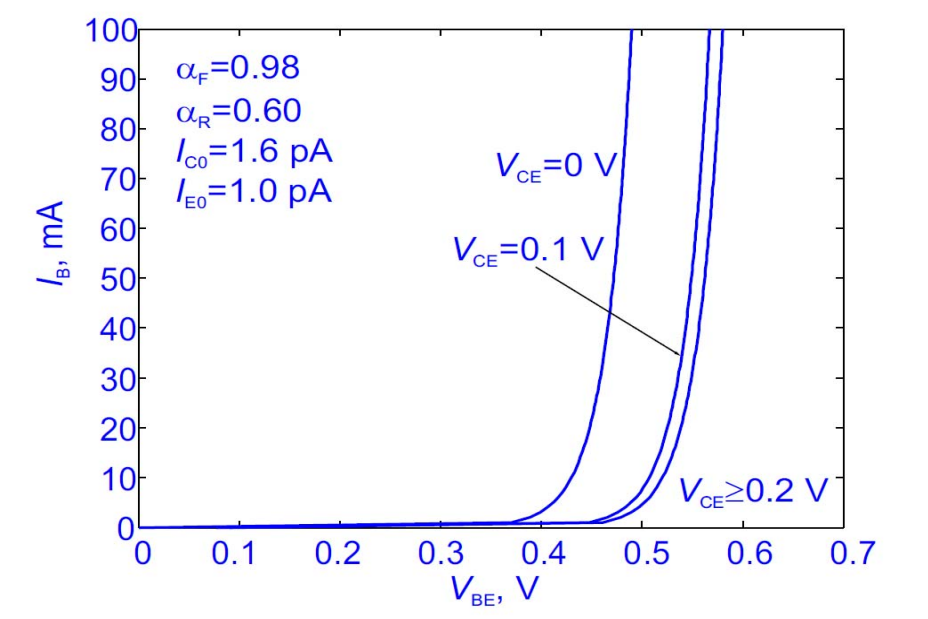


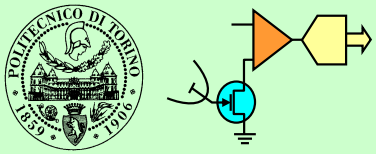


BJT input characteristic and model

- BE junction:
  - Emitter current (approx.)
  - $V_{BE} \approx 0.6$ V
- Single model fits all operating regions
- Strong temperature dependence

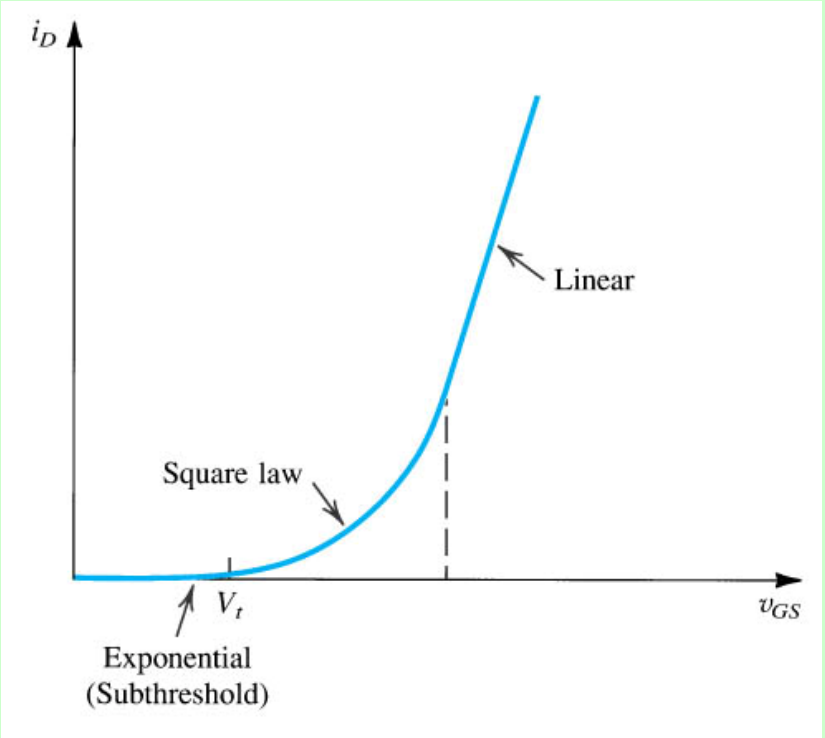
$$I_F = I_{E0}\left[\exp\left(\frac{V_{BE}}{V_T}\right) - 1\right]$$





MOS models

- Model depends on operating point
  - Low Vgs (sub-threshold):
    - » Exponential
  - Medium Vgs:
    - » Square law
  - High Vgs:
    - » Linear



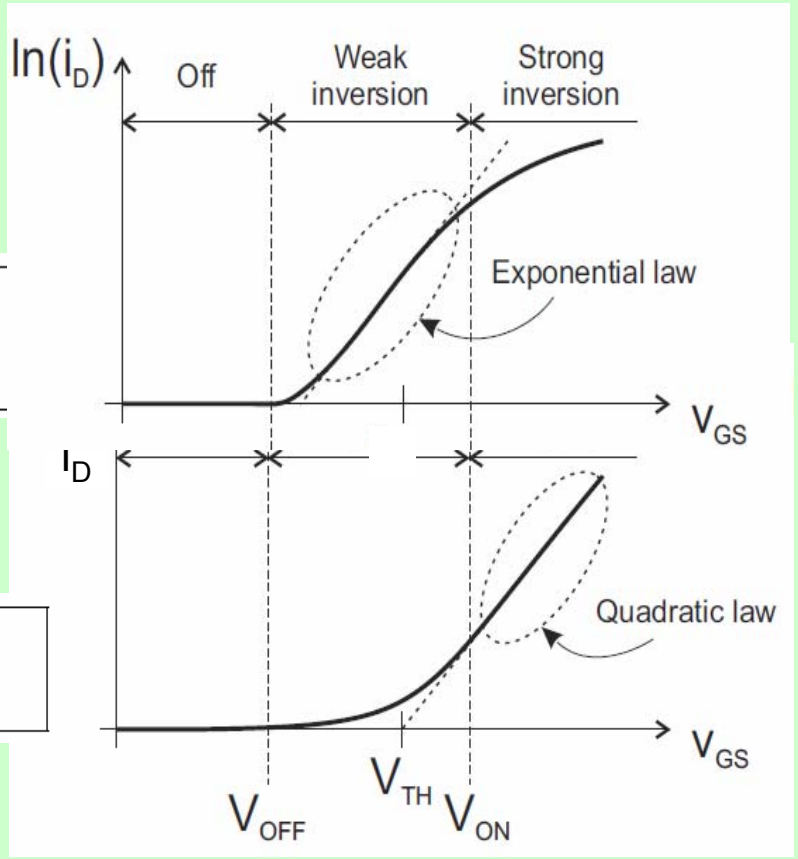
MOS transcharacteristic

- No unique Id(Vgs) relation
  - Weak inversion: exponential

$$i_D = I_{DO}\frac{W}{L}e^{\frac{v_{GS}}{\eta V_T}}$$

  - Strong inversion: quadratic

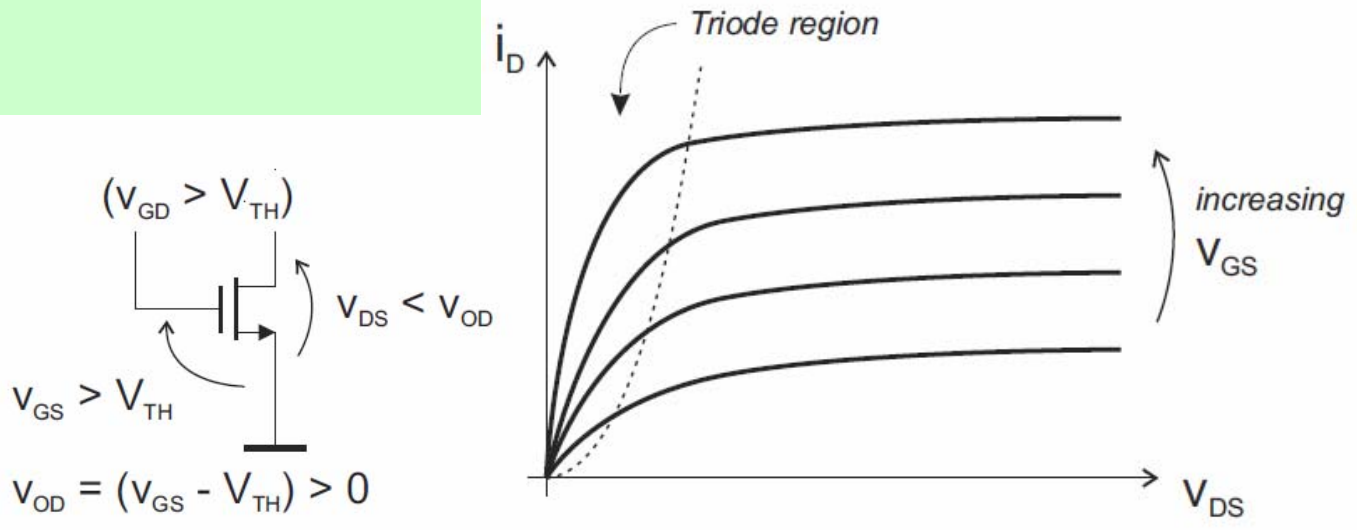
$$i_D = \mu_n \frac{C_{ox}}{2}\frac{W}{L'}(v_{OD})^2$$

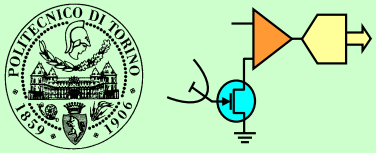


MOS Triode region

$$v_{OD} \triangleq v_{GS} - V_{TH}.$$ (overdrive voltage)

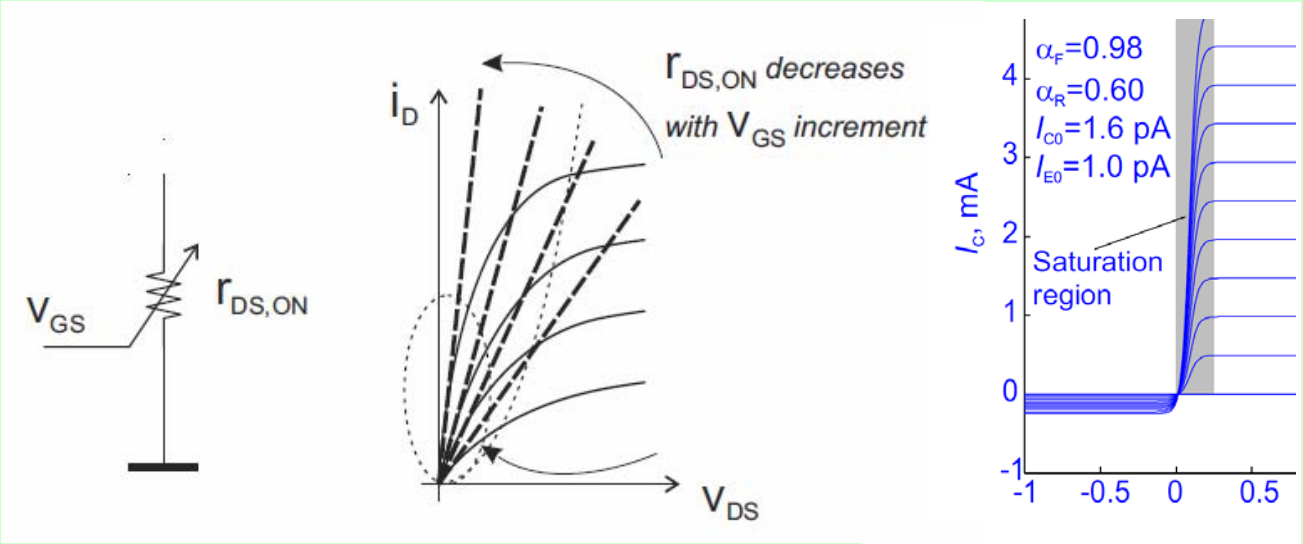
$$i_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(2v_{OD}v_{DS} - v_{DS}^2)$$



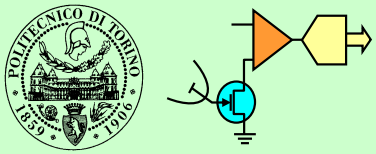


MOS as variable resistor

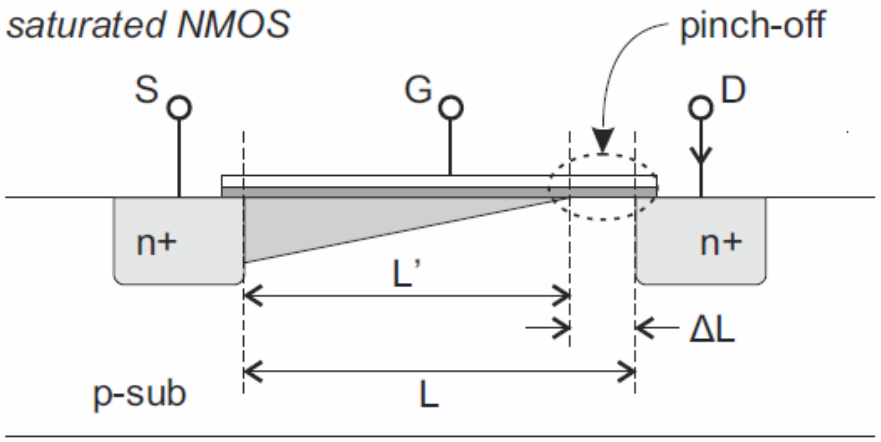
- MOS with low V_{DS} → $r_{DS} = dV_{DS}/dI_D$ depends on V_{GS}
- BJT has fixed dV_{CE}/dI_C → not good as variable resistor



MOS BJT



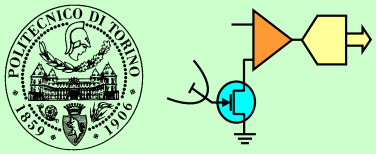
Channel pinch-off



$$i_D = \mu_n \frac{C_{ox}}{2} \frac{W}{L'} (v_{OD})^2$$

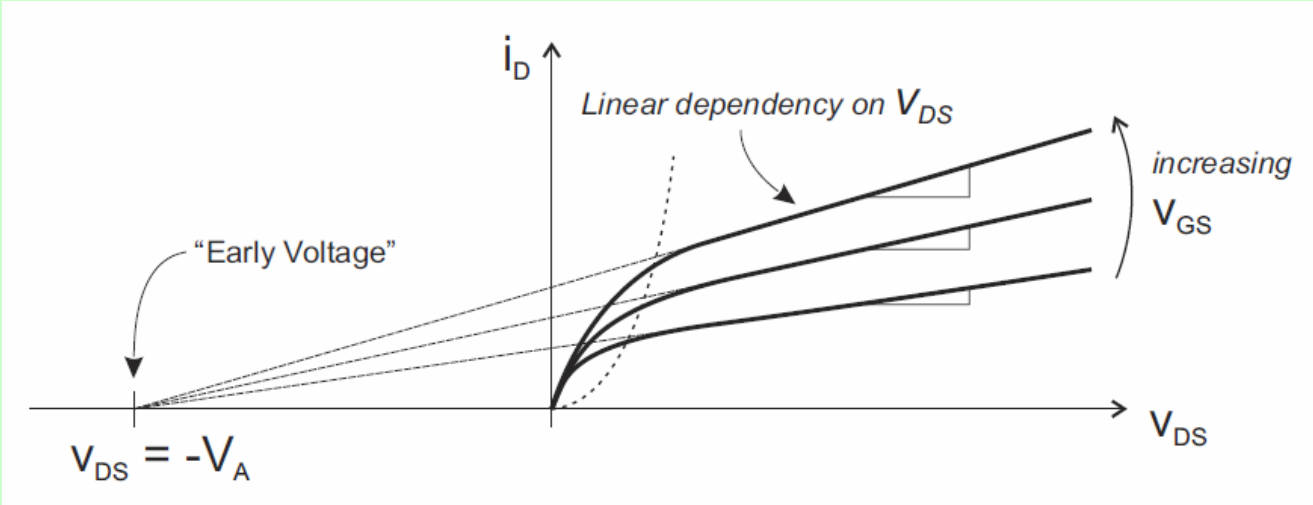
$$v_{OD} \triangleq v_{GS} - V_{TH}.$$

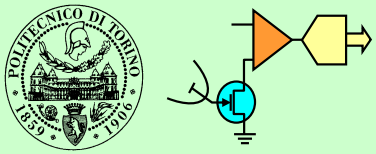
$$i_D = \mu_n \frac{C_{ox}}{2} \frac{W}{L} (v_{OD})^2 (1 + \lambda v_{DS}).$$



MOS Channel lenght modulation

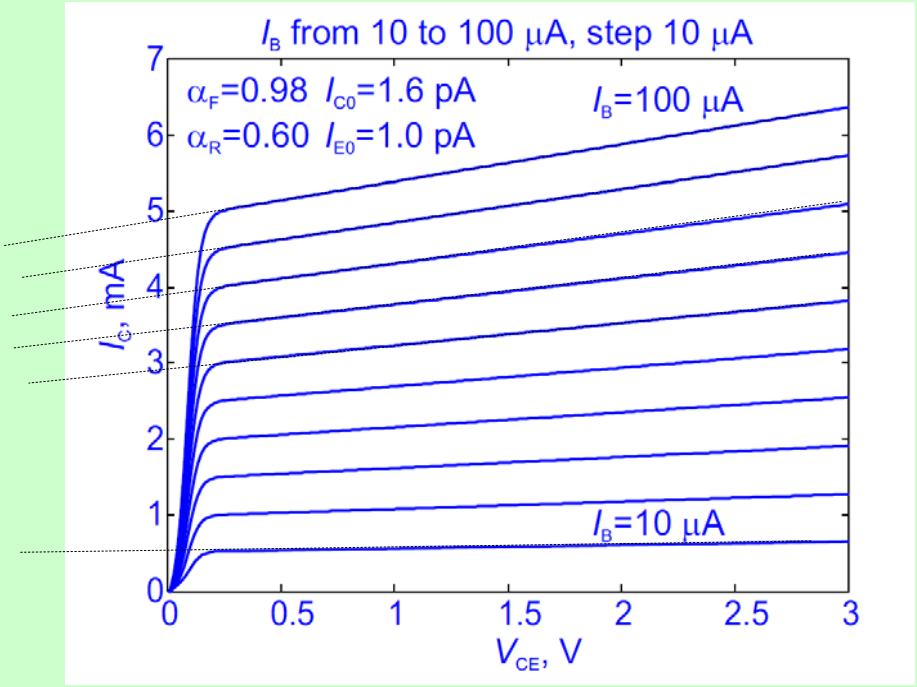
- Id depends on Vds
- Model in saturation region must include an equivalent output resistance r_O
- Similar to Early effect in BJT





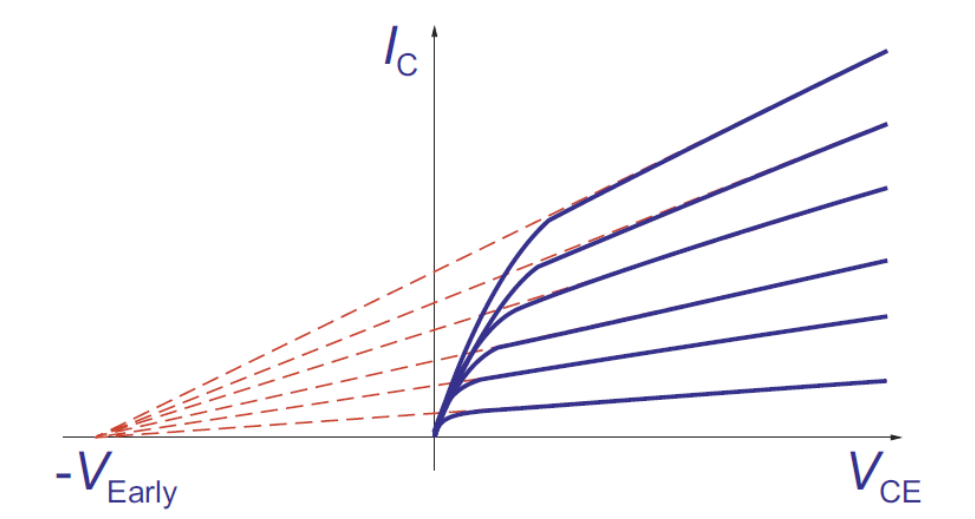
BJT Early effect

- As V_{CE} increases base region width decreases
  - In the active region, I_C depends on V_{CE}

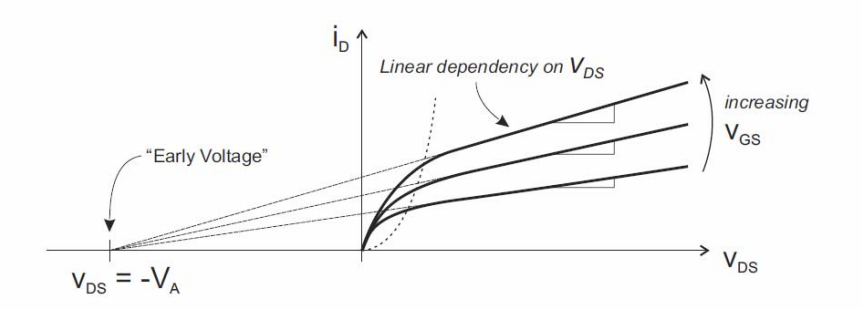


BJT Early voltage

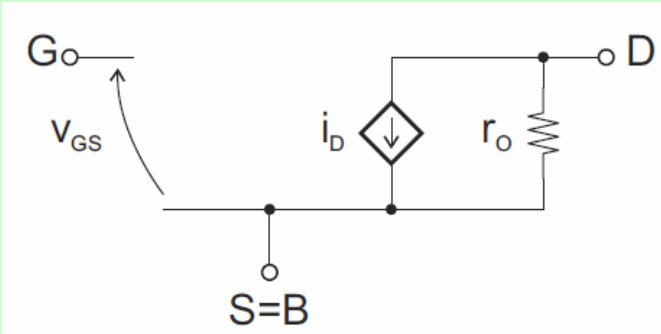
- r_O in small signal model



- Similar to channel lenght modulation in MOS

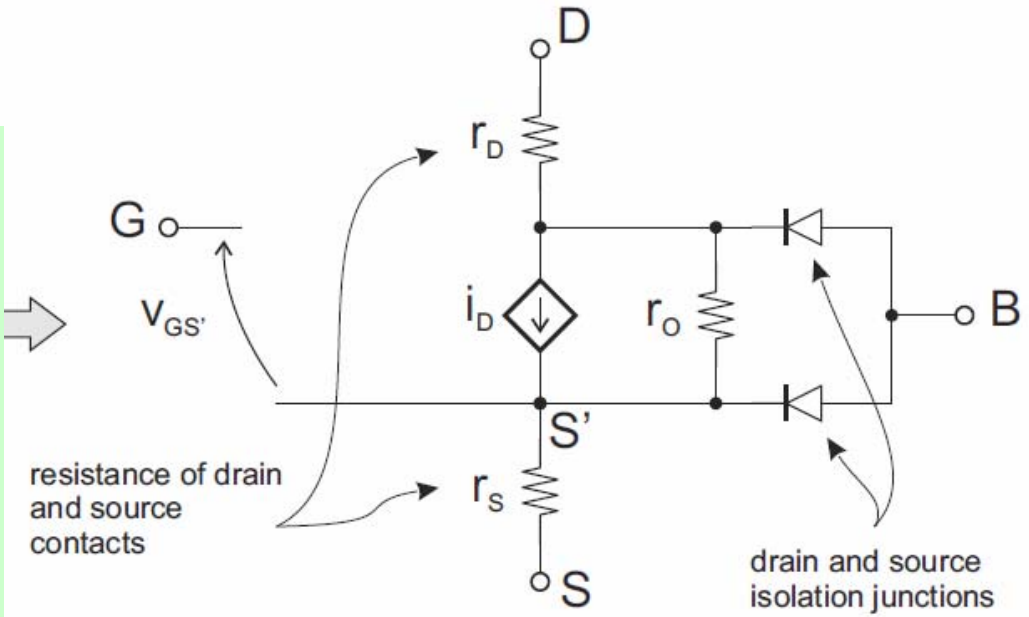


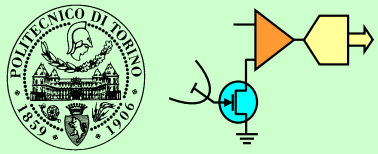
MOS large signal model (saturation)



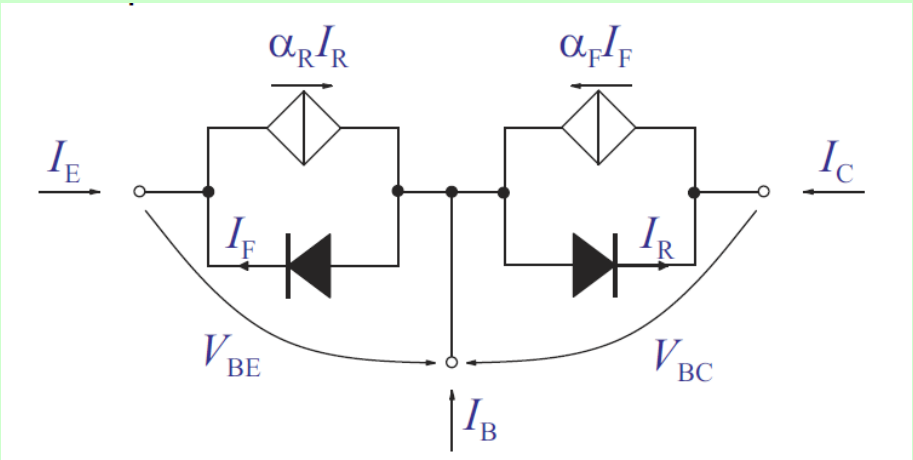
$$i_D = \mu_n \frac{C_{ox}}{2} \frac{W}{L} (v_{OD})^2 (1 + \lambda v_{DS}).$$

Power MOS-FET





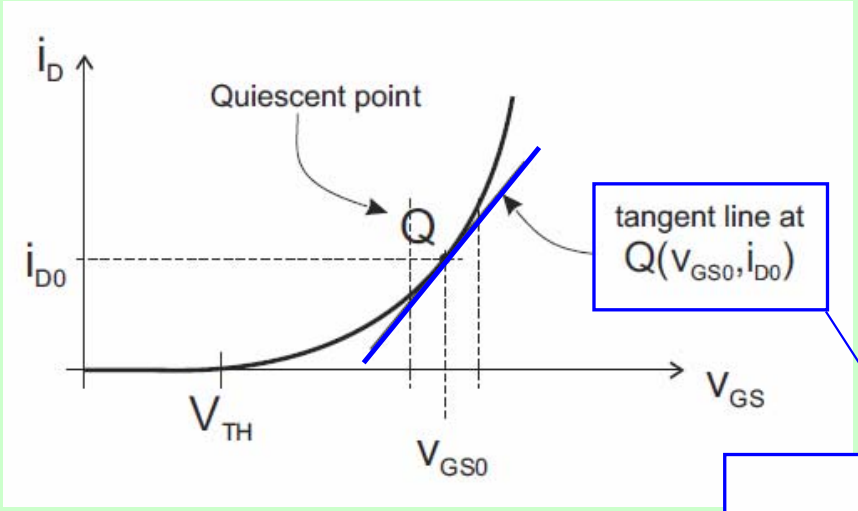
BJT Ebers-Moll model



$$I_C \approx \frac{qAD_{nB}n_i^2}{N_{AB}L_{nB}} \left[\sinh\left(\frac{w_B}{L_{nB}}\right)\right]^{-1} \left[\exp\left(\frac{V_{BE}}{V_T}\right) - 1\right]$$

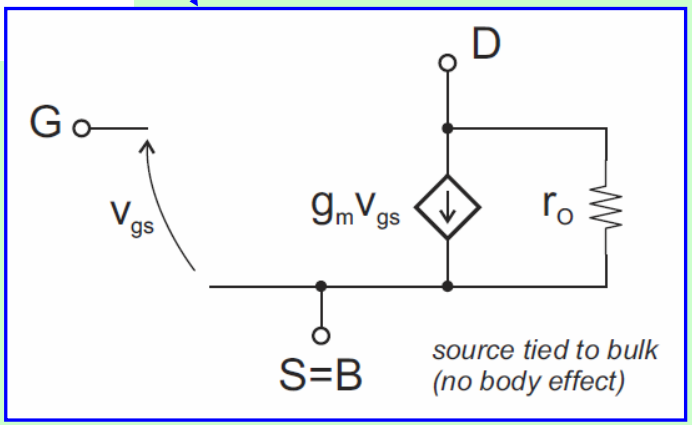
$$I_C = I_E = I_S\, e^{\frac{V_{BE}}{V_T}}$$

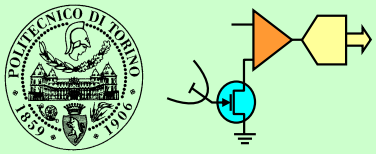
MOS small-signal model



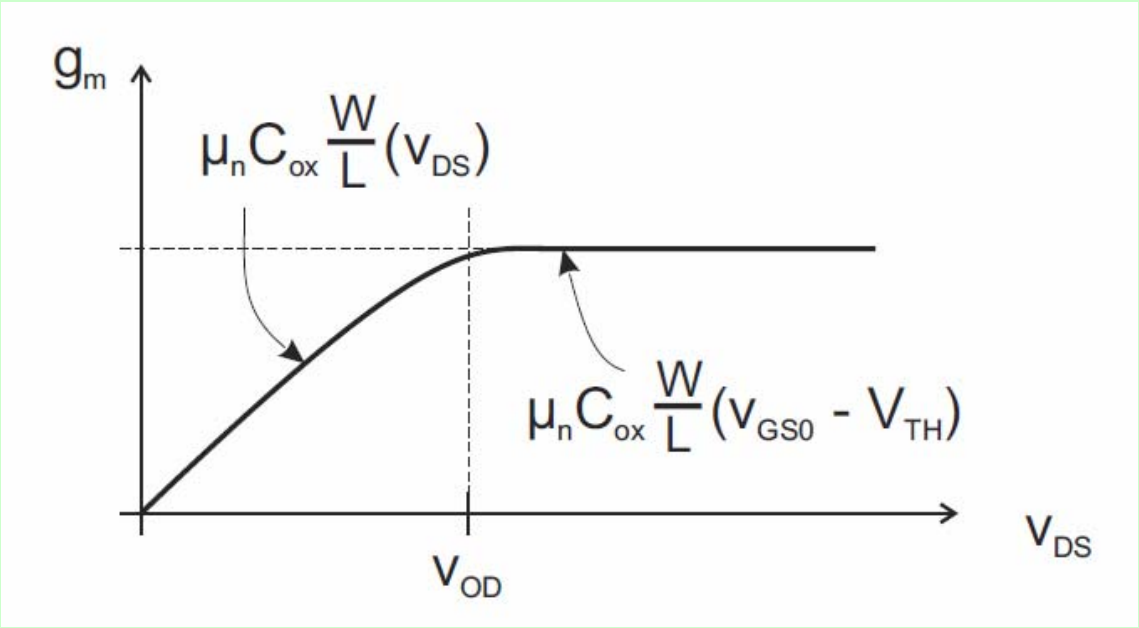
$$i_D = \mu_n \frac{C_{ox}}{2} \frac{W}{L} (v_{GS} - V_{TH})^2$$

$$g_m = \mu_n C_{ox} \frac{W}{L} (v_{OD}) .$$





MOS g_m in triode and saturation regions



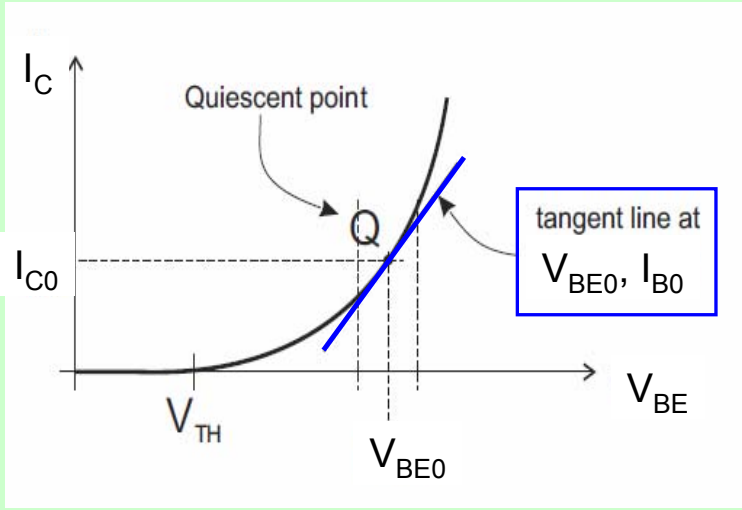
- Key parameter: W/L

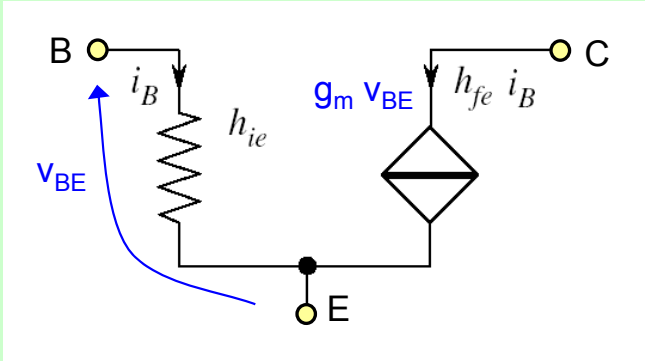
BJT small-signal model

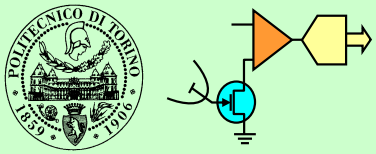
- If $V_{BE} >> V_T$

$$I_C = I_E = I_S\, e^{\frac{V_{BE}}{V_T}}$$

- Linear approximantion (tangent) near an operating point (V_{BE0}, I_{B0})
- Simplified models
  - Hibrid
  - Transconductance

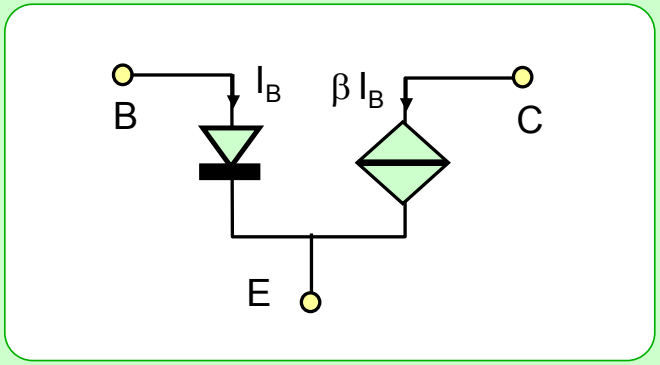






BJT simplified models

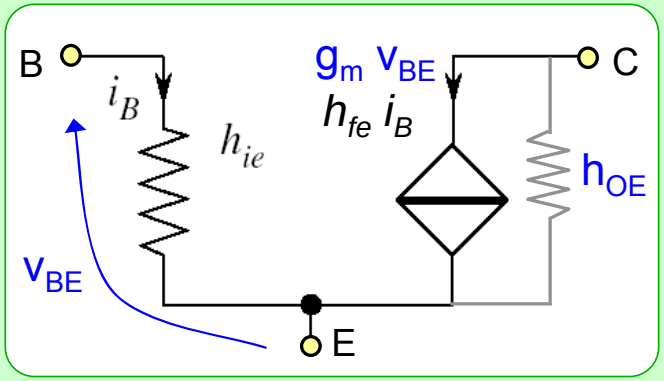
1) Simplified model for bias point analysis (active area)

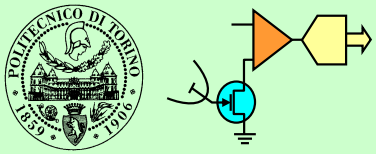


2) Simplified model for small signal analysis, CE configuration. Parameters:
h_{fe} i_B or g_m v_{BE}

$$g_m = I_C/V_T$$

$$h_{ie} = V_T * h_{fe}/I_C$$





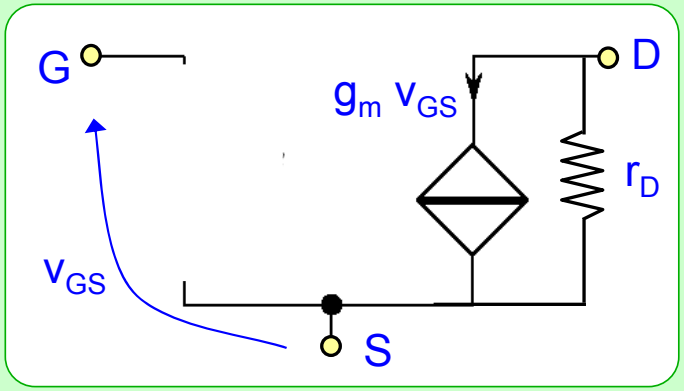
MOS simplified models

1) Bias point analysis with nonlinear model
   - Define the parameters to be used for small-signal analysis
   - Use Id(Vgs) equation (order 2 or better model)

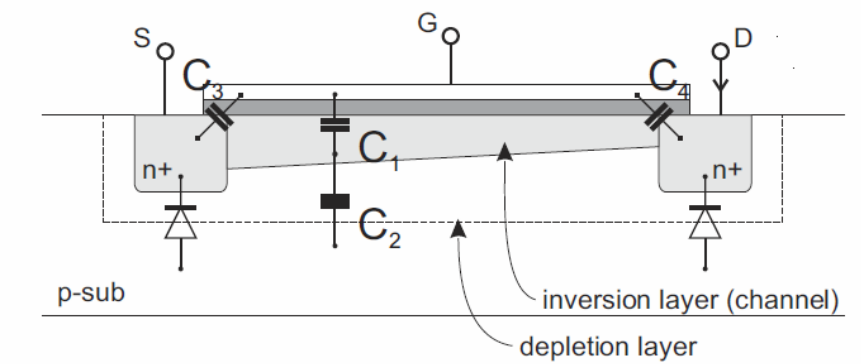
2) Simplified model for small signal analysis (similar to BJT), CS configuration. Parameters: g_m , r_D

g_m = ….(II ord)

$r_D = dV_{DS}/dI_D$



MOS parasitic capacitances

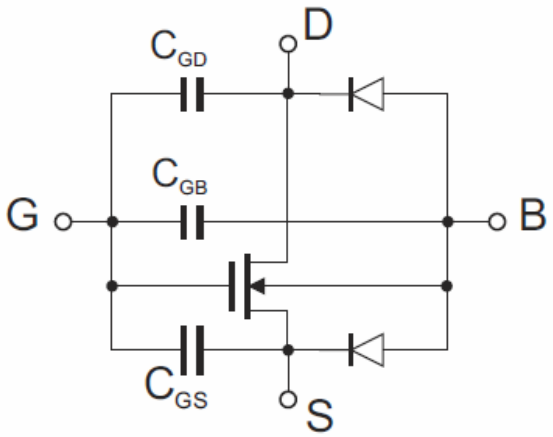


- C3 → C_{GS}
- C4 → C_{GD}

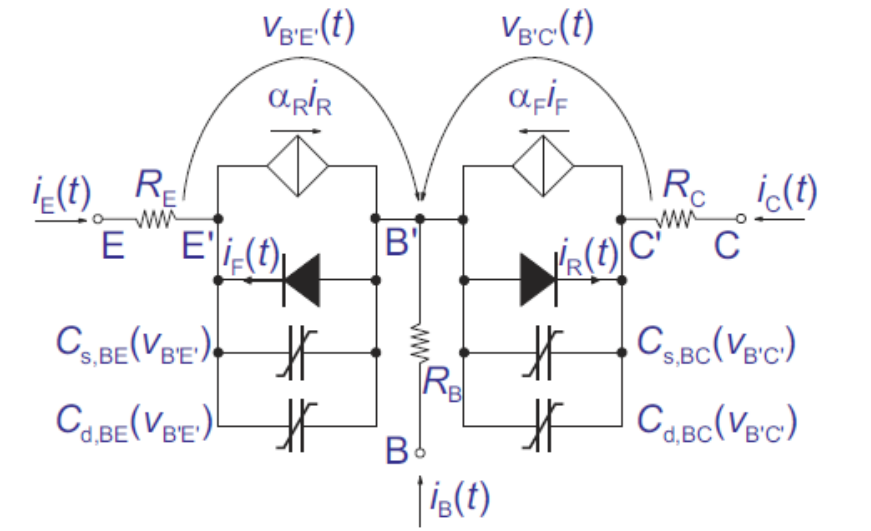
$$C_{GS} >> C_{GD} > C_{GB}$$

$$C_{GS} \approx C_{ox} L_D W_{eff} + \frac{2}{3} C_{ox}(W_{eff} L_{eff})$$

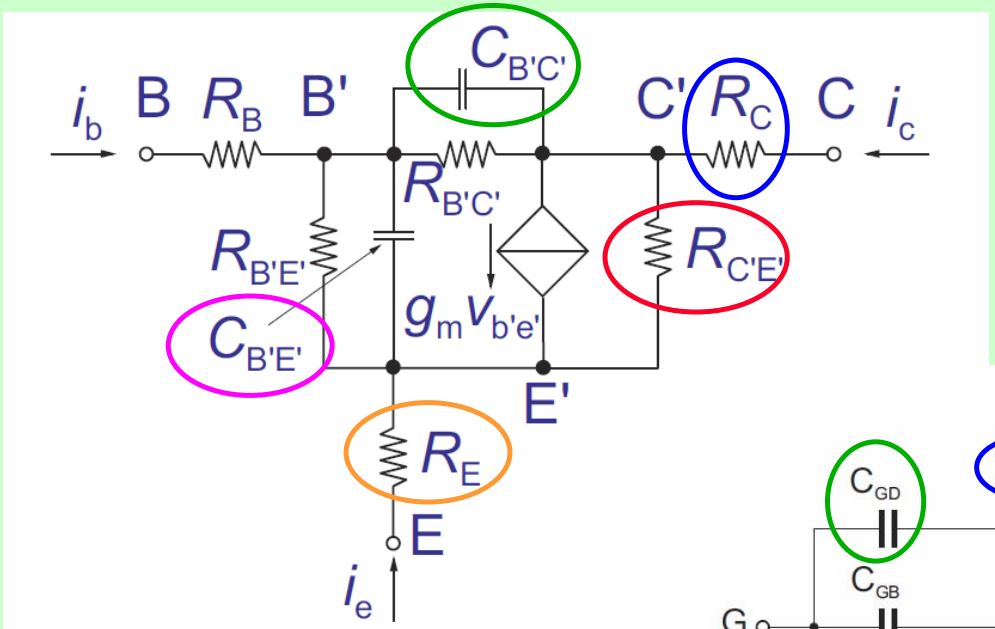
$$C_{GD} = C_{ox} L_D W_{eff}$$

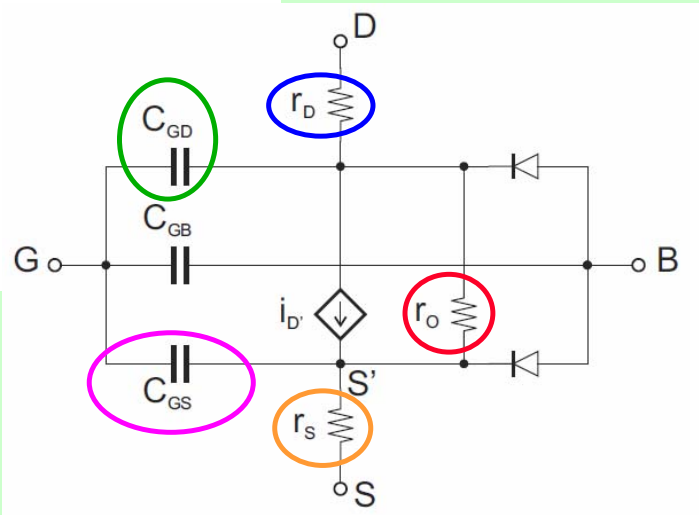


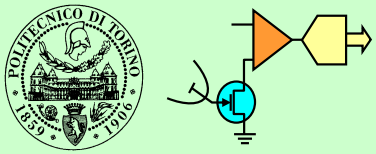
BJT Parasitic capacitances



HF small signal models (π)







Summary of MOS and BJT models

- Small signal
  - BJT, MOS, MOS-FET
  - Same linear model (gm or hybrid)
- Large signal: same method, different models
  - BJT: exponential large signal model (rather simple)
  - MOS: lin/exp/quadratic large signal model (complex !)
  - Analytic model for BJT
  - Analytic or heuristic models for MOS
  - Similar effects and countermeasures
    - » Distortion, harmonics, gain compression, …
    - » Feedback, tuned circuits, ….

Operating limits: Safe Operating Area

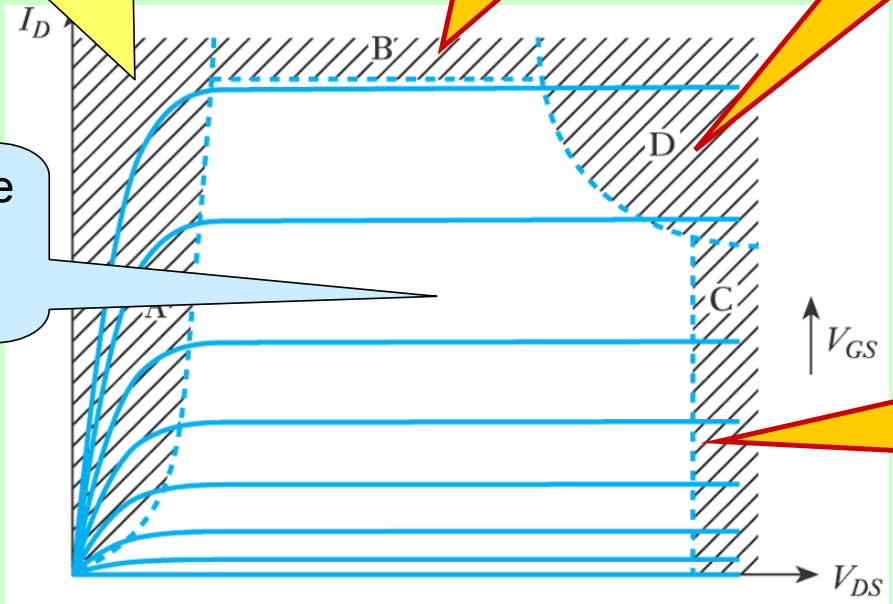
Ohmic region (MOS: a low-value resistor)

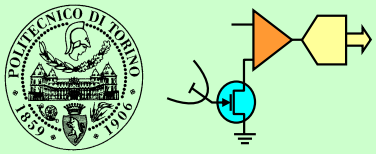
Too high current

Too high V x I (power)

Active & Safe Operating Area (SOA)

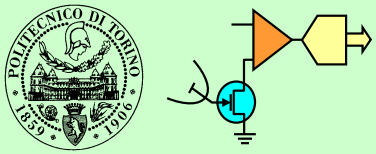
Too high voltage





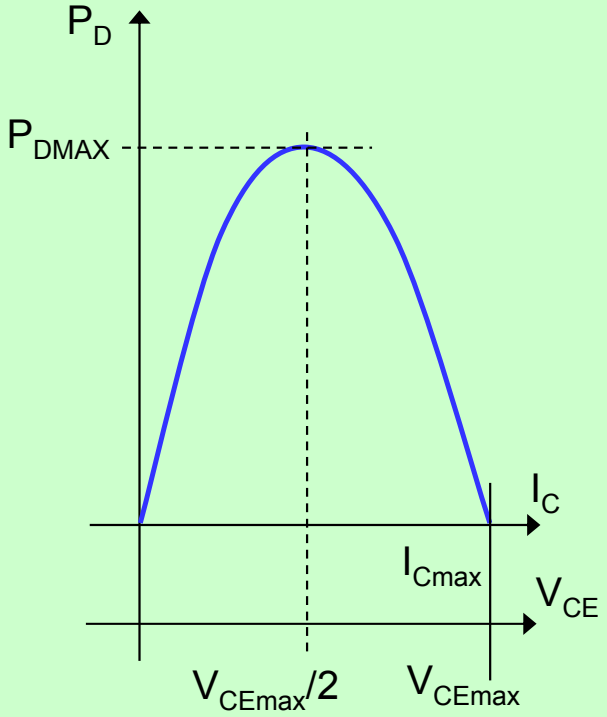
Evaluation of P_{DMAX}

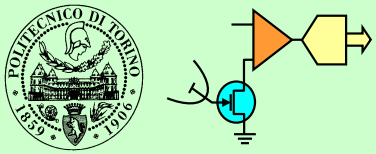
- Bipolar device:
  - $P_D = I_C V_{CE}$; $V_{CE} = V_{CC} - I_C R_C$
  - Max P_D for $d(P_D)/dI_C = 0 \rightarrow V_{CE} = V_{CC}/2$
  - P_{DMAX} = …
- MOS device – same approach:
  - $P_D = I_D V_{DS}$; $V_{DS} = V_{DE} - I_D R_D$
  - Max P_D for … $V_{DS} = V_{DD}/2$
  - P_{DMAX} = ….
- In both cases P_D has parabolic shape
  - P_D = 0 at cutoff (I = 0) and saturation (V ≈ 0)
  - Max at the mid-point



P_D vs operating point

- P_D has parabolic shape
  - P_D = 0 at cutoff (I = 0) and saturation (V ≈ 0)
  - Max at the mid-point
- Critical parameters must be verified for P_{DMAX}
  - $V_{CE} = V_{CC} - I_C R_C$
  - $P_{DMAX} = (I_{Cmax}/2) * (V_{CEmax}/2)$;
- Same shape for MOS
  - Parameters I_D, V_{DS}





Lesson A1 – final test

- Draw the static Id(Vds) characteristic of a MOS transistor. Compare with corresponding Ic(Vce) characteristic of BJT.
- Describe the difference between n-channel and p-channel devices.
- Describe a small signal model for MOS and BJT and related parameters.
- Which are the limits of small signal models?
- Draw small signal models for MOS and BJT with parasitic capacitances.
- Compare large signal models for MOS and BJT.
- Describe the difference between analytical and heuristic models.