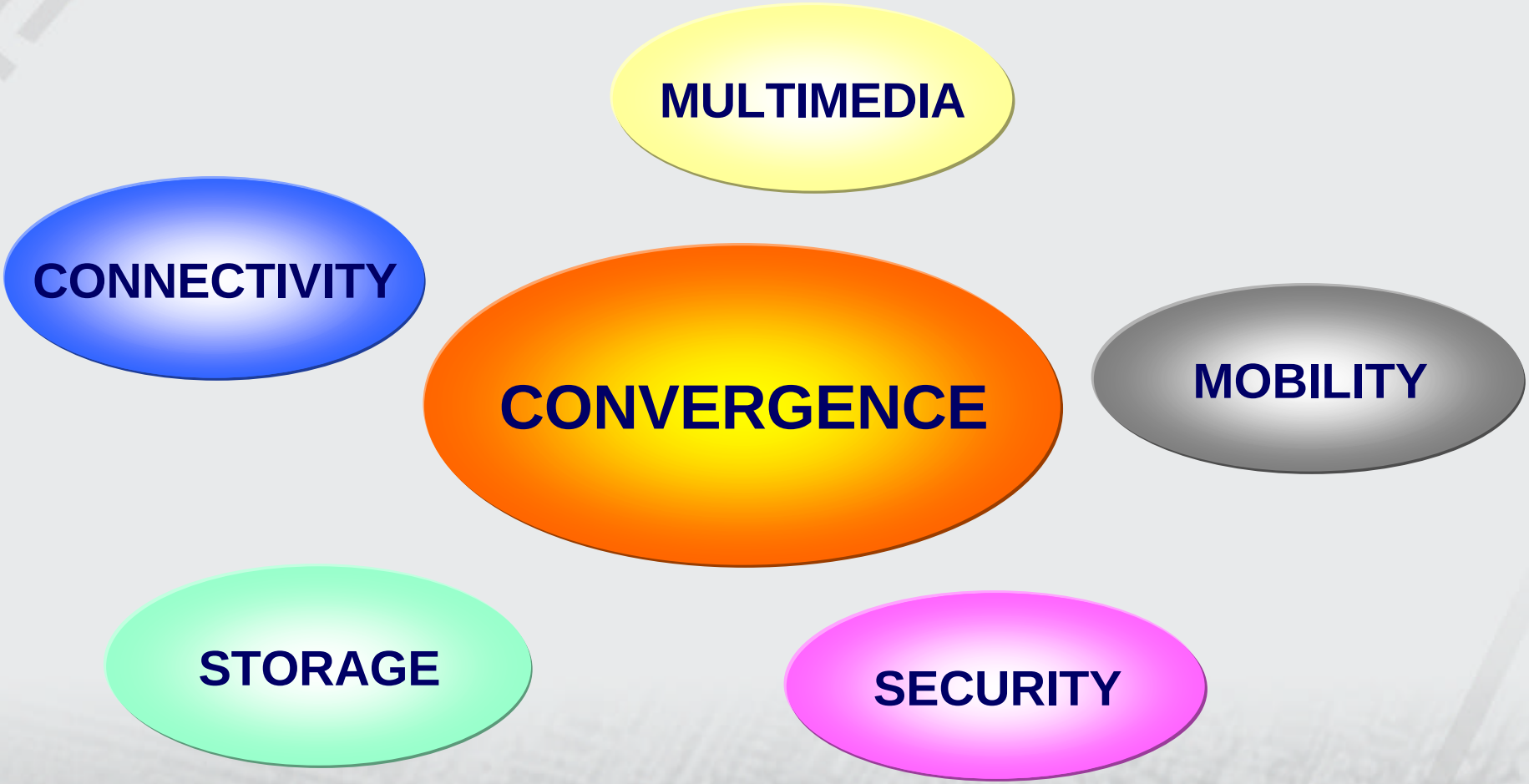
Parallel Processing Forum
Paris, March 28, 2002

Embedded systems, architectures, methodologies, outlook

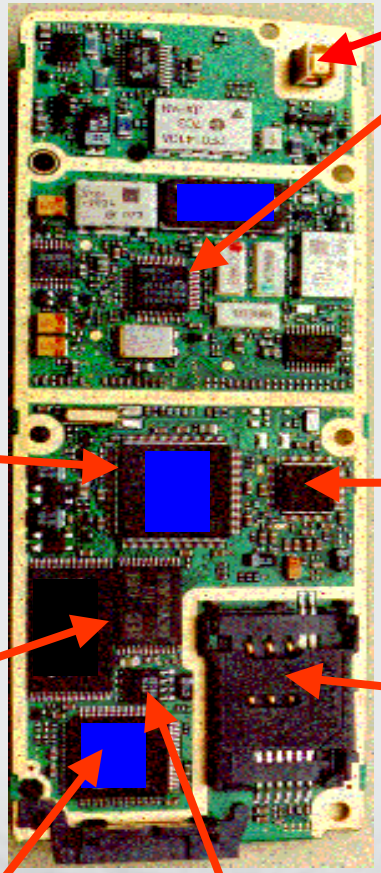
Andrea Cuomo, Corporate Vice President
Advanced System Technology

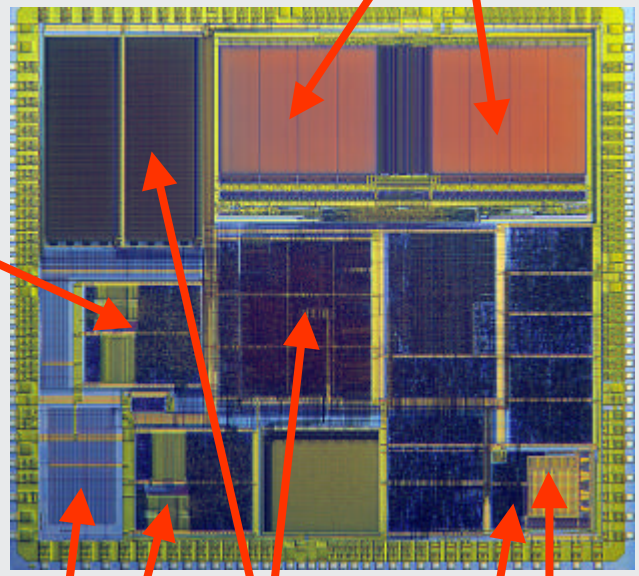
A Wide Variety of Terminals

Defining Convergence

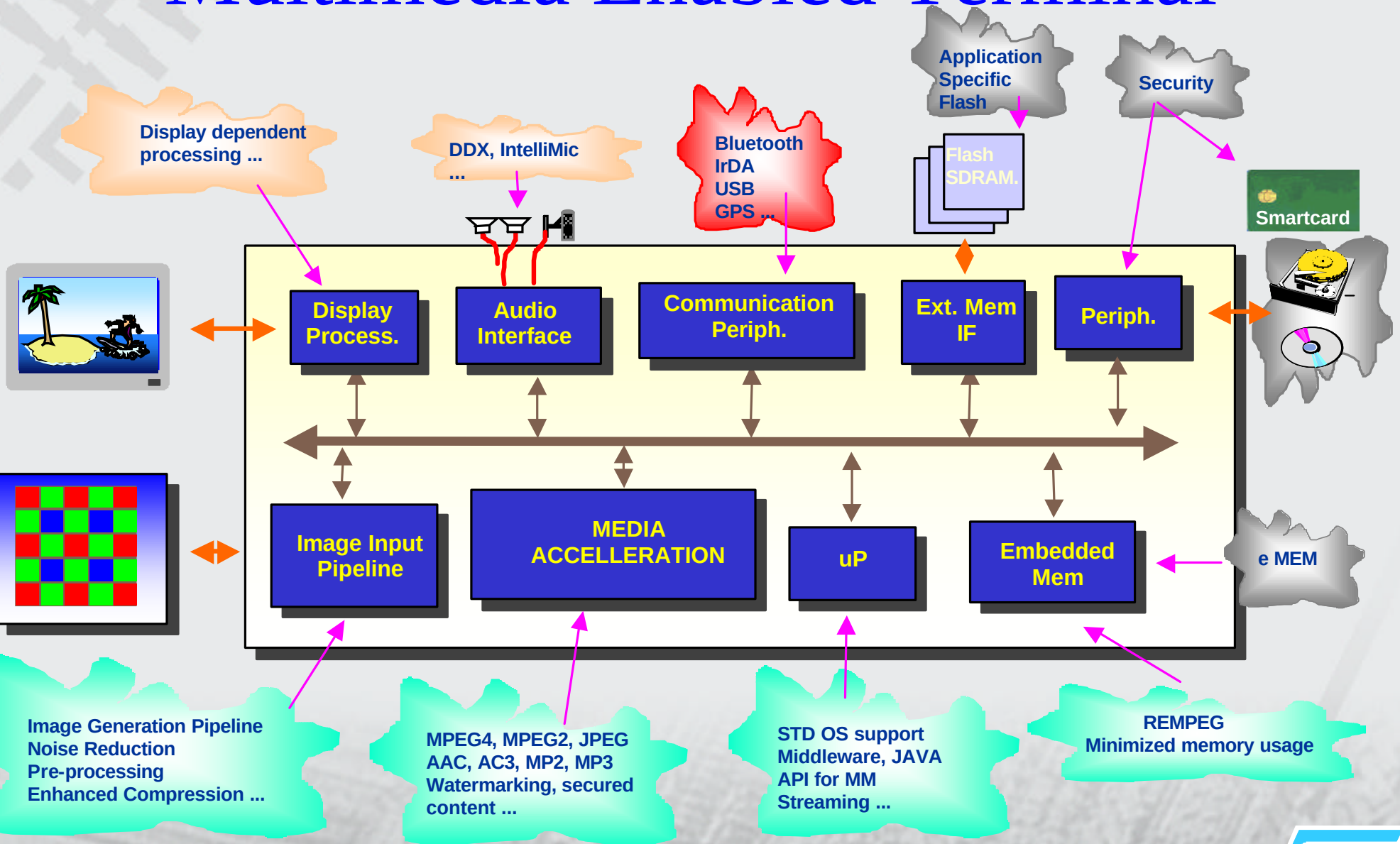


Convergence & SoCs Go Hand In Hand





Multimedia Enabled Terminal



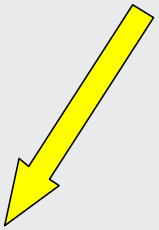
From The SIA Roadmap...

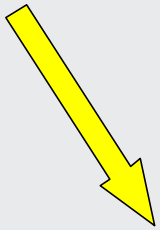
On one chip we shall have

900 M Transistors
10 GHz Clock Rate
175 Watts power

HOW SHALL WE DO IT ?

Two Paths forward





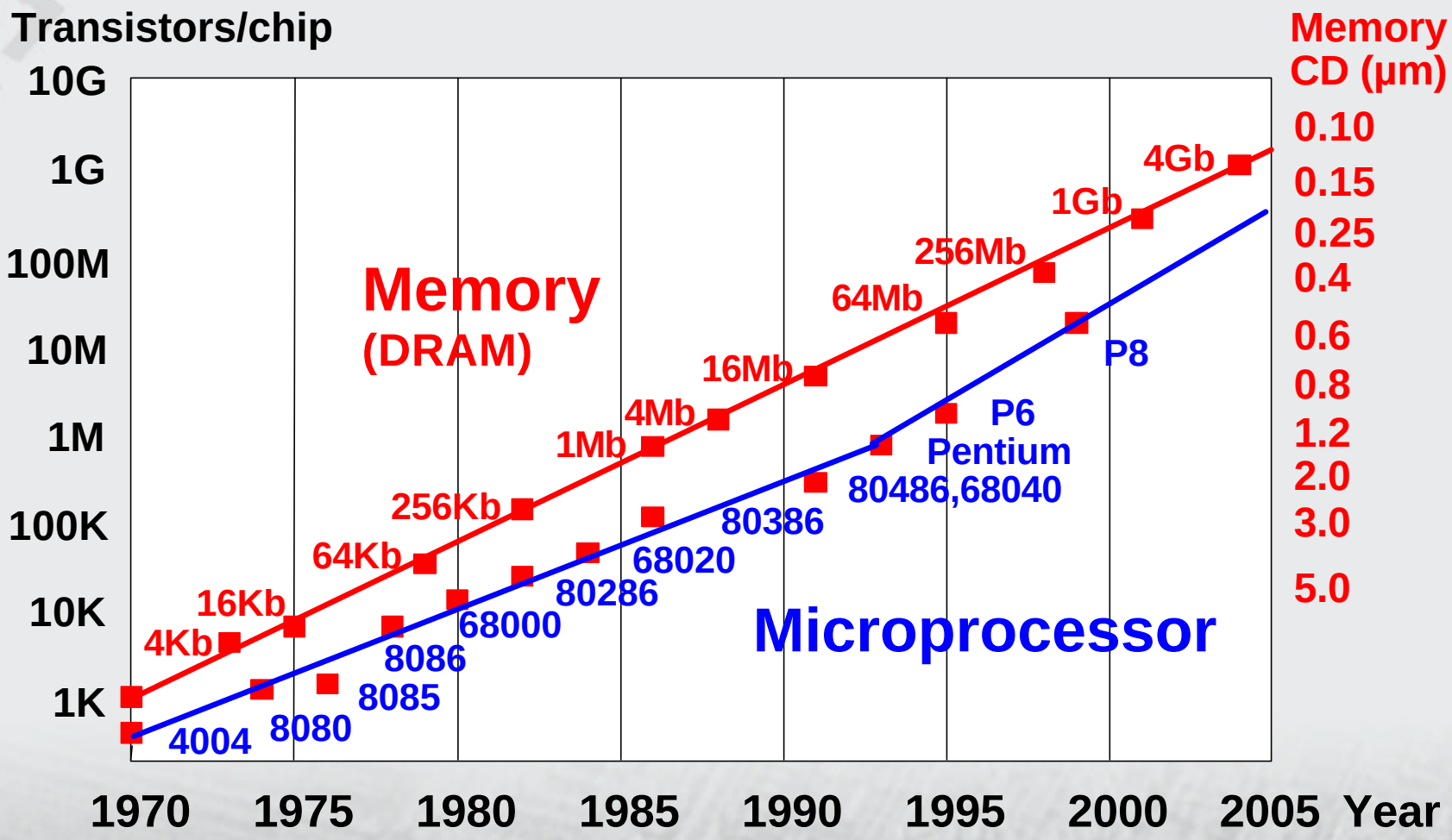
BRUTE FORCE

- GIPS
  10's GIPS
  100's GIPS
- …
  ALL IN SOFTWARE

SMART

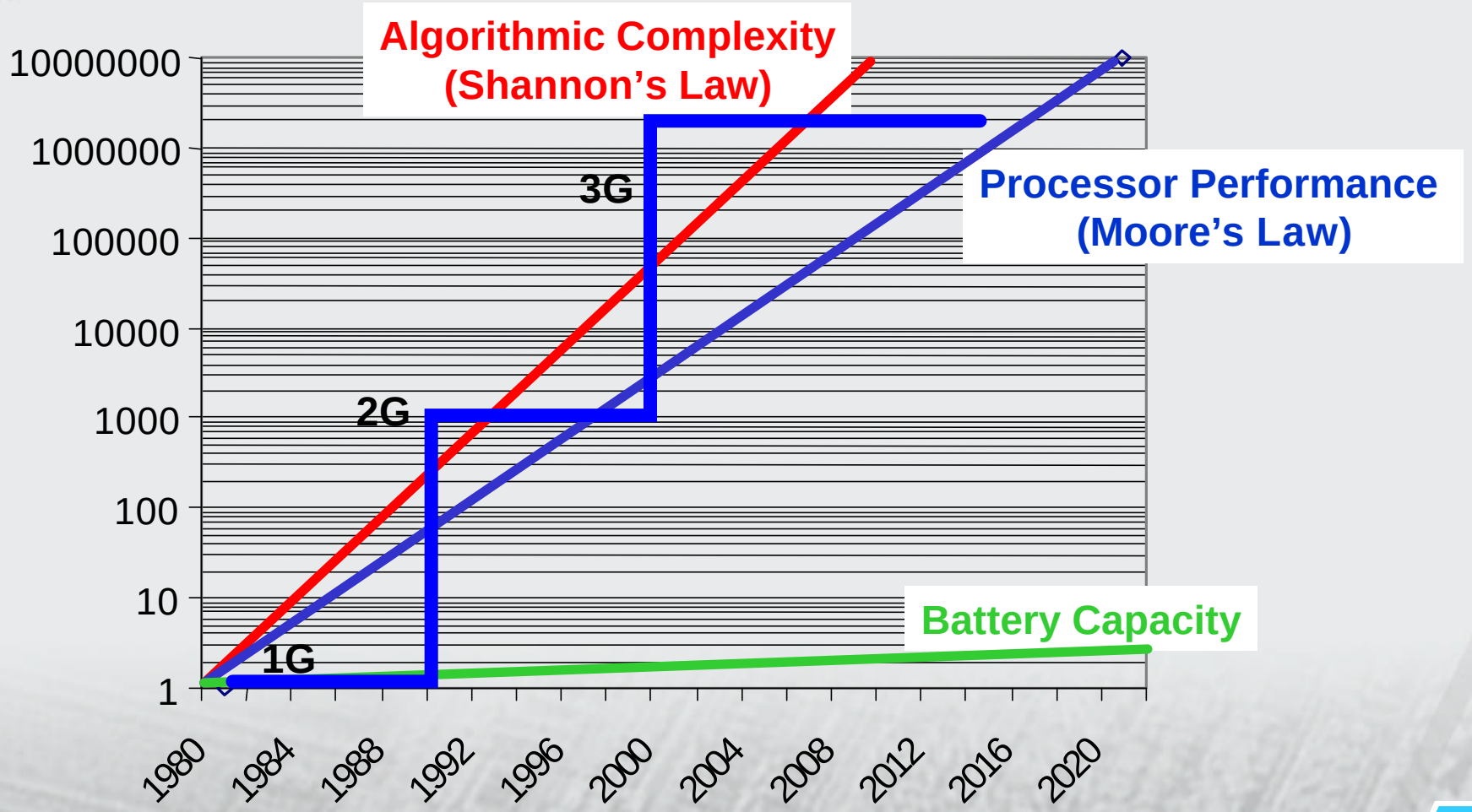
- IDENTIFY SYSTEM INVARIANT
- HARDWIRE INVARIANTS
  SOFTWARE TO PERSONALIZE
  THE VARIABLE PART

Moore's Law


Transistors/chip
10G
1G
100M
10M
1M
100K
10K
1K
Memory CD (µm)
0.10
0.15
0.25
0.4
0.6
0.8
1.2
2.0
3.0
5.0
Memory
(DRAM)
4Kb
16Kb
64Kb
256Kb
1Mb
4Mb
16Mb
64Mb
256Mb
1Gb
4Gb
Microprocessor
4004
8080
8085
8086
68000
80286
68020
80386
80486,68040
Pentium
P6
P8
1970
1975
1980
1985
1990
1995
2000
2005
Year

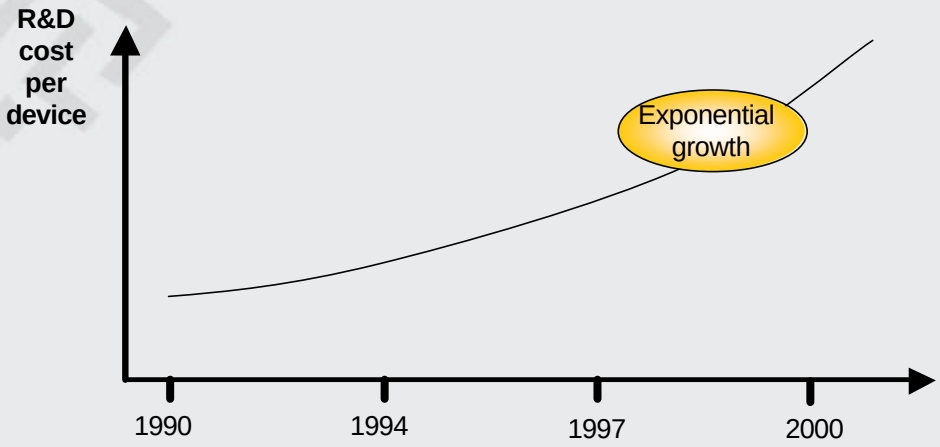
The Algorithmic Driving Force

Shannon asks for more than Moore can deliver...

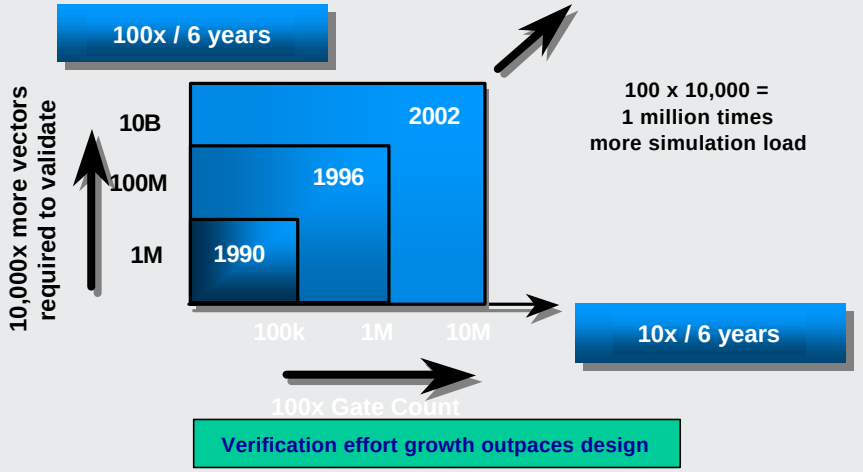


IC Design Challenges

Growing Cost per IC



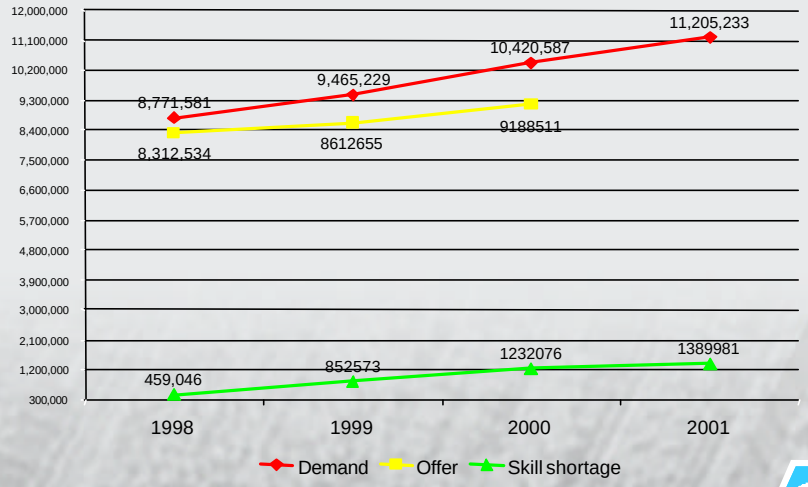
The Verification Challenge



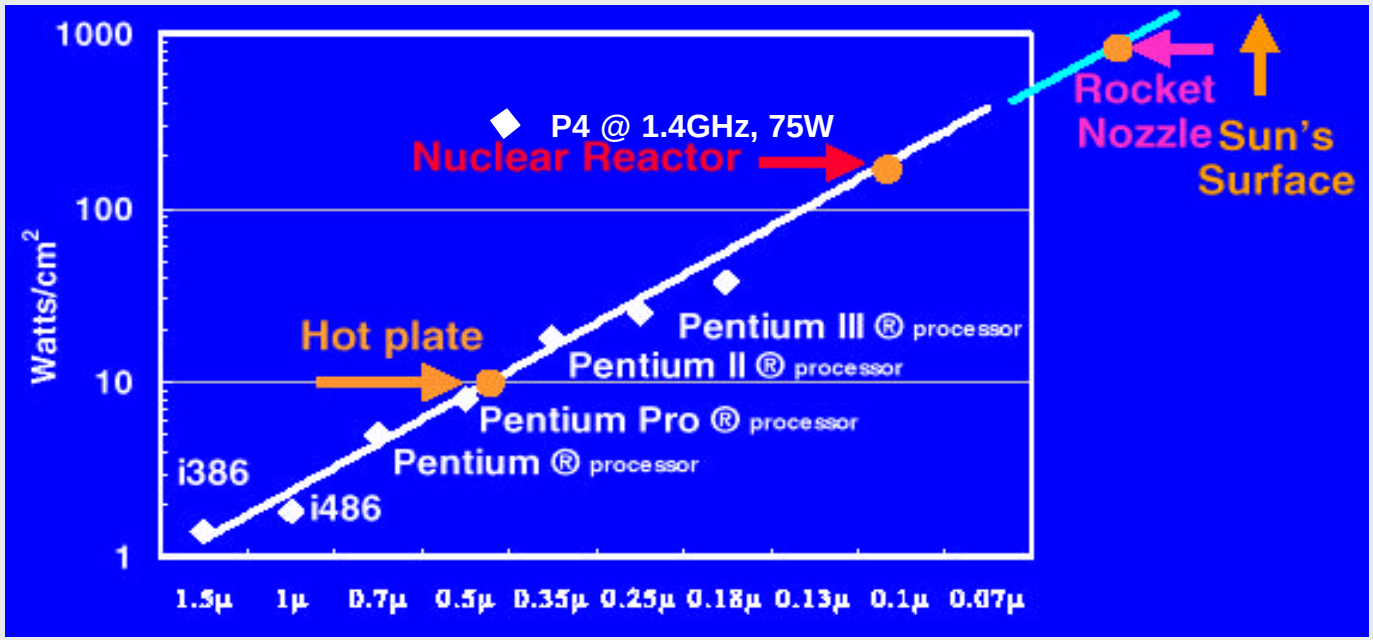
Process Impact on Design

	1.0	0.8	0.7	0.5	0.35	0.25	0.18	0.15	0.13
Area	■	■	■	■	■	■			
Speed	■	■	■	■	■	■	■	■	■
Power				■	■	■	■	■	■
Metal-Migration					■	■	■	■	■
Signal Integrity						■	■	■	■
EMI								■	■

IC Shortage in Europe

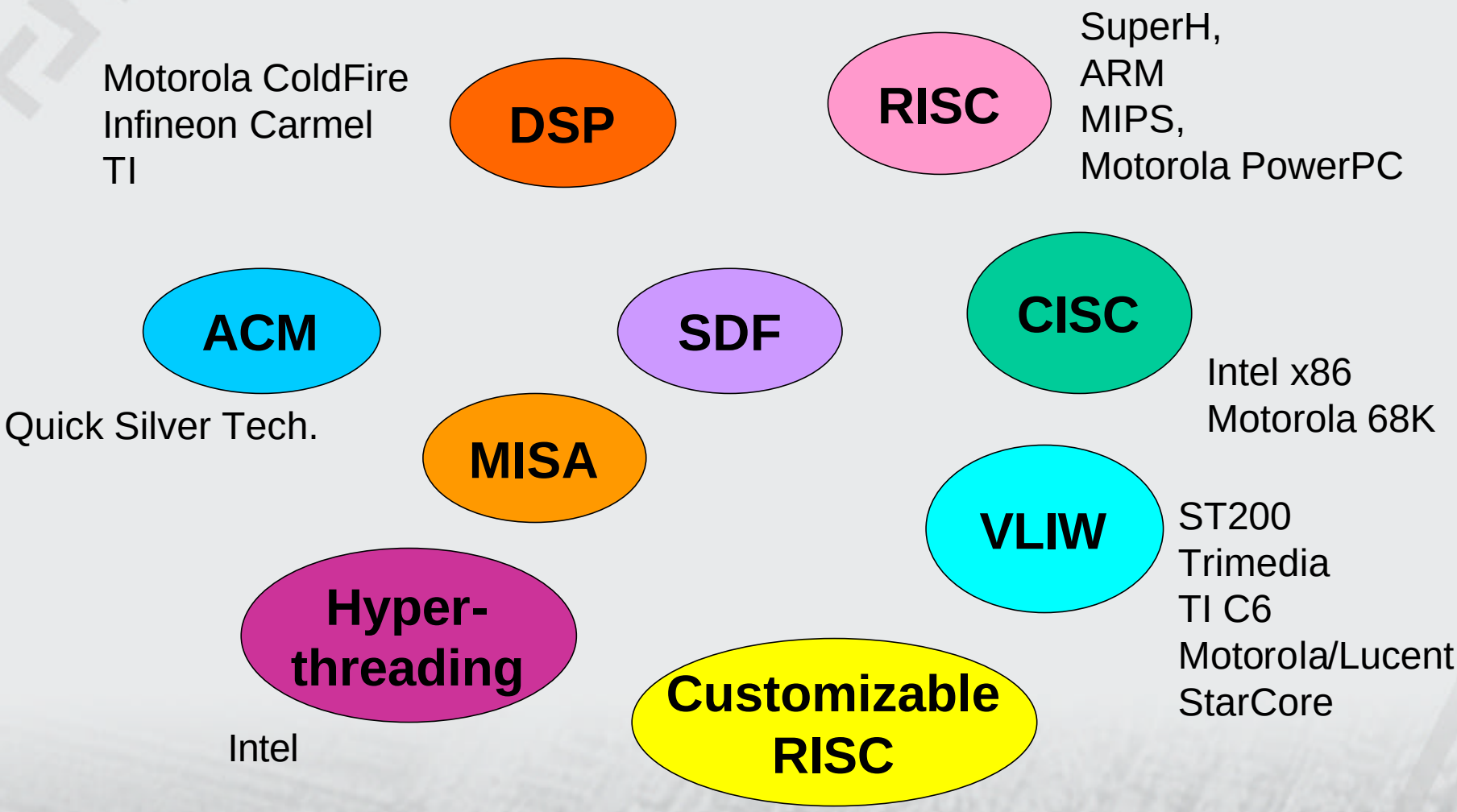


Challenge



Courtesy of Fred Pollack, Intel
Keynote speech, MICRO-32

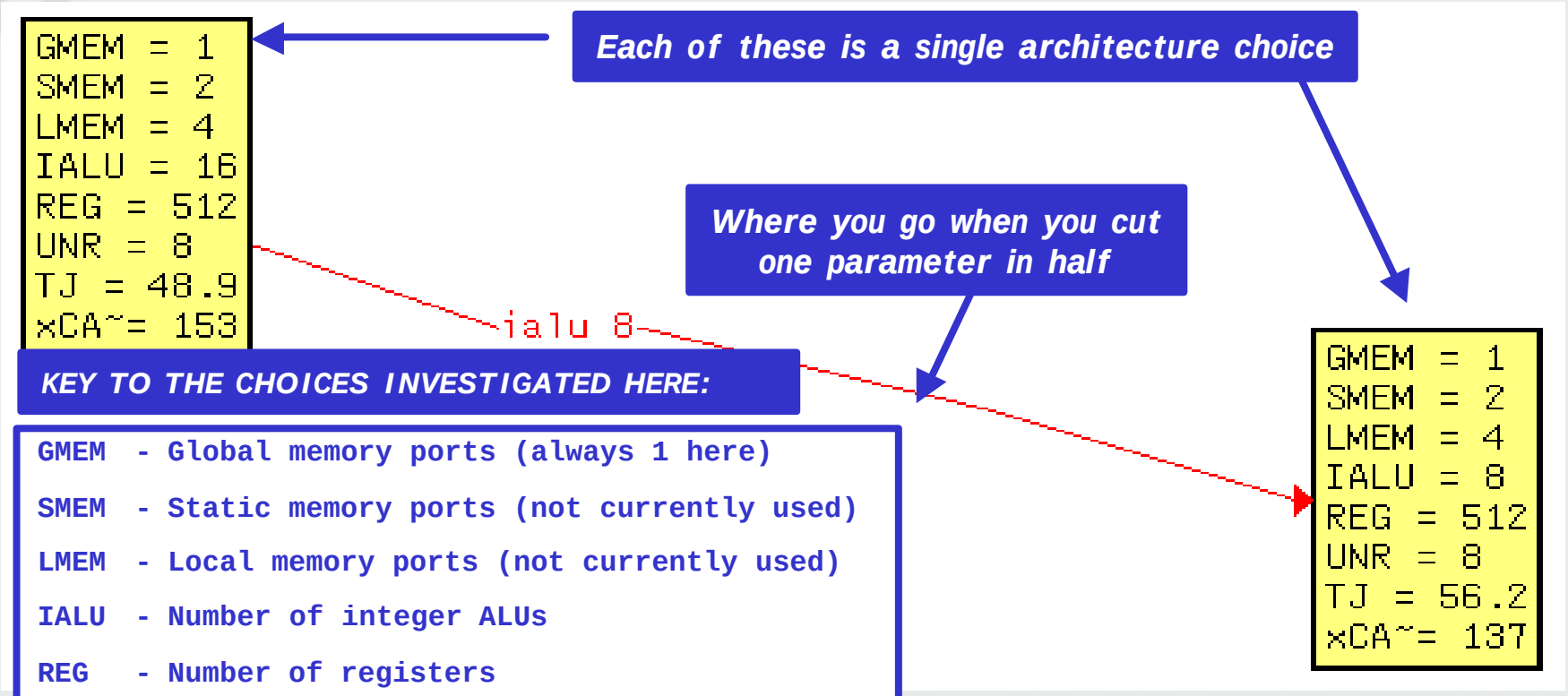
Which computing engines?



Parallel Processing (1)
Instruction-Level Parallelism

The schedule: 4 pixels processed in 229/4 = 57.25 cycles per pixel.

Navigating The Space of Custom Architectures



KEY TO THE CHOICES INVESTIGATED HERE:

GMEM - Global memory ports (always 1 here)

SMEM - Static memory ports (not currently used)

LMEM - Local memory ports (not currently used)

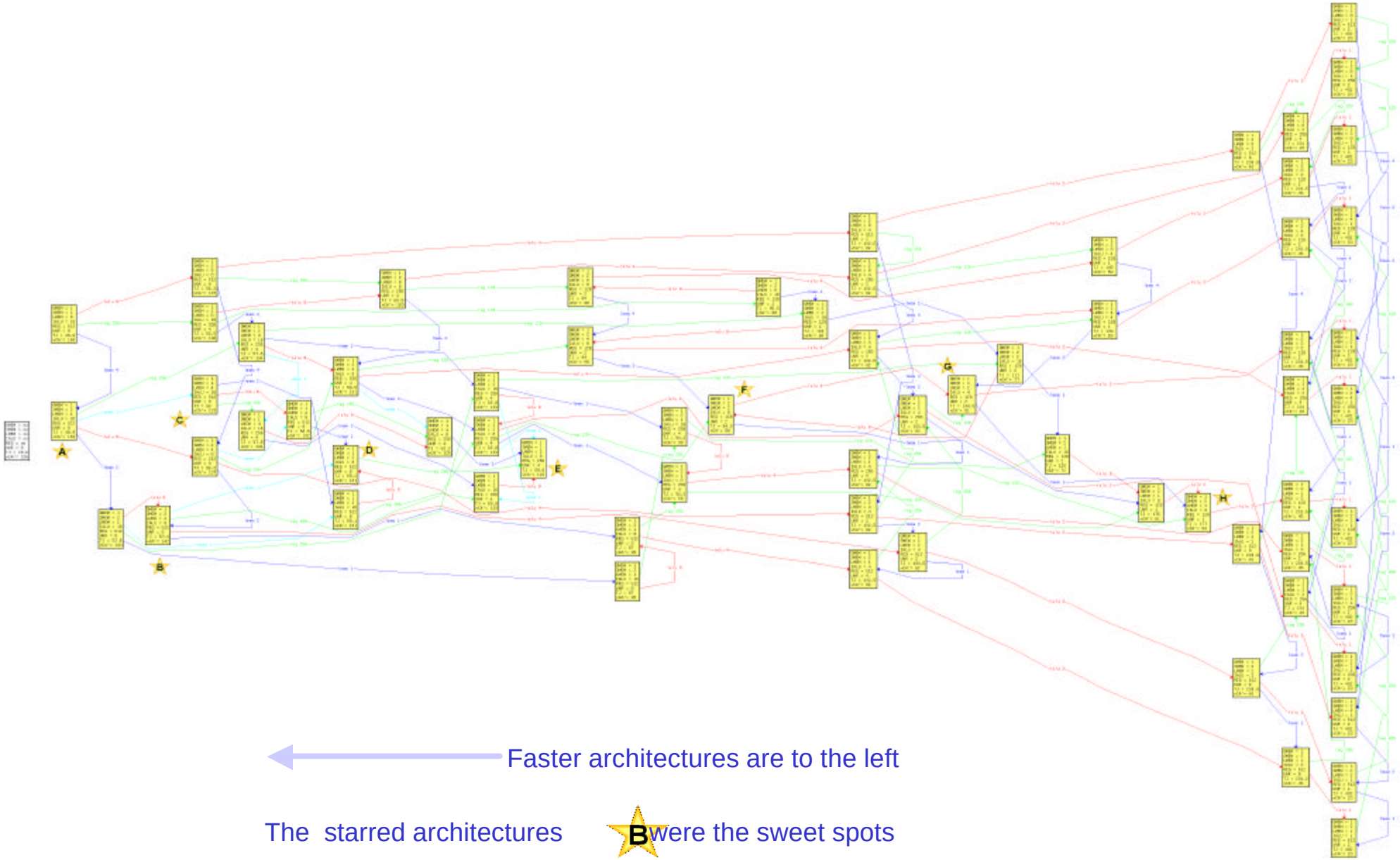
IALU - Number of integer ALUs

REG - Number of registers

UNR - Optimal number of pixels to consider at once for this architecture choice

TJ - Cycles per pixel (measure of performance)

xCA~ - Factor faster than i960/CA (another measure of performance)



Faster architectures are to the left

The starred architectures (B) were the sweet spots

HEWLETT PACKARD

Embedded System Design Turned Right-Side-Up

Traditional CPU Design

BUILD HARDWARE for what **you think** is a good embedded CPU

BUILD A COMPILER and other system tools for that CPU

give it to the user to **PORT THE USER APPLICATION** TO. Hope the match is good

Right-Side-Up CPU Design

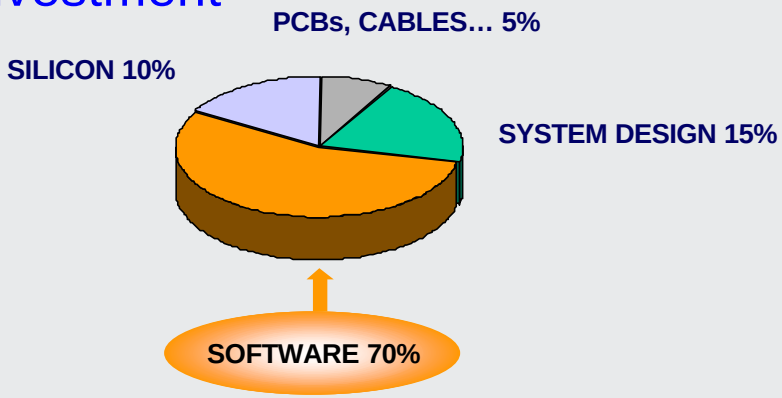
With the user, **PORT THE APPLICATION** to family toolset

ARCHITECT THE CPU and related system tools

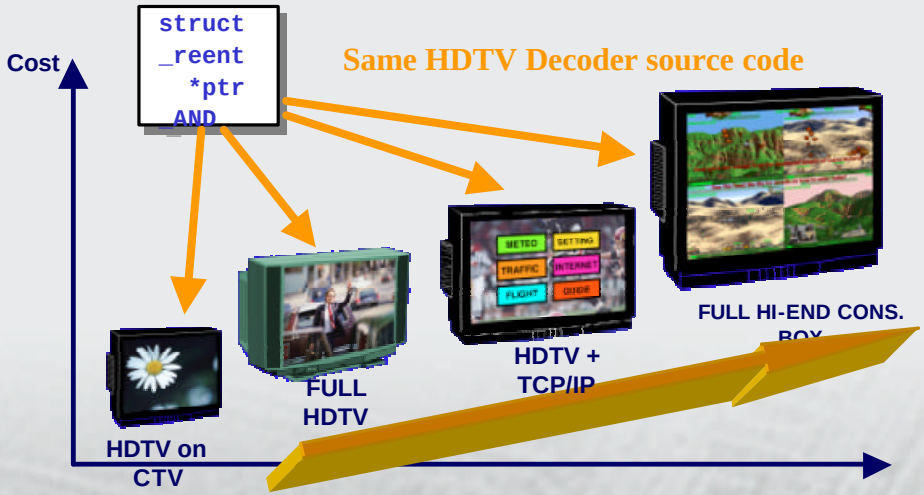
BUILD HARDWARE for what **you know** is a good CPU for the application

A New Design Methodology

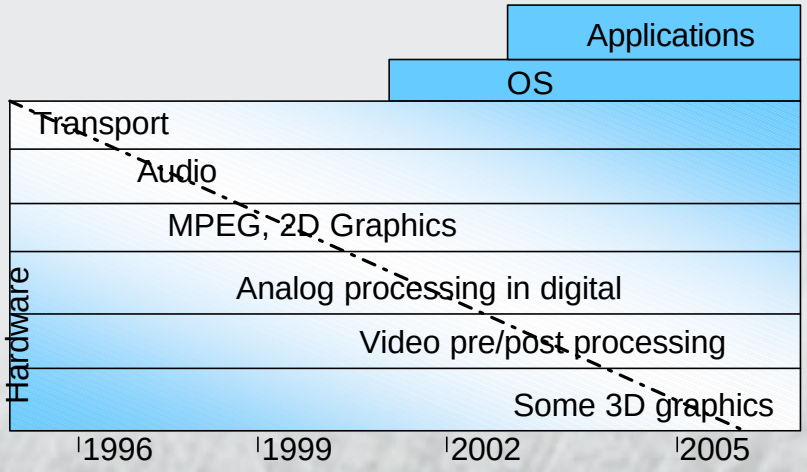
Customers' SW investment



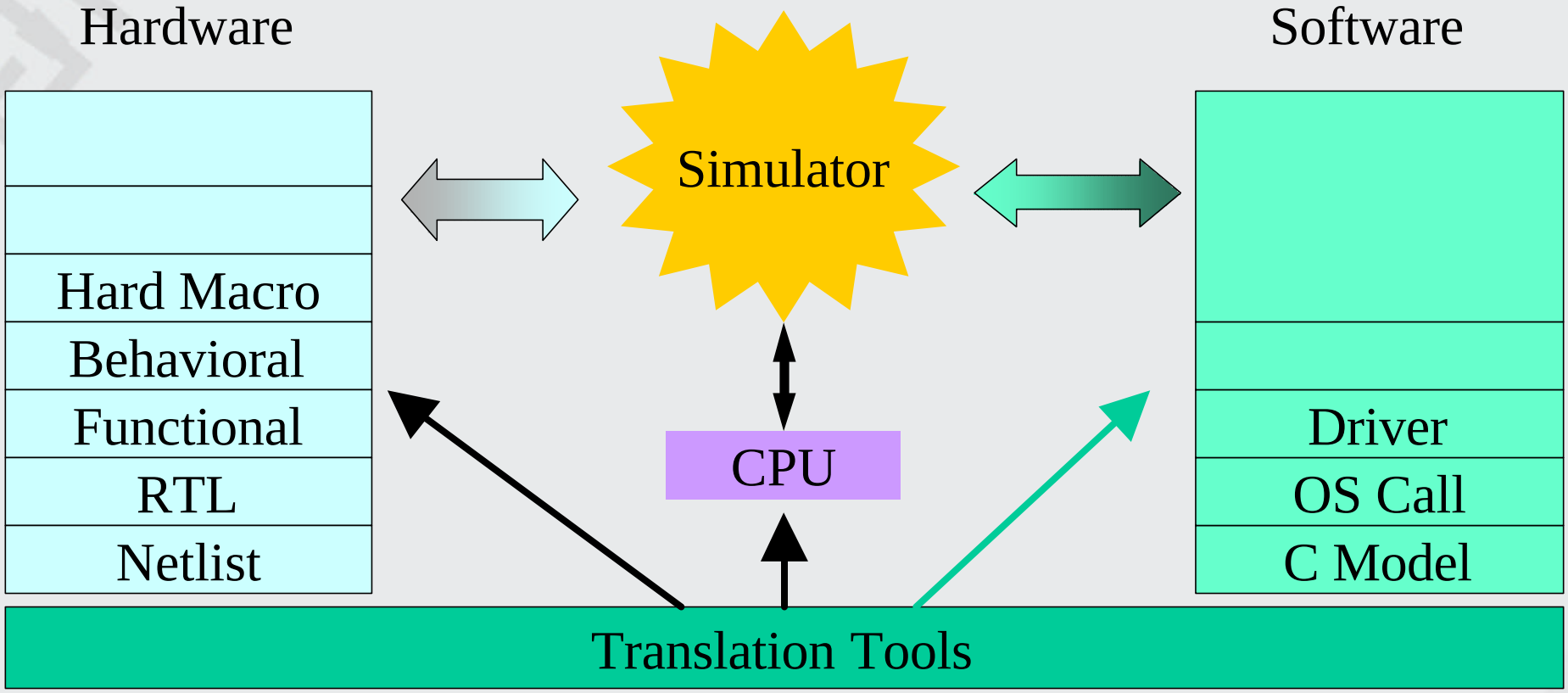
Scalability



Portability



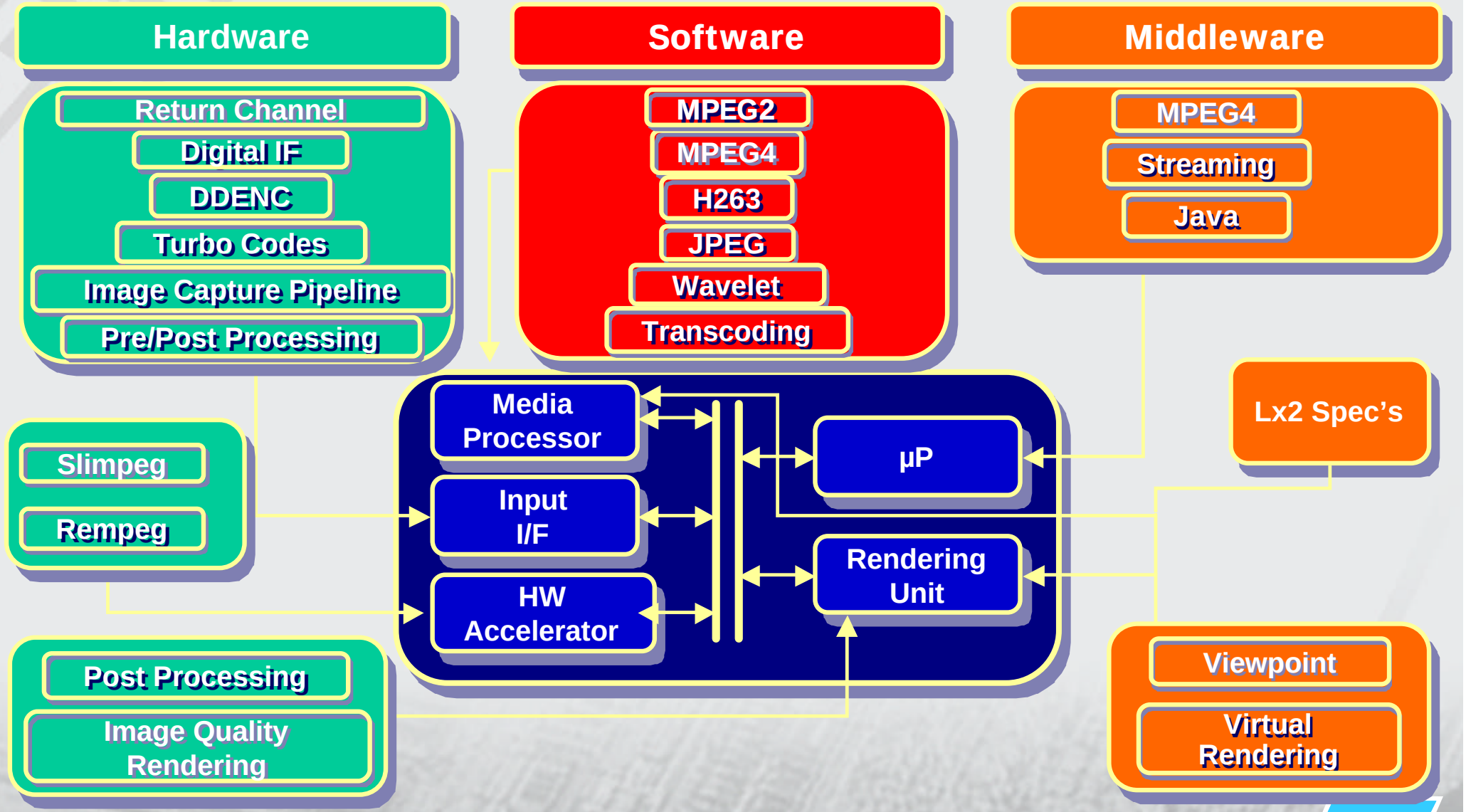
The Environment



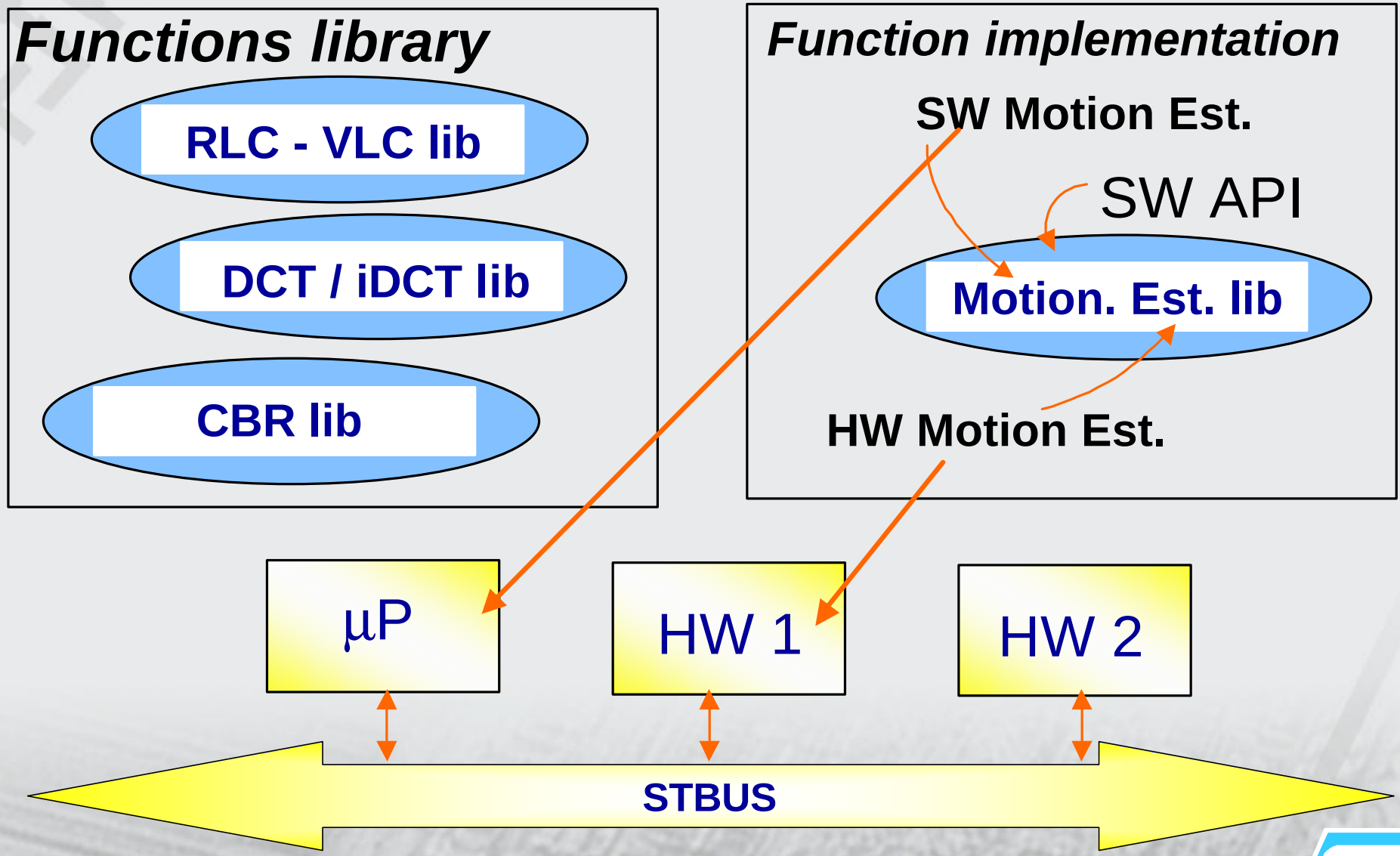
IP

Analog TV Processing	Graphics	AC-3	MPEG	Transport
Processor Accelerator	Video Processing	Memory Management	Network Interface	DENC

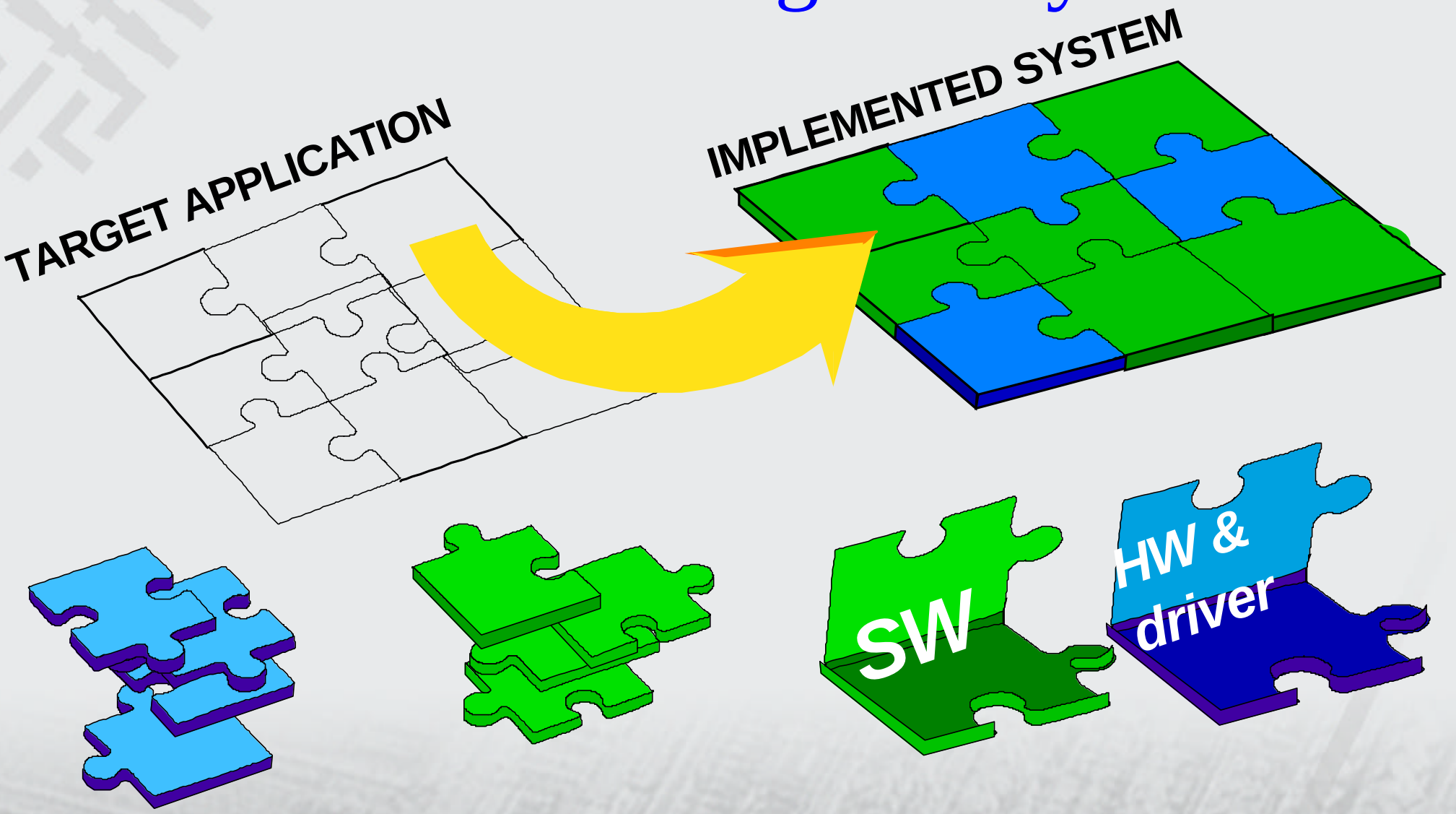
Multimedia Platform



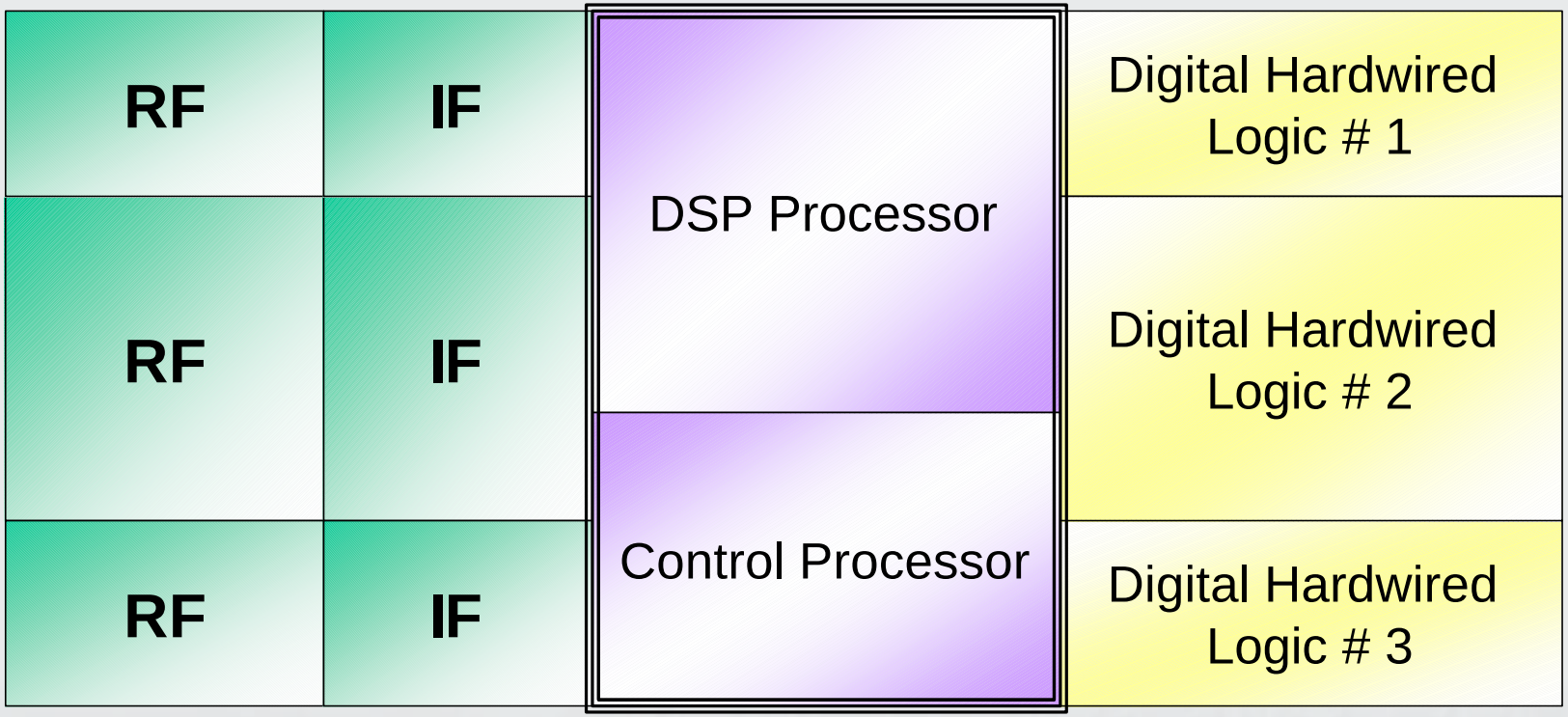
HW/SW Plug & Play



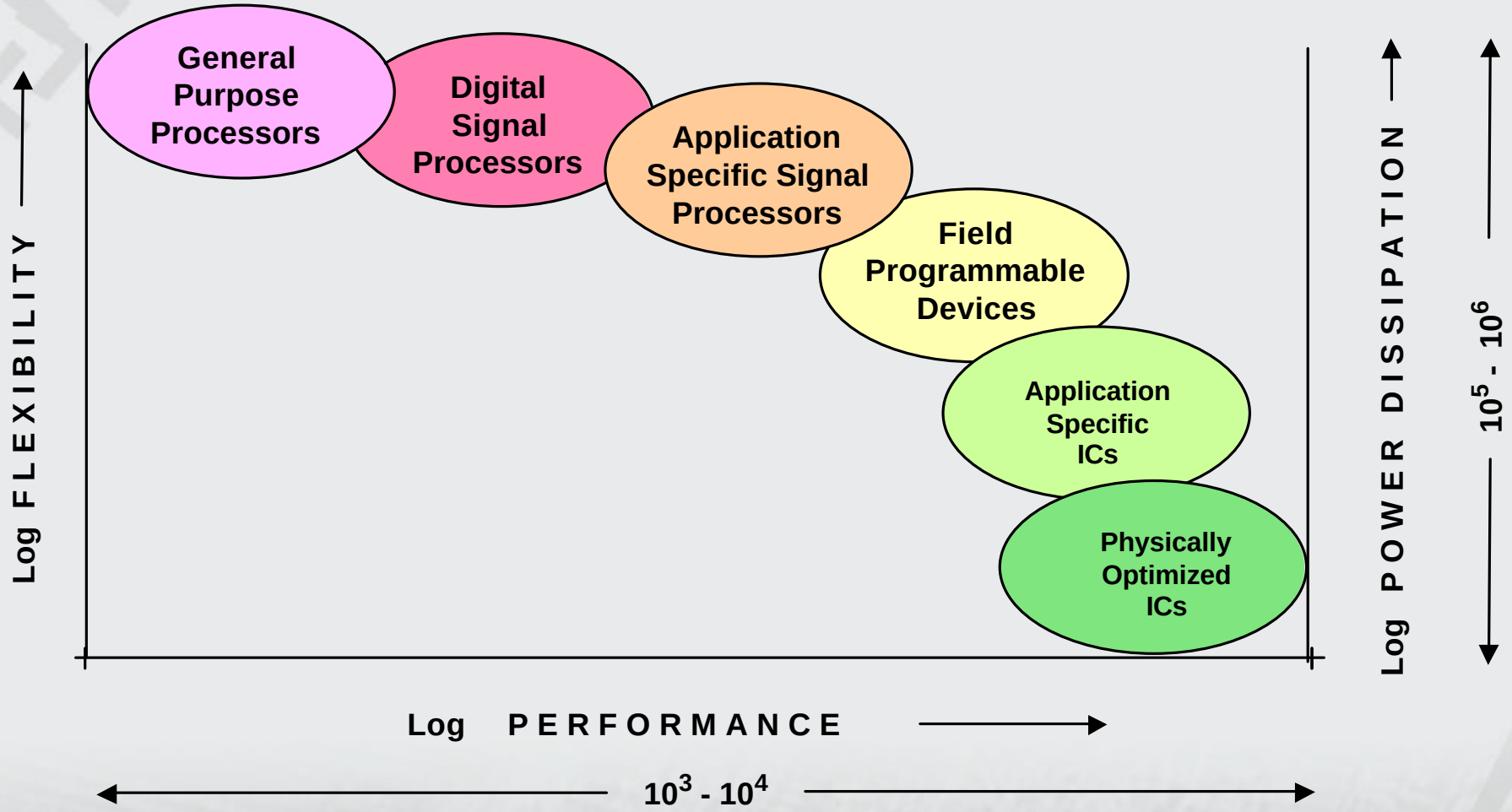
HW/SW Plug & Play



Power Conscious Multistandard Terminal Architecture

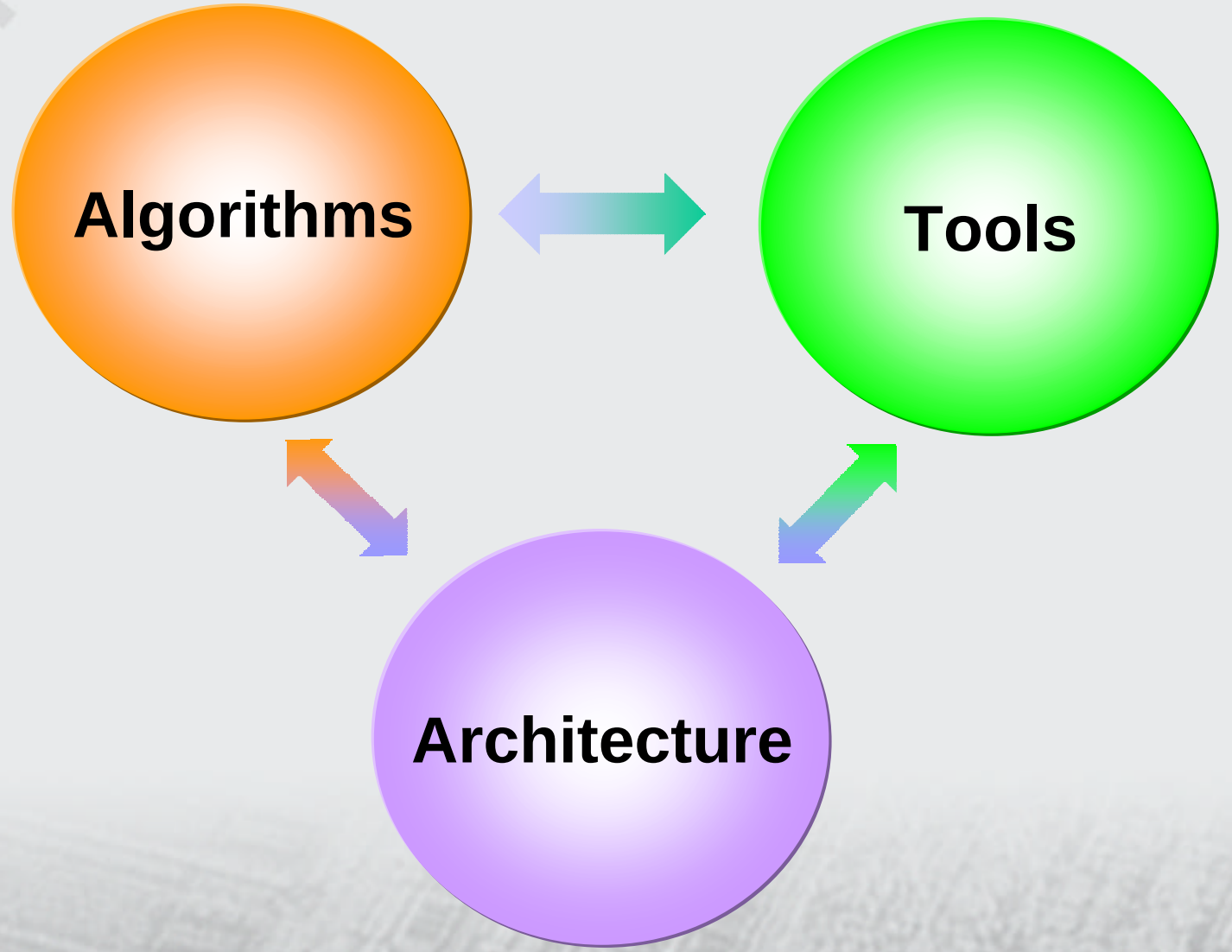


Implementation Space



Source: T.Noll, RWTH Aachen

A New Approach To Design



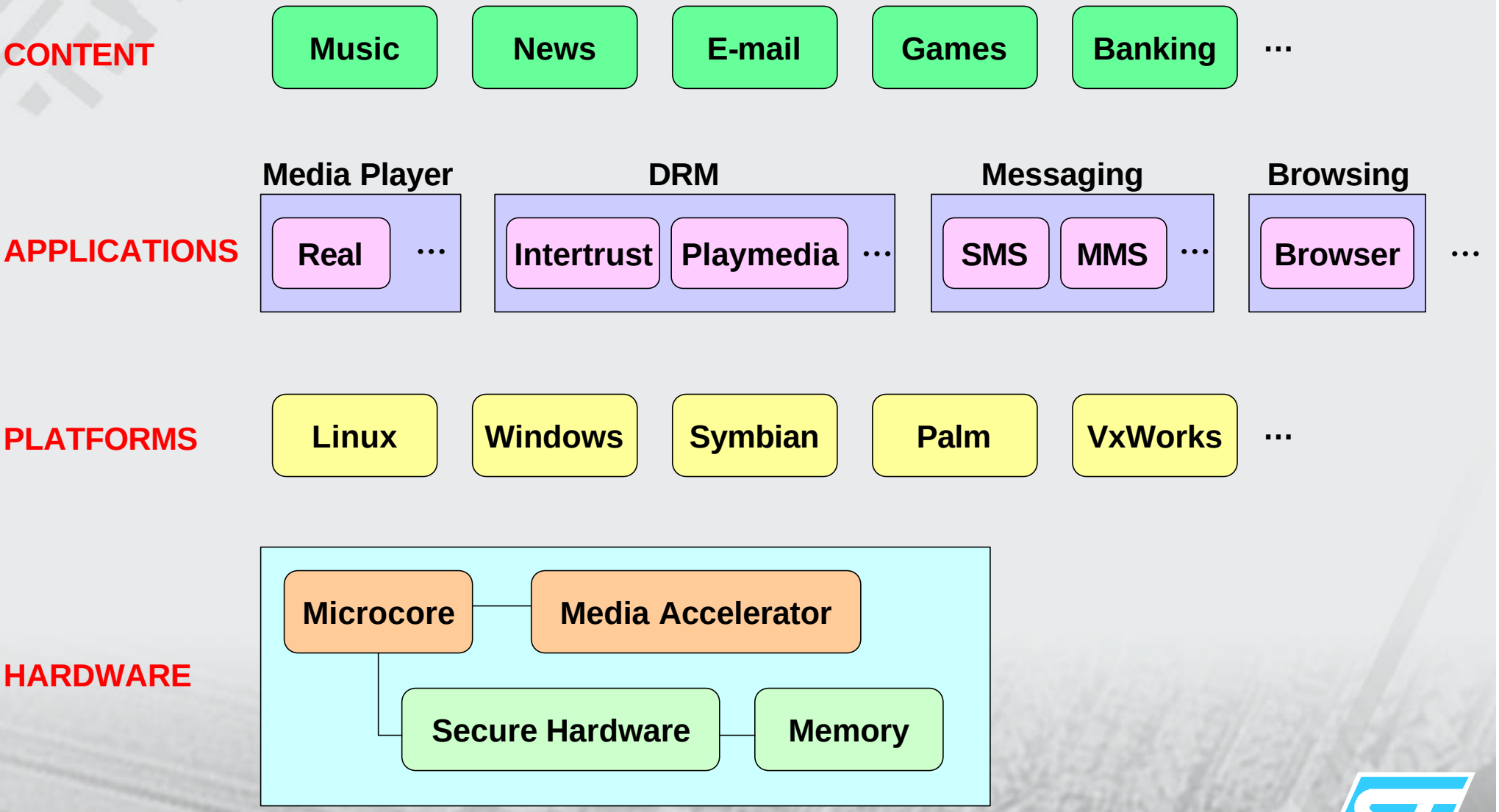
Parallel Processing (2)

Multiprocessing: the new fronteer

- Compilers
- Architectures
- Toolchain

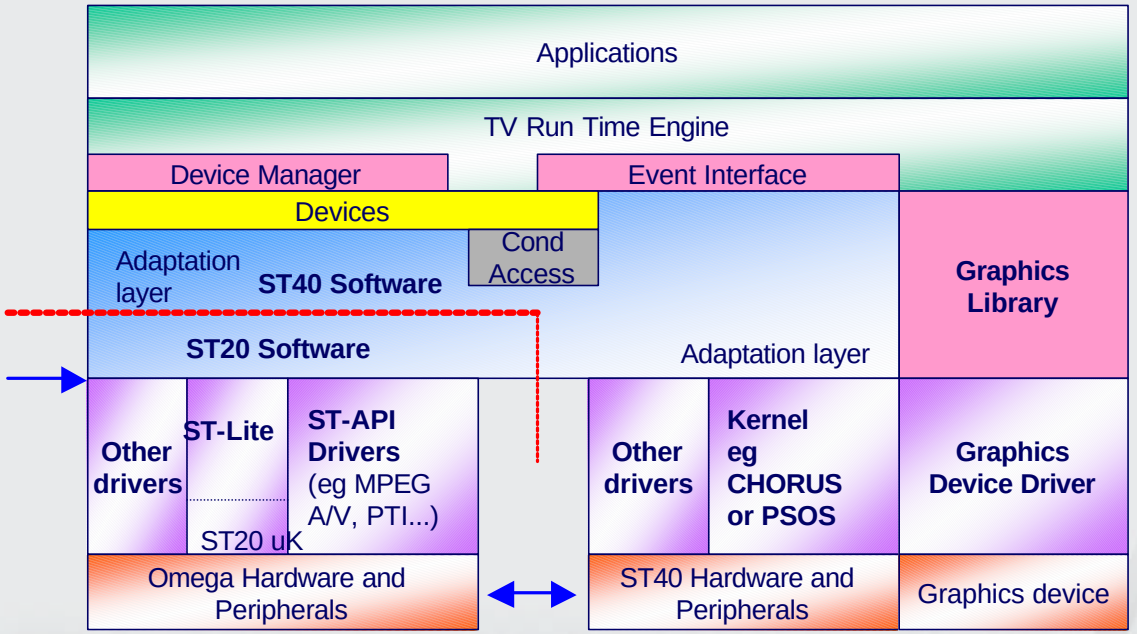
can we leverage grid technology?

The Future of Embedded Systems



Business Models
For a Semiconductor Company

- System house?
- System integrator?
- Solution provider?
- Subsystem provider?
- Technological leader?
- IP provider?
- Foundry?

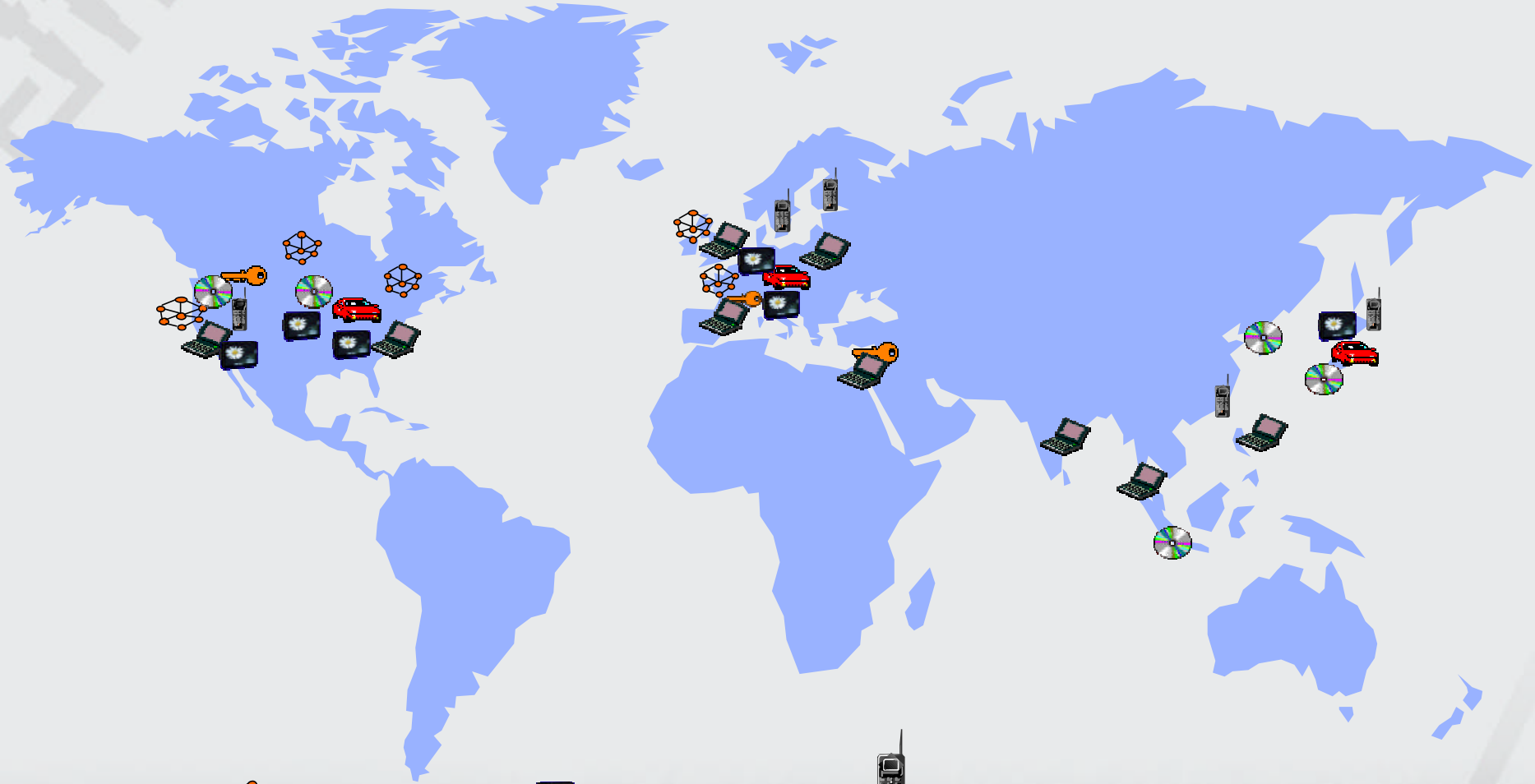


A Few Things To Do …..

GSM, XML, DAVIC, DVB, MPEG2, MPEG4, MPEG7, TINA-C, QTP, ATM, WAN, LAN, SONET, SDH, IPVG, COFDM, QAM, QPSK, VLIW, RISC, CISC, GPRS, EDGE, UMTS, CDMA, WBCDMA, ADSL, VDSL, G-LITE, REMPEG, SLIMPEG, SPKI, PKI, SDMI, DVD, MP3, AC-3, BLUETOOTH, USB, ETHERNET, DSS, JPEG, 1394, DOS, WINDOWS, EPoC, OS/2, CD-ROM, BBNT, HOMERF, 802.11, HYPERLAN II, SIRLAN, CRYPTO, ZERO-IF, PRML, AGENTS, LINUX, VXWORKS, TURBOCODES, CORBA, DCOM, JAVASCRIPT, JINI, CSSI, UNIX, SCSI, POSICS, OST, OPENIP, WINCE, CMIP, KERBEROS, WBEM, CA-TV, ITTI, FDMA, DECT, SDR, HSCCSD, SIM, STK, WAP, WAN, PALMOS, GEOS, MAGICLAP, ORBITOR, IS-95, POTS, SS7, T1, CCBS, VPN, GUI, UICC, USIM, DIRECT-X, MMX, MHI, MeXe, 3GPP, APIs, SPS, DWDH, CCBI, QoS, PROXY, VCSEL, UWB, SWANET, MSP, MSC, PCS, MIMOWL, MCFD, ADFED, OPENGL, FDTD, FFT, PDC, HTTP, CTI, DSP, CPU, EPLD, IFFT, TCM…

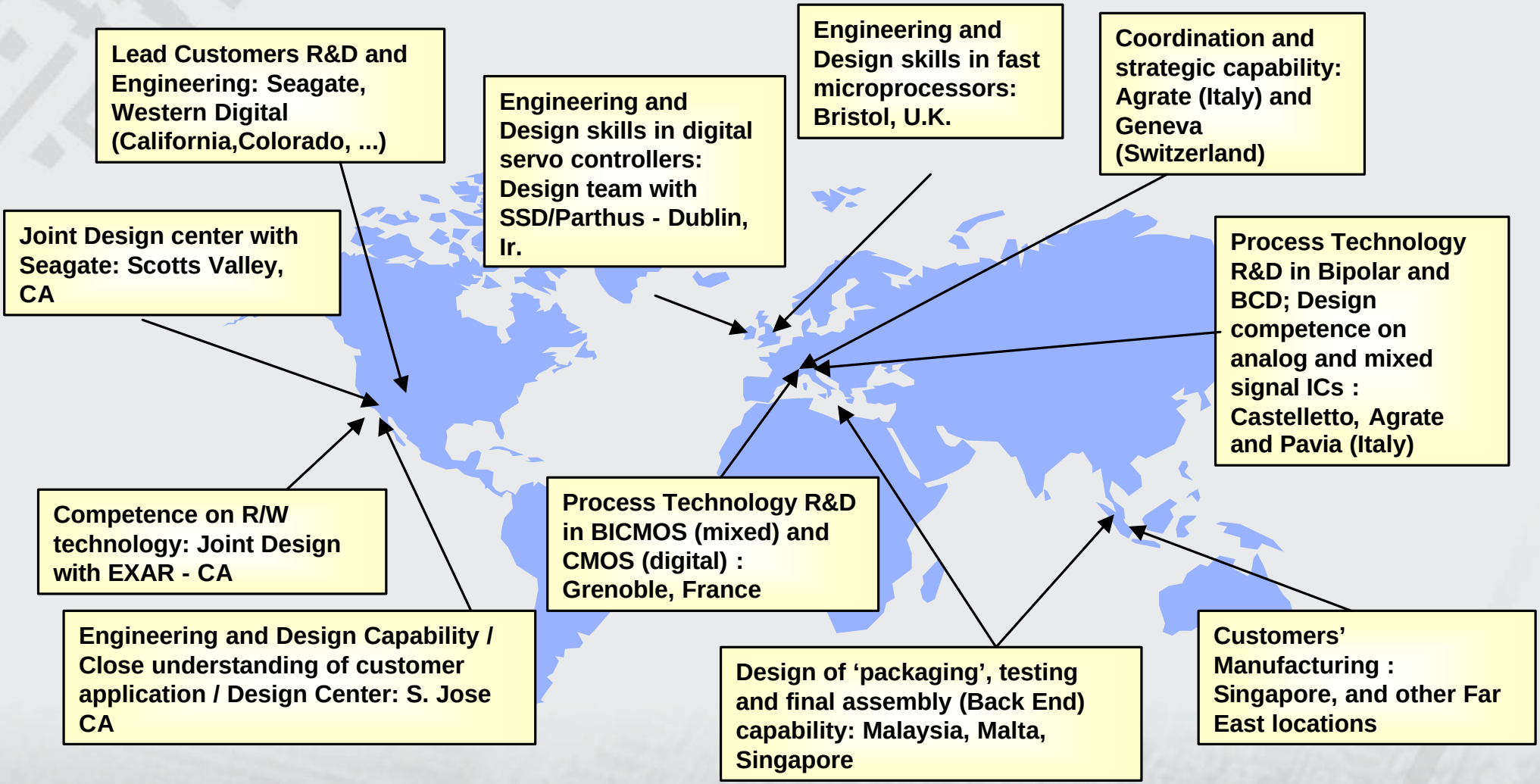
just to mention a few…

A Global World



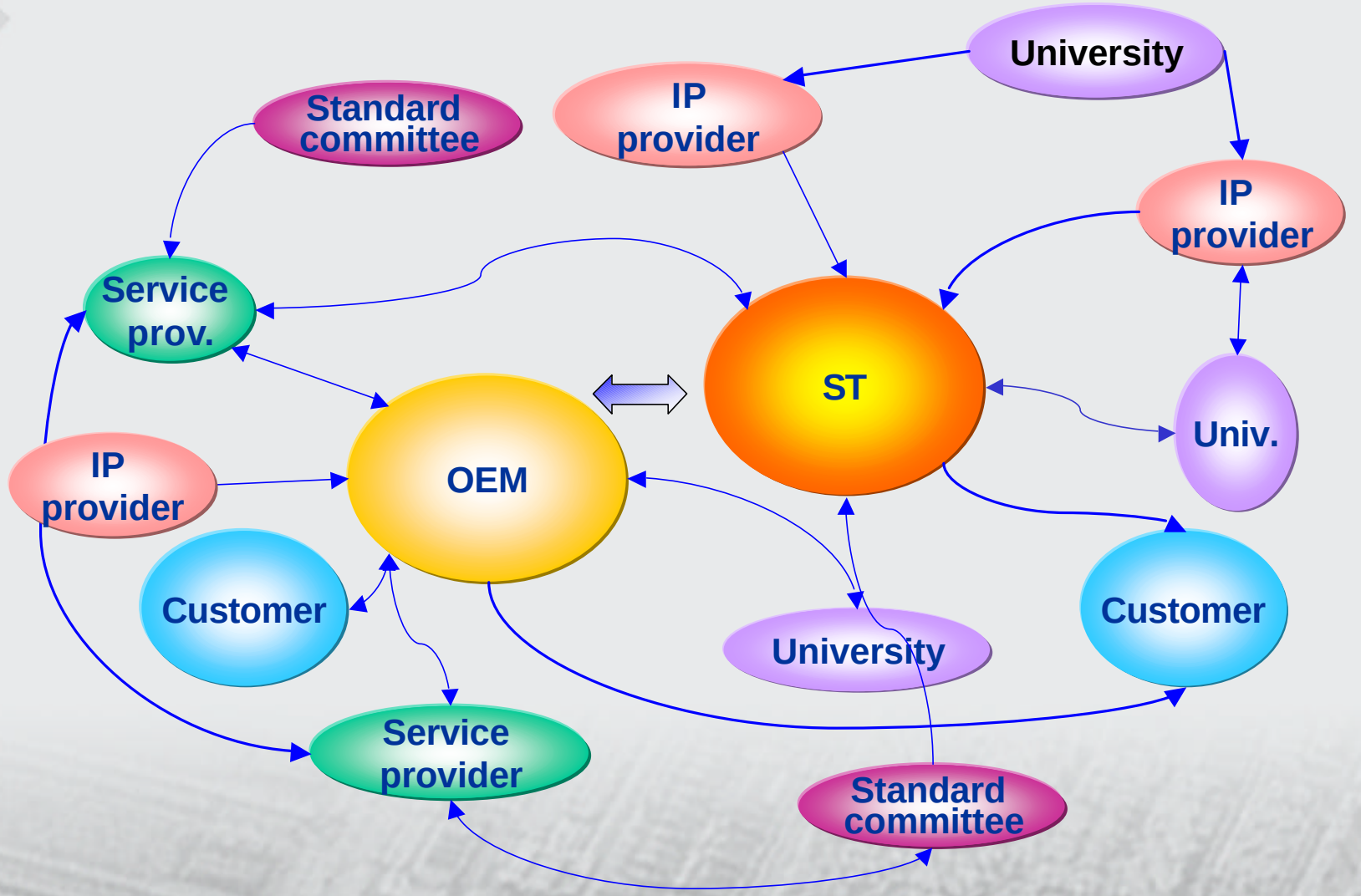
Security
Networking
Consumer
Wireless
Storage
Automotive
Computer Science

Learning From The World

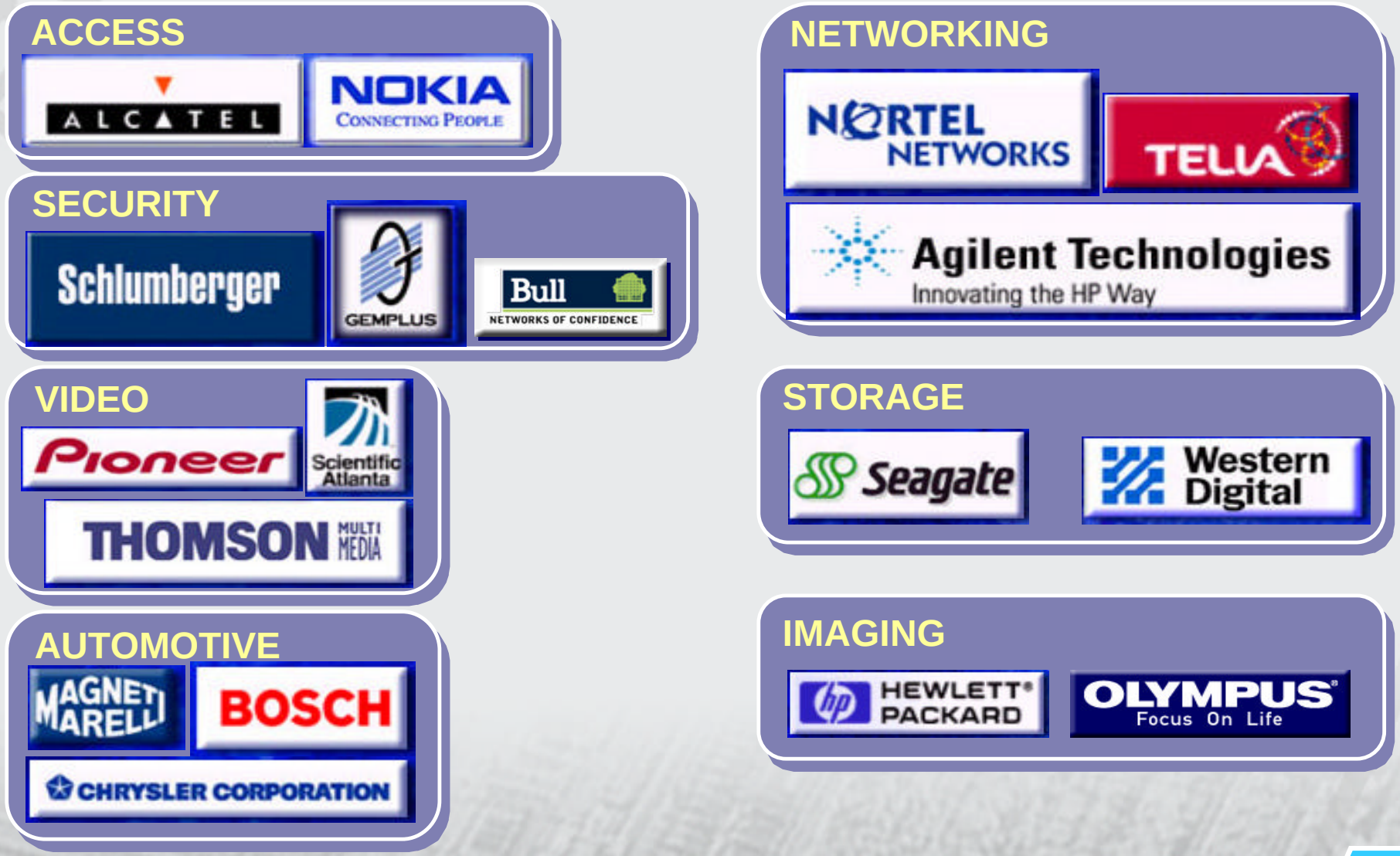


(Source: Doz, Santos, & Williamson, "From Global to Metanational: How Companies Win in the Knowledge Economy", Harvard Business School Press, 2001 forthcoming)

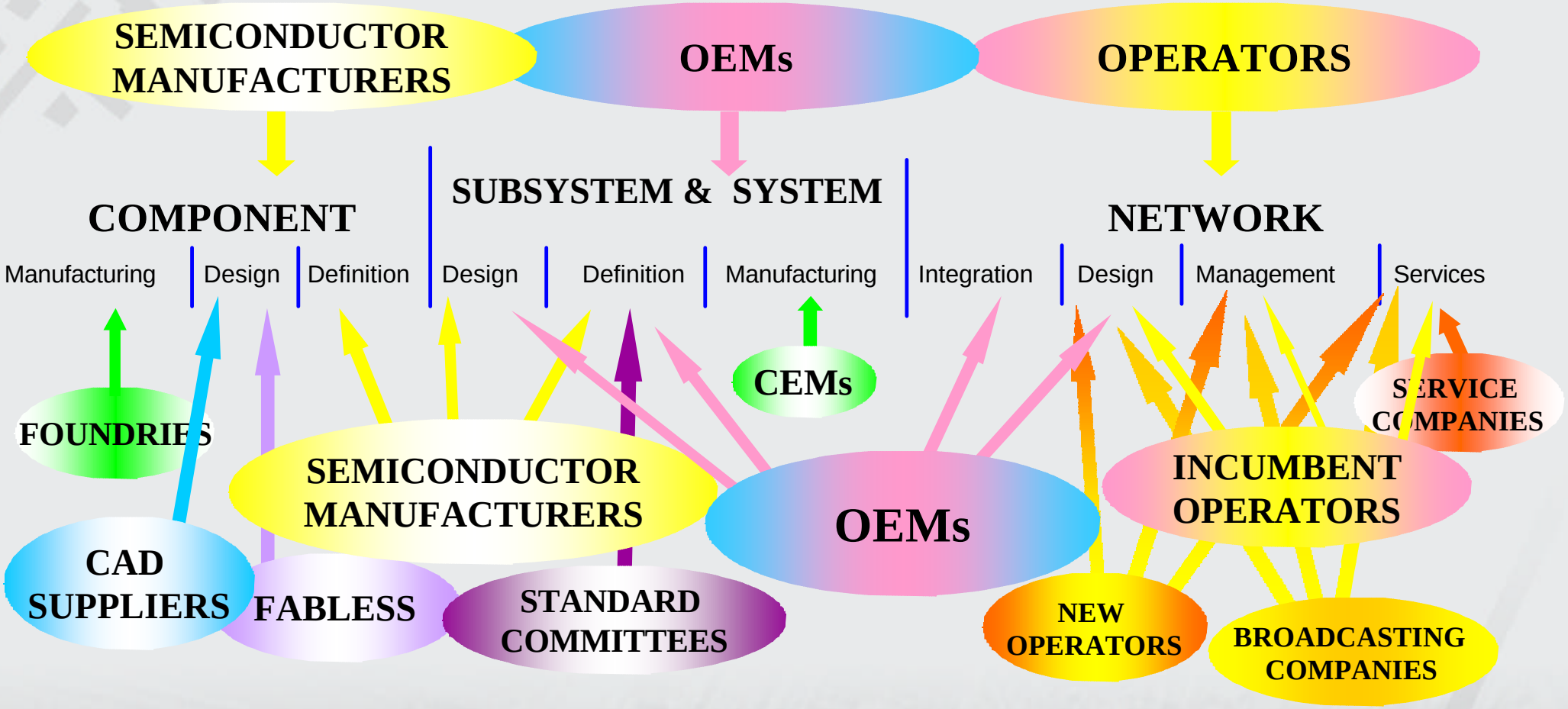
A World of Opportunities



Working With Leaders

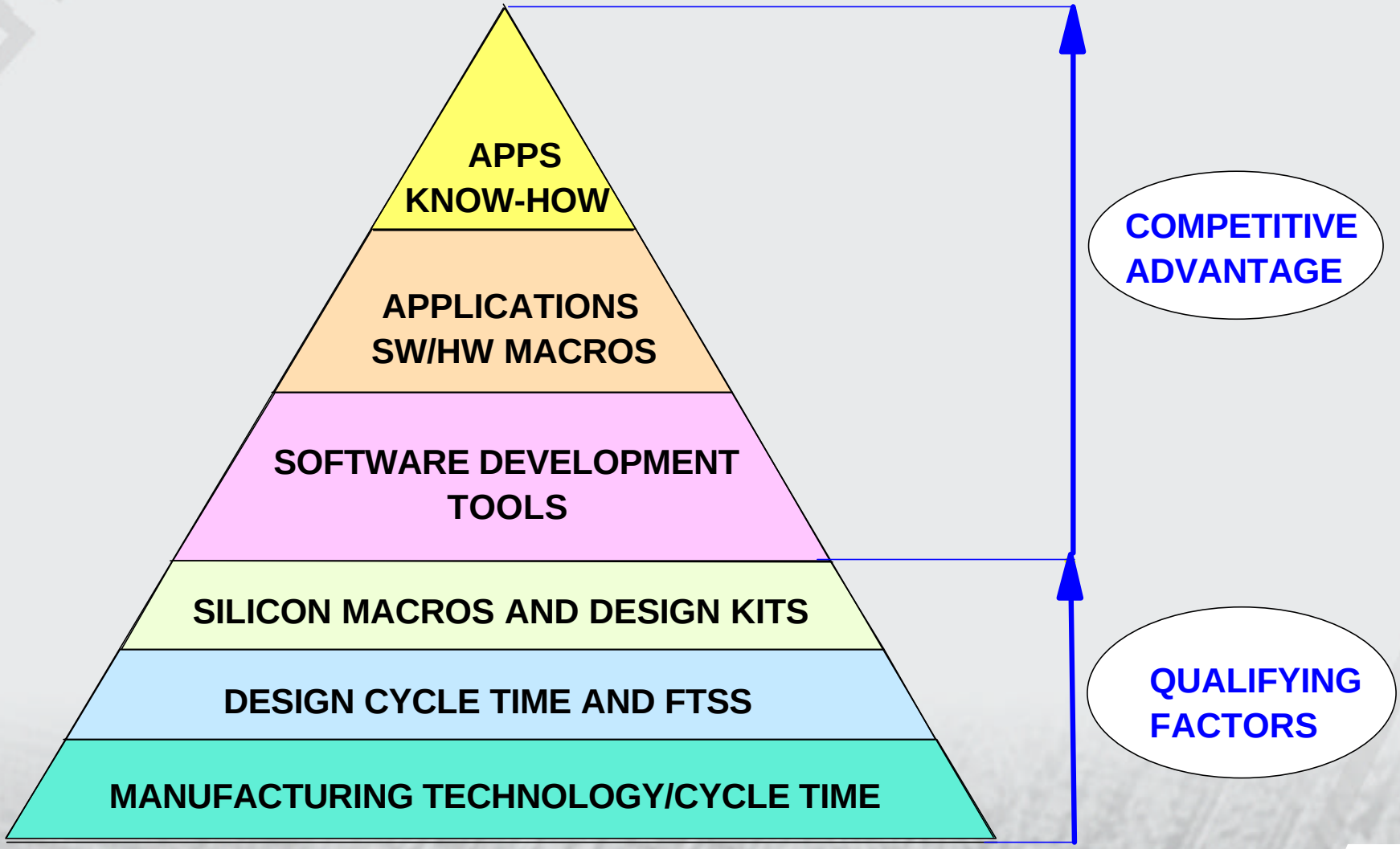


Moving Down the Value Chain



THE STRATEGIC FOCUS MOVES TO THE BUSINESS MODEL

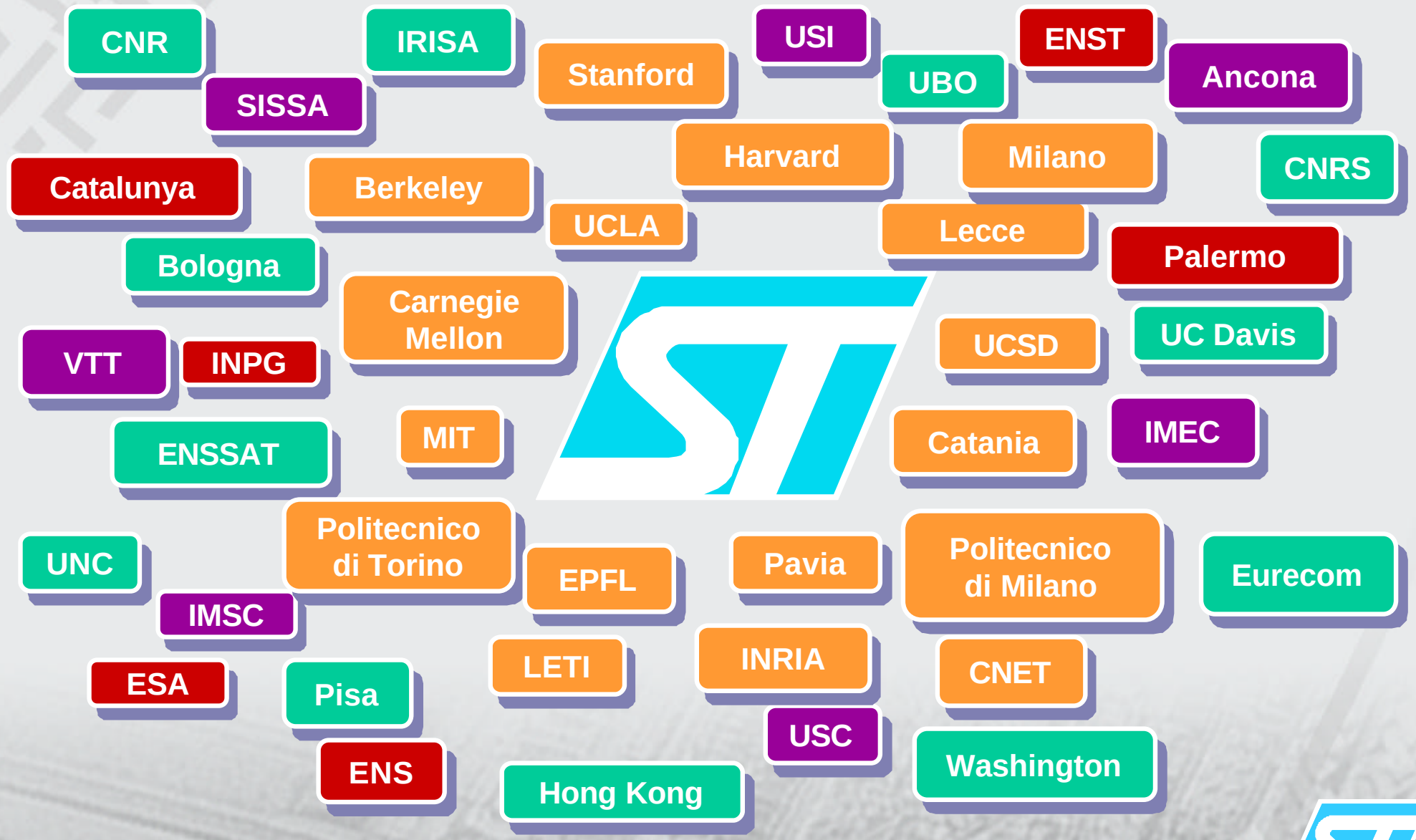
The Value-Added Proposition



A World-Class Network of Partnerships

- EDA VENDORS
- IP PROVIDERS
- FOUNDRIES & SUBCONTRACTORS
- COMPETITORS
- START-UPS
- SOFTWARE PROVIDERS
- OPERATORS

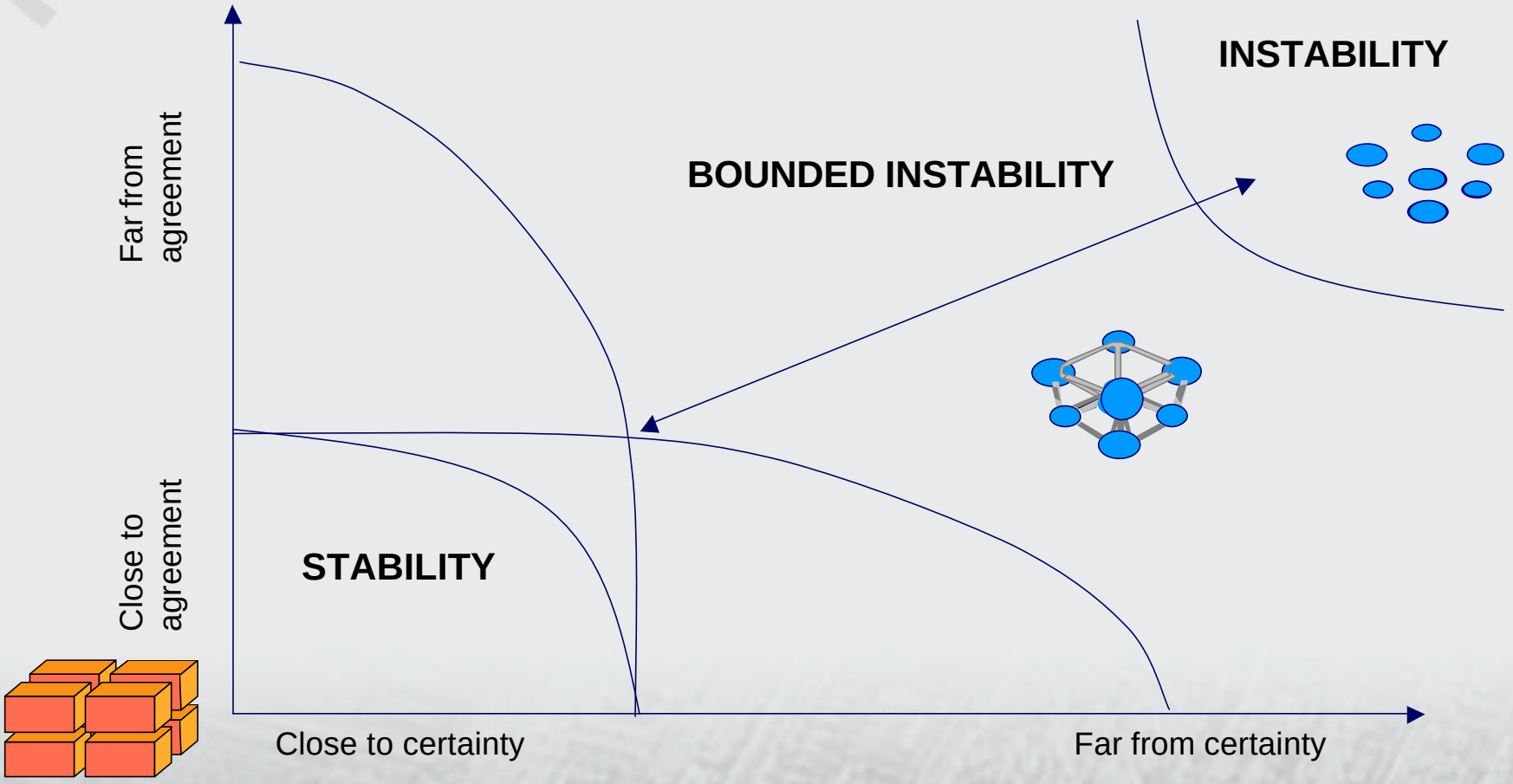
World-Class Academic Network



You have to be able to live with a lot of different cultures, and above all you have to get used to the fact that you can’t give orders.

P. Drucker

New Organization Models



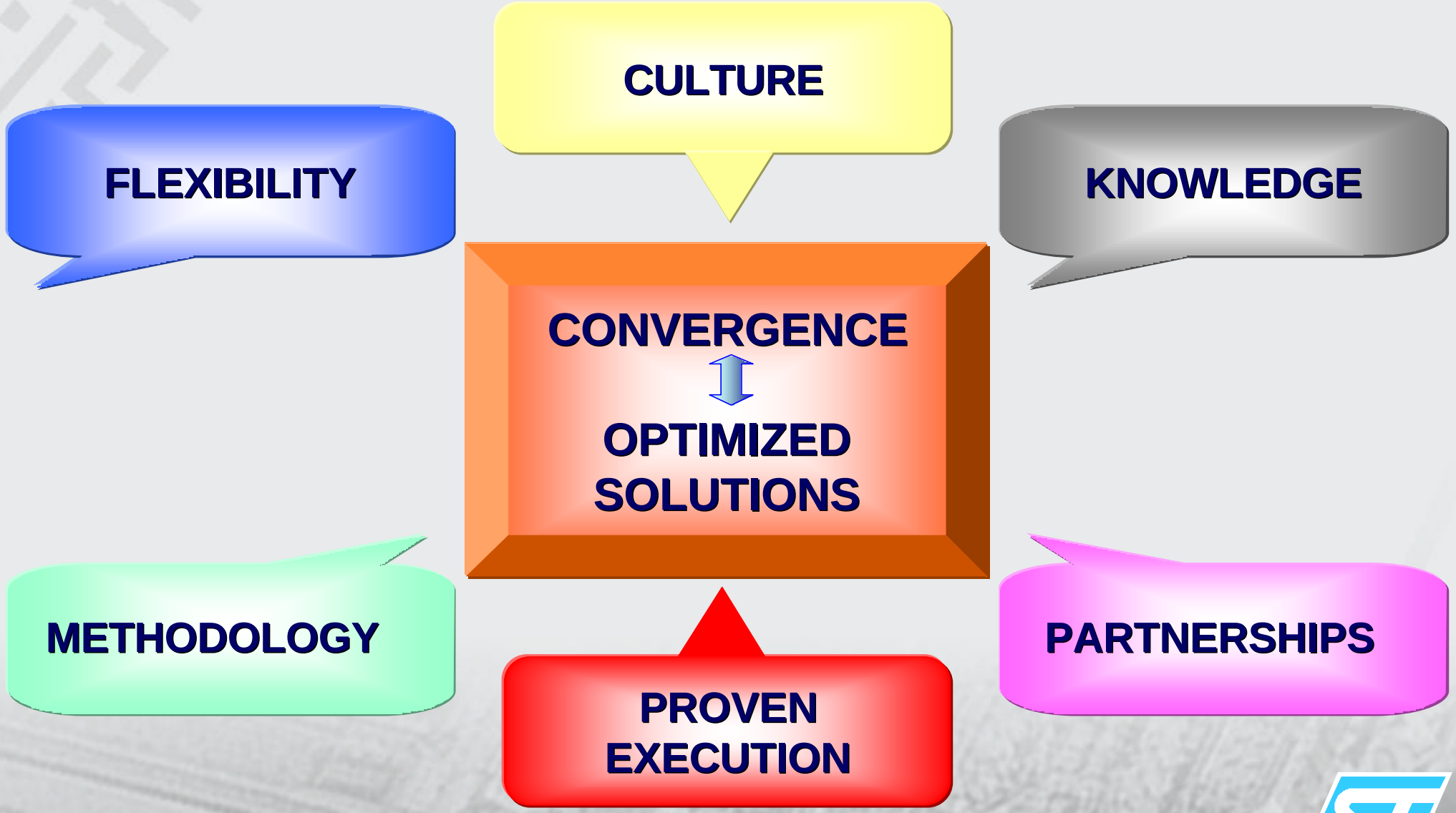
From The Machine Model To Complex Adaptive Systems

Predictable	———	Uncertain
Hierarchical	———	Ambiguous
Defined	———	Volatile

planning

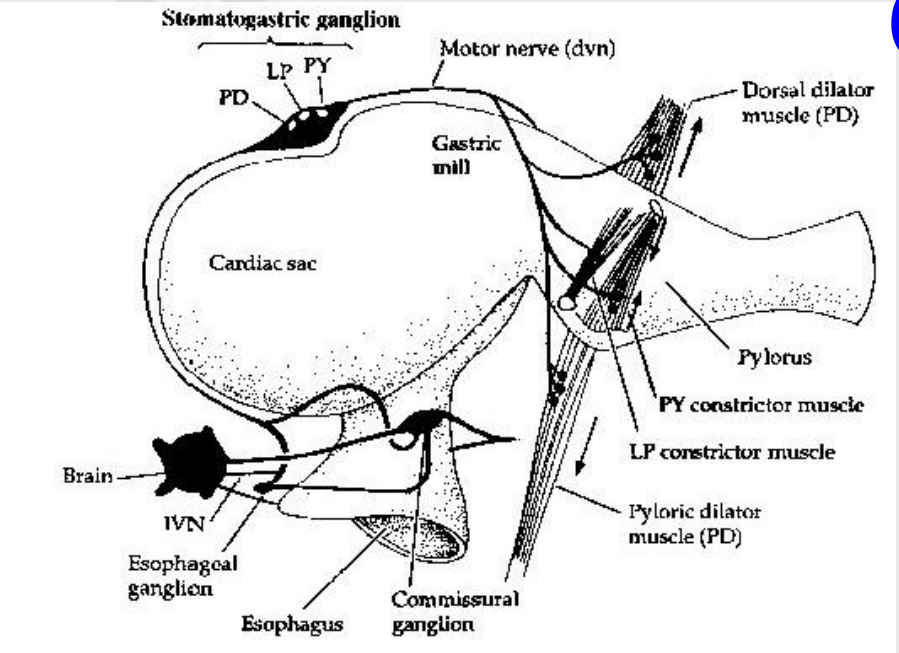
adaptability

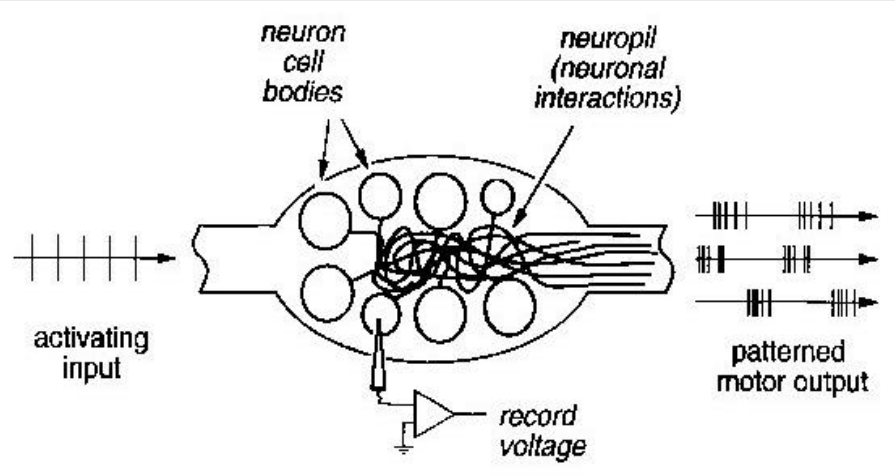
Leading Convergence



Professor Sandro Mussa-Ivaldi's Team
Northwestern University Medical School, Chicago, USA

Central Pattern Generators in the California spiny lobster





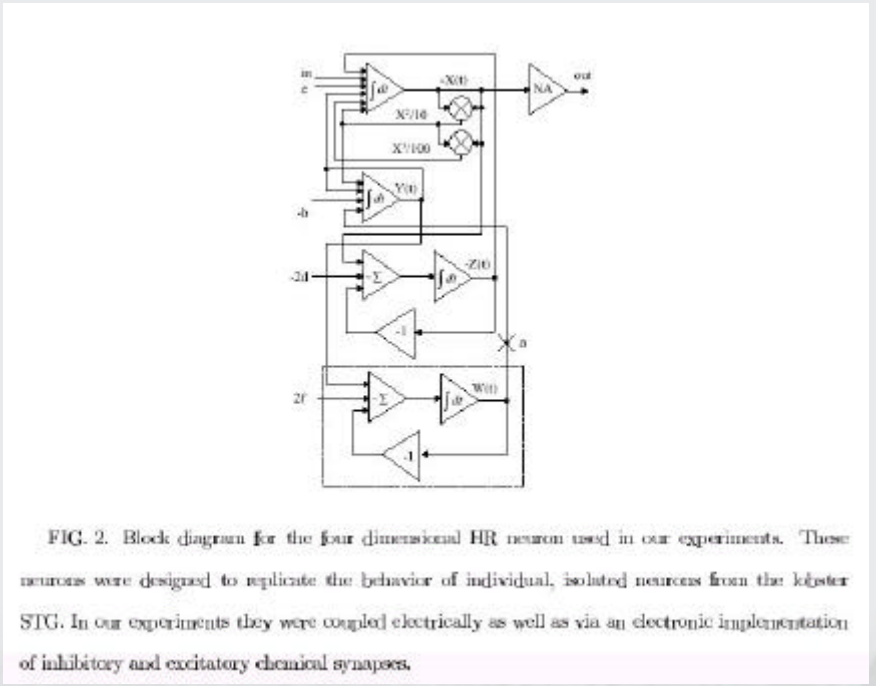
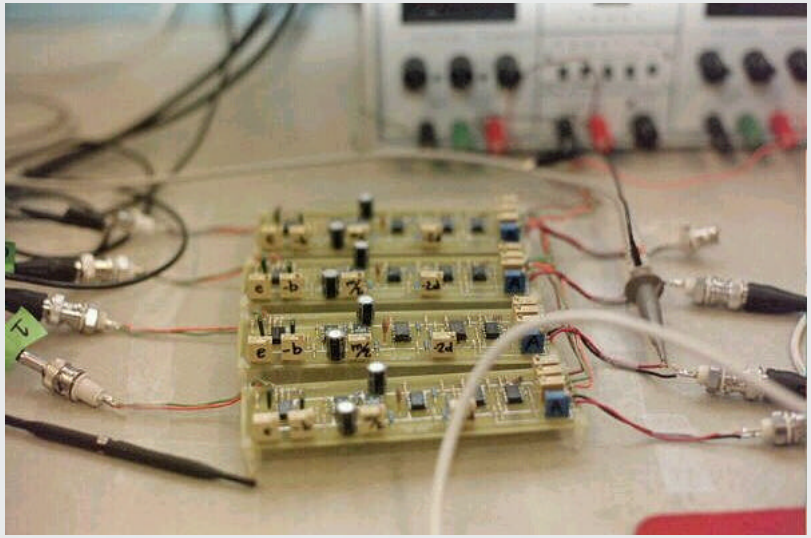


FIG. 2. Block diagram for the four dimensional HR neuron used in our experiments. These neurons were designed to replicate the behavior of individual, isolated neurons from the lobster STG. In our experiments they were coupled electrically as well as via an electronic implementation of inhibitory and excitatory chemical synapses.

Courtesy of Henry Abarbanel, Director
Institute for Nonlinear Science
University of California, San Diego, USA

Coupling of Biological And Electronic Neurons

- **Succeeded in coupling the e-neurons to the biological neurons, and even in replacing an e-neuron.**



Courtesy of Henry Abarbanel, Director
Institute for Nonlinear Science
University of California, San Diego, USA

THE MERGE OF MICROMECHANICS, ELECTRONICS, BIOLOGY, GENETICS WILL OPEN A COMPLETELY NEW HORIZON TO MANKIND.
AND TO COMPUTER SCIENCE, TOO.