EMI Noise Reduction Techniques

for High Frequency Power Converters

Yuchen Yang

Dissertation submitted to the Faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
in
Electrical Engineering

Fred C. Lee (Chair)
Qiang Li
Jaime De La Ree
Virgilio Centeno
Steve C. Southward

April 16th, 2018
Blacksburg, Virginia

Keywords: Wide-band-gap devices, high frequency, EMI, Magnetic integration

EMI Noise Reduction Techniques for High Frequency Power Converters

Yuchen Yang

Abstract

Switch mode power supplies are widely used in different applications. High efficiency and high power density are two driving forces for power supply systems. However, high *dv/dt* and *di/dt* in switch mode power supplies will cause severe EMI noise issue. In a typical front-end converter, the EMI filter usually occupies 1/3 to 1/4 volume of total converter. Hence, reducing the EMI noise of power converter can help reduce the volume of EMI filter and improving the total power density of the converter.

The EMI noise can be separated as differential mode (DM) noise and common mode (CM) noise. For off-line switch mode power supplies, DM noise is dominated by PFC converter. CM noise is a more complicated issue. It is contributed by both PFC converter and DC/DC converter. The DM noise is contributed by input current ripple. Therefore, one method to reduce DM noise is interleaving. There are three methods to reduce CM noise: symmetry, balance and shielding. The idea of symmetry concept is generating another dv/dt source to cancel the original dv/dt source. However, this method is very difficult to achieve and usually has more loss. The balance technique forms a Wheatstone bridge circuit to minimize the CM noise. However, the balance technique cannot achieve very good attenuation at high frequency due to parasitics. Shielding technique is very popular in isolated DC-DC converters to reduce CM noise. However, the previous shielding

method requires precise control of parasitic capacitance and dv/dt. It is very difficult to achieve good CM noise attenuation in mass production.

In this dissertation, a novel one-layer shielding method for PCB winding transformer is provided. This shielding technique can block CM noise from primary side and also cancel the CM noise from secondary side. In addition, shielding does not increase the loss of converter too much. Furthermore, this shielding technique can be applied to matrix transformer structure. For matrix transformer LLC converter, the inter-winding capacitor is very large and will cause severe CM noise problem. By adding shielding layer, CM noise has been greatly reduced. Although flyback and LLC resonant converter are used as examples to demonstrate the concept, the novel shielding technique can also be applied to other topologies that have similar transformer structure.

With Wide-band-gap power devices, the switching frequency of power converter can be pushed 10 times higher than traditional Si based converters. This provides an opportunity to use PCB winding magnetics. In order to reduce the switching loss, critical conduction mode is used in PFC converter. Because of high AC current in the inductor winding, litz wire was used to build the inductor. However, with coupled inductor concept and the proposed winding structure, CRM inductor is integrate into PCB winding for the first time. Furthermore, balance technique is applied to reduce CM noise for PFC converter. With PCB winding, the balance technique has better high frequency performance. The PCB winding inductor can achieve high power density, high efficiency and automated manufacture.

Traditionally, two-stage EMI filter was utilized to achieve required EMI noise attenuation. With the developed high frequency, low EMI noise converter, single-stage EMI filter can be applied. However, there are self-parasitic and mutual parasitic components to impact the filter performance on high frequency. The near-field measurement is utilized to visualize the magnetic

flux near those filter components. Thus, a better filter design and layout can be achieved to have better high frequency performance.

EMI Noise Reduction Techniques for High Frequency Power Converters

Yuchen Yang

General Audience Abstract

Switch mode power supplies are widely used in different applications. High efficiency and high power density are two driving forces for power supply systems. In a world full of electronic devices, it is very important that these devices can work properly in a complicated electromagnetic environment. Thus, electromagnetic compatibility (EMC) is a significant characteristic of electronic devices. However, high *dv/dt* and *di/dt* in switch mode power supplies will cause severe EMI noise issue. In a typical front-end converter, the EMI filter usually occupies 1/3 to 1/4 volume of total converter. Hence, reducing the EMI noise of power converter can help reduce the volume of EMI filter and improving the total power density of the converter. In this dissertation, several methods to reduce EMI noise are proposed and analyzed. First, the shielding method for PCB winding transformer is proposed. It can effectively reduce EMI noise at wide frequency range. Second, balance technique is applied to reduce EMI noise of PFC converter. Traditionally, two-stage EMI filter was utilized to achieve required EMI noise attenuation. With the developed high frequency, low EMI noise converter, single-stage EMI filter can be applied. However, there are self-parasitic and mutual parasitic components to impact the filter performance on high frequency. The near-field measurement is utilized to visualize the magnetic flux near those filter components. Thus, a better filter design and layout can be achieved to have better high frequency performance.

To My Family

My parents: Shijun Yang and Ying Lu

My parents-in-law: Jiquan Li and Qiusha Dai

My wife: Zhuxuan Li

Acknowledgments

First and foremost I would like to thank my advisor, Dr. Fred C. Lee for his guidance, encouragement and education. It is him who opens the door of power electronics for me and show me the right way to do research. He is not only a wise and farsighted advisor in academic, but also a mentor in life. He pointed out my character weaknesses and helped me become a better person. His profound knowledge, rich experience, rigorous attitude, and challenging spirit have been a great value for me. It is most honored to be advised by Dr. Lee. The experience of studying at CPES is a life-changing experience.

I am very grateful to my other committee members Dr. Qiang Li, Dr. Jaime De La Ree, Dr. Virgilio Centeno, and Dr. Steve Southward. I still remember the weekly meeting with Dr. Li when I first came to CPES. He taught me how to start a research and how to express my ideas. Thanks for all the constructive and helpful suggestions offered by Dr. Li.

My very special thanks go to my colleagues Dr. Zhengyang Liu and Mr. Bin Li. As a team, we have worked on several projects. I cannot accomplish so much without their help.

I really appreciate the discussions and suggestions from Dr. Dushan Boroyevich, Dr. Khai Ngo, Dr. Rolando Burgos, and Dr. Guo-Quan Lu in High Density Integration (HDI) group.

I really want to thank all my colleagues in the Power Management Consortium (PMC) group: Dr. David Reusch, Dr. Mingkai Mu, Dr. Yingyi Yan, Dr. Weiyi Feng, Dr. Daocheng Huang, Dr. Zijian Wang, Mr. Shu Ji, Mr. Haoran Wu, Dr. Yipeng Su, Mr. Wei Zhang, Mr. Li Jiang, Dr. Shuilin Tian, Dr. Pei-Hsin Liu, Dr. Dongbin Hou, Dr. Yang Jiao, Mr. Sizhao Lu, Mr. Chao Fei, Mr. Xuebing Chen, Ms. Yincan Mao, Mr. Zhongsheng Cao, Mr. Syed Bari, Mr. Tao Liu, Ms. Virginia

Li, Mr. Junjie Feng, Mr. Yi-Hsun Hsieh, Mr. Mohamed Ahmed, Mr. Yadong Lyu, Mr. Rimon Gadelrab, Mr. Shishuo Zhao, Mr. Shuo Wang, Mr. Yinsong Cai, Mr. Feiyang Zhu. Mr. Owen Jong, Mr. Ahmed Nabih, Dr. Xinke Wu, Dr. Xin Ming, Dr. Weijing Du, Dr. Shuojie She, Mr. Yan-Cun Li, Dr. Kenichiro Tanaka, Dr. Minfan Fu, Mr. Furong Xiao, Mr. Guo Xu, and Dr. Rong Xu. My thanks also go to many of the other students and visiting scholars I have met in CPES.

I sincerely thank all the wonderful CPES staffs: Ms. Teresa Shaw, Mr. Douglas Sterk, Mr. David Gilham, Ms. Linda Gallagher, Ms. Teresa Rose, Ms. Marianne Hawthorne, Ms. Linda Long, Mr. Igor Cvetkovic, and Ms. Lauren Shutt for their help and support.

In addition, this work was supported by CPES Power Management Consortium, and the Engineering Research Center Shared Facilities supported by the National Science Foundation under NSF Award Number EEC-9731677. Any opinions, findings and conclusions or recommendations expressed in this material are those of the author and do not necessarily reflect those of the National Science Foundation.

The information, data, or work presented herein was funded in part by the Office of Energy Efficiency and Renewable Energy (EERE), U.S. Department of Energy, under Award Number DE-EE0006521 with North Carolina State University, PowerAmerica Institute.

The information, data, or work presented herein was funded in part by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement,

recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

This material is partially based upon work supported by the U.S. Department of Energy, Office of Energy Efficiency and Renewable Energy, under the project of High Efficiency High Density GaN Based 6.6kW Bi-Directional On-board Charger for PEVs, through Delta Products Corp, under contract number DE-EE0006834.

Table of Contents

List of Figures

List of Tables

Chapter 1. Introduction

1.1 Introduction to EMI and EMC

In a world full of electronic devices, it is very important that these devices can work properly in a complicated electromagnetic environment. Thus, electromagnetic compatibility (EMC) is a significant characteristic of electronic devices. The definition of EMC according to International Electrotechnical Commission (IEC) is "The ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment."[1]. Nowadays, EMC is becoming more and more important. First, more and more applications are going to be electrified, such as automobile, ship, and aircraft. Every devices in these applications must work properly to assure safety. In addition, recent years have seen a dramatically growth of personal electronic devices. We are facing a more complicated electromagnetic environment that we have never met before. Second, modern electronic devices are more susceptible to electromagnetic disturbances. The lower supply voltage is more easily affected by noises. Higher switching frequency is introducing severe disturbances. Furthermore, the pursuing of power density is making electronic devices closer to each other.

Electromagnetic interference is defined as "degradation of the performance of an equipment, transmission channel or system caused by an electromagnetic disturbance" [2]. There are four methods that the electromagnetic interference can propagate from the noise source to the victim:

(1) Conducted interference;

(2) Radiated interference;

(3) Inductive interference;

(4) Capacitive interference.

The conducted interference means the noise propagates through conductors. Radiated interference propagates through the radiation of electromagnetic field. The inductive and capacitive interference combined as the near field coupling propagates from the noise source to the victim.

EMI can cause malfunction of electronic devices, from the annoying cell phone interference to lethal failure of life support equipment in the hospital. In order to avoid those impacts, there are several EMI standards to limit both the conducted and radiated EMI noise, such as FCC part 15 in United States and CISPR 22 in Europe. Fig. 1.1 shows the EN55022 Class B standards for conducted EMI noise.

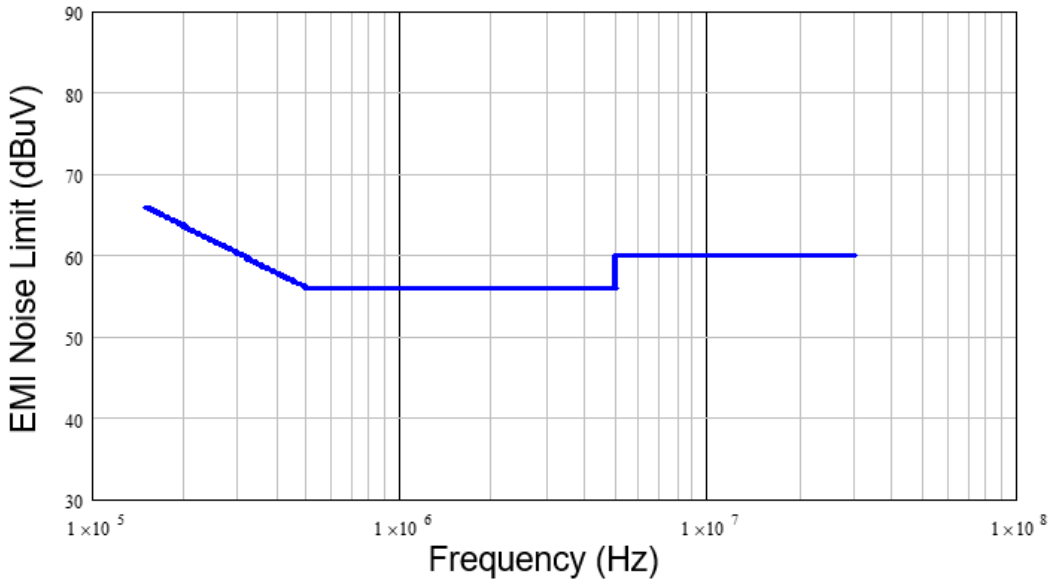


Fig. 1.1 EMI standard EN55022 Class B for conducted noise

1.2 EMI Measurement

Because of the complexity of EMI propagation path, different measurement setup leads to different result. In order to get a constant measurement condition, EMI standards provide the specified measurement setup. The FCC measurement setup is shown in Fig. 1.2.

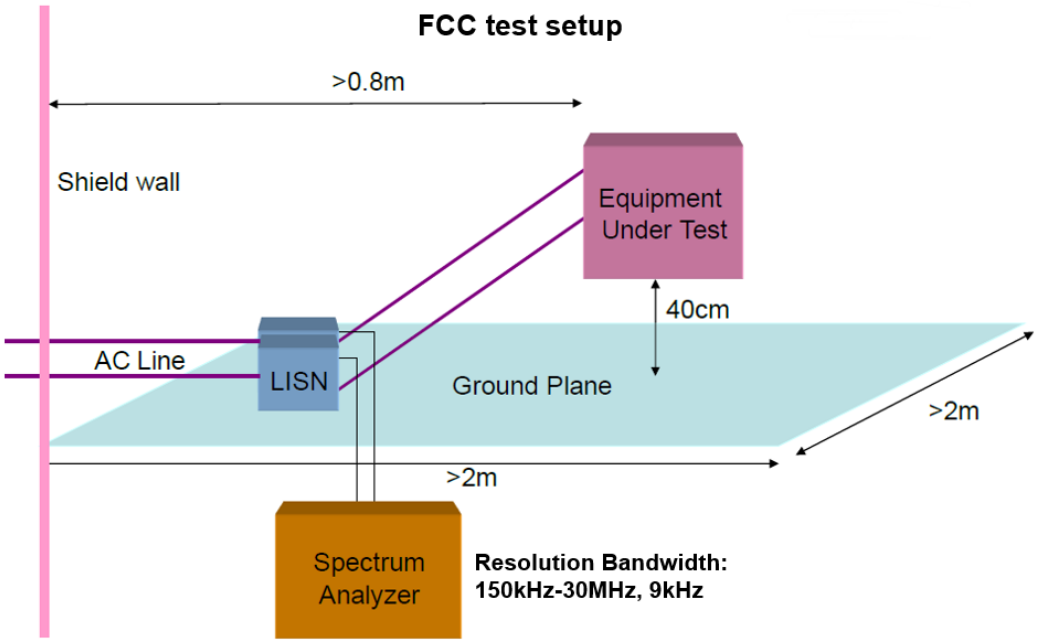


Fig. 1.2 FCC measurement setup

Line Impedance Stabilization Network (LISN) is used to guarantee constant measurement condition. Fig. 1.3 shows the internal circuit of a LISN. The main function of LISN is that it provide a stable loop impedance that can get repeatable measurements of the EMI noise. LISN works like a low-pass filter that it can block high frequency noise from the power source and allow low frequency power flow to the Equipment-Under-Test (EUT).

In the real measurement setup, two LISNs are needed to connect between power source and EUT as shown in Fig. 1.4. A spectrum analyzer is connected to one LISN to pick up the total noise while a standard 50Ω terminator is connected to the other LISN.

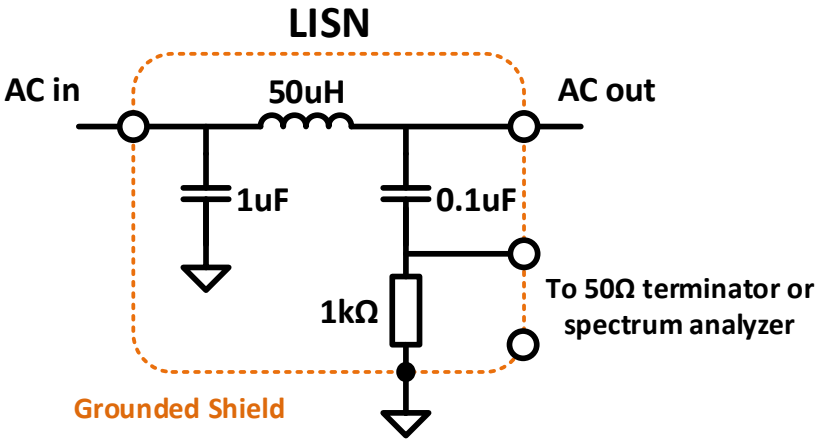


Fig. 1.3 Internal circuit of a LISN

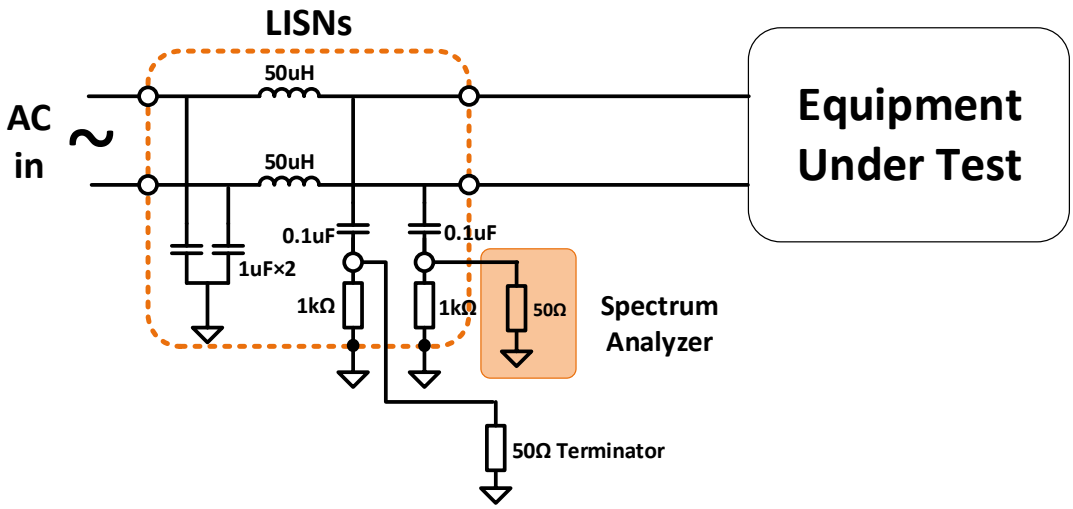


Fig. 1.4 Practical noise measurement circuit

There are three different methods to measure EMI noise: peak, average and quasi-peak. The peak detector picks the maximum amplitude of the noise signal for each frequency. The average detector takes an envelope-detected signal and passes it through a low-pass filter with a bandwidth

much less than the resolution bandwidth. The filter integrates (averages) the higher-frequency components such as noise. Quasi-peak detector is a weighted form of peak detection. The measured value of the quasi-peak detector drops as the repetition rate of the measured signal decreases [3].

1.3 Conducted EMI Noise in Switch Mode Power Supplies

Switch mode power supplies are widely used in different applications, such as power supply for telecom and server, silver box for desktops, adapter for laptops and charger for personal mobile devices.

Switch mode power supplies is a complicated system and have different structures for different applications. Fig. 1.5 shows the structure of power supply below 75W. Because the power is below 75W, it do not need a power factor correction (PFC) circuit. The diode bridge rectifies the AC input voltage to DC voltage. The isolated DC-DC converter converts the DC voltage to desired DC bus voltage. Then the voltage regulator (VR) module converts the bus voltage to different load voltage and assures the required transient performance.

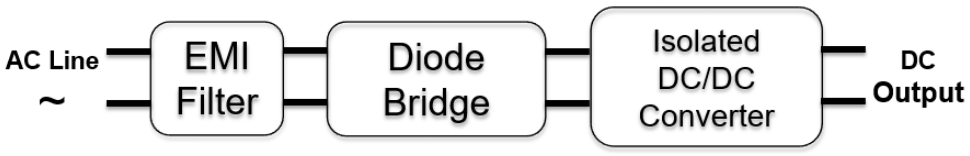


Fig. 1.5 Structure of low power converter

For the power supply for server and telecom system, the structure is a little different. Fig. 1.6 shows the structure of front-end converter for server and telecom system. First, the PFC converter rectifies the AC input voltage to 380V DC voltage. Second, the DC-DC converter converts the 380V DC voltage to a 48V/12V DC bus voltage. Then the voltage regulator module will take over.

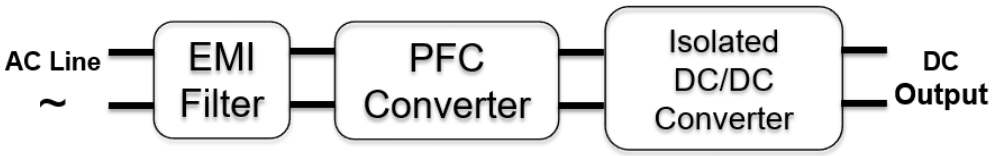


Fig. 1.6 Front-end converter for server and telecom

Switch mode power supplies never stop pursuing high efficiency and high power density. In order to reach this goal, new semiconductor devices, such as GaN and SiC, are being developed. In addition, circuit topologies, structure and control method continue improving to help make switch mode power supplies smaller, lighter and more efficient.

However, high *dv/dt* and *di/dt* in switch mode power supplies will cause severe EMI noise issue. Hence, EMI filter is always needed in switch mode power supply to attenuate severe conducted EMI noise. Fig. 1.7 shows a state-of-the-art front-end converter for server system. It can be seen that the EMI filter takes about 1/4 to 1/3 volume of total converter. Reducing the noise of power converter can reduce the size and volume of EMI filter and help improving the power density of total converter.

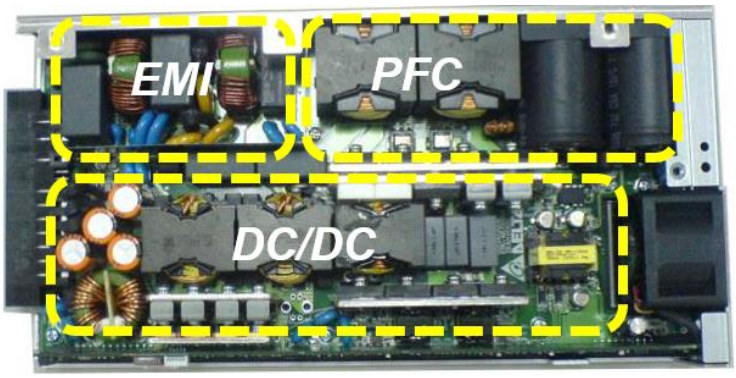


Fig. 1.7 State-of-the-art front end converter

The conducted EMI noise is always decoupled to differential mode (DM) noise and common mode (CM) noise. Because the DM noise and CM noise have different propagation path, they need

different attenuation method. Fig. 1.8 shows the propagation path of DM conducted noise. DM noise current i_{DM} flows between two power lines. Fig. 1.9 shows the propagation path of CM conducted noise. CM noise current i_{CM} flows between power lines and ground.

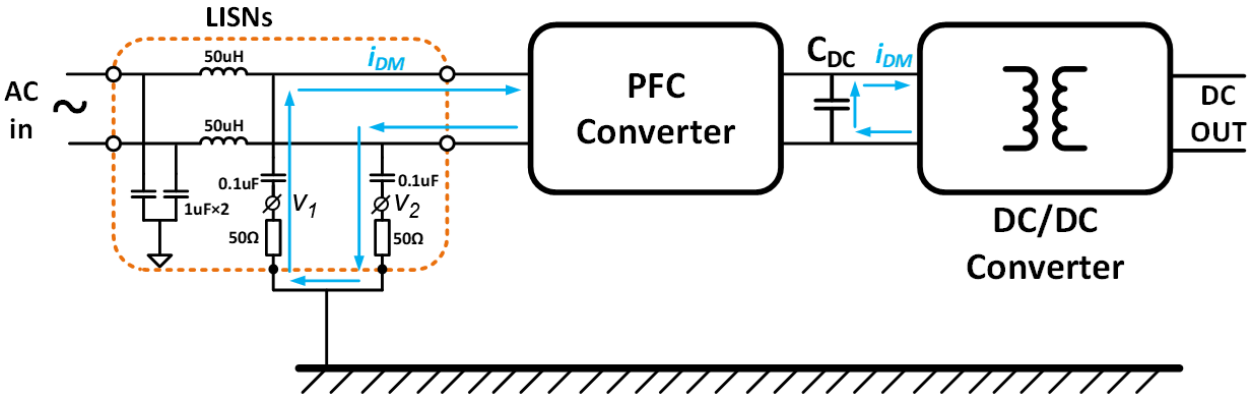


Fig. 1.8 DM noise propagation path

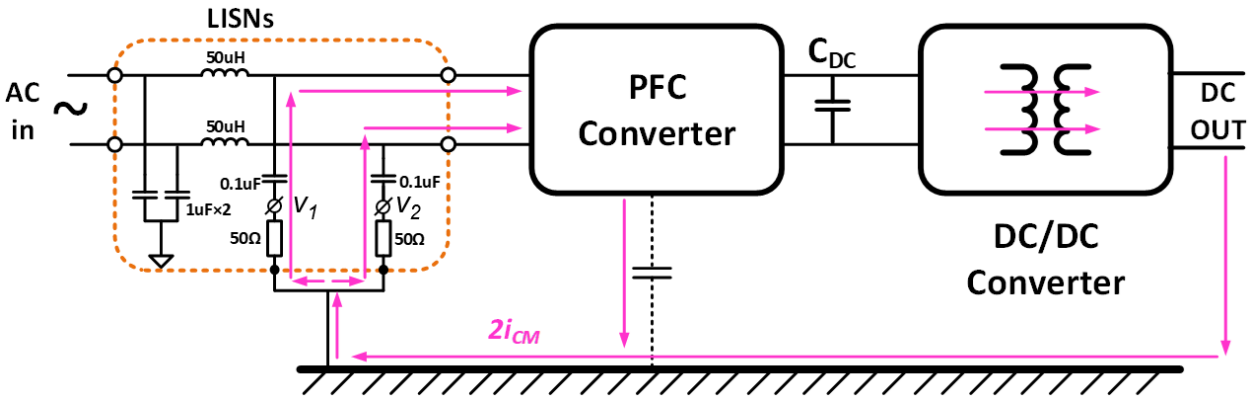


Fig. 1.9 CM noise propagation path

According to the EMI standard EN55022, the noise voltage on the 50Ω resistor is limited:

$$\begin{cases} v_1 = 50(i_{DM} - i_{CM}) \\ v_2 = 50(-i_{DM} - i_{CM}) \end{cases} \tag{1-1}$$

v_1 and v_2 both can represent total EMI noise. In the measurement, the amplitudes of v_1 and v_2 are almost identical because i_{DM} and i_{CM} are high frequency AC currents [5].

DM noise voltage and CM noise voltage can then be represented as:

$$\begin{cases} v_{DM} = 50 i_{DM} = \frac{v_1 - v_2}{2} \\ v_{CM} = -50 i_{CM} = \frac{v_1 + v_2}{2} \end{cases} \tag{1-2}$$

For off-line switch mode power supplies, DM noise is dominated by PFC converter. CM noise is a more complicated issue. It is contributed by both PFC converter and DC/DC converter. A lot researches have been done to reduce the CM noise of PFC converter [6]-[11]. However, the CM noise of DC/DC converter still remains a challenge.

1.4 EMI Noise Reduction Methods for Switch Mode Power Supplies

There are three types of CM noise reduction method, symmetry, balance and shielding.

CM noise current is formed by severe *dv/dt* on parasitic capacitance, as shown in (1-3). The idea of symmetry technique is forming two dv/dt sources that have same amplitude but opposite direction. With same capacitance in the propagation path, the two noise sources can cancel each other and minimize CM noise. Before the balance technique was proposed, several methods had been provided to reduce CM noise by using symmetry concept [12]-[19].

$$i_{CM} = C \frac{dv}{dt} \tag{1-3}$$

Fig. 1.10 shows the topology of full bridge LLC converter. The two switch nodes on primary side are symmetrical. When V_1 has a positive dv/dt, V_2 will have a negative dv/dt with same amplitude. The two switch nodes on the secondary side are also complimentary. Therefore, the CM noise generated by these noise sources will be canceled by each other.

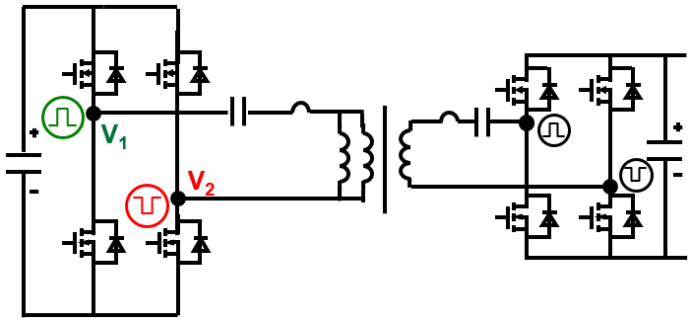


Fig. 1.10 Full bridge converter

However, in the real circuit, it is very difficult to match the two complimentary dv/dt sources. As shown in Fig. 1.11, the dv/dt of V_2 is a little slower than V_1. Thus, the two noise sources cannot be completely cancelled. And CM noise is not minimized.

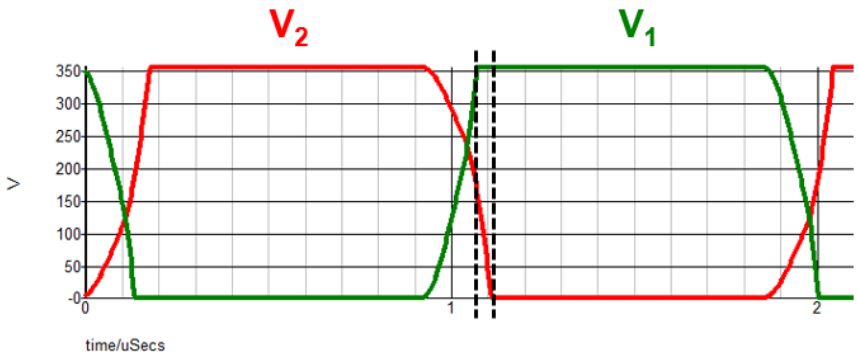
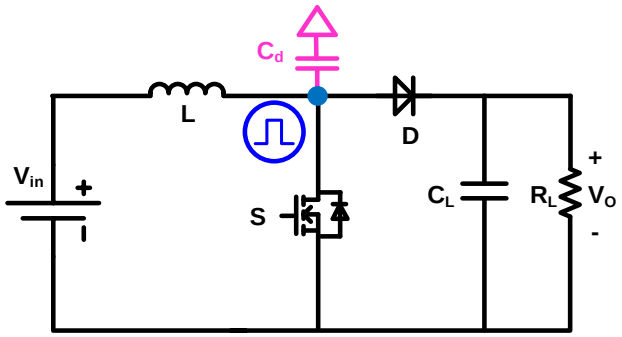


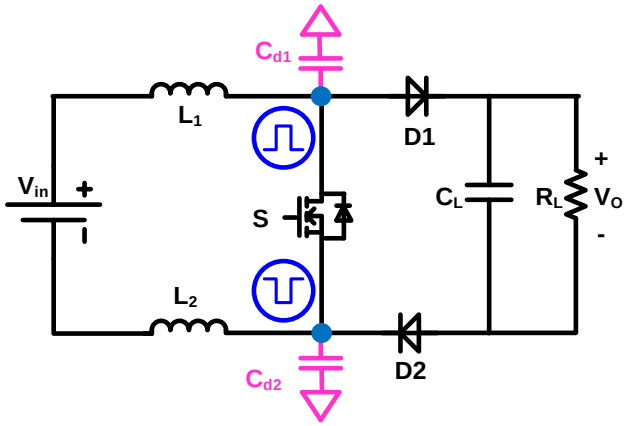
Fig. 1.11 Waveforms of V_1 and V_2

Another issue for symmetry method is that most circuit topologies are asymmetrical in nature. In order to achieve symmetry, additional components is required to be added in the circuit, such as diodes, power switches and windings. In [19], CM noise is cancelled by achieving symmetrical circuit topology for boost converter. Fig. 1.12 demonstrates the symmetrical boost topology versus a conventional boost topology [19]. The original boost inductor L is split into two identical coupled inductor L_1 and L_2. In addition, another diode D2 is introduced. Thus, another *dv/dt* source is introduced and it has the same amplitude and opposite polarity with node A. The parasitic capacitor

C_{d1} and C_{d2} is controlled to be the same value. Hence, the CM noise current flowing through C_{d1} and C_{d2} has the same amplitude but out-of-phase. Consequently, there is no net CM noise current flowing to the ground and CM noise has been cancelled.



(a) Conventional boost converter



(b) Symmetrical boost converter

Fig. 1.12 Boost converter with symmetry technique

Although the experiment shows significant CM noise reduction, symmetry technique has its own limitation. The additional components will make the converter more complicated and introduces extra loss and higher cost. It sacrifices too much to reduce CM noise, which is not applicable in commercial products.

In order to have good CM noise reduction without extra loss, balance technique is provided [7]. As shown in Fig. 1.13, the inductor is split in to L_1 and L_2, but there is no need to add another diode into the converter. C_d is the parasitic capacitance between MOSFET drain and ground. C_a is the parasitic capacitance between the cathode of diode D, large area of output traces, load and the ground. C_c is the parasitic capacitance between load, large area of output traces and the ground.

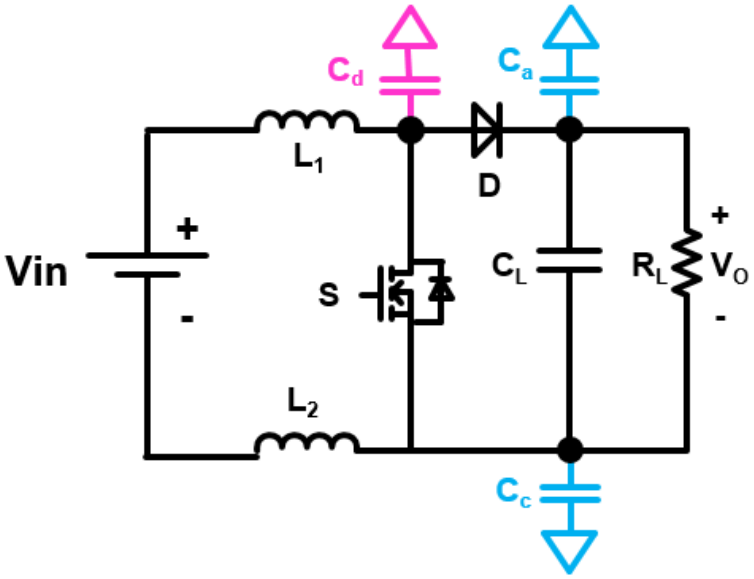


Fig. 1.13 Balanced boost converter

According to the substitution theorem, if the MOSFET branch is substituted by a voltage source V having the same voltage as the original branch, the circuit behavior keeps the same. Hence, the MOSFET can be replaced by a voltage source V, as shown in Fig. 1.14.

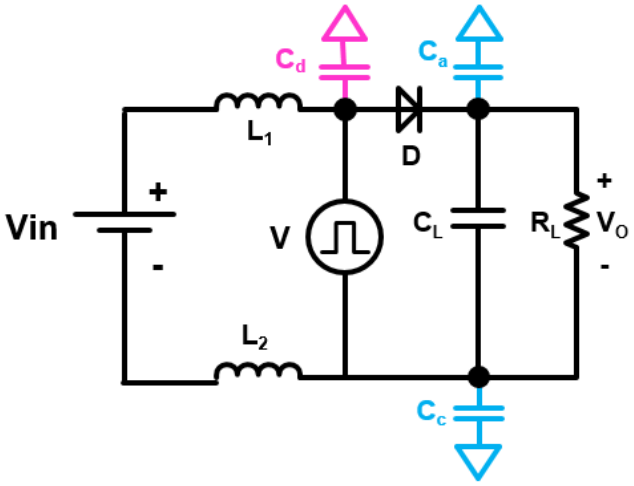


Fig. 1.14 Replace the MOSFET with a voltage source

In the CM noise frequency range, the input and output capacitor can be treated as short circuit. In addition, the diode bridge can also be treated as short circuit since it is always conducting current. Thus, the CM noise model of this boost converter is shown in Fig. 1.15.

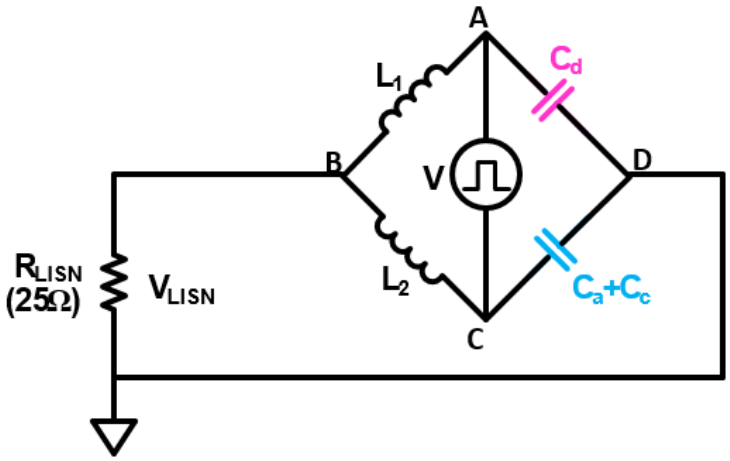


Fig. 1.15 CM noise model of balanced boost PFC converter

It can be seen that this CM noise model is a Wheatstone bridge circuit. In a general Wheatstone bridge structure shown in Fig. 1.16, if the balance equation (1-4) is satisfied, point B and point D have identical voltage and there is no current going outside this circuit.

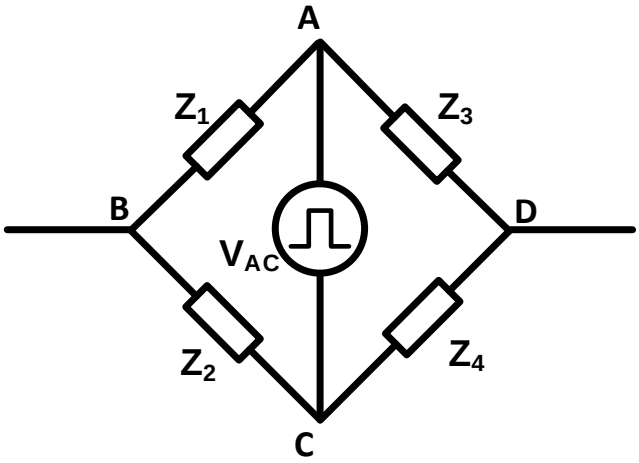


Fig. 1.16 Wheatstone bridge structure

$$\frac{Z_1}{Z_2} = \frac{Z_3}{Z_4} \tag{1-4}$$

Thus, for the CM noise model of boost PFC converter in Fig. 1.15, as long as the balance equation (1-5) is satisfied, there is no CM noise current generated by converter going through LISN.

$$\frac{Z_{L1}}{Z_{L2}} = \frac{Z_{Cd}}{Z_{Ca+Cc}} \tag{1-5}$$

In contrast to the symmetry technique, this ratio in the balance technique do not need to be only 1:1. The impedance ratio can be any value as long as the balance condition is satisfied, CM noise can be cancelled. Hence, the balance technique offers additional freedom to the designer to choose the impedance ratio according to the converter design. Furthermore, balance technique do not require additional components in the circuit. This will not increase the complexity of the converter and will not increase the cost and loss while has significant CM noise reduction, which is preferred in the commercial products.

However, the balance equation is only valid at low frequency. At high frequency, the equivalent parallel capacitor (EPC) and equivalent parallel resistor (EPR) of the inductor dominant the impedance of inductor branch. Therefore, at high frequency, the balance equation may not be achieved. Fig. 1.17 [8] shows the CM noise reduction result with balance technique for boost converter. It can be seen that at low frequency, the balance technique can reduce CM noise. But after 2 MHz, the CM noise is not reduced.

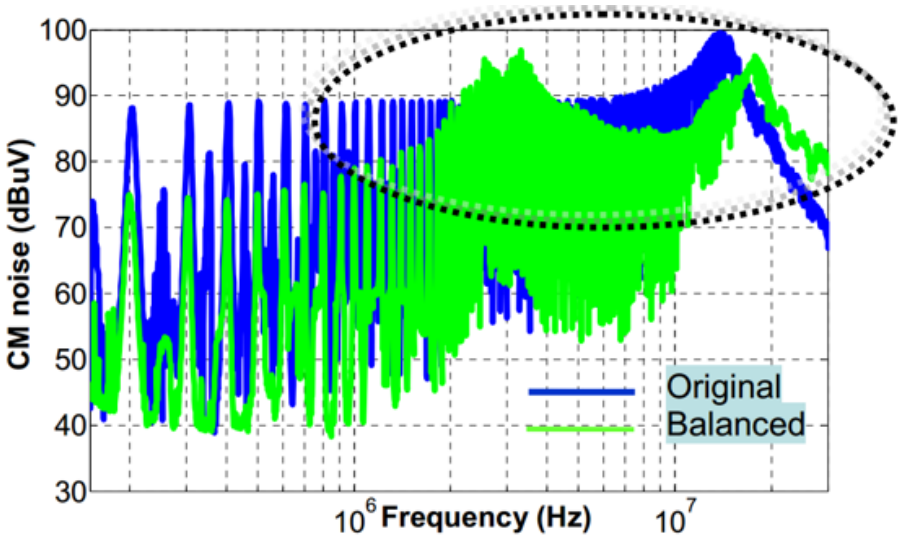
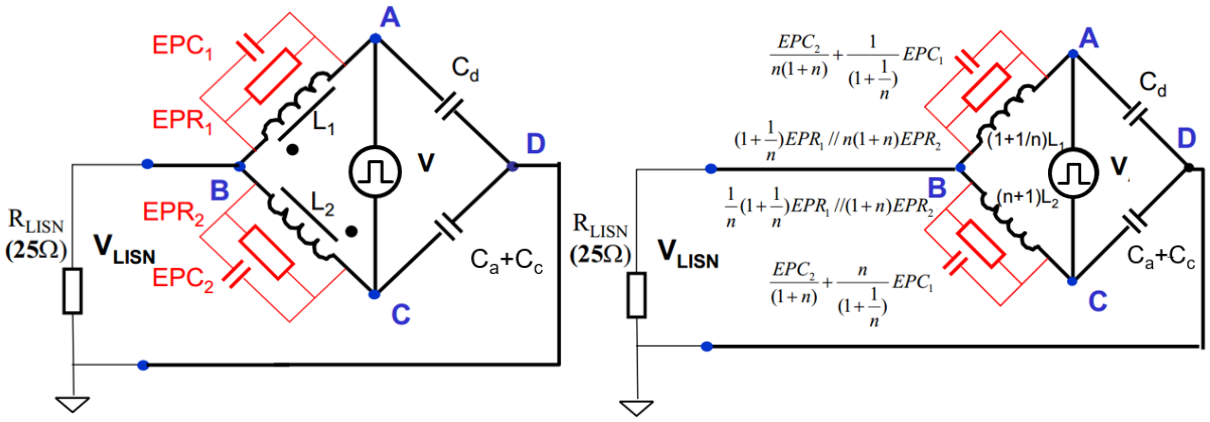


Fig. 1.17 CM noise reduction of boost converter with balance condition achieved at low frequency [8]

In order to improve the high frequency performance of balance technique, two inductors are coupled together, as shown in Fig. 1.18 [8]. It can be seen that with coupling, the ratio of inductance, EPC and EPR are all turns ratio of two inductor windings. The balance condition can be simplified as (1-6).



(a) CM noise model (b) Equivalent decoupled circuit

Fig. 1.18 Balance technique with coupled inductors [8]

$$n = \frac{C_b}{C_d} \tag{1-6}$$

The CM noise reduction result is shown in Fig. 1.19 [8]. The CM noise can be reduced significantly. However, the CM noise reduction is not good beyond 8 MHz. It is because that the balance equation (1-6) has an assumption: the coupling coefficient between L_1 and L_2 is 1. However, for a litz wire inductor with toroid core, it is difficult to achieve high coupling coefficient. The coupling coefficient between L_1 and L_2 are usually below 0.8. Therefore, the high frequency performance of balance technique is not as good as expected.

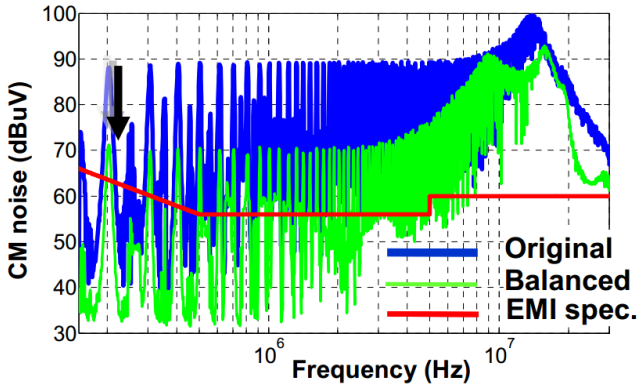


Fig. 1.19 CM noise of balanced boost converter with inductor coupling [8]

For the isolated DC/DC converter, the main CM noise path is the transformer. Take flyback converter as an example, it has two switches and one transformer, as shown in Fig. 1.20. The two switches can be modeled as two noise sources. The parasitic capacitance between the primary winding of transformer and secondary winding of transformer are the main propagation path of CM noise. Therefore, shielding method is very popular to reduce the CM noise in isolated converters.

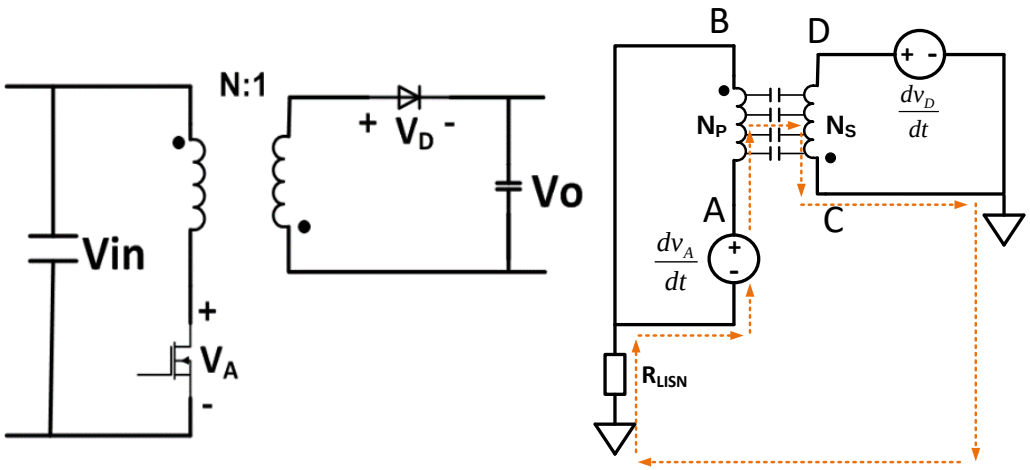


Fig. 1.20 Flyback converter and CM noise path

In a practical transformer, there is a large amount displacement current flowing between the primary and secondary windings. This contributes large CM noise current. The purpose of shielding is to block the CM noise propagation path through the transformer. [20] provides a method to block the CM noise current through transformer. Fig. 1.21 shows the proposed transformer structure. In this figure, half core of the transformer is implemented into the circuit. The primary winding has three layers and secondary winding has one layer. Instead of using one complete wire as the primary winding, this method breaks the primary winding into two parts. One part is normally winded primary winding P1, P2. The other part P3 is a shielding winding that is identical with secondary winding but connected in series with the primary winding. The

displacement current flows between primary windings does not contribute to the CM noise current because this current will circulating within the primary side. Fig. 1.22 shows the voltage distribution of the shielding and secondary windings. Assuming the voltage distributes linearly along the winding. It can be seen that for a specific point on the primary winding, it shares the same voltage potential as the corresponding point on the secondary winding. Consequently, there is no voltage difference between the shielding and secondary winding and no displacement current can flow between the shielding and secondary windings. Thus the CM noise current flowing through the transformer is blocked.

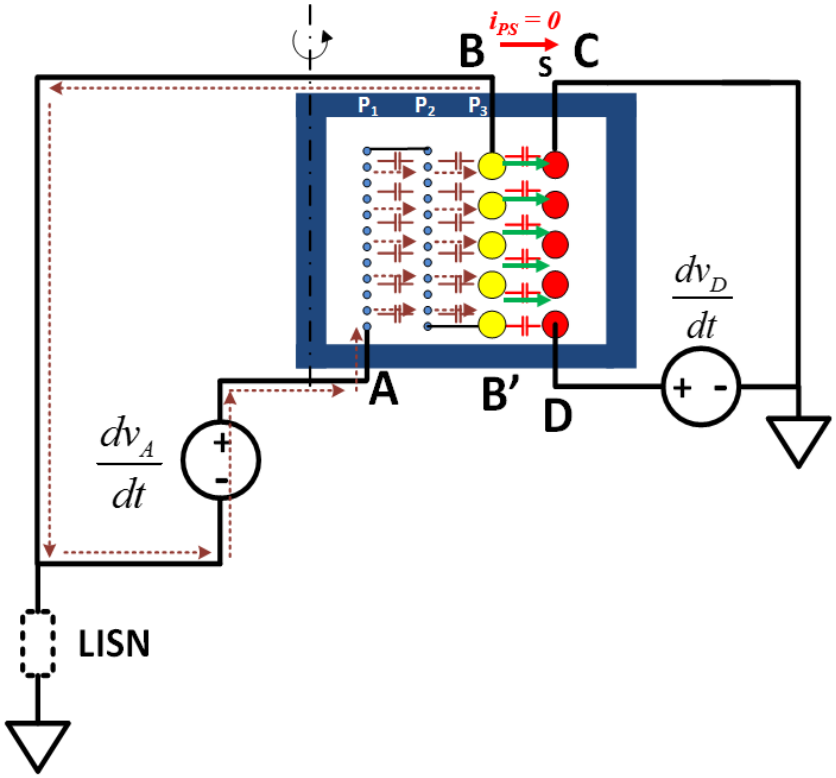


Fig. 1.21 Series Shielding method

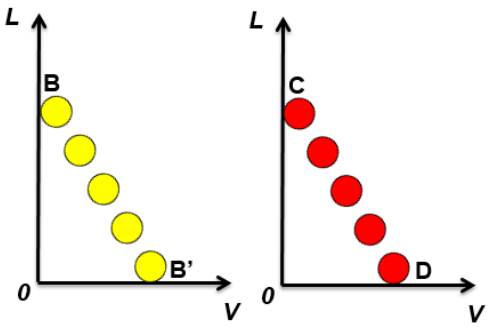
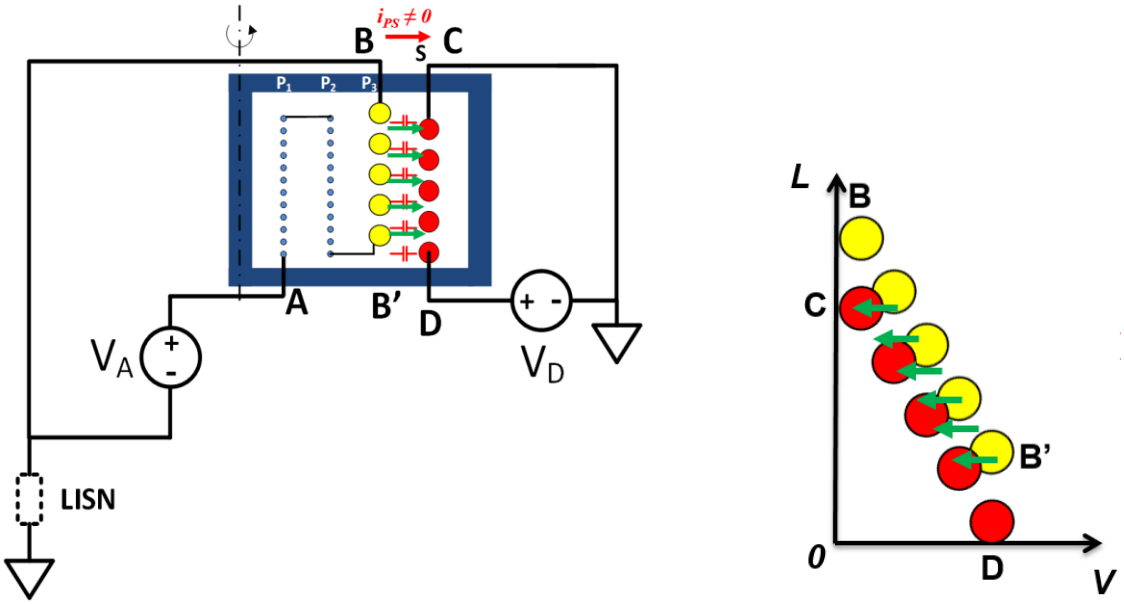


Fig. 1.22 Voltage distribution of P3 and S

However, this method requires that the shielding and secondary winding must be aligned perfectly. Fig. 1.23shows that if there is a misalignment between shielding and secondary winding, the voltage distribution will change. As shown in Fig. 1.23 (b), there will be voltage difference between the shielding and secondary winding and this will lead to CM noise current flow through the transformer. The benefit of this technique will be diminished. Because of this, this method is not effective in mass production.



(a) Winding position when misalignment (b) Voltage distribution of misalignment windings

Fig. 1.23 Misalignment between primary and secondary windings

In [21], a shielding method is provided that can reduce CM noise using cancellation concept. Fig. 1.24 shows its transformer structure. Instead of using a shielding that blocking the whole winding area, it reduces the shielding width and leaves a non-shielded area. In non-shielded area, the voltage of primary winding is higher than secondary winding. Displacement current i_1 flows from primary to secondary. In the shielded area, the voltage of secondary winding is higher than shielding, so the displacement current i_2 flows from secondary to primary. The equivalent CM noise model is shown in Fig. 1.25. The parasitic capacitor between primary winding and secondary winding forms the capacitor C_{AC}. The parasitic capacitor between secondary winding and shielding forms the capacitor C_{BD}. In order to achieve $i_1 = i_2$, (1-7) should be achieved. The value of C_{AC} and C_{BD} can be adjusted by changing the length of shielding.

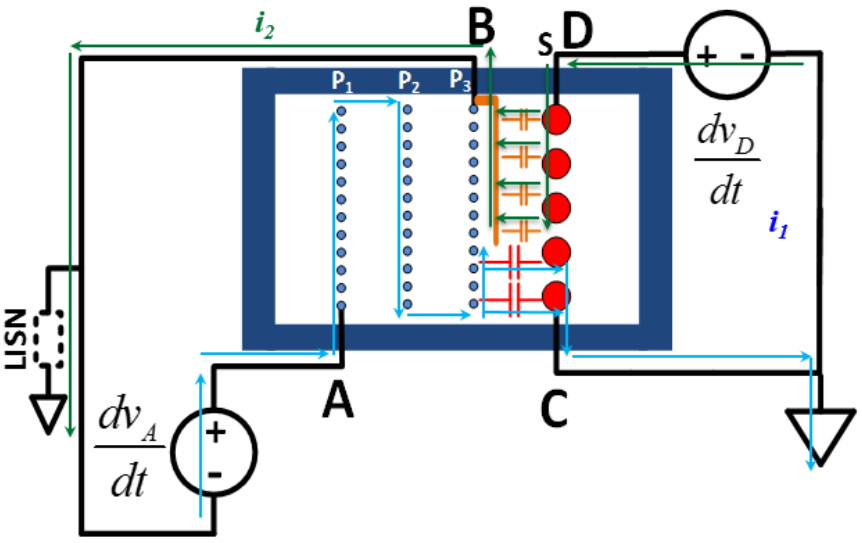


Fig. 1.24 Partial shielding method

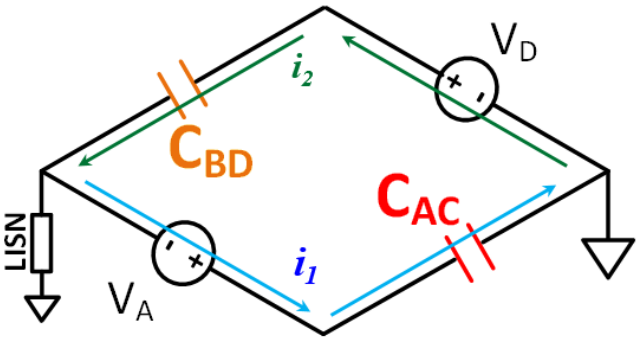


Fig. 1.25 CM noise model of partial shielding

$$C_{AC}\frac{dV_A}{dt} = C_{BD}\frac{dV_D}{dt} \tag{1-7}$$

However, this method has two issues. The first one is that the value of dV_A/dt and dV_D/dt are very different. The two noise sources are from two different devices, as shown in Fig. 1.26. It is very difficult to match dV_A/dt and dV_D/dt with exact ratio. In the real production, the optimal width of shielding is obtained by trial-and-error procedure and requires a lot effort. The second issue is that the value of C_{AC} and C_{BD} is very difficult to calculate and control in mass production. Hence this method requires a precise control on the relative position of windings and shielding. However, it is hard to guarantee this for every transformer in the real production and will diminish the effect on the CM noise reduction.

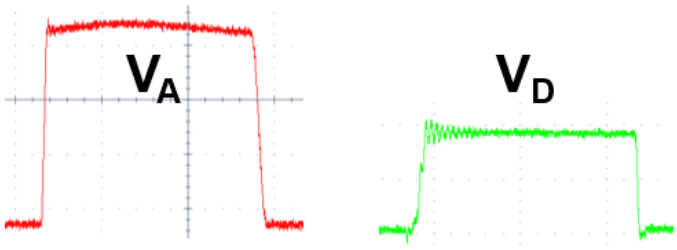


Fig. 1.26 Waveform of V_A and V_D

1.5 Proposed Dissertation Outline

As discussed in this chapter, the EMI is an important issue in switch mode power supply design. With the pursuing of higher efficiency and higher power density, new method to help reduce EMI noise is needed. With the wide-bandgap devices, the switching frequency of power converters has been increased 10 times higher. The design of power converter has been dramatically changed. Therefore, the EMI analysis needs to be viewed in a new angle. High switching frequency provides both challenges and opportunities in EMI research.

Chapter 2 introduces the shielding technique for PCB winding transformer. With wide bandgap (WBG) devices, the switching frequency of converters has been increased 10 times higher than traditional Si MOSFET design. This dramatically changes the magnetic design. With the PCB winding transformer, the converter is smaller and efficient. However, due to large inter-winding capacitance, the CM noise of PCB winding transformer is very large. A novel shielding method for PCB winding transformer is proposed. This shielding method can not only effectively reduce the CM noise, but also improve the converter efficiency. Furthermore, the PCB shielding method can also be implemented into matrix transformer.

Chapter 3 proposes the novel PCB winding inductor for CRM PFC converter. In today's industry practice, litz wire inductor is widely used because of high efficiency. With the increasing demanding of high efficiency and high power density, the litz wire inductor is not suitable. In this chapter, two PCB winding inductor designs are proposed, one for 1 kW server power supply, another for 6.6 kW on-board battery charger of electric vehicle. The challenge of PCB winding inductor design is high AC winding loss. In this chapter, a novel winding structure is proposed to solve this issue. The PCB winding inductor can achieve similar efficiency as litz wire inductor

with smaller volume and reduced labor intensive work. Furthermore, the balance technique is applied to PCB winding inductor to help reduce CM noise. With PCB winding inductor, the balance technique has better high frequency performance.

Chapter 4 investigates the EMI filter design for 1 kW server power supply. Conventionally, people have to use two-stage EMI filter to meet the EMI standard. The two-stage EMI filter are bulky and expensive. With the EMI noise reduction methods proposed in previous chapter, one-stage EMI filter can be applied. This chapter analyzes the self-parasitic and mutual coupling of one-stage EMI filter. The near field measurement method is applied to visualize the flux near filter components. The methods to reduce the self parasitics and mutual coupling of one-stage EMI filter is analyzed and demonstrated in 1 kW server power supply system.

Chapter 5 gives conclusions and discussion about future work.

Chapter 2. Shielding Technique for Isolated DC/DC Converter

2.1 PCB Winding Transformer with Shielding Technique

People always want the power supply to be smaller and more efficient. That makes the power density and efficiency are the two major driving forces for power supply system [22][23]. With traditional Si MOSFETs, the switching frequency of power converter is limited to 100 kHz. With low switching frequency, the magnetic components are usually bulky. In addition, because of the high volt-sec, the magnetic components have to use many turns of litz wire. The relationship between core size and voltage-sec can be expressed as:

$$N \cdot A_e = \frac{V_O(1-D)}{2 \cdot \Delta B \cdot f_s} \tag{2-1}$$

For conventional Si based flyback converter, the turns number of transformer is very high. As shown in Fig. 2.1, the primary winding has 39 turns, and the secondary winding has 7 turns. People use litz wire to build this transformer. It is impossible to build such many turns with PCB winding and maintaining high efficiency.

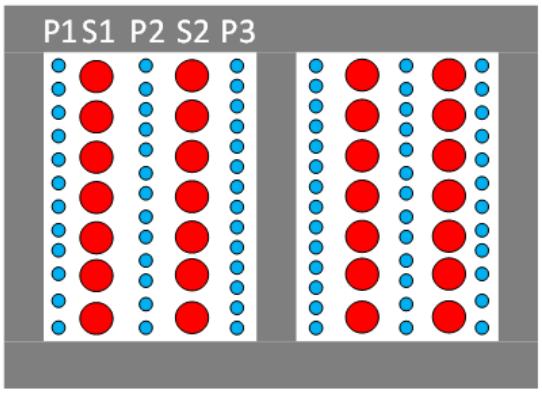


Fig. 2.1 Conventional flyback converter transformer

However, with the development of wide-band-gap power devices, including gallium nitride (GaN) transistors and silicon carbide (SiC) transistors, the switching frequency of power converter can be pushed to hundreds of kHz, even above MHz. At such high switching frequency, the size of magnetic components can be reduced a lot. Furthermore, the turns number can also be greatly reduced. This provides an opportunity for magnetic components to use PCB winding. Comparing with traditional litz wire magnetics, the PCB winding magnetics can achieve small volume, better tolerance control, and automated production without labor intensive work. Therefore, the PCB winding is a promising technique for high frequency converters.

The 65W flyback adapter discussed in previous section can be built with GaN devices switching above 1MHz [24]. In this flyback converter, PCB winding transformer is applied in the 4-layer PCB motherboard. As shown in Fig. 2.2, the 1 MHz PCB winding transformer is 5 times smaller than traditional litz wire transformer.

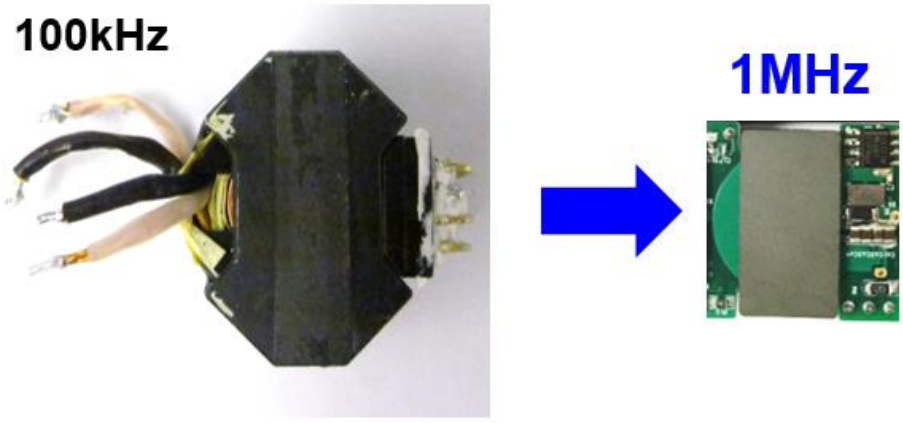


Fig. 2.2 Size comparison between 1 MHz PCB winding transformer and 100 kHz litz wire transformer

Fig. 2.3 shows the cross-section view of PCB winding transformer. The primary winding has 10 turns and secondary winding has 2 turns. It has much less turns than the traditional low frequency litz wire transformer. Thus, the transformer can be built with 4-layer PCB motherboard.

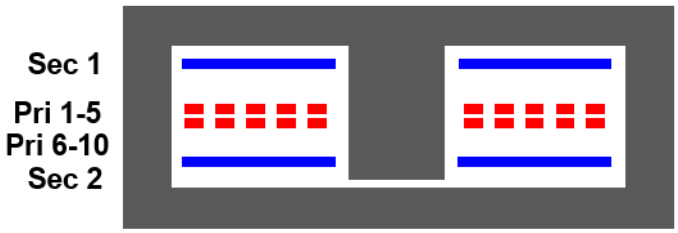


Fig. 2.3 Cross-section view of PCB winding transformer

However, the PCB winding transformer has a significant drawback, which is very large parasitic capacitance between primary winding and secondary winding. Large capacitance will lead to large CM noise current. Fig. 2.4 shows the CM noise measurement result for the PCB winding flyback converter. The noise amplitude is much higher than low frequency flyback converter with litz wire transformer. Furthermore, the CM noise remains very large on high frequency range. This brings a great challenge to EMI filter design.

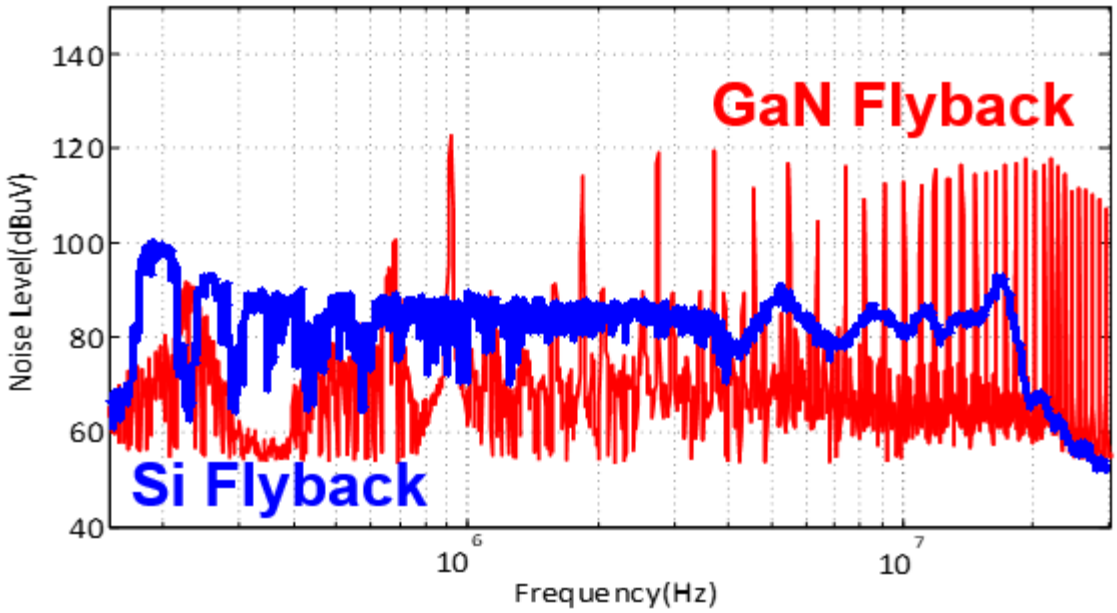
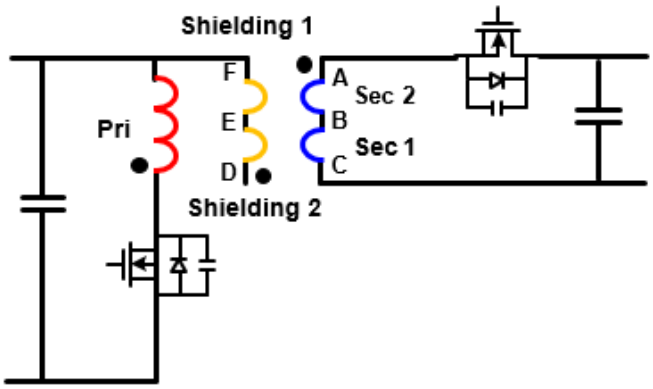
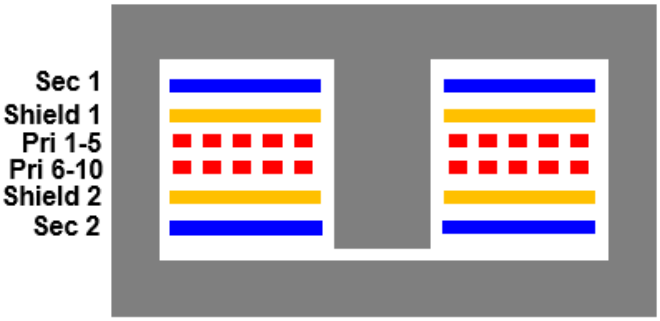


Fig. 2.4 CM noise measurement for PCB winding flyback converter

In order to solve this issue, a novel shielding technique is applied to PCB winding transformer [25]. Fig. 2.5 shows the circuit topology and transformer cross-section view of flyback converter with shielding layer. The shielding is connected to primary side. Therefore the CM noise current generated by primary side will circulate within primary side. If the shielding is made exactly same and align with secondary winding, as shown in Fig. 2.6, there will be no CM noise current between shielding and secondary winding. Thus, the CM noise is blocked from primary winding to secondary winding. However, in the real implementation, there must be a jumper wire to connect the shielding to primary winding. In a high frequency transformer design, the jumper wire is not acceptable. Therefore the shielding layer must have a different layout design.



(a) Flyback converter with shielding



(b) Transformer cross-section view

Fig. 2.5 Flyback converter with shielding layer

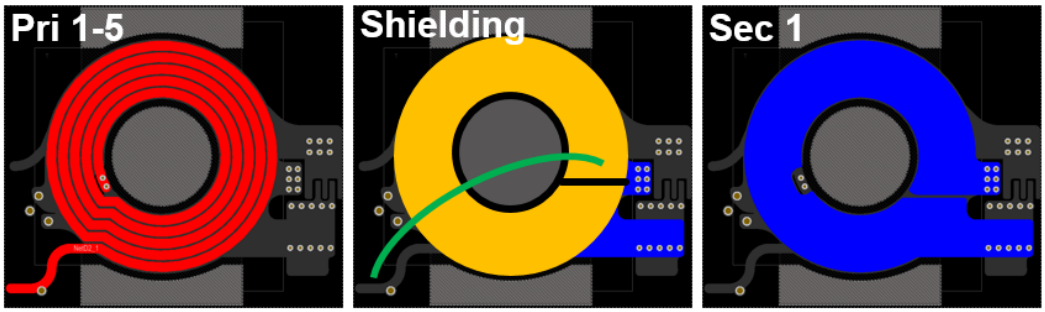


Fig. 2.6 Detailed PCB layout with jumper connection

Fig. 2.7 shows that shielding has 180 °rotation with secondary winding. Thus, it is easy to connect the shielding with primary ground. However, after rotation, there will be voltage potential

difference between shielding and secondary winding. Fig. 2.8 shows 3D structure of shielding and secondary winding. Point B, C, E and F are marked in Fig. 2.5(a), and point F on shielding layer is connected to primary ground. In order to analyze the displacement current flowing between shielding layer and secondary winding, the voltage distribution needs to be described. Shielding layer can be treated as a one-turn winding. There will be voltage induced on the shielding layer according to Faraday's Law. An X-Y coordinate system is built to analyze the voltage distribution of shielding layer and secondary winding. Zero point is set between point F and point E on shielding. The X axis is built along the winding and representing the position of certain point on the winding. The Y axis indicates the voltage potential of certain point. Fig. 2.9 shows the voltage distribution of shielding layer and secondary winding. One assumption is made that the voltage is linearly distributed along the winding. For shielding, from point E to point F the voltage decreases from V to 0. For secondary winding, because the zero point is set in the middle of secondary winding, at zero point, the voltage on shielding is V/2. First, the voltage on shielding decreases linearly from V/2 to 0. Then, at point B, the voltage is V and decreases to V/2. It can be seen that on one half, the voltage of secondary winding is higher than shielding. The displacement current flows from secondary winding to shielding. On the other half, the voltage of shielding is higher than secondary winding. The displacement current flows from shielding to secondary winding. Those two currents have same amplitude and opposite direction. Thus, there is no net CM noise current flowing out of the transformer. In summary, the function of shielding is: (1) it blocks the displacement current from primary side; (2) the displacement current between shielding and secondary winding will not generate CM noise current.

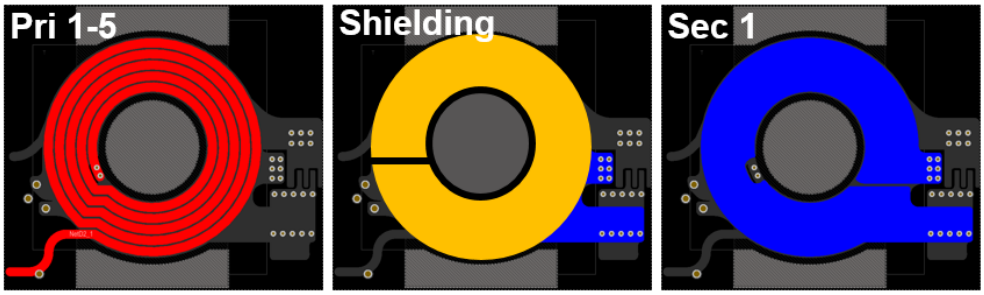


Fig. 2.7 Shielding has a 180 ºrotation with secondary winding

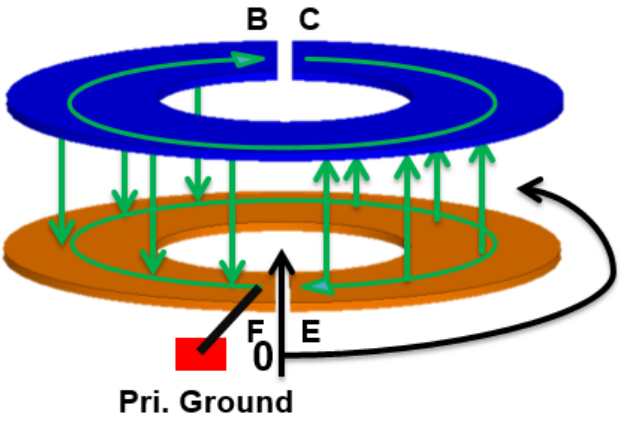


Fig. 2.8 3-D structure of shielding and secondary winding

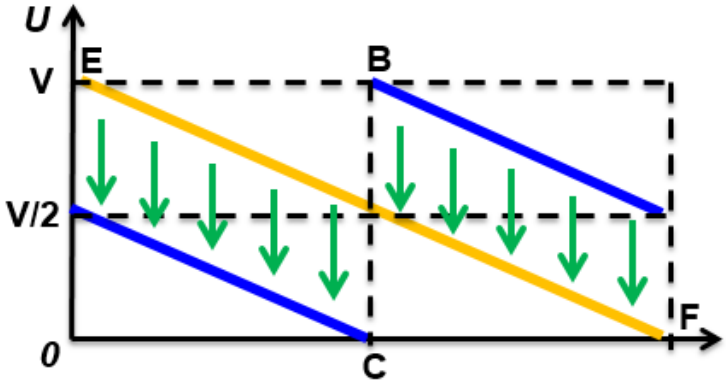


Fig. 2.9 Voltage distribution of shielding and secondary winding

Furthermore, the shielding can be integrated into primary winding, so that the shielding serves as the first two turns of primary winding, as shown in Fig. 2.10. The transformer cross-section

view is shown in Fig. 2.11. With the integration, the transformer can achieve 13% winding loss reduction as well as shielding effect.

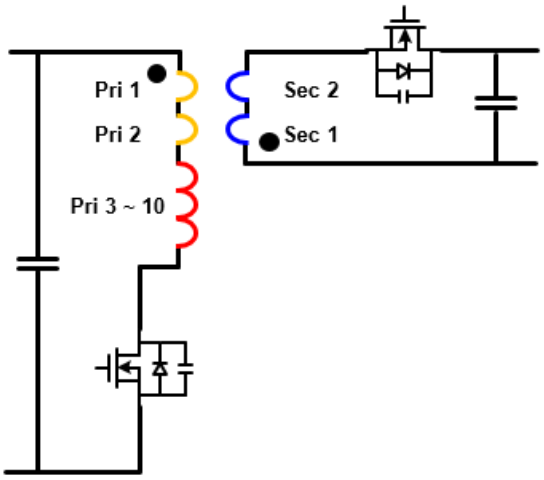


Fig. 2.10 Shielding serving as part of primary winding

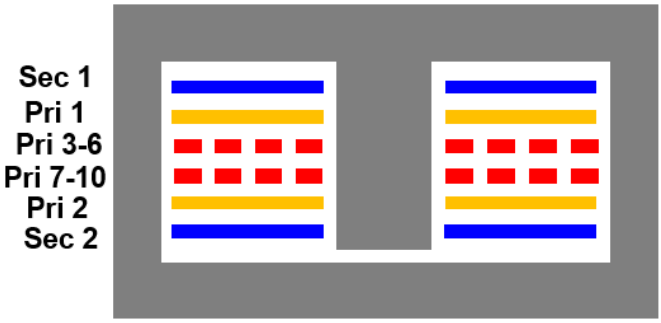


Fig. 2.11 Transformer cross-section view with shielding

Fig. 2.12 shows the CM noise measurement result for the PCB winding flyback converter with shielding. It can be seen that shielding can achieve 27dB noise reduction. Furthermore, shielding remains very effective on high frequency up to 30 MHz. Since high frequency noise attenuation is the most difficult part on designing EMI filter. This shielding method can greatly benefit EMI filter design.

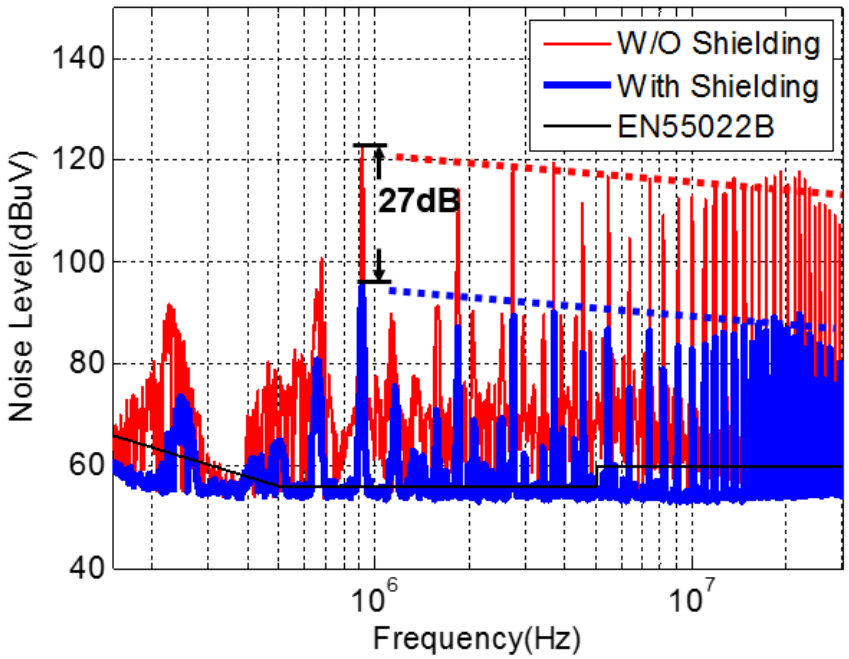


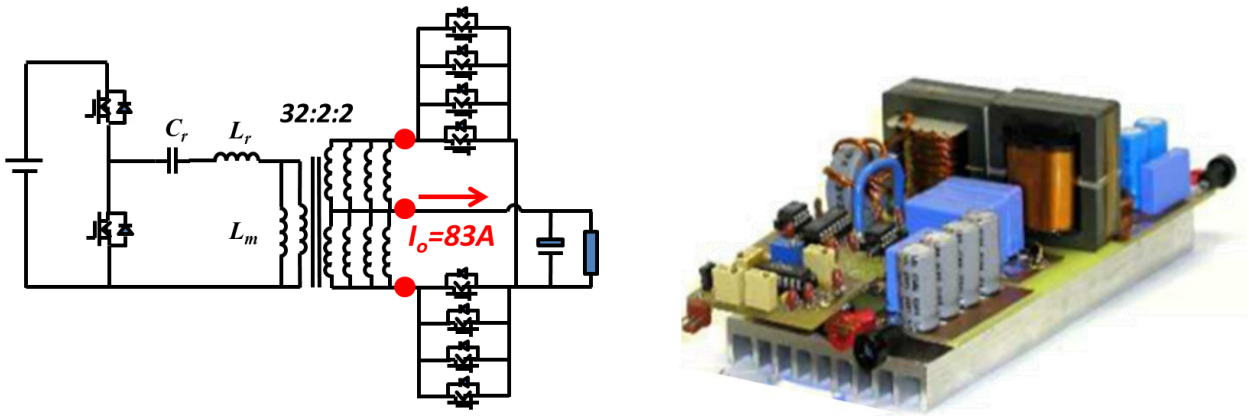
Fig. 2.12 CM noise reduction for flyback converter with shielding

2.2 Matrix Transformer with Shielding Technique

Pulse-width modulation (PWM) converters is widely used in front-end DC/DC converters. However, because of the hard switching performance, the switching loss is large in PWM converters. This limits the efficiency of PWM converters and impedes the converter going to high switching frequency. Hence, it is hard for PWM converter to achieve high power density and high efficiency. Soft switching technique can make PWM converter achieve zero voltage switching (ZVS). So the switching loss of PWM converter can be reduced and it has the ability to go to high switching frequency to improve power density. However, another disadvantage of PWM converter still limits its performance. For the computing electronic systems, such as desktop, laptop, server and telecom applications, certain hold-up time is required to assure data security. Normal PWM converters require bulky hold up capacitors to guarantee the hold-up time. Thus the power density of PWM converters are still limited.

LLC resonant converter, is becoming more and more popular because of the high efficiency and high power density [24]-[32]. LLC resonant converter can achieve ZVS for primary side switches from zero to full load range. Meanwhile, the secondary side synchronous rectifier (SR) can achieve zero current switching (ZCS). Because of this, the switching loss of LLC resonant converter can be minimized and high efficiency can be achieved. In addition, low switching loss provides the LLC resonant converter the ability to achieve high switching frequency. This can continue reduce the size of passive components and improve power density. Furthermore, it is easy to integrate magnetic components into the transformer to further reduce size and cost of LLC resonant converter. In addition, the voltage gain characteristic of LLC resonant converter makes it have good hold-up capability to reduce the volume of hold-up capacitor. In summary, LLC resonant converter is becoming dominant in off line power supply systems.

The server applications require low output voltage and high output current. For example, a 1 kW, 12V output server power supply will have more than 80 A output current. 4-8 SRs should be paralleled to reduce the secondary conduction loss. The circuit is shown in Fig. 2.13 (a). This design will have several issues. First, it is difficult to achieve both static and transient current sharing between the paralleled SRs. Second, there will be large AC current flow through the terminations of transformer and SRs (red dots in Fig. 2.13(a)), which will generate large termination loss. Third, because of the low switching frequency, the transformer has to use litz wires and copper foil to build primary and secondary winding. In this way, the transformer is bulky and expensive. The manufacture procedure is labor intensive and the quality control is poor. Fig. 2.13 (b) shows the prototype of the conventional LLC converter.



(a) Circuit schematic (b) Hardware prototype

Fig. 2.13 Conventional LLC converter

The matrix transformer is defined as an array of elements intertwined so that the whole functions as a single transformer [33][34]. Each element being a single transformer that contains a set turns ratio, i.e. 1:1, 2:1 ....n:1. The desired turns ratio is obtained by connecting the primary windings of the elements in series and the secondary's in parallel. For the high current design cases only a single turn secondary will be considered. The benefits of the matrix transformer are that it can split current between secondary windings connected in parallel, reduce leakage inductance by lowering the N^2 value of the secondary loop inductance, and improve thermal performance by distributing the power loss throughout the elements [35]. In addition, the matrix transformer structure also can effectively reduce the magnetomotive force (MMF) of the windings, especially for the PCB winding. That also means a reduction in leakage inductance and winding AC resistance [36]. This makes the matrix transformer a very attractive structure for high current, high switching frequency applications.

Fig. 2.14 shows a design of 400V/12V, 1kW LLC resonant converter with matrix transformer [36]. The switching frequency of this converter is 1MHz. It uses GaN devices as primary switches to reduce switching related loss [37][38]. By utilizing flux cancellation method [39], this converter

uses two U-I cores for four sets of transformers. Comparing with normal design, this can reduce the core loss and core size by more than 30% [36]. For each small cell of transformer, the primary winding has four turns and secondary winding has two one-turn center-tap structure. The primary windings are in series and secondary windings are in parallel. Hence, the total turns ratio is 16:1. As shown in Fig. 2.15, by using matrix transformer structure, four-layer PCB can achieve 16:1 turns ratio. Primary windings are at the two middle layers and secondary windings are at top and bottom layers. Thus, secondary SR devices and output capacitors can be directed mounted on top of the secondary winding, as shown in Fig. 2.16. By doing this, there is no extra termination loss. The primary and secondary windings are exactly overlapped.

This LLC resonant converter can achieve more than 95% efficiency and 710W/in^3 power density, which is comparable with the state-of-the-art industry product.

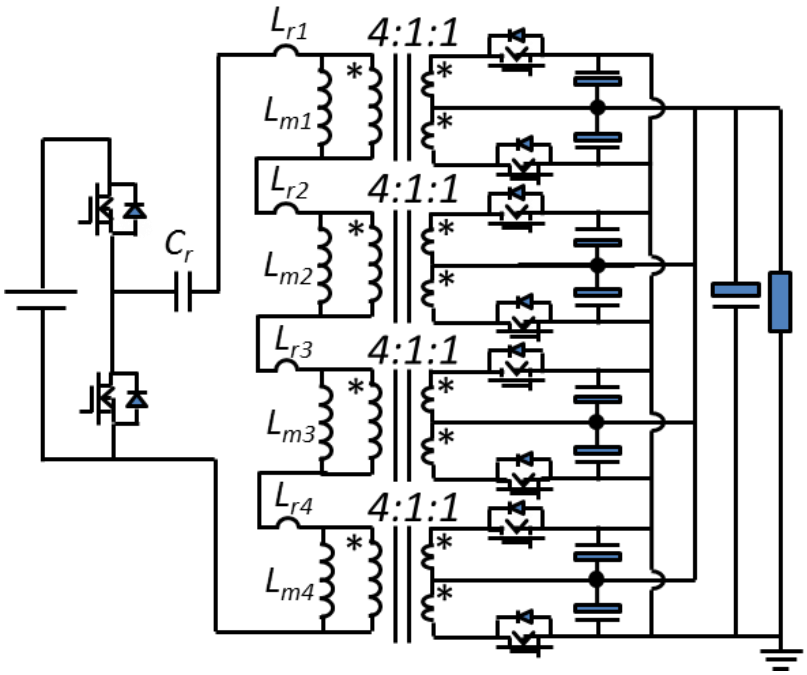


Fig. 2.14 LLC resonant with matrix transformer

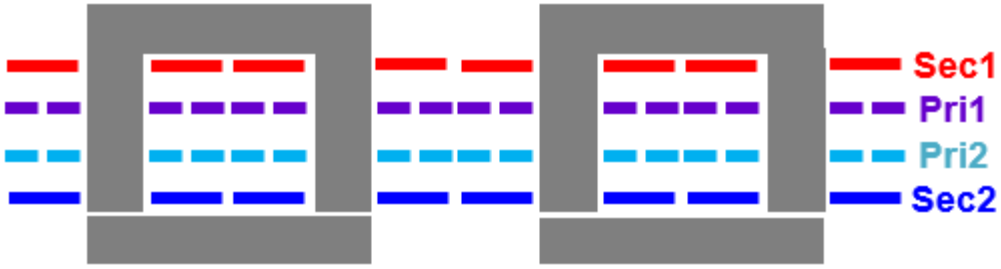


Fig. 2.15 Matrix transformer structure

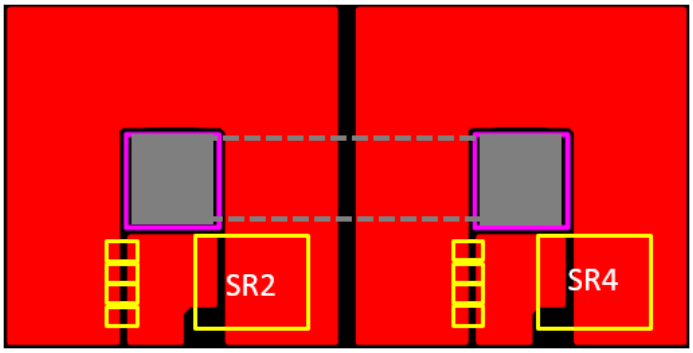


Fig. 2.16 Mount secondary devices and output capacitors on top of secondary winding

Matrix transformer brings a lot of benefits. However, there is always a price to pay. In the matrix transformer, the winding area is large, which can introduce large inter-winding capacitance. Furthermore, because of the interleaving structure, the inter-winding capacitance is further increased. This large inter-winding capacitance between primary and secondary windings will bring large CM noise current. As shown in Fig. 2.17, the measured CM noise of LLC converter is way above the EMI standard. Large CM noise filter is needed to achieve the required EMI noise level. The high power density may be diminished by huge CM noise filter.

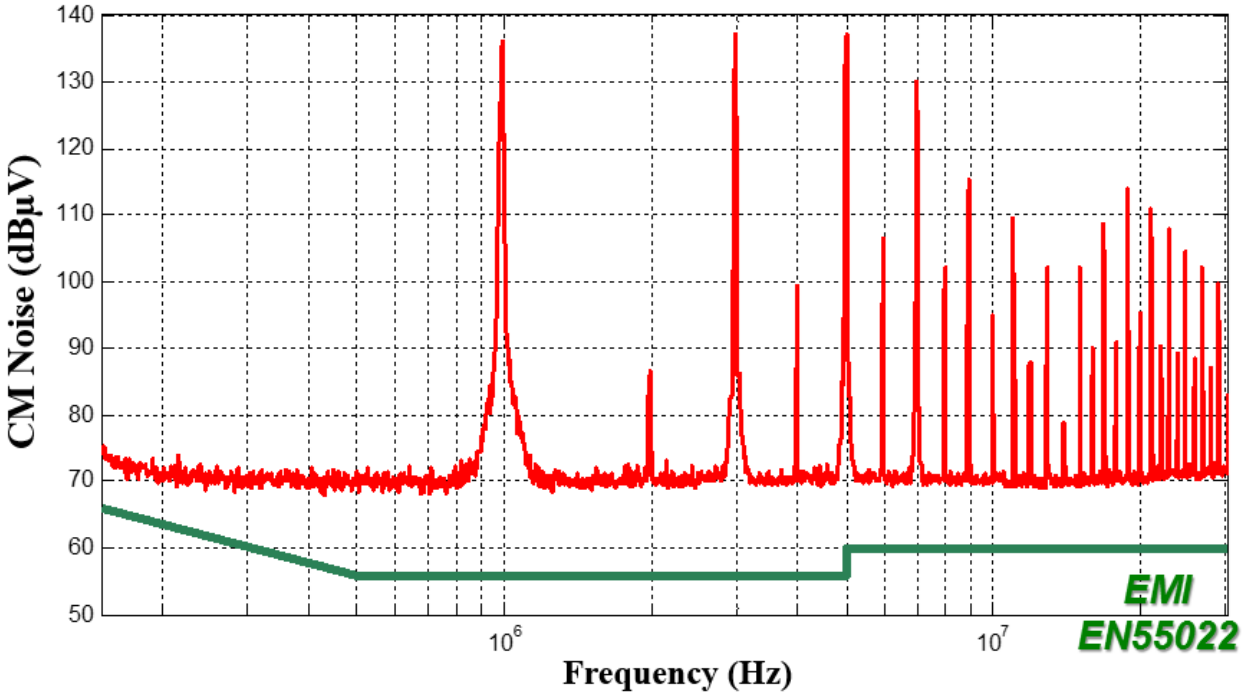


Fig. 2.17 CM noise measurement result for LLC resonant converter with matrix transformer

The shielding method is provided for matrix transformer to reduce CM noise [40]. Fig. 2.18 shows the circuit structure after adding shielding layers between primary and secondary windings. Fig. 2.19 shows the cross section view of transformer with shielding layers. Shielding layer is added between each primary-secondary cell. Thus, the transformer need six layers of PCB after adding shielding. It can be seen from Fig. 2.18 that all shieldings are connected to the primary ground. Thus, the noise current coming from primary side will be blocked by shielding and confined in the primary side. This noise current will not cause CM noise.

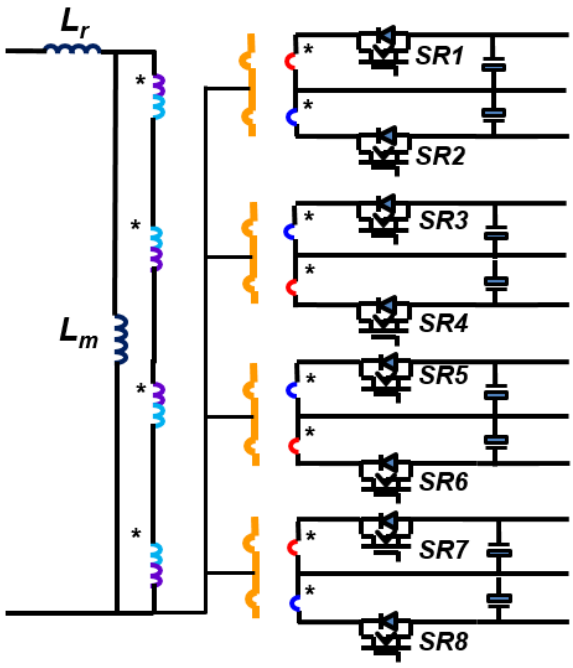


Fig. 2.18 Adding shielding into matrix transformer

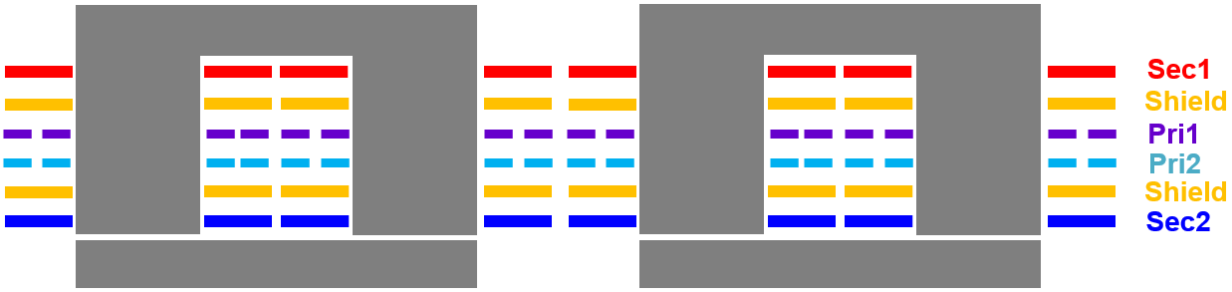


Fig. 2.19 Transformer structure with shielding

However shielding, treated as a one-turn winding, becomes another voltage pulse source. Therefore the shielding need to be carefully designed otherwise there will be CM noise current between shielding and secondary winding. One shielding-Sec. winding is used as an example to illustrate the shielding design. As shown in Fig. 2.20, Secondary winding is on top of the shielding, and node A, B, A', B' is noted in Fig. 2.18. Shielding is rotated 180 degree with secondary winding to have an easy connection to primary ground. Assuming voltage is distributed linearly along the winding, Fig. 2.21 Voltage distribution of shielding and secondary winding shows the voltage

distribution of shielding and sec. winding. The coordinate is build: set zero on point A and the x-axis is along the winding; y-axis is the voltage of each point on the winding. For secondary winding, node A is the *dv/dt* point and node B is connected to the ground. Hence from A to B, the voltage distributes from V to 0. For shielding, node B' is connected to ground, and the zero point of the axis is at the middle point of shielding. Hence the voltage of shielding first distributes from V/2 to 0, then jump to V (node A') and decrease to V/2. It can be seen that on one half, the voltage of secondary winding is higher than shielding. There is displacement current go from secondary winding to shielding. On the other half, the voltage of shielding is higher than secondary winding. There is displacement current go from shielding to secondary winding. These two current are at the same magnitude but has opposite direction. Therefore, displacement current is circulating within shielding and secondary winding. Therefore, the shielding is designed to not only block the primary noise source, but also block the noise from secondary side.

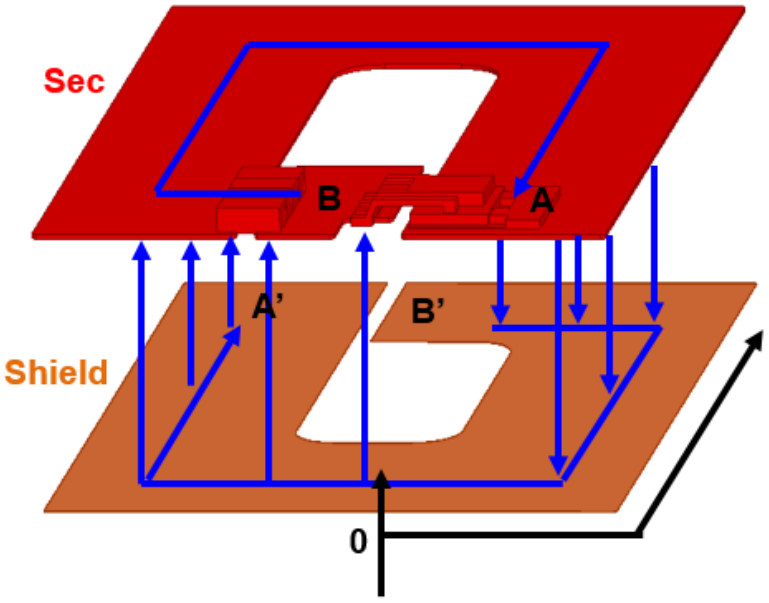


Fig. 2.20 3D structure of secondary winding and shielding

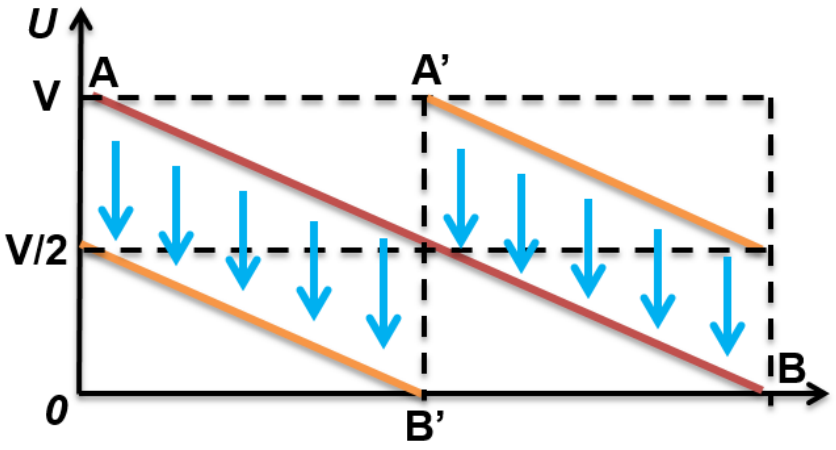


Fig. 2.21 Voltage distribution of shielding and secondary winding

The experiment result is shown in Fig. 2.22. For an easy observation, the peak points are connected as the envelope. It can be seen that the proposed shielding technique can have a 23dB reduction at 1MHz. Further, the shielding is still effective at very high frequency range.

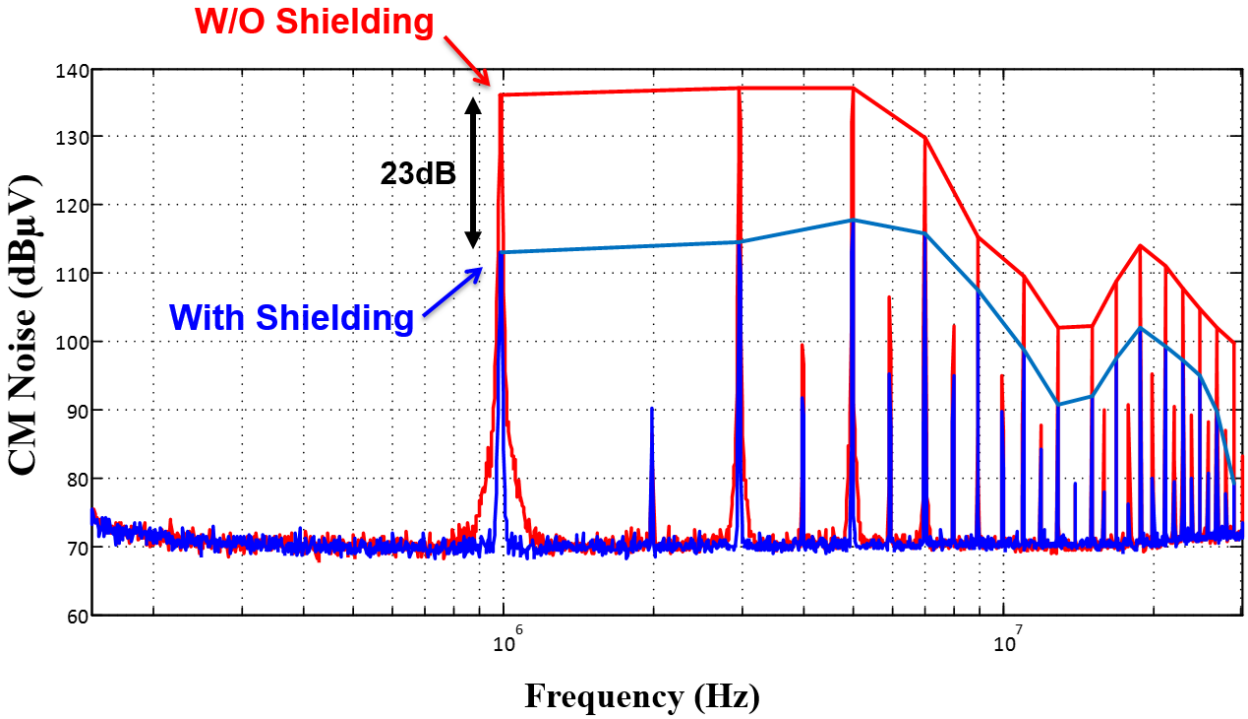


Fig. 2.22 CM noise measurement result for matrix transformer with shielding

The efficiency comparison is shown in Fig. 2.23. It can be seen that less than 0.5% efficiency difference between shielding version and original design. In summary, the shielding technique has good CM noise reduction result while little sacrifice of efficiency.

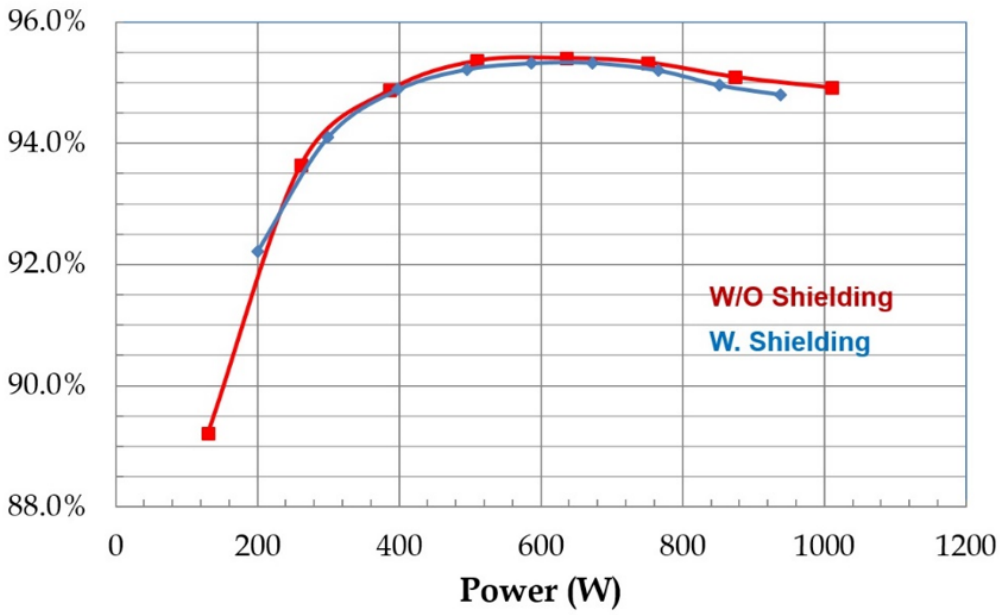


Fig. 2.23 Efficiency comparison between shielding version and original version

2.3 Conclusions

In this chapter, the shielding method is proposed to reduce CM noise for isolated converters. With GaN and SiC devices, the switching frequency of power converters has been increased 10 times higher. This provides the opportunity to use the PCB winding transformer. The PCB winding transformer is high efficient, high power density and good manufacturability. However, the CM noise of PCB winding transformer is very high due to large inter-winding capacitance. In this chapter, a novel shielding method is proposed to reduce the CM noise of PCB winding transformers. The implementation of this shielding method is simple. The shielding method can effectively reduce the CM noise of a 65 W flyback converter by 27 dB. Furthermore, the shielding

remains effective up to 30 MHz. In addition, the shielding can be integrated with primary winding to further reduce the winding loss of the transformer.

The PCB shielding method can also be applied to matrix transformer structure. A 1 kW LLC converter with matrix transformer is set as an example. With this shielding method, the CM noise can be reduced by 23 dB. The shielding has 10 dB to 20 dB attenuation at very high frequency. This can greatly help the EMI filter design since the high frequency noise is the most difficult to attenuated by EMI filter.

Chapter 3. Balance Technique for Coupled Inductors Integrated into PCB

In previous chapter, the magnetic integration and EMI noise attenuation for DC/DC converter is discussed. For the power over 75W, the PFC converter is required in the power supply to ensure good power factor. In commercial products, the switching frequency of the PFC converter is usually lower than 100 kHz. Fig. 3.1 shows a typical 1 kW AC-DC converter. With low switching frequency, the converter is very bulky. Over 40% of the components are manually assembled, especially the inductors and transformers. Manufacturing this converter is labor intensive. Furthermore, the tolerance control of these components is poor. The PFC converter consumes approximately one third of the power supply. Increasing the switching frequency can reduce the volume of the PFC converter. Furthermore, increasing the switching frequency can greatly raise the corner frequency of the EMI filter and reduce the filter size. Thus, the power density of power supply can be increased significantly.

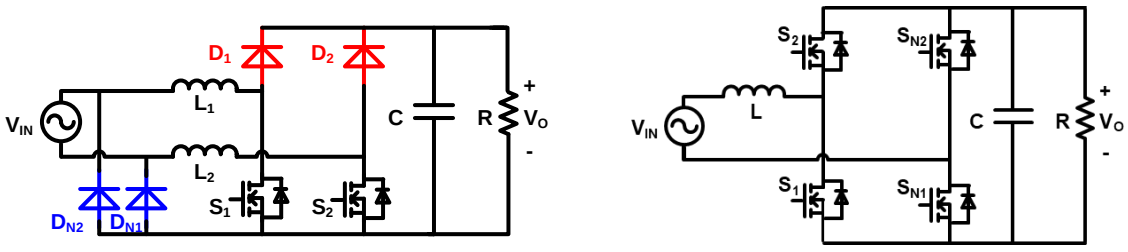
Fig. 3.1 A typical AC-DC converter

With wide-band-gap devices, the switching frequency can be pushed to hundreds of kHz, even above MHz. Furthermore, with higher switching frequency, the turns number of inductor can be reduced. This provides an opportunity to use PCB winding to build the inductors for high frequency PFC converter. This chapter focuses on PCB winding inductor integration and EMI noise attenuation for PFC converters. Two applications of PFC converter will be discussed. The first one is 1kW PFC converter for server power supply, the second one is 6.6kW PFC converter for on-board battery charger.

3.1 PCB Winding Negative Coupled Inductor with Balance Technique [41]

3.1.1 1.2kW GaN Based Totem-pole Bridgeless PFC above MHz

Comparing with the boost PFC converter, the bridgeless PFC converter has clear advantages. It eliminates the diode rectifier bridge and reduces the conduction loss of the semiconductors. Among the topologies of bridgeless PFC converter, the dual-boost bridgeless PFC converter (Fig. 3.2(a)) is the most popular topology in industry products. However, the totem-pole PFC converter (Fig. 3.2(b)) is simpler and requires less semiconductor devices than dual-boost PFC converter. With the limitation of Si MOSFET, the totem-pole PFC converter is only used in low frequency, low power applications. When operating in continues-current mode (CCM), the turn-on loss is very large due to the reverse recovery of the antiparallel body diode of Si MOSFET. The critical-mode (CRM) operation can eliminate the turn-on loss but the turn-off loss of Si MOSFET is very large. For many years, the Si MOSFET limits the use of totem-pole PFC converter [42].



(a) Dual-boost bridgeless PFC rectifier (b) Totem-pole bridgeless PFC rectifier

Fig. 3.2 Bridgeless PFC converter topologies

With the recent development of wide-band-gap (WBG) power devices, the design of power converters can be dramatically changed. The reverse-recovery charge of gallium-nitride (GaN) devices is greatly reduced. Thus, the totem-pole PFC converter can operate at CCM with high efficiency. It is demonstrated in [43], the CCM totem-pole PFC can achieve 99% efficiency. However, in order to achieve such high efficiency, the switching frequency is limited at 50 to 100 kHz. The power density of GaN based PFC converter is similar as Si based design.

In order to get more system level benefits, the switching frequency needs to push higher. One characteristic of GaN devices is that the turn-off loss is extremely small. As shown in Fig. 3.3, the E_{off} of GaN devices is significantly smaller than E_{on}. This makes the CRM a suitable operation for high switching frequency. Fig. 3.4 shows the waveform of CRM operation. During the off-time, after the inductor current touches zero, the inductor is resonating with device junction capacitor. Therefore, the voltage of device V_{DS} will resonate to zero. The device turns on after V_{DS} reaches zero and zero-voltage switching (ZVS) is achieved. In the CRM operation, the turn-on loss is eliminated [44]-[47]. Although the turn-off current is very high, the small E_{off} will guarantee small switching loss.

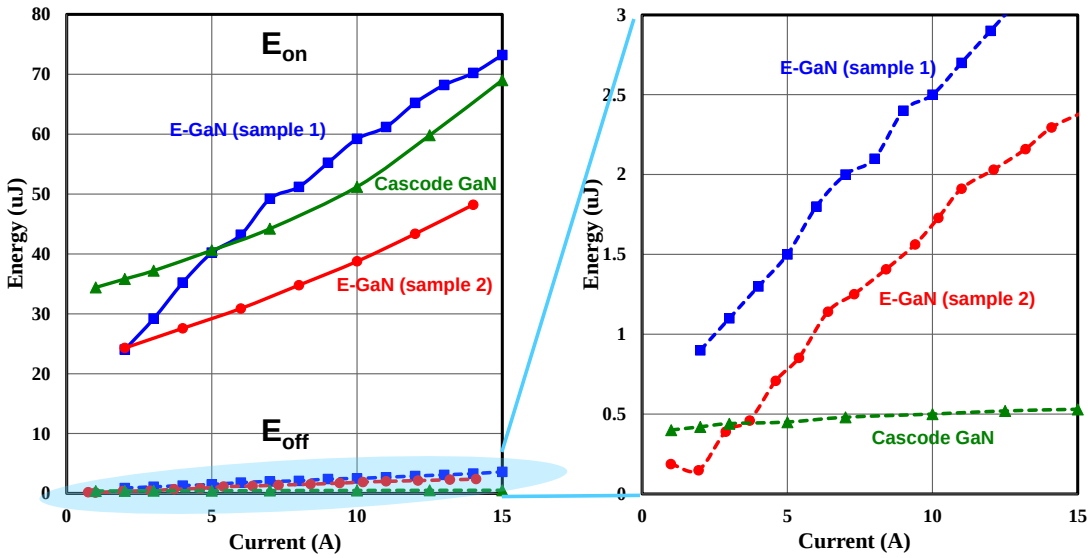


Fig. 3.3 Measured switching loss distribution of different GaN device samples

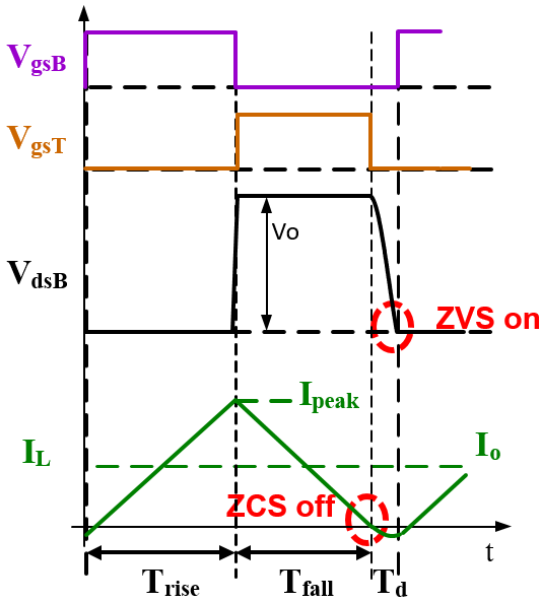


Fig. 3.4 Critical mode operation

However, the CRM totem-pole PFC converter has its own limitations. The first one is large current ripple. In CRM PFC converter, the current ripple is two times of the average current. Such high current ripple will lead to high DM noise and require very large DM filter. The method to solve this issue is to use two-phase interleaved structure, as shown in Fig. 3.5. The waveforms are

shown in Fig. 3.6. It can be seen that the phase current i_{L1} and i_{L2} have very large ripple. But the ripple of input current i_{in} is much smaller.

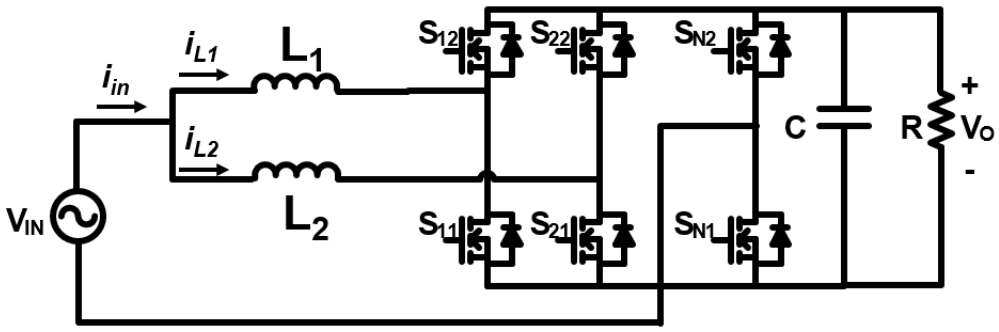


Fig. 3.5 Two-phase interleaved totem-pole PFC converter

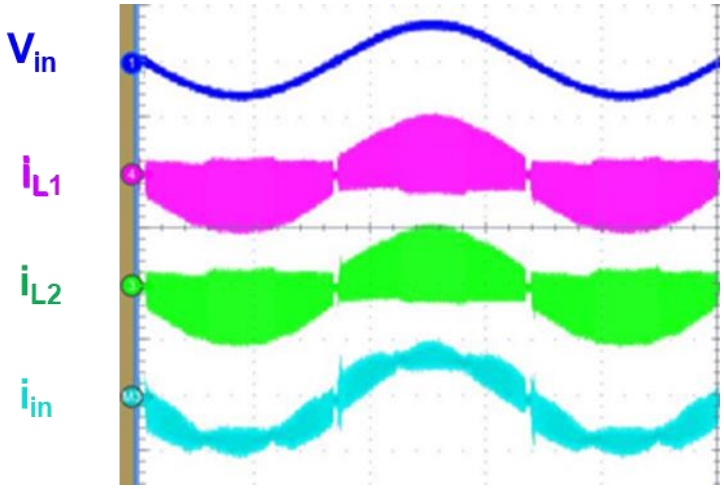


Fig. 3.6 Waveforms of two-phase interleaved totem-pole PFC converter

Fig. 3.7 shows the DM noise measurement result. The blue curve is the DM noise of CRM PFC without interleaving. The green curve is the DM noise of CRM PFC with two-phase interleaving. It can be seen that the DM noise can be greatly reduced with two-phase interleaving. For the one-stage DM filter with 40db/dec attenuation ability, the filter corner frequency can be increased from 80 kHz to 600 kHz. This can greatly reduce the DM filter size.

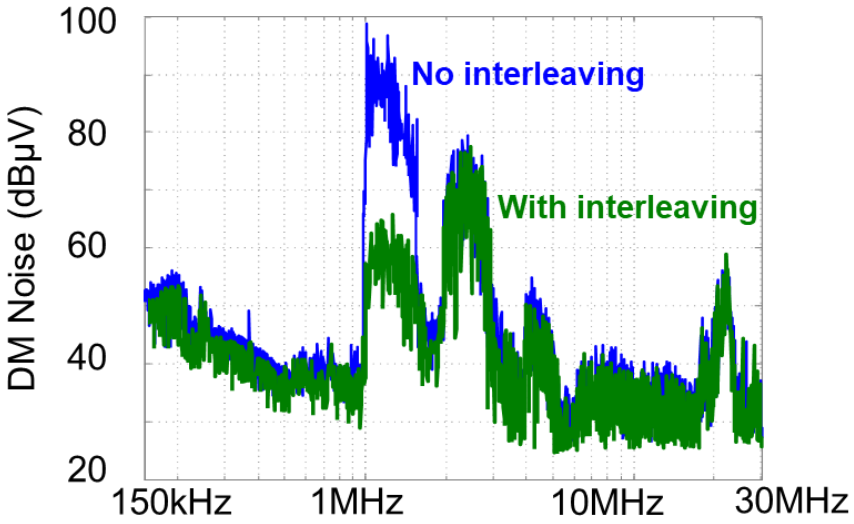


Fig. 3.7 DM noise measurement result

In [48], a 230 Vac to 400 Vdc two-phase interleaved 1.2 kW totem-pole PFC converter with 1 MHz switching frequency is demonstrated, as shown in Fig. 3.8. The power density is around 220W/in^3. The DC-link capacitors are not included here because the DC-link capacitors design is determined by the hold-up time requirements. The value of DC-link capacitors are related with the design of DC-DC converters.

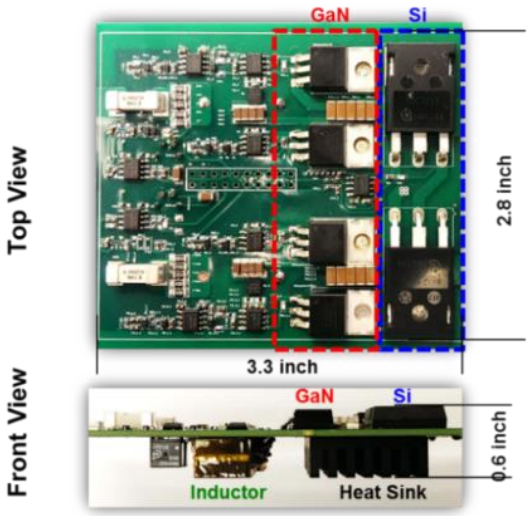


Fig. 3.8 Prototype of two-phase interleaved 1.2 kW totem-pole PFC converter

Comparing with the Si MOSFET based PFC converter, the power density of GaN based totem-pole PFC converter is 5 times higher. However, the MHz CRM PFC converter still has several issues. One is large variation in switching frequency. The operation principle of the CRM PFC converter is that when the inductor current touches zero, the switch turns on. And the inductor current begin to rise. After a fixed on-time, the switch turns off, the inductor current begins to fall. Hence, the peak current of the inductor follows the equation below.

$$i_{pk} = \frac{V_{in}}{L} T_{on} \tag{3-1}$$

As long as T_{on} is fixed, the peak current of the inductor follows V_{in}. Theoretically, the waveform of the inductor current is a series of triangle waveforms with the maximum value described in (3-1) and minimum value as zero. Because the input voltage is AC, with fixed on-time, the switching frequency will change with different input voltage value.

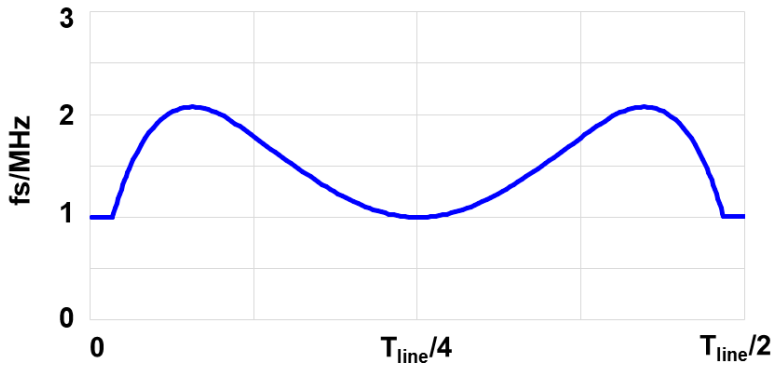
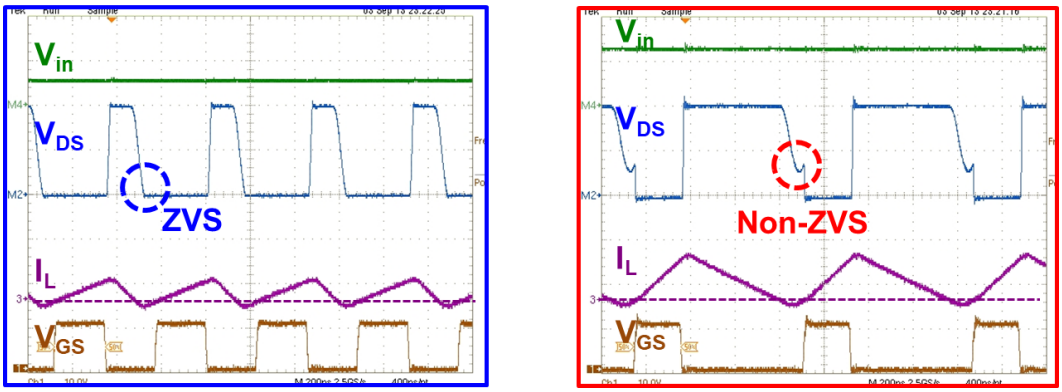


Fig. 3.9 Switching frequency variation of CRM PFC converter

Fig. 3.9 shows the switching frequency variation during a half-line cycle. It can be seen that with a minimum switching frequency of 1 MHz, the converter can have a switching frequency above 2MHz. This high switching frequency will cause greater loss.

Another issue is that the CRM PFC converter cannot achieve zero voltage switching (ZVS) all the time. When the inductor current drops to zero, the inductor will oscillate with the junction capacitors. The peak-to-peak oscillation amplitude of the device voltage is $2(V_o-V_{in})$. Hence, when the input voltage is larger than $0.5V_o$, the switch can only achieve valley switching instead of ZVS, as shown in Fig. 3.10. This will bring a great deal of extra switching loss for converters with a high switching frequency.



(a) $V_{in} < 0.5V_o$ (b) $V_{in} > 0.5V_o$

Fig. 3.10 Non-ZVS at high input voltage

3.1.2 Negative Coupled Inductor in MHz CRM PFC Converter

The concept of the coupled inductor has been widely applied in multi-phase VRMs to reduce loss and improve transient performance [49]. In [50], a coupled inductor is evaluated in an interleaved CRM boost PFC converter. In [51], the impact of using a coupled inductor during the resonant period is analyzed. These analyses shows that the coupled inductor is a promising technique for high-frequency CRM PFC converters.

Fig. 3.11 shows the interleaved totem-pole PFC converter with a coupled inductor. Inductors L_1 and L_2 are inversely coupled. Fig. 3.12 shows the inductor structure demonstration. The two

inductors L_1 and L_2 are winded on an EI shaped magnetic core. L_1 is on the left leg and L_2 is on the right leg. The red arrows indicate that the terminals of input current. The blue arrows indicate the terminals of output current. The black dash lines are the direction of mutual flux of L_1 and L_2. The green dash lines are the direction of leakage flux of L_1 and L_2. It can be seen that the flux generated by L_1 and L_2 are on opposite direction. Hence, L_1 and L_2 are negatively coupled. Fig. 3.13 shows the typical waveforms for different duty cycles. In [49], the derivations of equivalent inductances L_{eq1}, L_{eq2} and L_{eq3} are provided. The expressions of L_{eq1}, L_{eq2} and L_{eq3} are listed below.

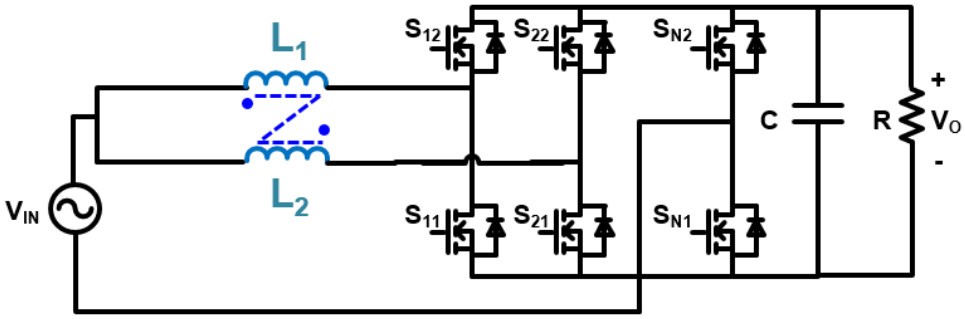


Fig. 3.11 Interleaved totem-pole PFC converter with coupled inductor

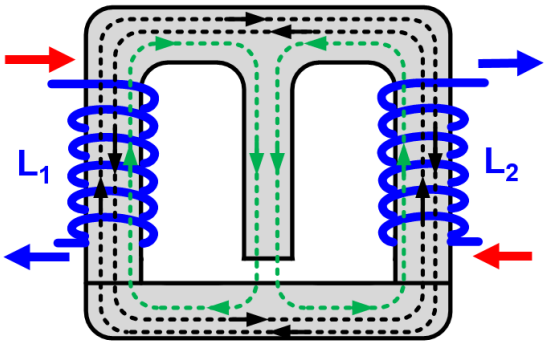
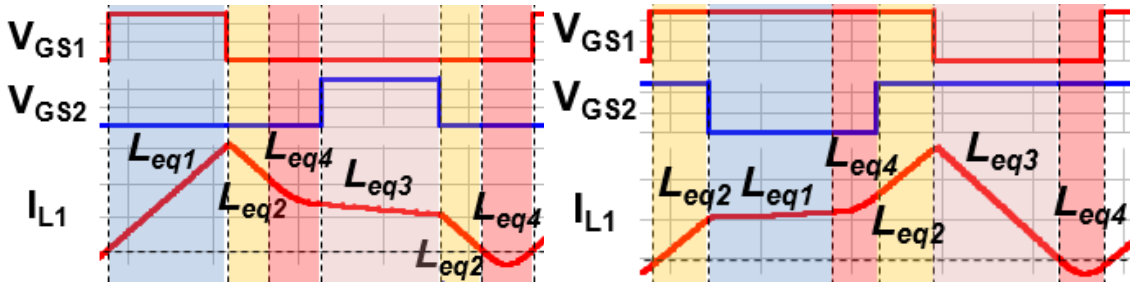


Fig. 3.12 Negative coupled inductor structure demonstration



(a) D < 0.5 (b) D > 0.5

Fig. 3.13 Inductor current waveforms of coupled inductor

$$L_{eq1} = \frac{L^2 - M^2}{L + \frac{D}{D'}M},\ L_{eq2} = L + M,\ L_{eq3} = \frac{L^2 - M^2}{L + \frac{D'}{D}M} \tag{3-2}$$

When the input voltage is high and the duty cycle is smaller than 0.5, L_{eq1} determines the phase current ripple. Hence, L_{eq1} can be considered as steady-state inductance when duty cycle is smaller than 0.5. When the input voltage is low and the duty cycle is larger than 0.5, L_{eq3} determines the phase current ripple. Thus L_{eq3} is the steady-state inductance when the duty cycle is larger than 0.5. Therefore, for a CRM PFC converter with a coupled inductor, the steady-state inductance changes with the input voltage during a half-line cycle, as shown in Fig. 3.14. The blue line represents the non-coupled case. The inductance is a constant value during half-line cycle. The red, green, purple and light blue lines represent the coupled inductor with coupling coefficient as -0.5, -0.6, -0.7 and -0.8 respectively. When duty cycle is smaller than 0.5, $L_{ss} = L_{eq1}$. When duty cycle is larger than 0.5, $L_{ss} = L_{eq3}$. If the same steady-state inductance is kept for the non-coupled inductor and coupled inductor at $T_{line}/4$, the coupled inductor has larger steady-state inductance when the duty cycle approaches 0.5. Because of this, the on-time also needs to change during the half-line cycle in order to achieve unity power factor. In the CRM operation, if the inductance is larger, the switching frequency is lower. If the inductance is smaller, the switching frequency is higher. Thus, the switching frequency with a coupled inductor during the half-line cycle is different

from the non-coupled case. Fig. 3.15 shows the switching frequency during a half-line cycle with different coupling coefficients. The blue line represents the non-coupled case. The red, green, purple and light blue lines represent the coupled inductor with coupling coefficient as -0.5, -0.6, -0.7 and -0.8 respectively. Because the same steady-state inductance is kept for the non-coupled inductor and coupled inductor at $T_{line}/4$ instant, the switching frequency of non-coupled inductor and coupled inductor are the same 1 MHz. It can be seen that the coupled-inductor CRM PFC converter has a much lower switching frequency than the non-coupled case, except for the zero-crossing area. Thus, the coupled inductor can reduce the average switching frequency of the CRM PFC converter, and this can improve the converter efficiency. This is the first benefit of coupled inductor in CRM PFC converter.

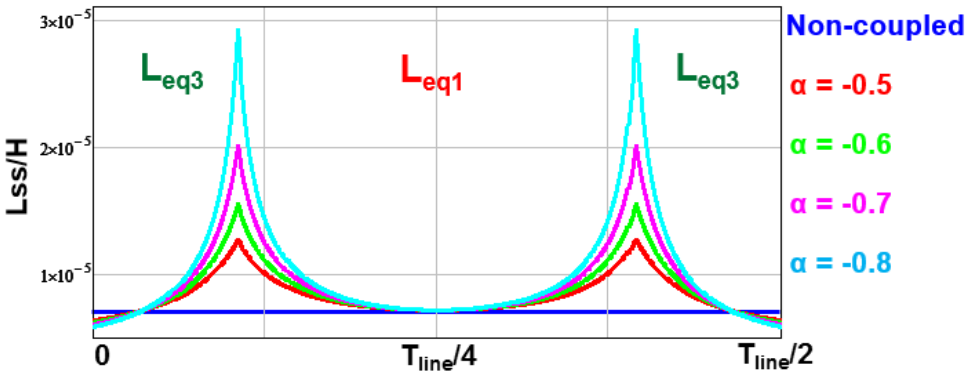


Fig. 3.14 Steady-state inductance variance during half-line cycle

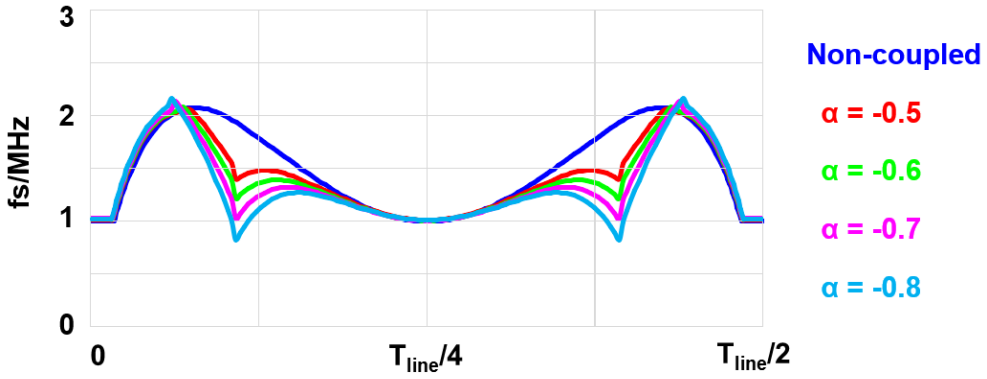


Fig. 3.15 Switching frequency variance of coupled inductor during half -line cycle

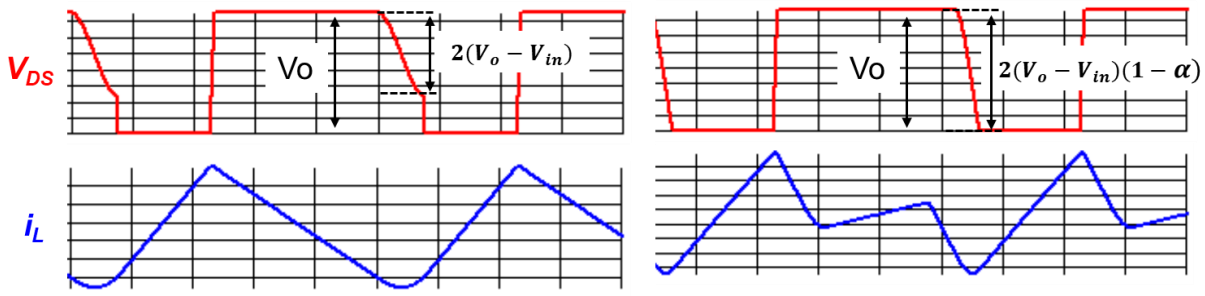
As analyzed in [51], the equivalent inductance during the resonant period is L_{eq4}. The expression of L_{eq4} is shown in (3-3). With the same steady state inductance as non-coupled inductor (3-4), L_{eq4} can be expressed as (3-5). With negative coupling, it can be seen that L_{eq4} is always smaller than the non-coupled inductor. Hence the resonant period with a coupled inductor is shorter than the non-coupled case. A shorter resonant period means a larger portion of energy transferring time. Thus, the conduction loss is smaller.

$$L_{eq4} = L - \frac{M^2}{L} \tag{3-3}$$

$$L_{nc} = L_{eq1} = \frac{L^2 - M^2}{L + \frac{D}{D'}M} \tag{3-4}$$

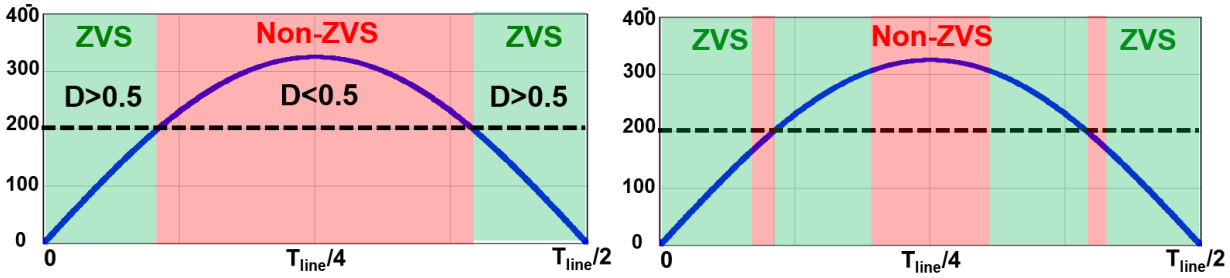
$$L_{eq4} = L_{nc}\left(1 + \frac{D}{D'}\alpha\right) < L_{nc} \tag{3-5}$$

In [51], the coupled inductor is proven to have the ability to help achieve ZVS when the duty cycle is smaller than 0.5. As shown in Fig. 3.16 (a), the resonant amplitude without coupling is $2(V_o\text{-}V_{in})$. Therefore, when input voltage is higher than one half of output voltage, V_{DS} cannot resonant to zero. With coupled inductor, the resonant amplitude is $2(V_o\text{-}V_{in})(1\text{-}\alpha)$, which is higher than $2(V_o\text{-}V_{in})$. Therefore, V_{DS} has the ability to resonant to zero, as shown in Fig. 3.16 (b). This is a great benefit for the CRM PFC converter. As shown in Fig. 3.17 (a), the converter cannot achieve ZVS when input voltage is higher than 200V. The red zone is the non-ZVS range. However, the coupled inductor, the non-ZVS range is greatly reduced, as shown in Fig. 3.17 (b). This can help reduce the non-ZVS loss by 50%.



(a) Non-coupled case (b) Coupled inductor case

Fig. 3.16 Coupling can help achieve ZVS



(a) Non-coupled case (b) Coupled inductor case

Fig. 3.17 Coupling can help extend ZVS range

A coupled inductor can also reduce circulating energy when the duty cycle is larger than 0.5 [51]. This characterization of coupled inductors can help improve the performance of the CRM PFC converter. When the input voltage is low, the converter will have extra circulating energy. The coupled inductor can reduce circulating energy during this time period. Thus the coupled inductor can reduce conduction loss for the CRM PFC converter.

3.1.3 PCB Winding Inductor Design

In the conventional AC-DC converter, the switching frequency is around 100 kHz, the inductor is very bulky and manually assembled. This bulky and sloppy magnetic design cannot meet the demand of increasing efficiency and power density. With 1 MHz switching frequency,

the inductor size can be greatly reduced, as shown in Fig. 3.18. The volume and weight of inductor are reduced 80%. Conventional magnetic materials are not suitable for such high switching frequency. In this high frequency inductor, P61 material is used. The core loss is shown in Fig. 3.19. It can be seen that the P61 has much lower core loss than 3F45 at 1 MHz and 2 MHz. With the new material, the inductor can be designed smaller and more efficient.

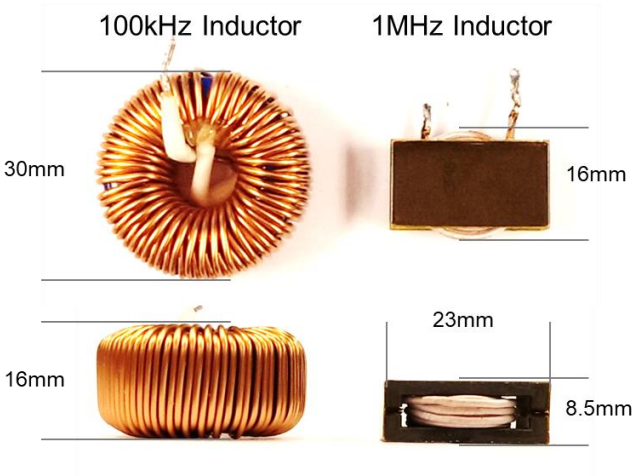


Fig. 3.18 Size comparison between 100 kHz inductor and 1 MHz inductor

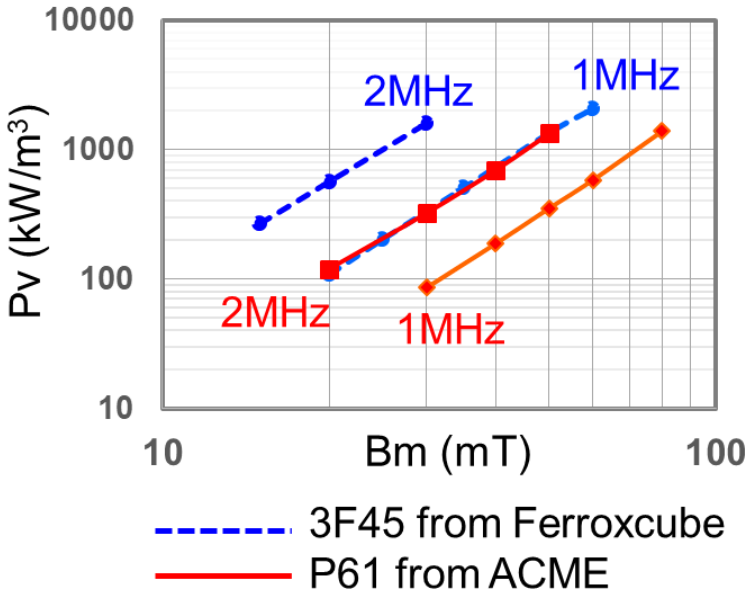


Fig. 3.19 Core loss density of 3F45 and P61

Table 3-1 shows the loss breakdown for two non-coupled inductors. The non-coupled inductor uses two ER23 cores. The winding is 250/46 litz wire with 10 turns for each inductor.

Table 3-1 Loss breakdown for non-coupled inductor

Winding Loss (W)	Core Loss (W)	Total Loss/W
2.3	2.3	4.6

Although this inductor is small and high efficient, it still need to be manually assembled and the tolerance control is poor. In order to achieve automated manufacture and good quality control, PCB winding magnetic is a better choice. People have been using PCB winding to build transformers for many years [36][52]. However, PCB winding inductor for CRM PFC is still a challenge. There is no PCB winding inductor can achieve same efficiency as conventional litz-wire inductor.

The non-coupled inductor design above provides a baseline of inductor size and loss. The design of a coupled inductor is shown below. Based on the previous analysis, in order to reduce the average switching frequency, strong coupling is preferred. In this paper, $\alpha = -0.7$ is chosen. However, the typical EI core structure cannot achieve such high coupling coefficient. Therefore the first attempt is made with a UI core (Structure I). PCB winding has been used in many applications because it is easy to manufacture and easy to control the parasitics. Fig. 3.20 Coupled inductor in UI core shows the structure of a coupled inductor with PCB winding in a UI core. L_1 is wound on the left leg with a five-layer PCB; each layer has two turns. L_2 is wound on the right leg with 10 turns PCB winding. Table 3-2 shows the simulated loss breakdown of this coupled inductor in the UI core structure. It can be seen that this coupled inductor has much higher winding

loss than the non-coupled inductor. Therefore the total loss of this coupled inductor is much higher than the non-coupled inductor. This is because for CRM operation, the AC current ripple is dominant. High AC current ripple will lead to large AC winding loss in the PCB winding. Because of this, PCB winding inductor is not adopted in this application.

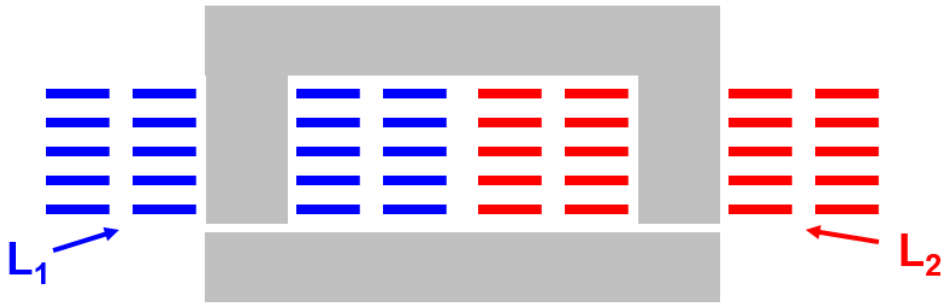


Fig. 3.20 Coupled inductor in UI core

Table 3-2 Loss breakdown for coupled inductor Structure I

Winding Loss (W)	Core Loss (W)	Total Loss/W
6.7	1.3	8.0

In order to reduce the winding loss, a new structure of coupled inductor is developed (Structure II). As shown in Fig. 3.21, the core structure is an EI core. In addition, the interleaving concept is applied to this structure. Now there are eight turns of L_1 and two turns of L_2 on the left leg, and eight turns of L_2 and two turns of L_1 on the right leg. Table 3-3 shows the simulated loss breakdown of this new inductor structure. With this interleaving effect, the AC winding loss has been greatly reduced. However, the total loss of this coupled inductor is still higher than the non-coupled inductor. FEA simulation is conducted to study the loss, and Fig. 3.22 shows the FEA

simulation result of the left leg. It can be seen that there is strong fringing flux near the air gap, which will cause large loss on the winding.

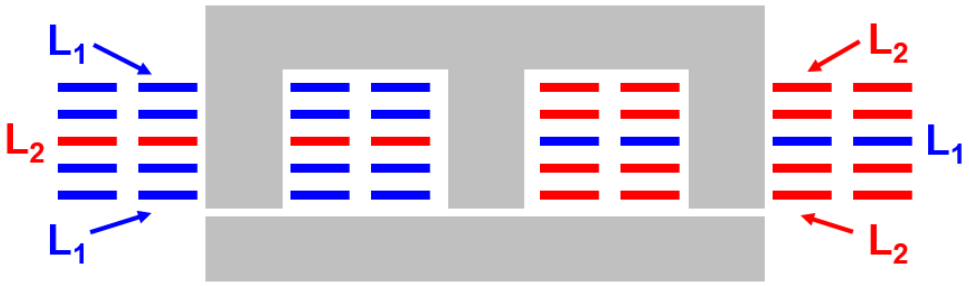


Fig. 3.21 Coupled inductor with interleaved winding

Table 3-3 Loss breakdown for coupled inductor Structure II

Winding Loss (W)	Core Loss (W)	Total Loss/W
3.1	1.9	5.0

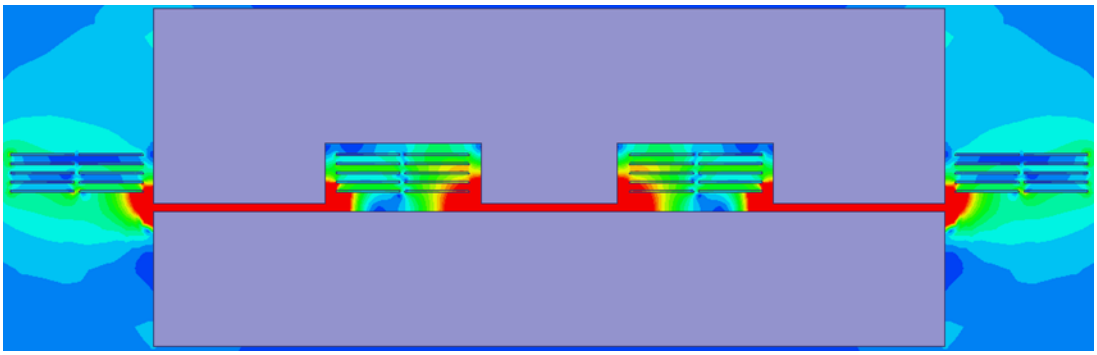


Fig. 3.22 Simulation of flux distribution with large fringing flux

According to [53], the winding can be cut to avoid fringing flux. Fig. 3.23 shows the new winding structure to further reduce the winding loss (Structure III). In this structure, there is a total of six layers of PCB winding. The bottom two layers have only one turn. The winding on the fourth

layer has been cut to avoid the fringing flux. Table 3-4 shows the simulated loss breakdown of the inductor in Structure III. With the new structure, the AC winding loss has been further reduced. Fig. 3.24 Simulation result of avoiding fringing flux shows the FEA simulation result of the left leg. It can be seen that the winding has avoid the fringing flux. The total loss of the coupled inductor Structure III is smaller than the non-coupled inductor. The result shows that for coupled inductor, a good PCB winding structure can achieve similar loss as litz wire. With the PCB winding, a great amount of labor can be removed in manufacture.

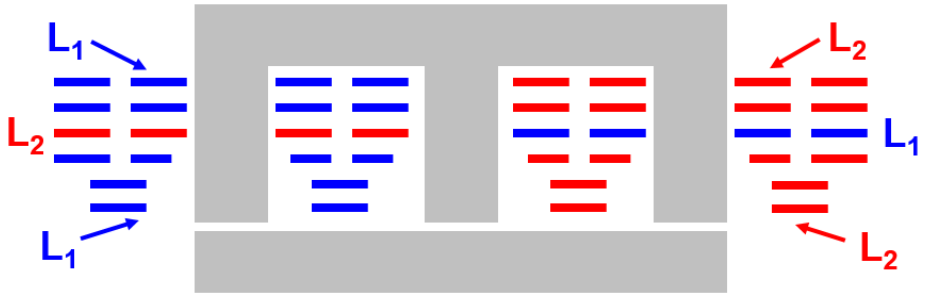


Fig. 3.23 Coupled inductor structure III

Table 3-4 Loss breakdown for coupled inductor Structure III

Winding Loss (W)	Core Loss (W)	Total Loss/W
2.4	1.9	4.3

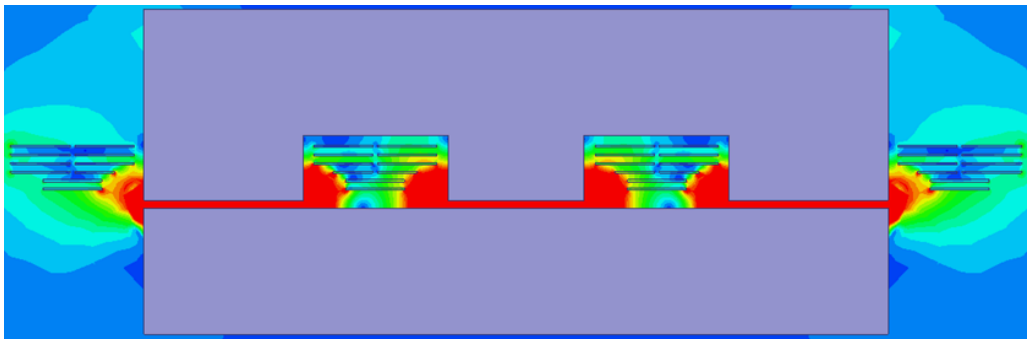


Fig. 3.24 Simulation result of avoiding fringing flux

3.1.4 Balance Technique for Coupled Inductor

One drawback of this PFC converter is high CM noise. As shown in Fig. 3.25, the CM noise of this GaN based PFC converter is much higher than conventional Si based PFC converter. This high CM noise will impact the EMI filter design and increase the total system volume.

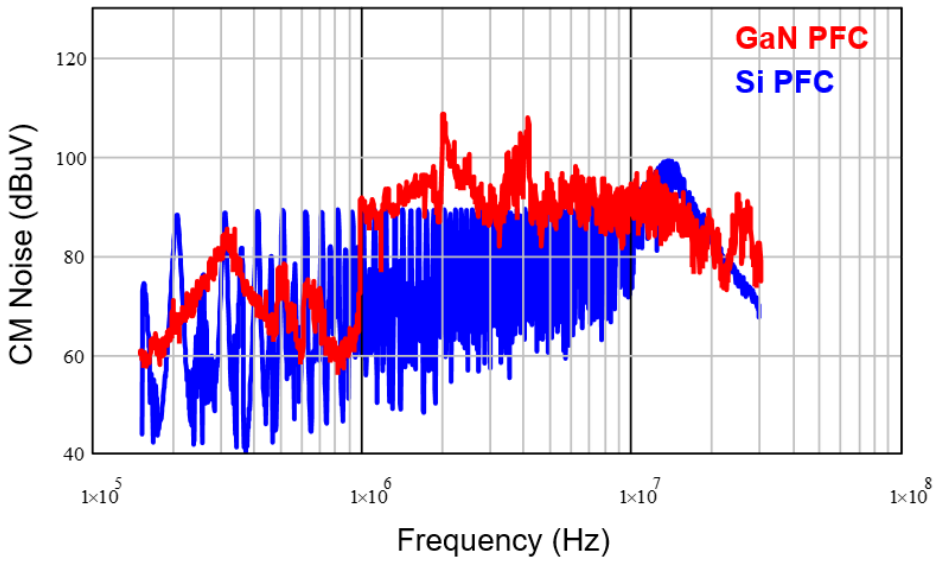


Fig. 3.25 CM noise comparison between GaN based PFC and Si based PFC

In [54], a balancing technique is introduced for the interleaved boost PFC converter to reduce CM noise. The balancing technique can also be applied to the interleaved totem-pole PFC converter with a coupled inductor. As shown in Fig. 3.26, an extra inductor is added to achieve balance. The CM noise model is shown in Fig. 3.27. The dv/dts of the active devices are the dominant CM noise sources. Hence they are modeled as two voltage sources: V_{N1} and V_{N2}. C_b is the parasitic capacitance between the output trace and ground, and C_d is the drain-to-ground capacitance. According to the superposition theory, the two independent noise sources can be studied separately. Fig. 3.28 shows the CM noise model of source V_{N1}. Here, V_{N2} is a short circuit. The balance condition for this circuit is shown in (3-6). In order to get the balance equation, the

ratio of Z_1/Z_2 needs to be calculated first. From the circuit we can get the equation (3-7). Then the ratio of Z_1/Z_2 can be derived as (3-8). Thus the balance equation can be derived as (3-9). It can be derived that the balance condition for noise source V_{N2} is also (3-9). It is apparent that for the coupled inductor, the mutual inductance does not impact the balance condition.

$$\frac{Z_a}{Z_b} = \frac{C_d + C_b}{C_d} \tag{3-6}$$

$$\begin{cases} V_1 = \dfrac{di_1}{dt} L_k + \dfrac{d(i_1 + i_2)}{dt} M \\ V_2 = \dfrac{di_2}{dt} L_k + \dfrac{d(i_1 + i_2)}{dt} M \\ V_2 = \dfrac{d(i_1 - i_2)}{dt} L_b \end{cases} \tag{3-7}$$

$$\frac{Z_a}{Z_b} = \frac{V_1/i_1}{V_2/i_1} = \frac{L_k + L_b}{L_b} \tag{3-8}$$

$$\frac{L_k}{L_b} = \frac{C_b}{C_d} \tag{3-9}$$

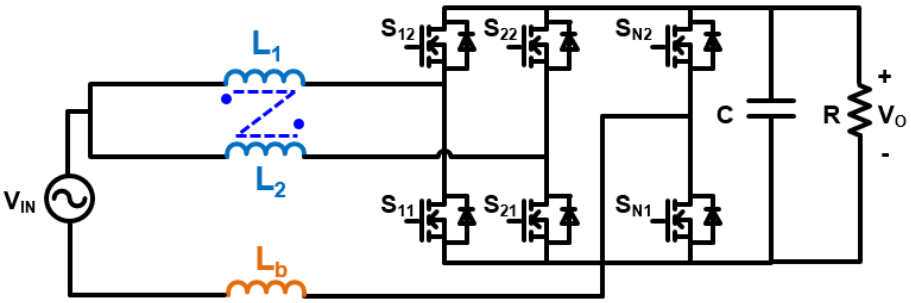


Fig. 3.26 Balancing technique for interleaved totem-pole PFC converter with coupled inductor

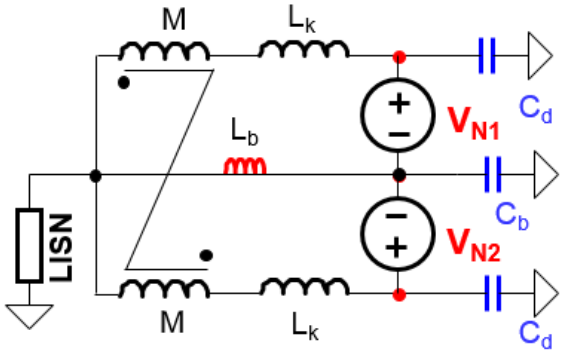


Fig. 3.27 CM noise model of PFC converter with balance

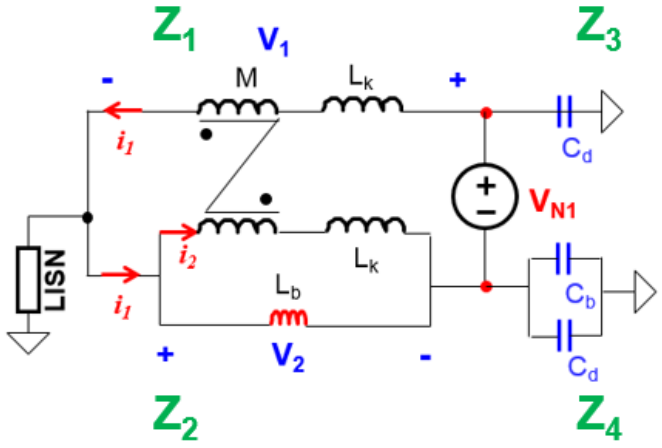


Fig. 3.28 CM noise model of one noise source

In [54], it is determined that in order to achieve better balance at high frequencies, the balance inductor L_b should be coupled with the original inductor. Hence, for the coupled inductor, two inductors L_3 and L_4 are applied to achieve better balance, and they are coupled with L_1 and L_2. Fig. 3.29 shows the circuit topology and Fig. 3.30 shows the magnetic structure. The CM noise model is shown in Fig. 3.31. Using the superposition theory, the model of noise source V_{N1} is shown in Fig. 3.32. The balance condition for this circuit is shown in (3-10). Still, the ratio of Z_1/Z_2 needs to be calculated first. It is assumed that L_1 and L_3 are perfectly coupled, and L_2 and L_4 are perfectly coupled. The number of turns of L_1 and L_2 is N_1. The number of turns of L_3 and L_4 is N_2. Thus, we have the equations shown in (3-11). Then the ratio of Z_1/Z_2 can be derived as (3-12). Thus, the

balance condition for source V_1 is (3-13). Similarly, the balance condition for noise source V_{N2} is also (3-13). The CM noise of this PFC converter can be minimized as long as this balance condition is achieved.

$$\frac{Z_1}{Z_2} = \frac{C_d + C_b}{C_d} \tag{3-10}$$

$$\begin{cases} \dfrac{V_1}{V_3} = \dfrac{N_1}{N_2} \\ \dfrac{V_2}{V_4} = -\dfrac{N_1}{N_2} \\ V_3 + V_4 = V_2 \\ i_1 = i_2 \end{cases} \tag{3-11}$$

$$\frac{Z_1}{Z_2} = \frac{V_1/i_1}{V_2/i_2} = \frac{N_1 + N_2}{N_2} \tag{3-12}$$

$$\frac{N_1}{N_2} = \frac{C_b}{C_d} \tag{3-13}$$

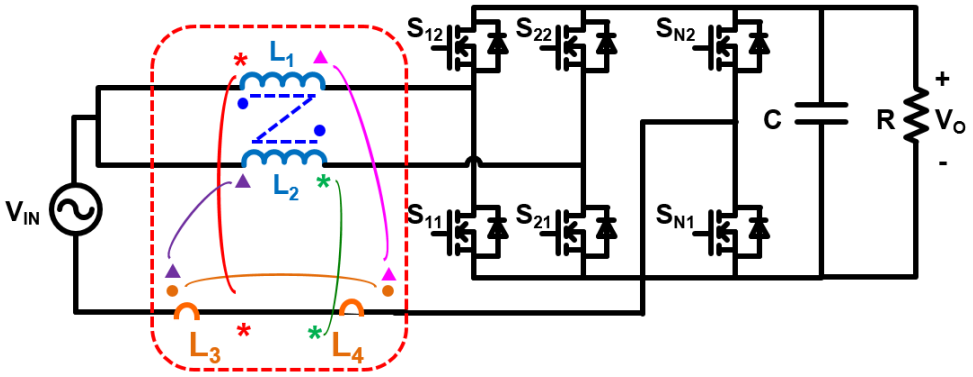


Fig. 3.29 Circuit structure of improved balance technique

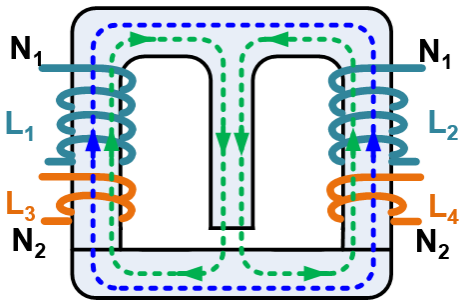


Fig. 3.30 Inductor structure demonstration of improved balance technique

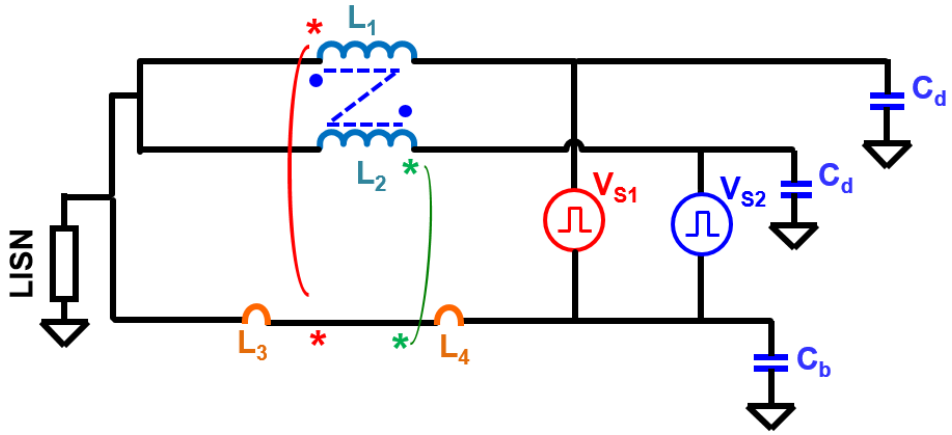


Fig. 3.31 CM noise model of improved balance technique

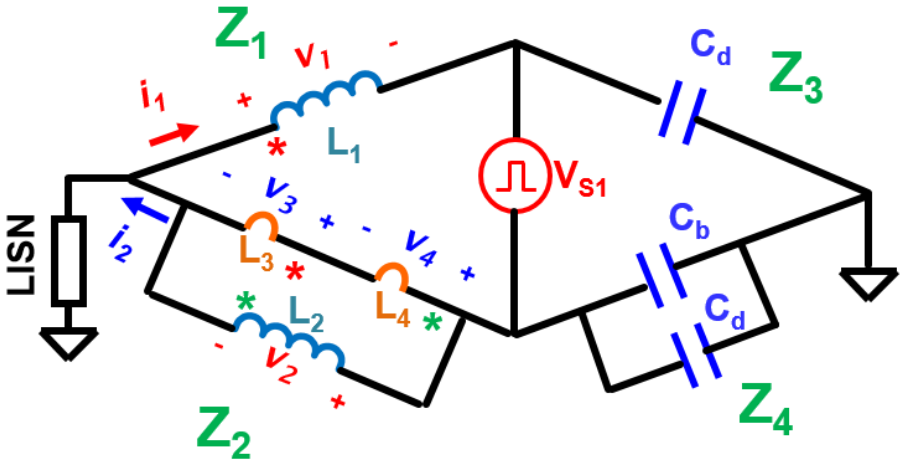


Fig. 3.32 Effect of only noise source V_{N1}

In the previous analysis, there are two inductors in the coupled inductor structure, and L_{eq1}, L_{eq2}, L_{eq3} and L_{eq4} are derived based on that structure. The circuit performance can then be analyzed

by using these four equivalent inductances. However, with the balance technique, there are four inductors coupled together. In order to analyze the performance of this circuit, we need to derive new values for L_{eq1}, L_{eq2}, L_{eq3} and L_{eq4}. In order to derive these new values, the inductance matrix need to be derived first. Fig. 3.33 shows the magnetic circuit. From the magnetic circuit, the inductance matrix can be derived as (3-14). The circuit in Fig. 3.29 can be transformed in to Fig. 3.34. Then the equations for V_{eq1} and V_{eq2} can be derived as (3-15). From (3-14) and (3-15) we can get (3-16). Then the simplified equivalent inductance Leq and Meq can be express as (3-17). The four-inductor circuit in Fig. 3.29 can be simplified as the two-inductor circuit structure in Fig. 3.35. The self-inductance is equal to L_{eq}, and the mutual inductance is equal to M_{eq}. Hence, the new expressions of L_{eq1}, L_{eq2}, L_{eq3} and L_{eq4} can be expressed using L_{eq} and M_{eq}.

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = L_1 \begin{bmatrix} 1 & \alpha & \frac{N_2}{N_1} & \alpha\frac{N_2}{N_1} \\ \alpha & 1 & \alpha\frac{N_2}{N_1} & \frac{N_2}{N_1} \\ \frac{N_2}{N_1} & \alpha\frac{N_2}{N_1} & \frac{N_2^2}{N_1^2} & \alpha\frac{N_2^2}{N_1^2} \\ \alpha\frac{N_2}{N_1} & \frac{N_2}{N_1} & \alpha\frac{N_2^2}{N_1^2} & \frac{N_2^2}{N_1^2} \end{bmatrix} \begin{bmatrix} di_1/dt \\ di_2/dt \\ di_3/dt \\ di_4/dt \end{bmatrix} \tag{3-14}$$

$$\begin{cases} v_{eq1} = v_1 + v_3 + v_4 \\ v_{eq2} = v_2 + v_3 + v_4 \end{cases} \tag{3-15}$$

$$\begin{cases} v_{eq1} = L1\left(\frac{N_1^2 + 2(1+\alpha)N_1N_2 + 2(1+\alpha)N_2^2}{N_1^2}\right)\cdot\frac{di_1}{dt} + L1(\frac{\alpha N_1^2 + 2(1+\alpha)N_1N_2 + 2(1+\alpha)N_2^2}{N_1^2})\cdot\frac{di_2}{dt} \\ v_{eq2} = L1\left(\frac{N_1^2 + 2(1+\alpha)N_1N_2 + 2(1+\alpha)N_2^2}{N_1^2}\right)\cdot\frac{di_2}{dt} + L1(\frac{\alpha N_1^2 + 2(1+\alpha)N_1N_2 + 2(1+\alpha)N_2^2}{N_1^2})\cdot\frac{di_1}{dt} \end{cases} \tag{3-16}$$

$$\begin{aligned} L_{eq} &= L1\left(\frac{N_1^2 + 2(1+\alpha)N_1N_2 + 2(1+\alpha)N_2^2}{N_1^2}\right) \\ M_{eq} &= L1\left(\frac{\alpha N_1^2 + 2(1+\alpha)N_1N_2 + 2(1+\alpha)N_2^2}{N_1^2}\right) \end{aligned} \tag{3-17}$$

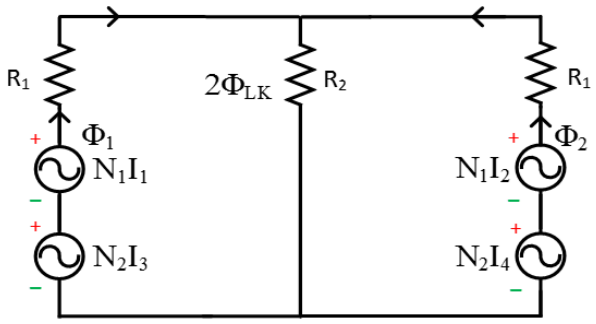


Fig. 3.33 Magnetic circuit of coupled inductor with balance

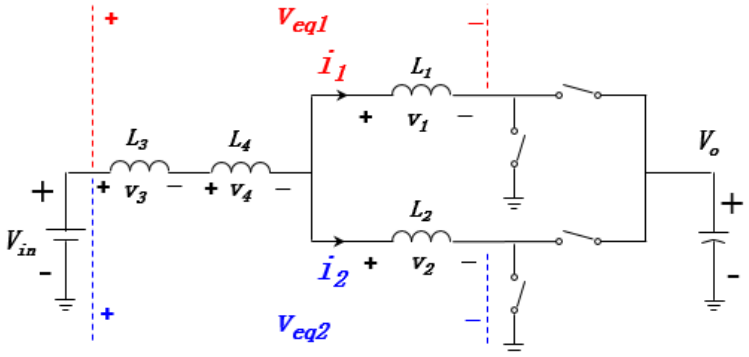


Fig. 3.34 Equivalent circuit of coupled inductor with balance

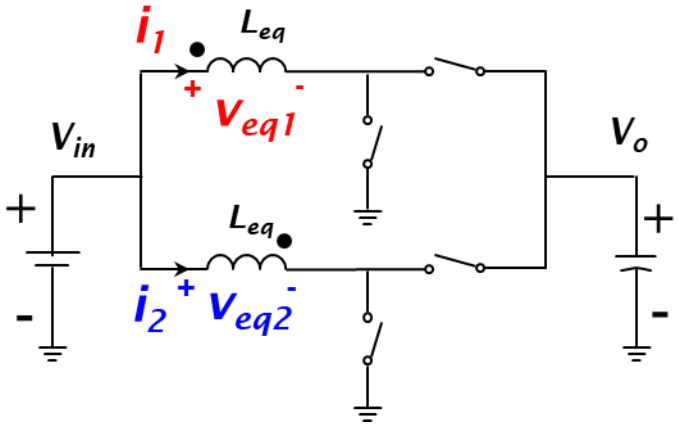


Fig. 3.35 Simplified equivalent circuit of coupled inductor with balance

In order to verify this theory, a simulation model is built where L_{eq} and M_{eq} of the balanced circuit are equal to L and M of the non-balanced circuit. From Fig. 3.36, it can be seen that the balanced circuit and non-balanced circuit have identical current waveforms.

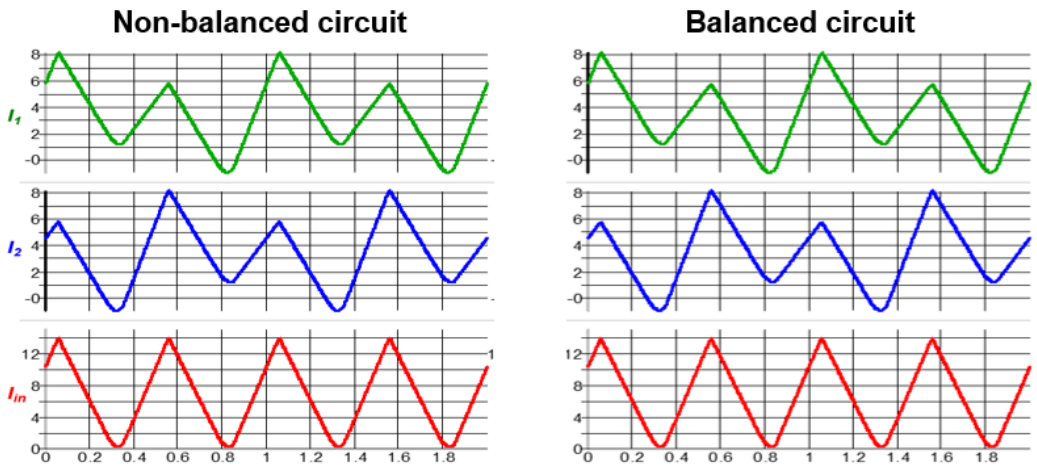


Fig. 3.36 Current waveforms verification

In the previous analysis, the inductor is integrated into PCB motherboard. The balance technique can be easily implement into the PCB winding inductor. Fig. 3.37 shows the inductor structure. By replacing the bottom layer of L_1 and L_2 with L_3 and L_4, the balance technique can be integrated. It can be seen that L_3 and L_4 have only one turn. Therefore the turns ratio of N_1:N_2 is 9:1. Based on equation (3-11), the capacitor value needs to be changed to achieve the balance condition. Fig. 3.38 shows that an external capacitor C_{add} is applied in parallel with C_b. And the new balance equation is shown in (3-16).

$$\frac{N_1}{N_2} = \frac{C_b + C_{add}}{C_d} \tag{3-18}$$

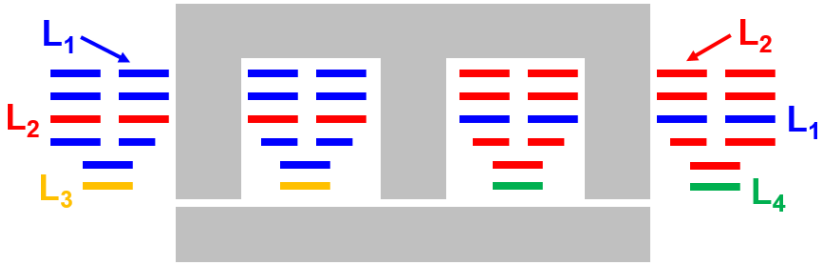


Fig. 3.37 Cross-section view of coupled inductor with balance technique

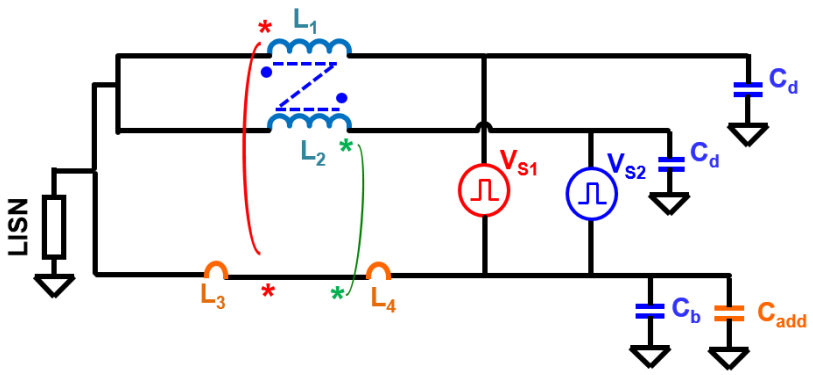
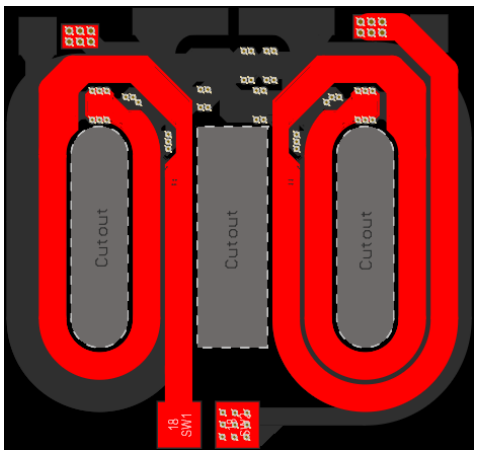


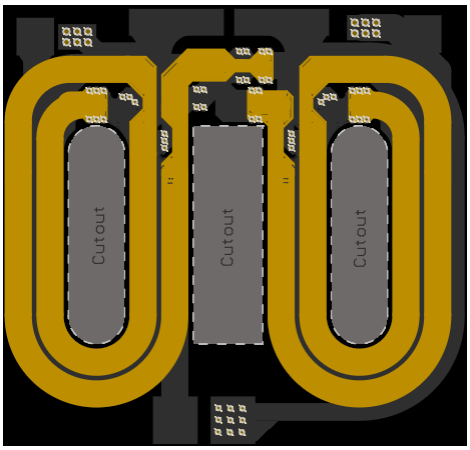
Fig. 3.38 Add capacitor to maintain balance condition.

3.1.5 Hardware Demonstration

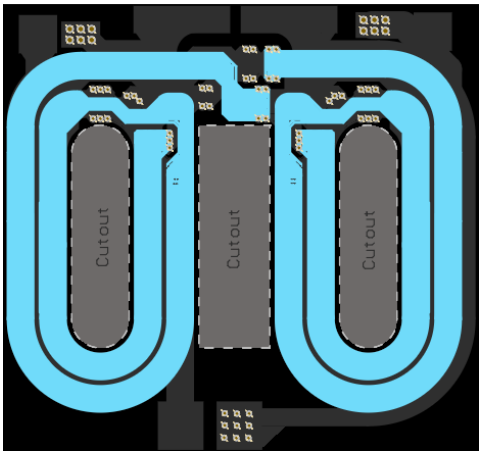
The detailed winding arrangement for the proposed PCB winding inductor is illustrated in Fig. 3.39. The windings are on the two outer legs of magnetic core. For inductor L_1 on the left leg, the current goes into the first layer, then goes to second layer through the vias. The third layer of L_1 should be on the right leg. On the fifth layer, the current goes back to the left leg. Then the current goes out from the forth layer. For inductor L_2 on the right leg, the current goes into the forth layer, then goes to fifth layer through vias. Then the current goes to the third layer on the left leg. After two turns on the left leg, the current goes back to the second layer on the right leg and goes out though the first layer. The bottom layer is the balance inductor L_3 and L_4. The terminals of L_3 and L_4 are left open. This is for the easy of configuration of balance and non-balance case.



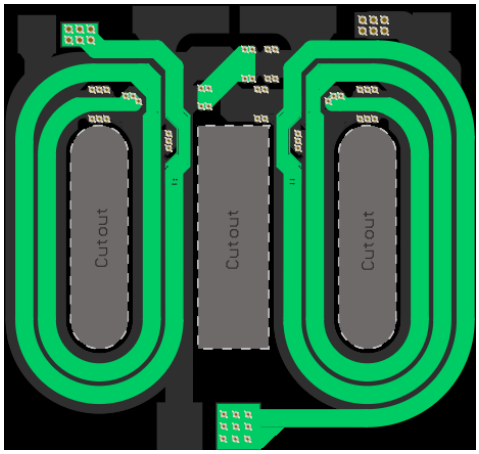
(a) Layer 1



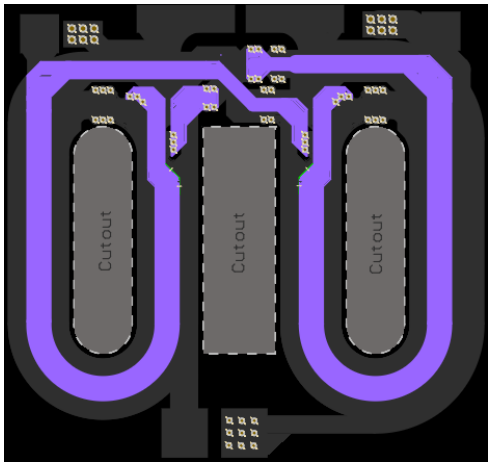
(b) Layer 2



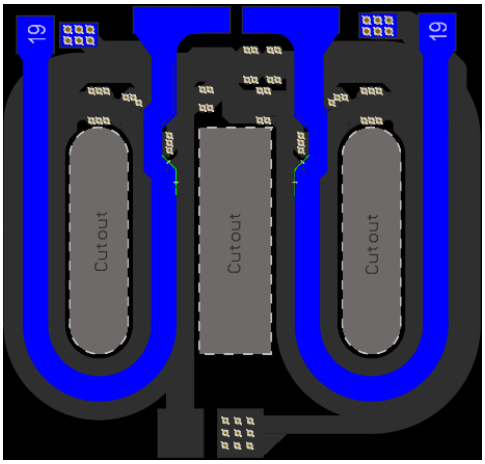
(c) Layer 3



(d) Layer 4



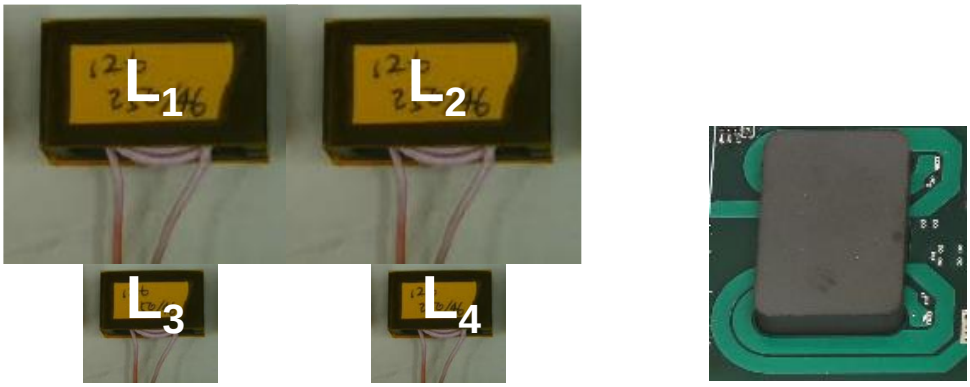
(e) Layer 5



(f) Layer 6

Fig. 3.39 Winding arrangement for proposed PCB winding inductor

In Fig. 3.40, the comparison between conventional discrete litz-wire inductor and proposed PCB winding integrated inductor is demonstrated. In order to achieve similar EMI performance, four discrete litz-wire inductors are needed. Two large inductors L_1 and L_2 are the main inductors for phase 1 and phase 2. Two small inductor L_3 and L_4 are balance inductors for CM noise reduction. This is a very complicated structure and implementation is labor intensive. Worse still, the parasitic control is poor, so the EMI noise reduction is not guaranteed. On the contrary, the proposed PCB winding inductor is able to integrate four inductors into one component. With the winding printed on the circuit board, the inductance and parasitics are well controlled. Therefore the circuit performance and EMI noise reduction is more consistent. Furthermore, the proposed integrated inductor can achieve fully automated manufacturer. The elimination of labor intensive work can further reduce the cost.



(a) Discrete litz-wire inductor (b) Integrated PCB winding inductor

Fig. 3.40 Comparison between discrete inductor and integrated inductor

Fig. 3.41 shows the hardware photo of the 1.2kW CRM PFC converter with PCB winding inductor. The power density of this converter is 700W/in^3 (without output capacitors). Fig. 3.42 shows the measured efficiency. The peak efficiency is above 99%. It is as good as the state-of-the-

art low frequency Si based PFC converter. However, the power density of this high frequency PFC converter is 10 times higher than the traditional low frequency design.

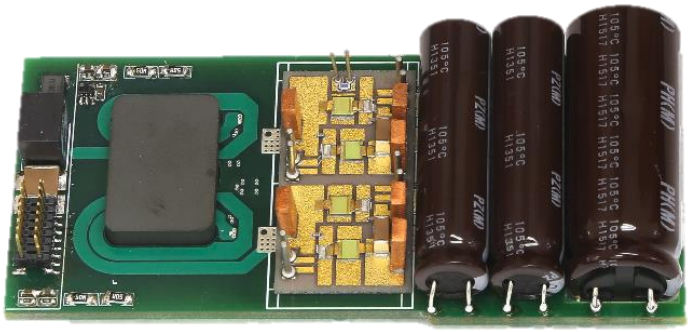


Fig. 3.41 Hardware photo of 1.2kW CRM PFC with PCB winding inductor

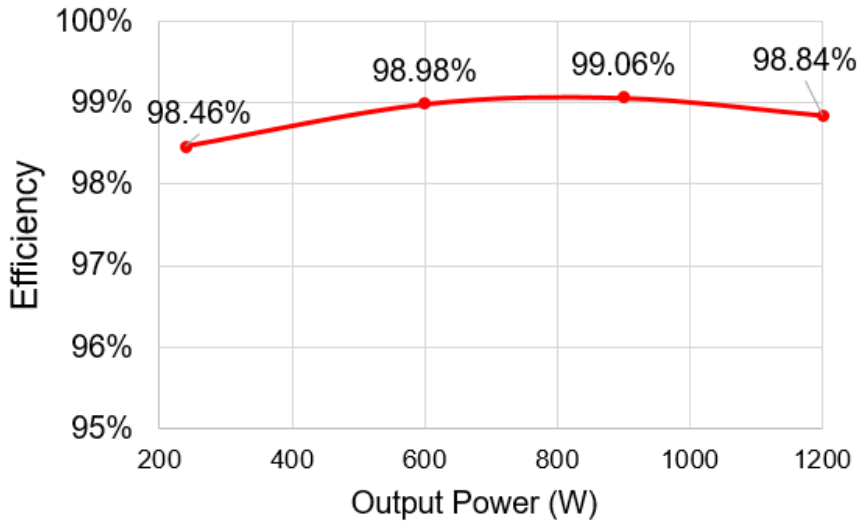


Fig. 3.42 Measured efficiency of 1.2kW PFC converter

Fig. 3.43 shows the CM noise measurement result. It can be seen that with the balance technique, the CM noise has a 20dB reduction. This proves the effectiveness of the balance technique. With PCB winding inductor, the parasitic can be easily controlled and therefore the balance technique has better high frequency performance than litz wire inductor.

With the PCB winding inductor, the CRM PFC converter can achieve high efficiency and high power density. Furthermore, this inductor design greatly simplifies the manufacturing process by eliminating the labor intensive procedure.

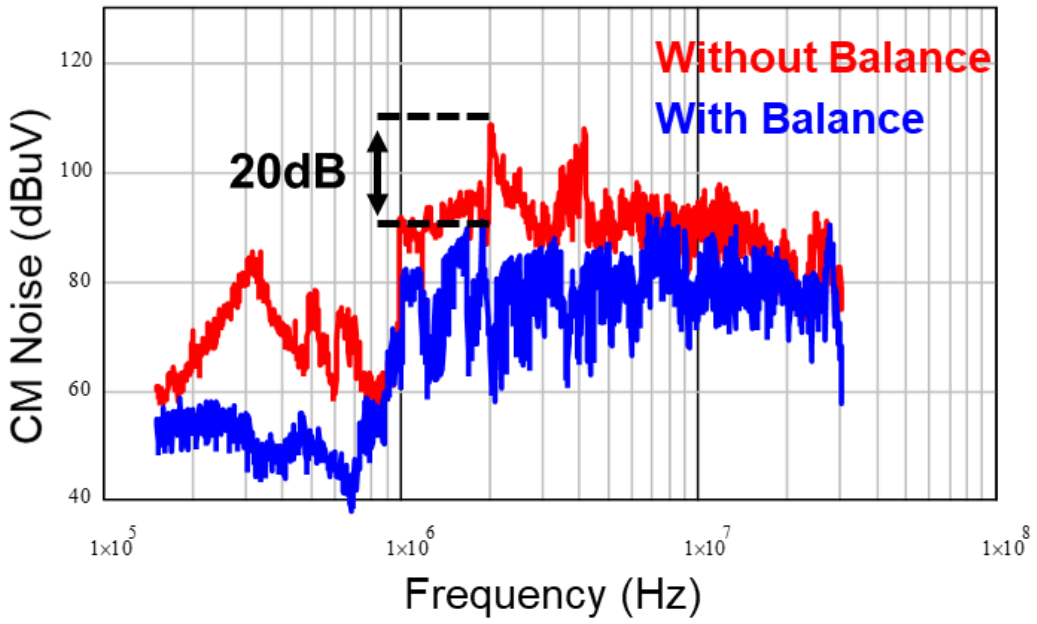


Fig. 3.43 CM noise measurement result

3.2 PCB Winding Positive Coupled Inductor with Balance Technique [55]

3.2.1 6.6kW SiC Based PFC Converter for On-board Battery Charger

With the increasing demand of energy efficiency and low combustion emissions, the Plug-in electric vehicles (PEVs) are becoming more and more popular. There are two types of PEVs, plug-in hybrid electric vehicles (PHEVs) and battery electric vehicles (BEVs). In the PEVs, the on-board battery charger (OBC) is an important component. Because the charging time is of the essence, the OBCs need to be high efficient. Furthermore, the limited space and weight in vehicle design requires the OBCs to be light weight and compact. In commercial products, the Si based OBCs are working at low switching frequency (<100 kHz), and have low power density (3-

12W/in^3) and low efficiency (92-94%) [56][57]. In addition, the customers show more and more interested on bidirectional power flow of PEVs. So the PEVs can provide power to house power grid, or power small electrical equipment in the fieldwork. However, conventional Si based OBCs cannot achieve this function without sacrifice of efficiency and power density.

With wide-bandgap (WBG) devices, the power density and efficiency of switch mode power supplies can be dramatically increased. With 1200V SiC MOSFET and 600V GaN devices, the target of this 6.6 kW OBC is to increase the switching frequency to be higher than 300 kHz. The power density should be doubled or tripled. The efficiency is higher than 95%. In addition, the OBC should achieve bidirectional power flow. Besides the high efficiency and high power density, the proposed design should also be able to achieve good manufacturability. Fig. 3.44 shows that state-of-the-art industry products and the design target of proposed OBC.

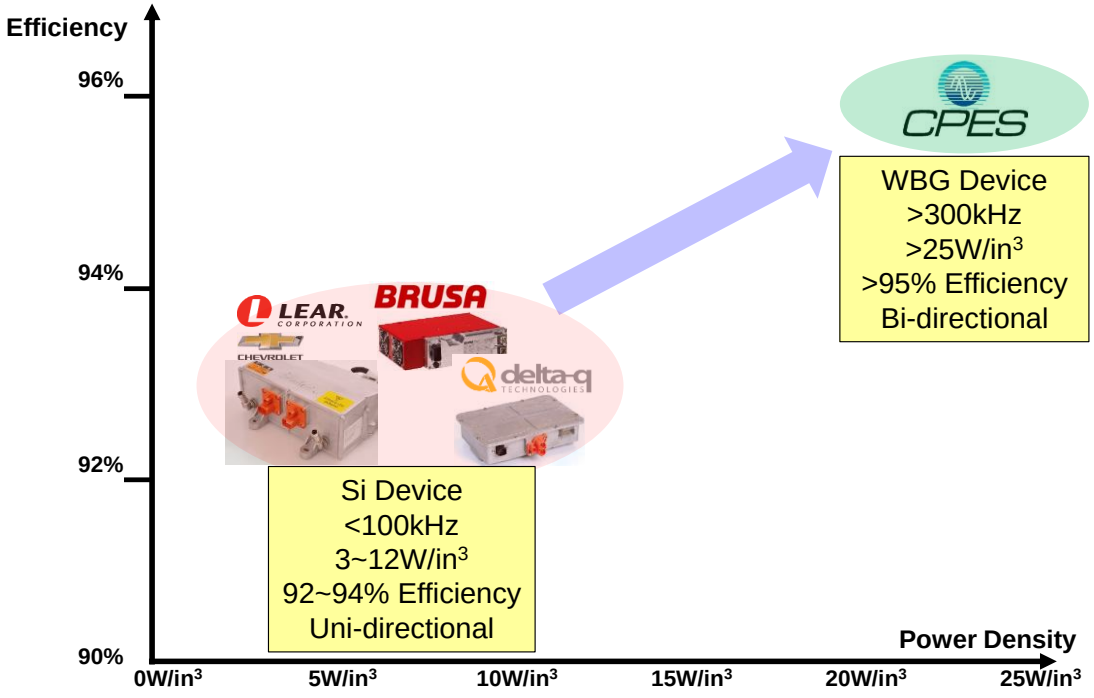


Fig. 3.44 Target of high efficiency high density bidirectional OBC

Different from the server power supply discussed in the previous section, the OBC has a very wide output range. Fig. 3.45 shows the lithium-ion battery charging profile. The OBC should have the ability to provide the desired voltage and current to the battery. The battery voltage range is 250 V to 450 V. This very wide output voltage range is a challenge in the design of OBC.

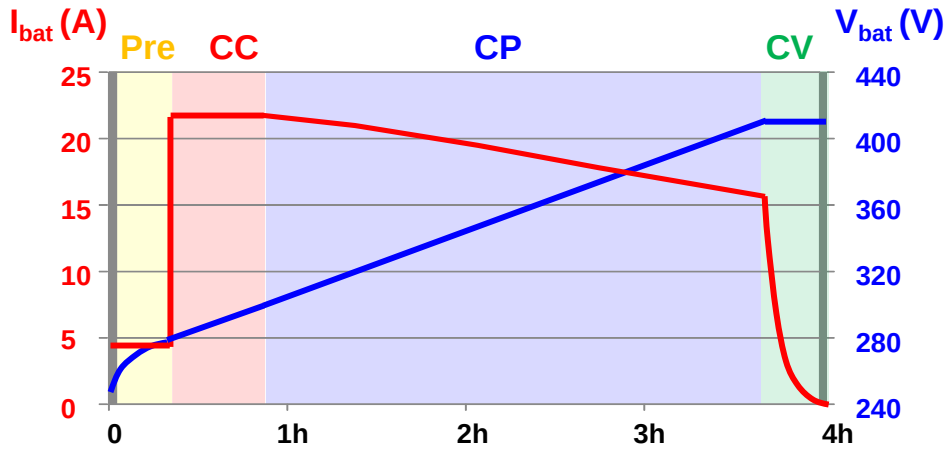


Fig. 3.45 Battery charging profile

Conventionally, the OBC is consist of PFC converter and LLC DC-DC converter. With fixed DC-link voltage, the LLC converter should be able to regulate the wide range of output voltage. However, the optimal operating point of a LLC resonant converter is the switching frequency equal to the resonant frequency. At this point, the LLC converter has highest efficiency. With wide output voltage range, the switching frequency of LLC converter is dramatically deviated from the resonant frequency to achieve the required wide range voltage gain. In this case, the efficiency of LLC converter drops dramatically.

In order to build an on-board charger with higher efficiency and higher power density, a new 6.6kW system structure is proposed, as shown in Fig. 3.46. In this proposed structure, the first stage is a two-phase interleaved totem-pole PFC converter with 1200V SiC devices. The second stage is a CLLC resonant converter. The DC-link voltage is designed to have a wide range from

500V to 840V, maintaining a 2:1 ratio to the battery voltage. Thus, the resonant converter can always working around the most efficient point. As shown in Fig. 3.47, the battery voltage is from 250 V to 450 V, the DC-link voltage is from 500 V to 840 V. Therefore, from 250 V to 420 V battery voltage, the gain of CLLC converter is 1, which means that the CLLC converter can run at optimum operation point. The gain range of CLLC converter is only 1 to 1.07. The CLLC converter can achieve high efficiency all the time. However, the burden was shifted to PFC side.

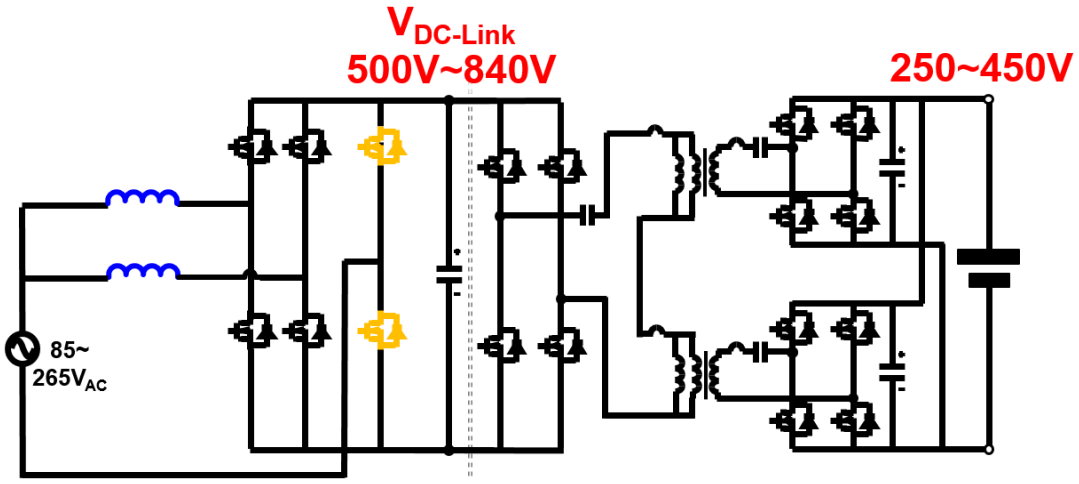


Fig. 3.46 Circuit structure for 6.6kW on-board battery charger

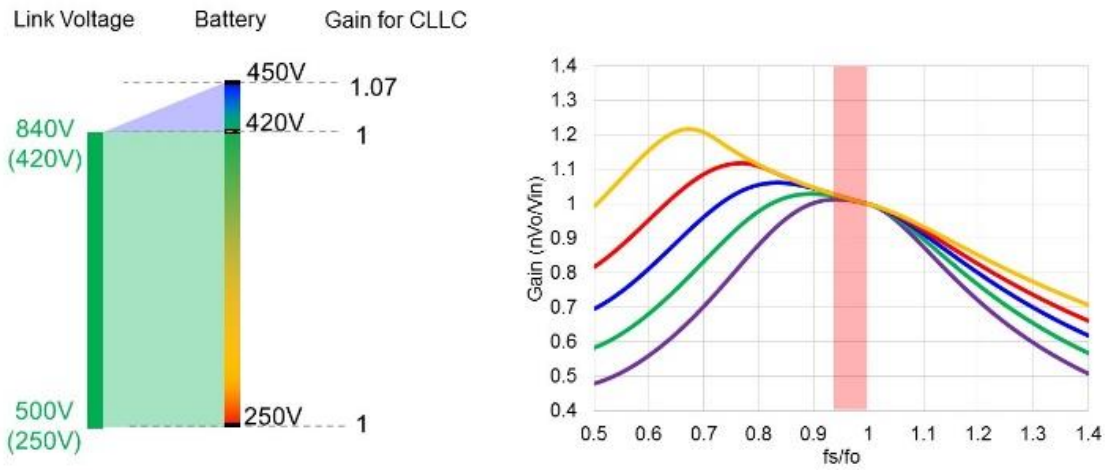


Fig. 3.47 Gain range of proposed CLLC converter

For this PFC converter, the totem-pole topology is still a good choice. The switching frequency of this PFC converter is above 300 kHz. However, high switching frequency can introduce great amount of switching loss. In order to overcome the high turn-on loss of SiC device, critical conduction mode (CRM) is a preferred control method.

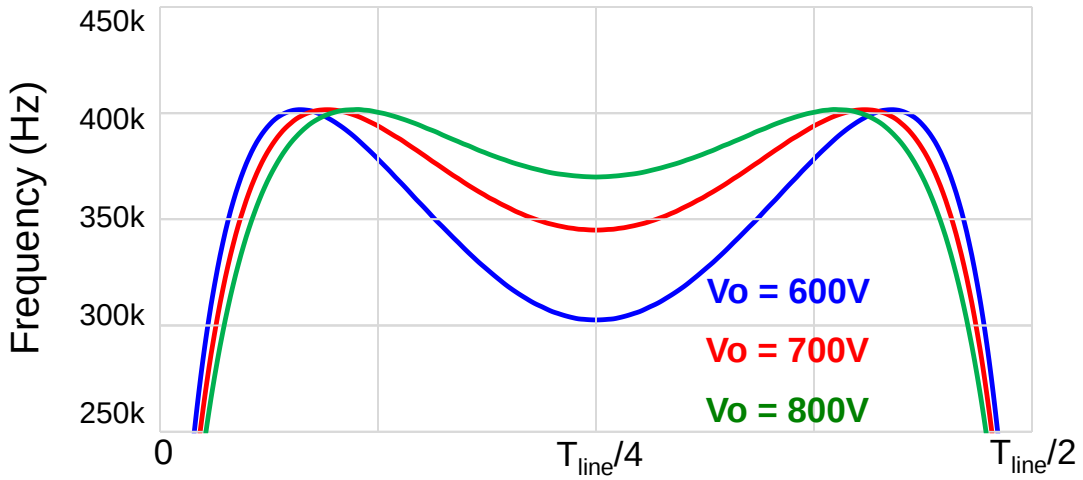


Fig. 3.48 Switching frequency variation during half line cycle

However, the CRM totem-pole PFC converter has its own limitations. The first one is large variation of switching frequency. Fig. 3.48 shows the switching frequency variation during half line cycle. As mentioned previously, the output voltage of PFC converter has a wide range from 500V to 840V. The full power operation range is above 600V. In this figure, the blue, red and green solid line represent the switching frequency when output voltage equal to 600V, 700V and 800V respectively. The switching frequency range is 300 kHz to 400 kHz.

The second issue is that the CRM PFC converter has large current ripple. Although two-phase interleaved structure is applied to reduce input current ripple, the CRM PFC converter still has larger input current ripple compared with continues conduction mode PFC converter. Therefore, the DM noise of CRM PFC converter is larger.

In order to solve these issues, the coupled inductor concept is applied to this PFC converter. Furthermore, the inductor will be integrated into PCB winding to achieve high power density and automated manufacture.

3.2.2 Negative Coupled Inductor for 6.6kW PFC

Negative coupled inductor is introduced in the Section 3.1. It is proved to achieve high power density, high efficiency, and automated manufacture. Therefore, the concept of negative coupled inductor is applied to this 6.6kW PFC converter. Fig. 3.49 shows the interleaved totem-pole PFC converter with coupled inductor. Inductor L_1 and L_2 are negative coupled. The waveforms and equivalent inductance of negative coupled inductor are introduced in Section 3.1.

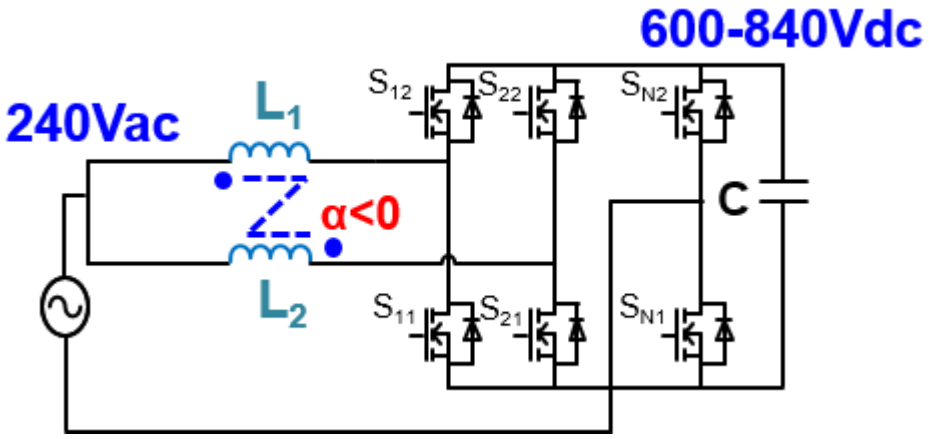


Fig. 3.49 Negative coupled inductor for 6.6kW PFC

When input voltage is high, the duty-cycle is smaller than 0.5, L_{eq1} determines the phase current ripple. Hence, L_{eq1} can be considered as steady state inductance when duty-cycle is smaller than 0.5. When input voltage is low, the duty-cycle is larger than 0.5, L_{eq3} determines the phase current ripple. Hence, L_{eq3} is the steady state inductance when duty-cycle is larger than 0.5. Therefore, for CRM PFC converter with coupled inductor, the steady state inductance is changing with input voltage during a half line cycle, as shown in Fig. 3.50. The dash line represents the non-

coupled case, which is constant 10uH. The blue, red and green lines represent the steady state inductance with negative coupled inductor for 600V, 700V and 800V output voltage respectively. It can be seen that with negative coupling, the steady state inductance will be smaller than the non-coupled inductance. In CRM operation, smaller inductance will lead to higher switching frequency, larger inductance will lead to lower switching frequency.

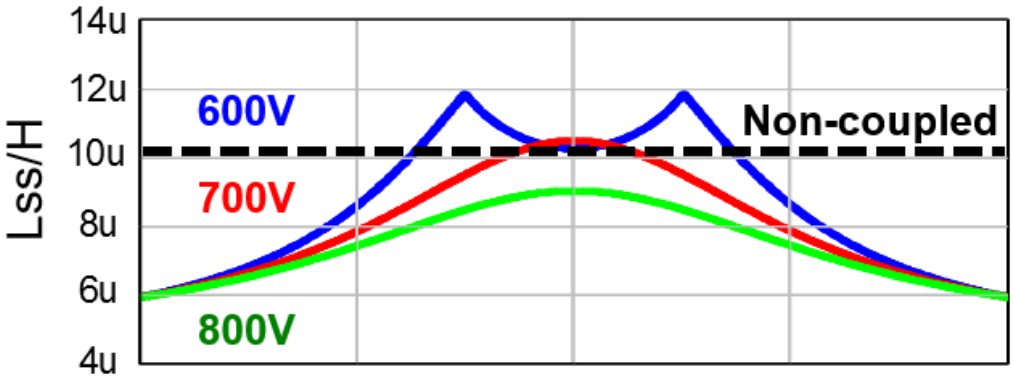


Fig. 3.50 Steady state inductance for 6.6kW PFC with negative coupled inductor

Thus, the switching frequency variation with coupled inductor during half line cycle is different from the non-coupled case. Fig. 3.51 shows the switching frequency during half line cycle with different output voltage. The dash lines represent the switching frequency for non-coupled inductor under different output voltage. The solid lines represent the switching frequency for negative coupled inductor. It can be seen that switching frequency of negative coupling is much higher than the non-coupled case. Therefore, the switching loss would increase a lot and negative coupling has no benefit.

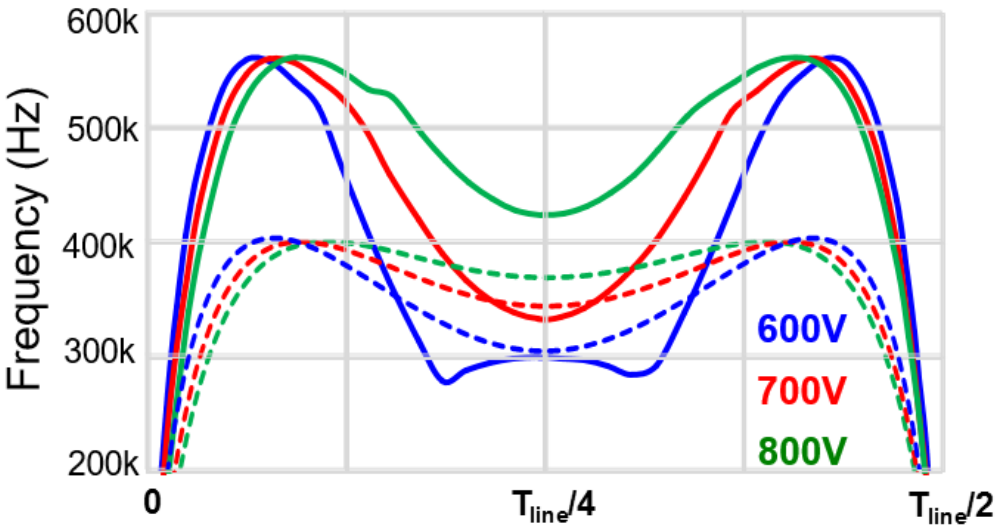


Fig. 3.51 Switching frequency for 6.6kW PFC with negative coupled inductor

The negative coupled inductor can help reduce switching frequency in the previous 1.2kW PFC converter. However, in this 6.6kW PFC converter, the negative coupled inductor actually increases the switching frequency range. This is because the two applications have different input and output voltage. The different input and output voltage will lead to different operation duty cycle. It is known from previous analysis that the steady state inductance is impacted by duty cycle. For the 1.2kW PFC converter, the input voltage is 230Vac, the output voltage is 400Vdc. During half line cycle, half of the time the duty cycle is larger than 0.5, the other half of the time duty cycle is smaller than 0.5, as shown in Fig. 3.52. For the 6.6kW PFC converter, the input voltage is 240Vac, the output voltage is from 600Vdc to 800Vdc. When output voltage is 600V, most of the time duty cycle is larger than 0.5. When output voltage is 700V or 800V, the duty cycle is always larger than 0.5, as shown in Fig. 3.53. Because of this different duty cycle range, the negative coupled inductor has opposite impact on switching frequency for the two PFC converters. And this proves that the negative coupled inductor is not suitable in this 6.6kW PFC converter.

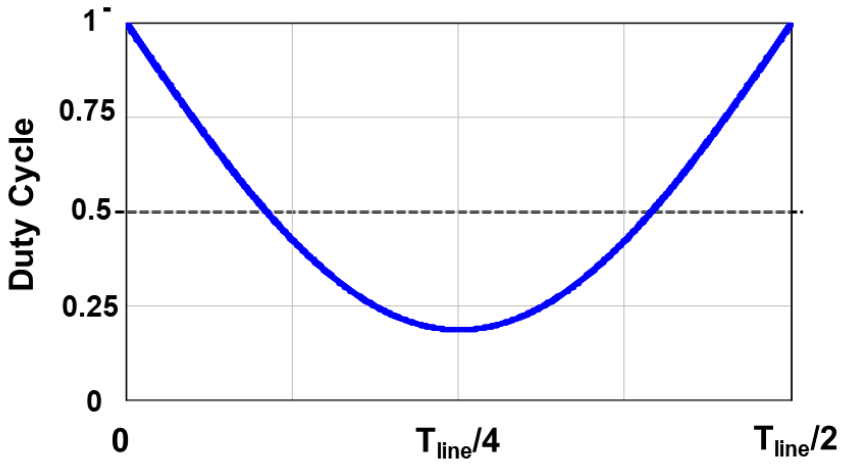


Fig. 3.52 Duty cycle range for 1 kW server power supply

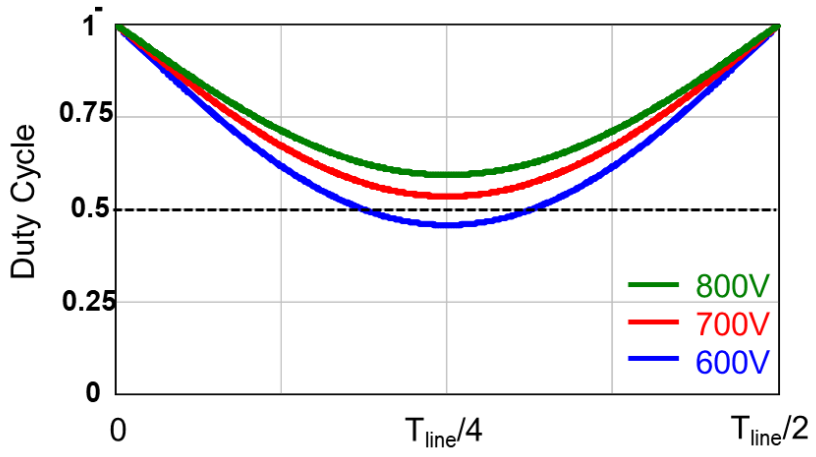


Fig. 3.53 Duty cycle range for 6.6 kW OBC

3.2.3 Positive Coupled Inductor for 6.6kW PFC

Then the positive coupling will be evaluated. Fig. 3.54 shows the positive coupled inductor for PFC converter. Fig. 3.55 shows the inductor structure demonstration. The two inductors L_1 and L_2 are winded on an EI shaped magnetic core. L_1 is on the left leg and L_2 is on the right leg. The red arrows indicate that the terminals of input current. The blue arrows indicate the terminals of output current. The black dash lines are the direction of mutual flux of L_1 and L_2. The green dash

lines are the direction of leakage flux of L_1 and L_2. It can be seen that the flux generated by L_1 and L_2 are same direction. Hence, L_1 and L_2 are positively coupled. Fig. 3.56 shows the typical inductor waveform of positive coupling. It has three equivalent inductance. The expression of these three equivalent inductance is shown in (3-19). L represents the self-inductance of L_1 and L_2. M represents the mutual inductance of L_1 and L_2. When input voltage is high, the duty-cycle is smaller than 0.5, L_{eq1} determines the phase current ripple. Hence, L_{eq1} can be considered as steady state inductance when duty-cycle is smaller than 0.5. When input voltage is low, the duty-cycle is larger than 0.5, L_{eq3} determines the phase current ripple. Hence, L_{eq3} is the steady state inductance when duty-cycle is larger than 0.5.

$$L_{eq1} = \frac{L^2 - M^2}{L + \frac{D}{D'}M}, \qquad L_{eq2} = L + M, \qquad L_{eq3} = \frac{L^2 - M^2}{L + \frac{D'}{D}M} \tag{3-19}$$

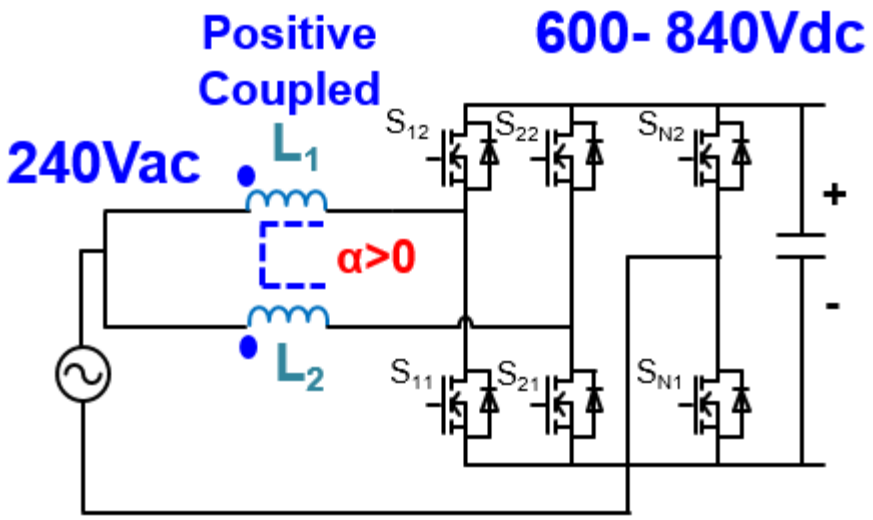


Fig. 3.54 Positive coupled inductor for 6.6kW PFC

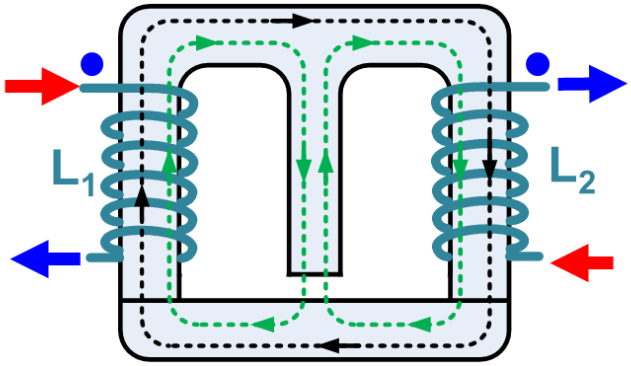


Fig. 3.55 Positive coupled inductor structure demonstration

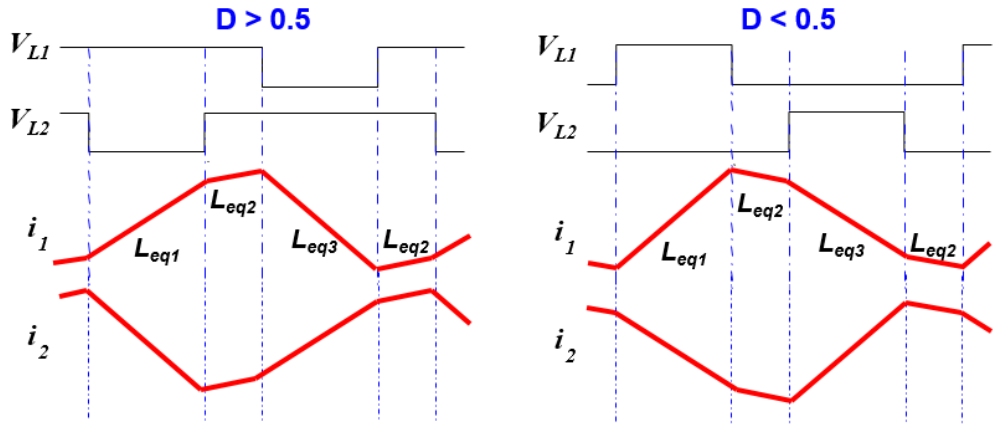


Fig. 3.56 Typical waveforms of positive coupled inductor

Fig. 3.57 shows the steady state inductance variation during a half line cycle for the positive coupled inductor. The dash line represents the non-coupled inductance, which is constant 10uH. The blue, red and green lines represent the steady state inductance with positive coupled inductor for 600V, 700V and 800V output voltage respectively. It can be seen that with the positive coupled inductor, the steady state inductance is higher than non-coupled inductor. Fig. 3.58 shows the switching frequency for positive coupled inductor. The dash lines represent the switching frequency of non-coupled inductor. The solid lines represent the switching frequency of positive coupled inductor. With the higher steady state inductance, the positive coupled inductor has lower switching frequency than the non-coupled inductor. Furthermore, with 700V and 800V output

voltage, the switching frequency is almost constant. Therefore the positive coupling will reduce the switching frequency range and thus reduce switching loss by 14%.

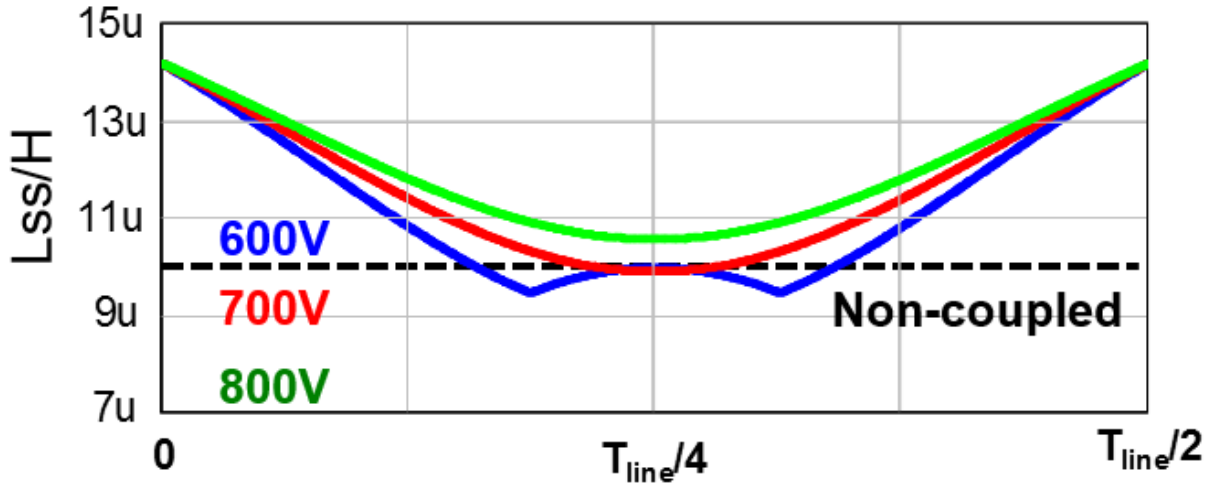


Fig. 3.57 Steady state inductance for 6.6kW PFC with positive coupled inductor

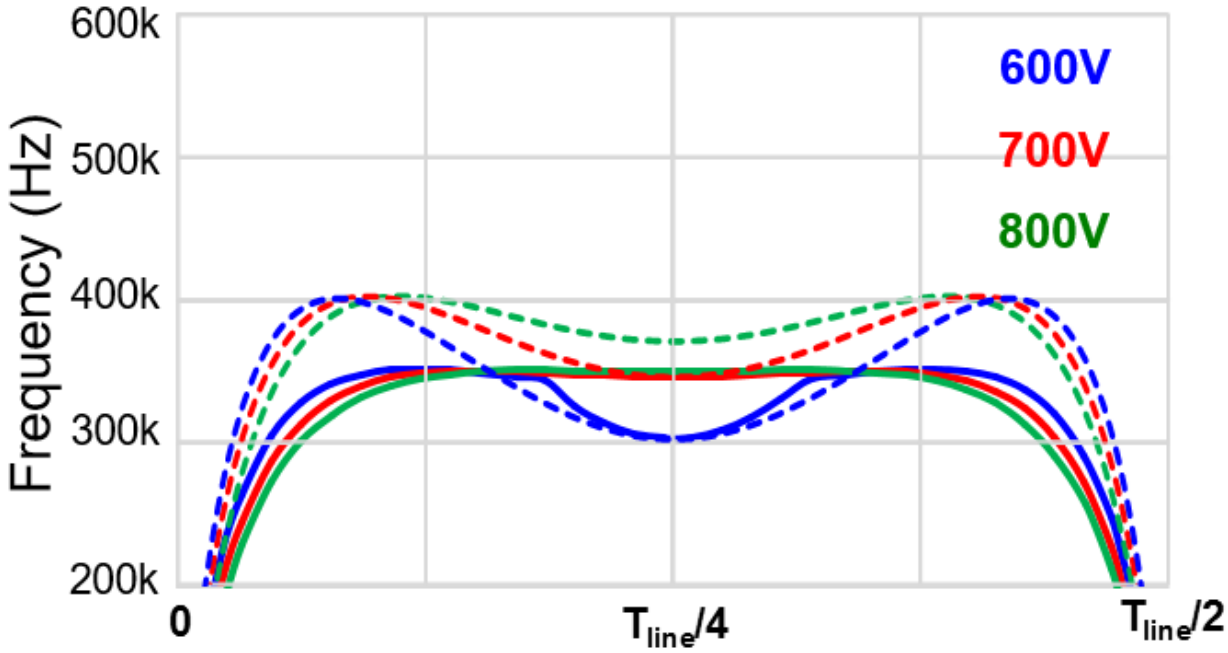


Fig. 3.58 Switching frequency for 6.6kW PFC with positive coupled inductor

3.2.4 PCB Winding Inductor Design

For conventional CRM PFC converter with high current, litz wire inductor is very popular. In CRM operation, the AC current ripple is very large. Litz wire can help reduce the skin effect and proximity effect losses in conductors. Fig. 3.59 shows the litz wire inductors for this 6.6 kW two-phase interleaved totem-pole PFC converter. The inductor is built with PQ 32/30 core with 3F36 material and 825/44 litz wire. The loss breakdown for the litz wire inductor is shown in Table 3-5.

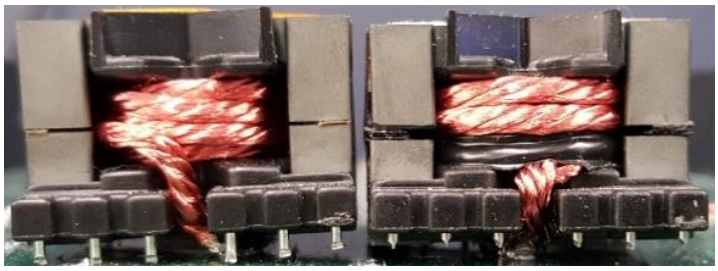


Fig. 3.59 Litz wire inductors for OBC

Table 3-5 Loss breakdown for litz wire inductor

	Winding Loss (W)	Core Loss (W)	Total Loss/W
Litz wire winding inductor	12	13	25

However, the litz wire inductor is bulky requires labor intensive work to assemble. Therefore the tolerance of the inductance is very large and the parasitic control is difficult. It is very difficult to build a coupled inductor with desired inductance value with litz wire. Worse still, it is difficult to achieve good CM noise reduction with balance technique using litz wire inductor. In order to overcome these drawbacks, the PCB winding inductor is a preferred solution.

However, the conventional PCB winding inductor will suffer a lot from the skin effect and proximity effect losses in this high AC current ripple application. As shown in Fig. 3.60, two inductors L_1 and L_2 are on the same EI shaped magnetic core. Therefore, the two inductors are coupled together. Each inductor has six turns in six layer PCB board. L_1 is on the left leg of the magnetic core, L_2 is on the right leg. The loss breakdown for this conventional PCB winding inductor is shown in Table 3-6. It can be seen that the winding loss is more than 10 times higher than litz wire inductor. This is because the PCB winding is a piece of solid copper. For this high frequency, high AC current ripple application, the AC winding loss is very large. Therefore, this design is not applicable in this application.

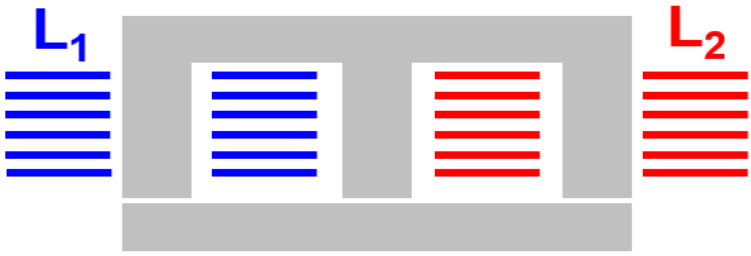


Fig. 3.60 Conventional PCB winding inductor

Table 3-6 Loss breakdown for conventional PCB winding inductor

	Winding Loss (W)	Core Loss (W)	Total Loss/W
Conventional PCB winding inductor	180	17	197

In order to reduce the high AC winding loss, the new PCB winding structure is proposed in Fig. 3.61. Instead of putting all the L_1 and L_2 leg on two separate legs, one layer of L_1 and L_2

swapped position. There is one turn of L_2 on the left leg, and one turn of L_1 on the right leg. With this wingding interleaving method, the magnetic field can be reduced and the skin effect and proximity effect losses can be greatly reduced. Table 3-7 shows the loss breakdown of this proposed PCB winding structure. It can be seen that the winding loss has been greatly reduced. The total loss of this PCB winding inductor now is comparable with the litz wire inductor.

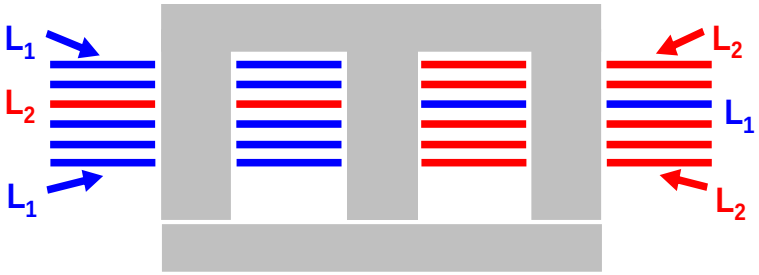


Fig. 3.61 Proposed PCB winding inductor with interleave

Table 3-7 Loss breakdown for proposed PCB winding inductor with interleave

	Winding Loss (W)	Core Loss (W)	Total Loss/W
Proposed PCB winding inductor	24	21	45

3.2.5 Improved PCB Winding Inductor Design

Fig. 3.62 shows the prototype of the 6.6kW on-board battery charger. The upper half is PFC converter, and the lower half is DC/DC converter. The power density of total system is 37W/in^3. It can be seen that both PFC inductor and DC/DC transformer are integrated into PCB motherboard. Thus, all the magnetic components in this converter are built by PCB winding. Thus, the converter can achieve fully automated manufacture.

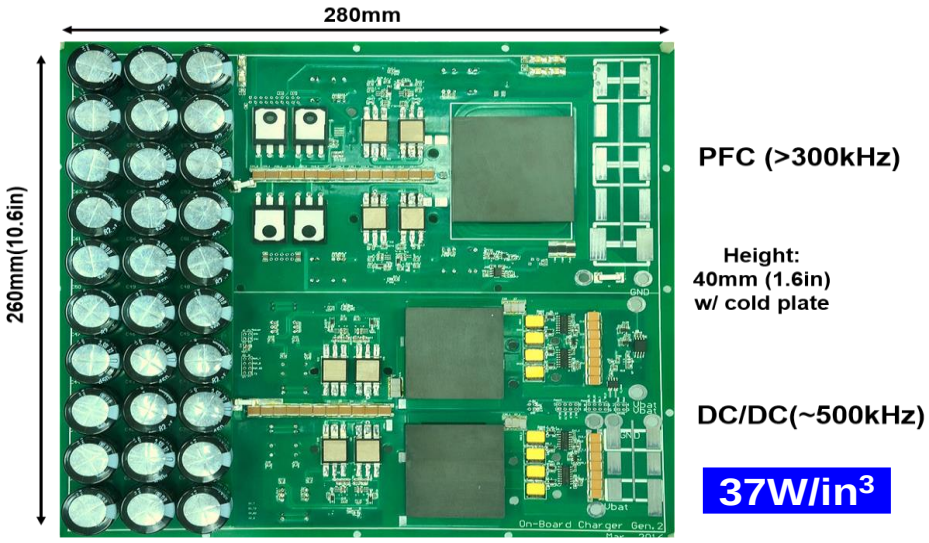


Fig. 3.62 Prototype of 6.6kW on-board battery charger

The efficiency of PFC converter is measured, as shown in Fig. 3.63. The blue curve is for litz wire inductor version. The green dash line is the estimated converter with PCB winding inductor. However, the measured efficiency with PCB winding inductor is shown in red line. It is much lower than the estimation.

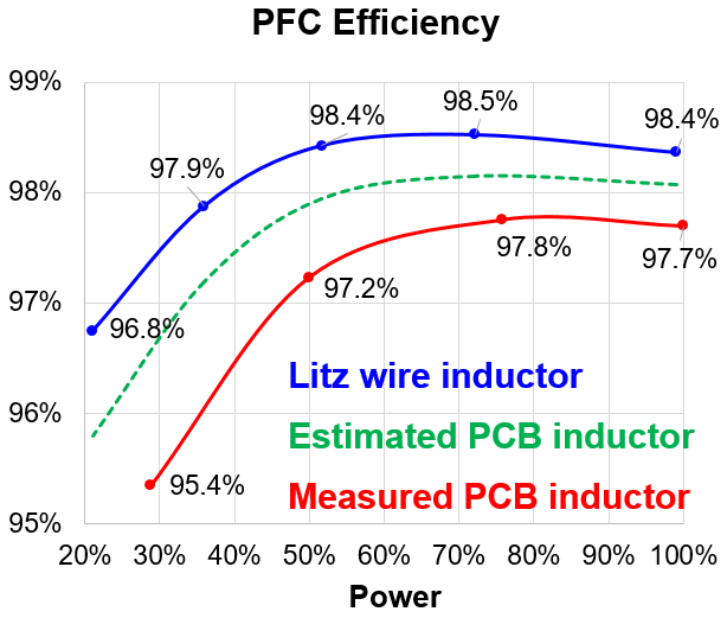


Fig. 3.63 Measured PFC converter efficiency

In order to find out the reason for extra loss, detailed waveforms are shown in Fig. 3.64. From the waveform it can be seen that there are spikes and ringing in the inductor current waveform. This is because of the equivalent parallel capacitor (EPC) of the inductor. In the PCB winding inductor, the windings have large overlapping area. Thus the EPC of PCB winding inductor is much larger than traditional litz wire inductor. During the switching transition, the dv/dt on the switch node will introduce displacement current through the EPC of inductor. Large EPC will lead to large current spike. The ringing current will go through the inductor and SiC devices to generate loss, as shown in Fig. 3.65.

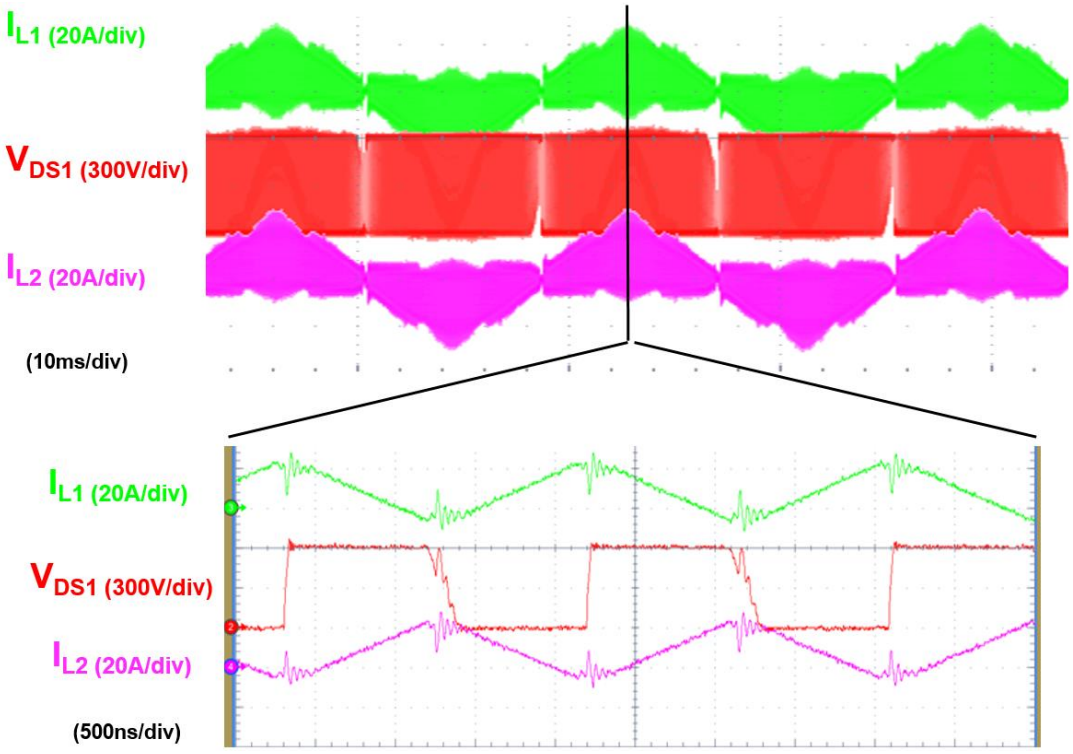


Fig. 3.64 Experimental waveforms of 6.6kW PFC converter

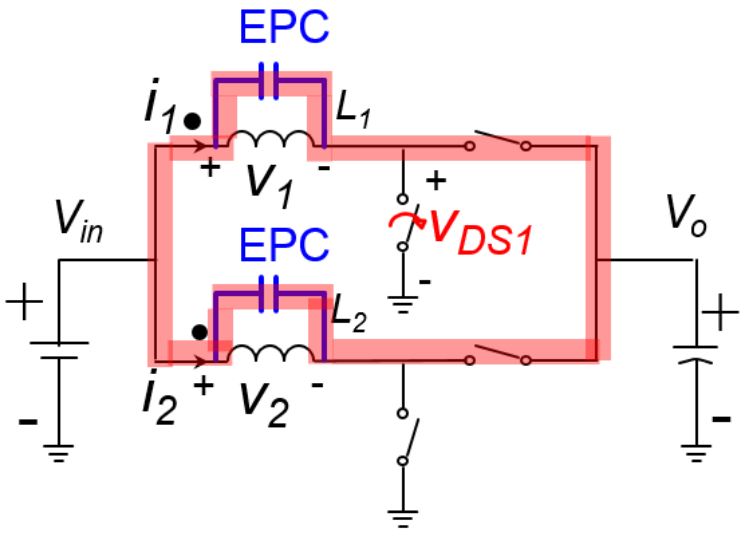


Fig. 3.65 Path of current spikes and ringing

In order to reduce the loss generated by EPC, the inductor design needs to be improved. Fig. 3.66 shows the inductor design parameters, winding width “a” and core length “b”. In the original design, the ringing loss generated by EPC was not considered. In this design the EPC loss will be taken into account.

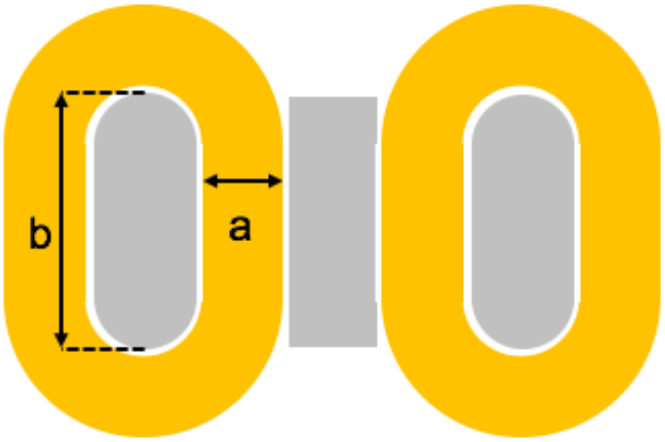


Fig. 3.66 Inductor optimization parameters

The inductor loss breakdown for different combination of parameter a and b is shown in Fig. 3.67. The contour of total inductor loss and footprint is shown in Fig. 3.68. From this figure, the

optimized design point can be closed. Table 3-8 shows the loss breakdown for the optimized inductor design. It can reduce the total inductor loss by 10W.

Table 3-8 Loss breakdown for optimized inductor design

	Winding Loss (W)	Core Loss (W)	Ringing Loss (W)	Total Loss/W
Optimized Design	29	27	3	59
Original Design	24	21	36	71

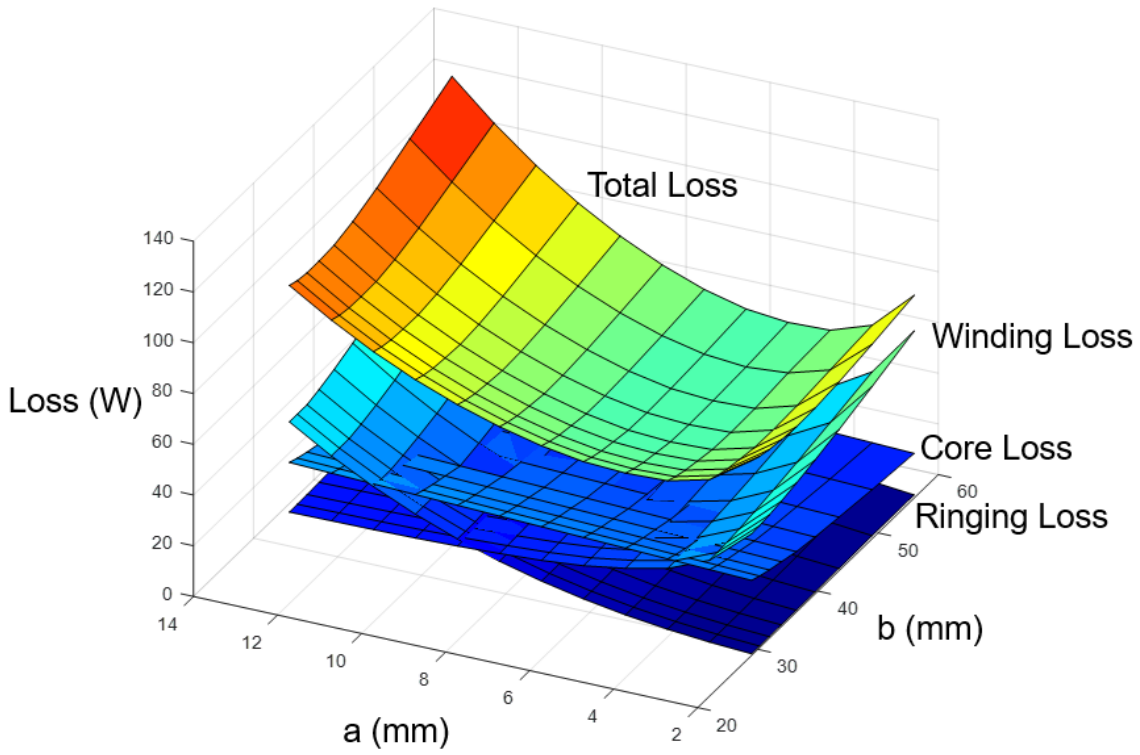


Fig. 3.67 Inductor loss breakdown for inductor design

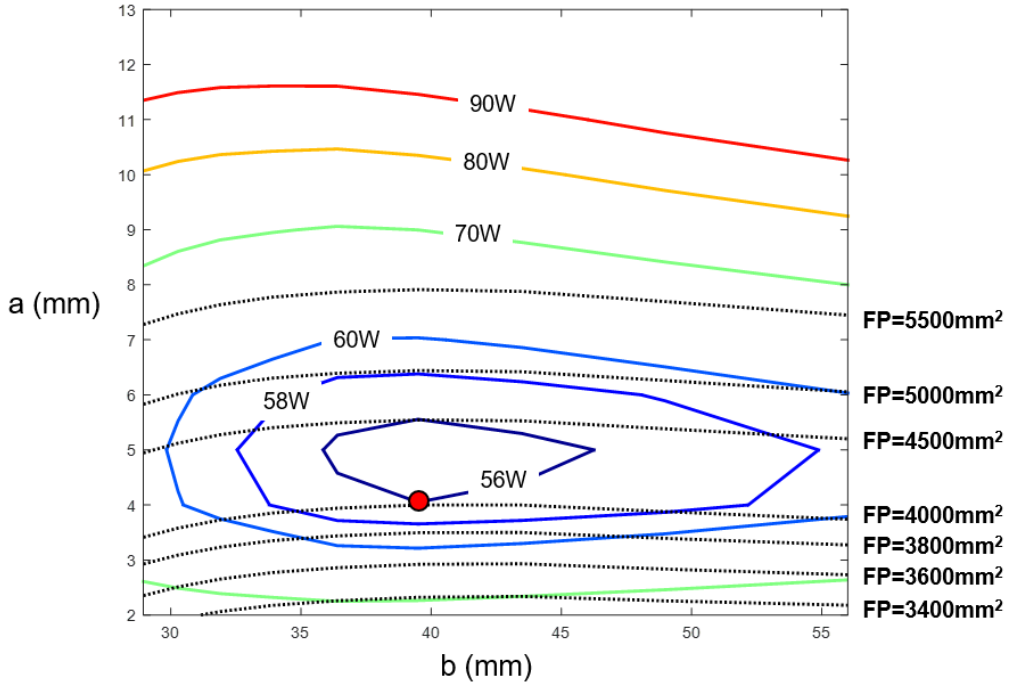


Fig. 3.68 Contour of total loss and footprint

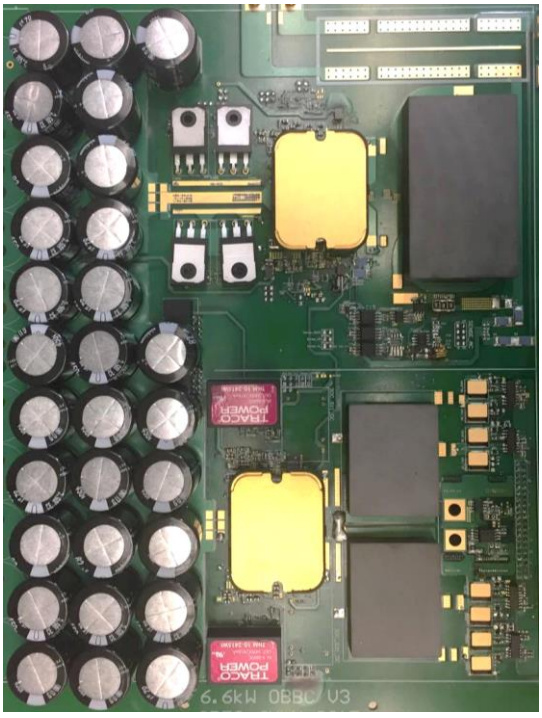


Fig. 3.69 Prototype Gen. 2 of 6.6kW on-board battery charger

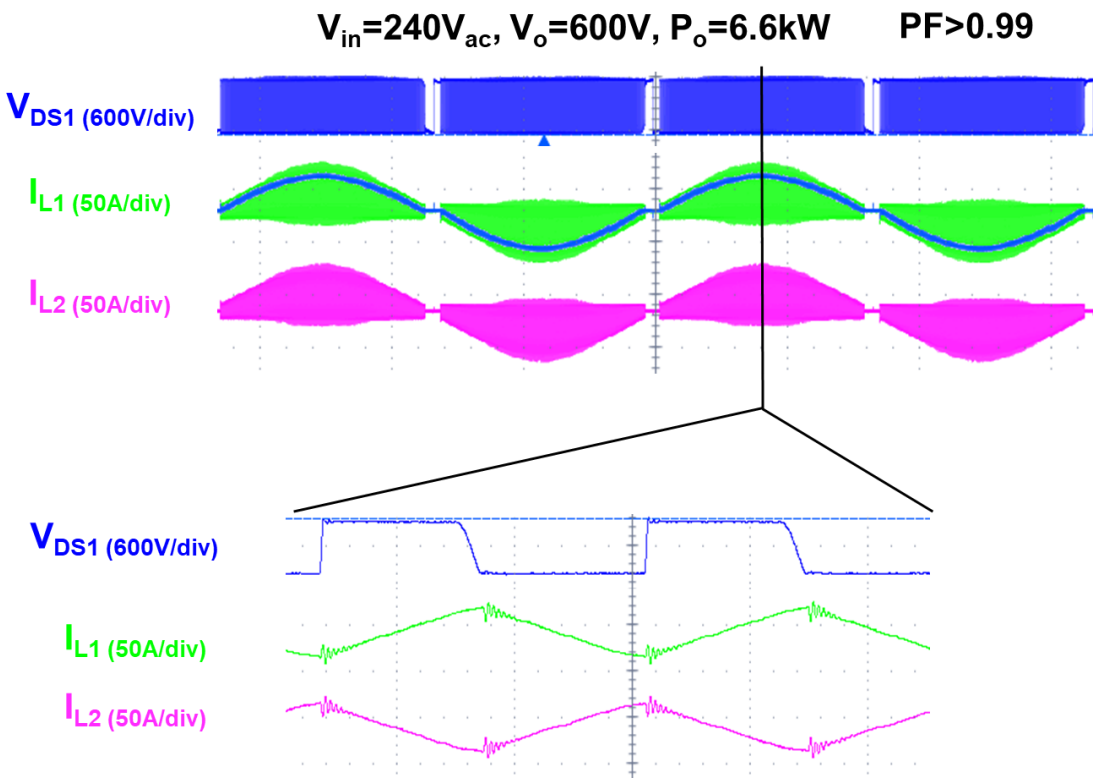


Fig. 3.70 Experimental waveforms of Gen. 2 6.6kW PFC converter

The Gen. 2 hardware is shown in Fig. 3.69. The experimental waveforms are shown in Fig. 3.70. It can be seen that the current spike and ringing has been greatly reduced. The efficiency is shown in Fig. 3.71. With the new PCB winding inductor design, the efficiency of PCB converter is improved. The peak efficiency is above 98%, which is much higher than the industry products.

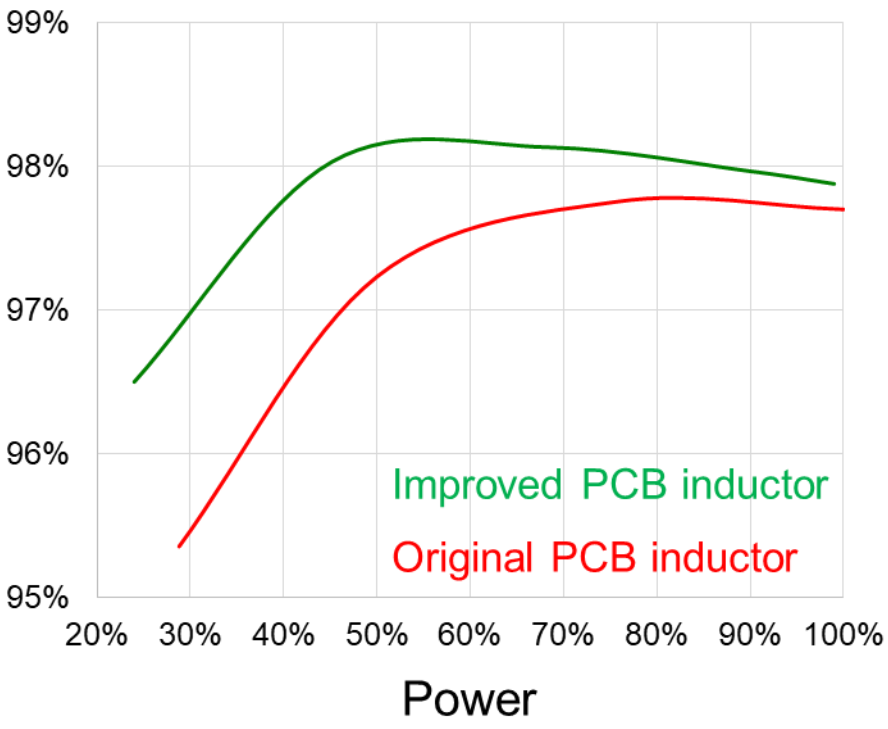


Fig. 3.71 Improved efficiency of Gen. 2 hardware

3.2.6 Balance Technique to Reduce CM Noise

Similar as previous analysis, balance technique can be applied to this PFC converter to reduce CM noise, as shown in Fig. 3.72. Fig. 3.73 shows the CM noise model of positive coupled inductor with balance. The two switch bridges are modeled as two noise sources. C_b is the parasitic capacitance between output trace and ground. C_d is the drain-to-ground capacitance. In order to achieve balance, L_3 and L_4 are applied to the circuit. An external capacitor C_{add} is applied to the circuit to obtain more freedom in design the balance circuit.

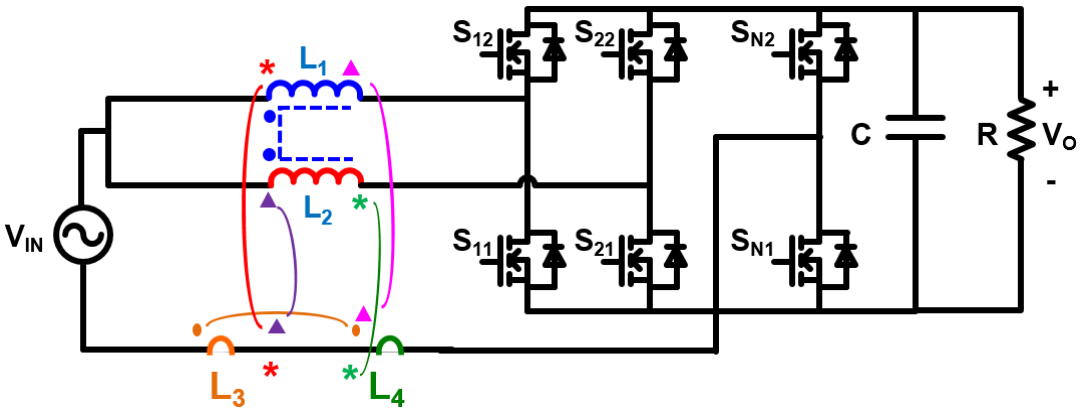


Fig. 3.72 Balance technique for positive coupled inductor

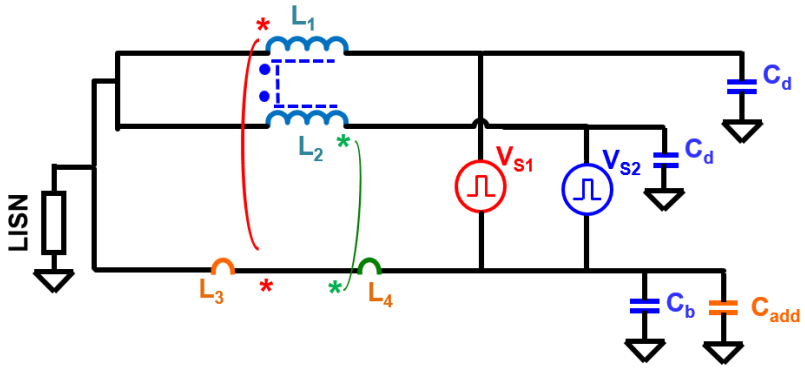


Fig. 3.73 CM noise model of balanced PFC converter

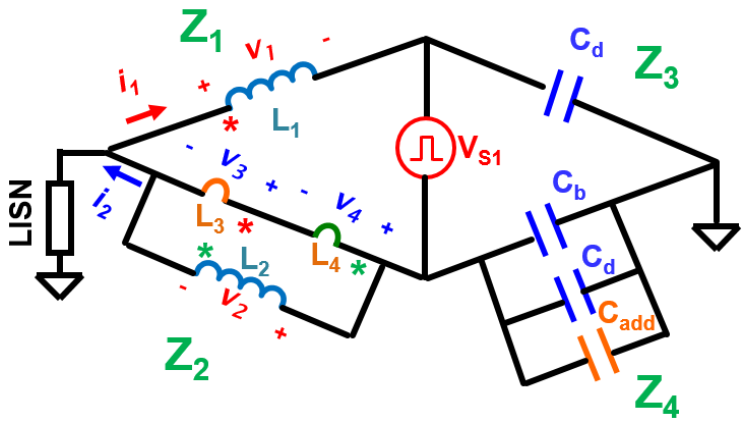


Fig. 3.74 Effect of noise source V_{S1}

Superposition theory can be applied to this circuit. As shown in Fig. 3.74, only V_{S1} is considered in the circuit, V_{S2} is treated as short circuit. The balance condition for this circuit is

shown in (3-20). Still, the ratio of Z_1/Z_2 needs to be calculated first. It is assumed that L_1 and L_3 are perfectly coupled, and L_2 and L_4 are perfectly coupled. The number of turns of L_1 and L_2 is N_1. The number of turns of L_3 and L_4 is N_2. Thus, we have the equations shown in (3-21). Then the ratio of Z_1/Z_2 can be derived as (3-22). Thus, the balance condition for source V_1 is (3-23). Similarly, the balance condition for noise source V_{N2} is also (3-23). The CM noise of this PFC converter can be minimized as long as this balance condition is achieved.

$$\frac{Z_1}{Z_2} = \frac{C_d + C_b + C_{add}}{C_d} \tag{3-20}$$

$$\begin{cases} \dfrac{V_1}{V_3} = \dfrac{N_1}{N_2} \\ \dfrac{V_2}{V_4} = -\dfrac{N_1}{N_2} \\ V_3 + V_4 = V_2 \\ i_1 = i_2 \end{cases} \tag{3-21}$$

$$\frac{Z_1}{Z_2} = \frac{V_1/i_1}{V_2/i_2} = \frac{N_1 + N_2}{N_2} \tag{3-22}$$

$$\frac{N_1}{N_2} = \frac{C_b + C_{add}}{C_d} \tag{3-23}$$

The positive coupled inductor can also be integrated into PCB winding. The inductor structure is shown in Fig. 3.75. Based on the experience of previous design, the interleaved winding structure is used to help reduce winding loss. In this inductor design, 6-layer PCB board is used and the last layer serves as the balance inductor.

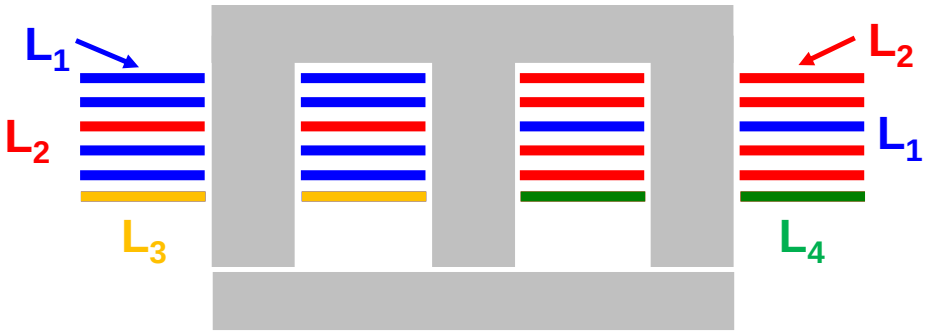


Fig. 3.75 PCB winding positive coupled inductor with balance

Fig. 3.76 shows the CM noise reduction by using balance technique. It can be seen that there is 23dB CM noise reduction with balance. This can greatly help the EMI filter design.

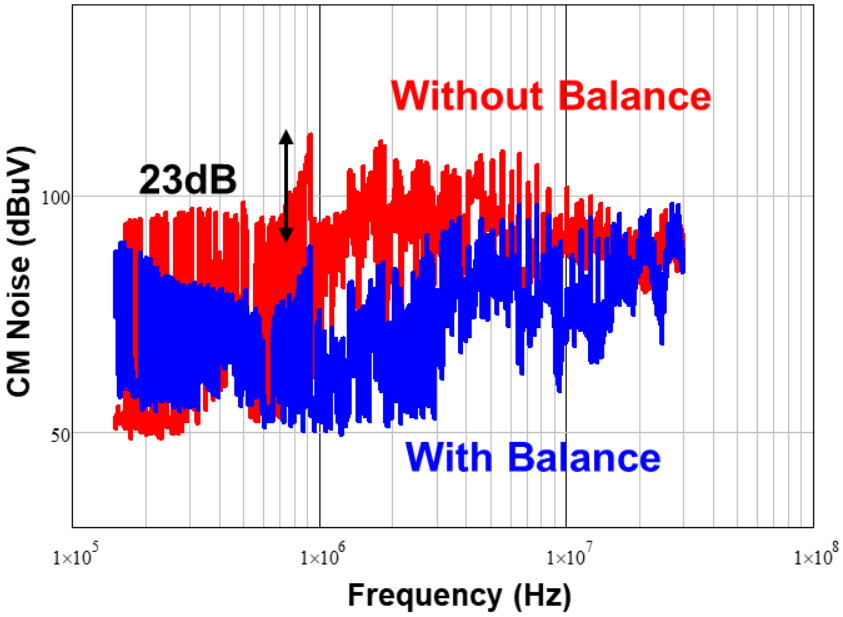


Fig. 3.76 CM noise reduction by balance technique

3.3 Conclusions

In this chapter, the proposed PCB winding inductor is demonstrated for both 1 kW server power supply and 6.6 kW on-board battery charger. For the 1 kW server power supply, the negative

coupled inductor is applied. The negative coupled inductor can help reduce the switching frequency to reduce switching loss. In addition, the coupled inductor can help achieve ZVS to reduce turn-on loss. In order to integrate the inductor into PCB winding, a novel inductor structure is proposed. The inductor winding is interleaved to reduce the high AC winding loss at high switching frequency. In order to avoid the fringing flux, the last three layers of the winding is specially designed. The balance technique is also applied to reduce CM noise. With PCB winding, the balance technique is easy to implement and the parasitic is easy to control. The balance technique can help reduce the CM noise by 20 dB. The inductor is integrated in a 6-layer mother board. The PFC converter can achieve 99% efficiency with 700 W/in^3 power density. This is the first time that the PCB winding inductor can achieve same efficiency as litz wire inductor at high switching frequency and high AC current ripple.

For the 6.6 kW OBC, the difference between negative coupled inductor and positive coupled inductor is analyzed. The positive coupled inductor is applied to reduce switching frequency. Furthermore, the coupled inductor can help further reduce input current ripple to reduce DM noise of the PFC converter. The PCB winding inductor is also implemented. Due to the large inductor size, the EPC of the inductor is very large and introduces extra loss. By redesigning this inductor, the EPC is greatly reduced and efficiency of the converter is improved. Balance technique is applied to this PFC converter and can reduce 23 dB CM noise. However, it can be seen that in this 6.6 kW system, the PCB winding inductor does not have good efficiency as litz wire inductor. This is because of large current and limited 6-layer board. In order to further improve the inductor efficiency, more PCB layers can be applied to reduce the winding loss of PCB winding inductor.

Chapter 4. EMI Filter Design Considerations

In today's power electronics area, the switch mode power supplies will generate a lot of high frequency noises. In order to prevent those noises interfere other components, the electromagnetic interference (EMI) filter are widely used in power converters.

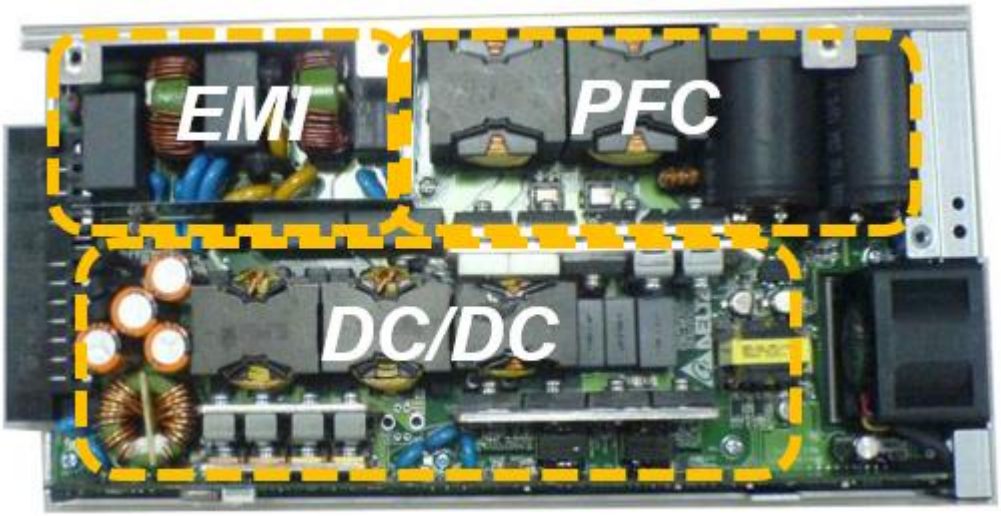


Fig. 4.1 State-of-the-art server power supply

Fig. 4.1 shows a typical server power supply. It has three major parts: the EMI filter, the PFC converter and DC-DC converter. It can be seen that the EMI filter occupies about 1/4 to 1/3 total volume and has many components. Traditionally, due to the low switching frequency and high EMI noise, two-stage EMI filter is used to attenuate EMI noise, as shown in Fig. 4.2 It requires three x-capacitors, four y-capacitors and two inductors. Sometimes more inductors are used for better attenuation. It is easily noticed that the two-stage EMI filter is bulky and more expensive. In a traditional power supply, the EMI filter occupies 1/3 of the total volume. The two-stage EMI filter limits the power density of the power supply.

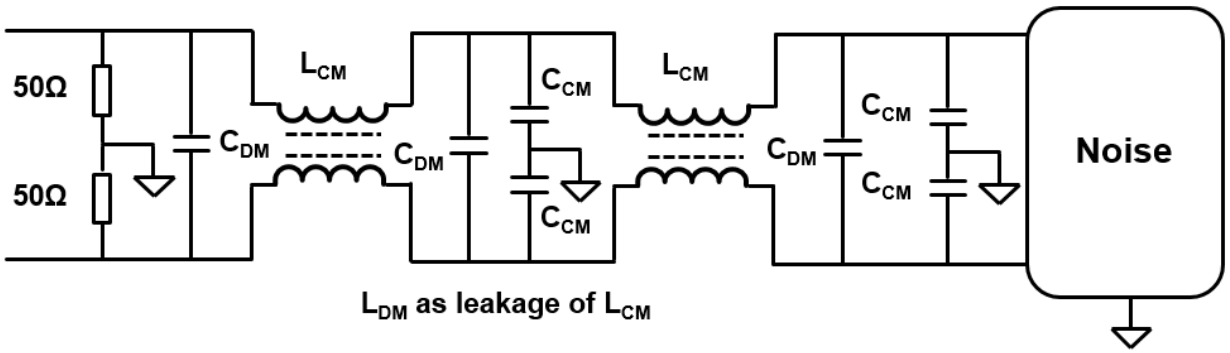
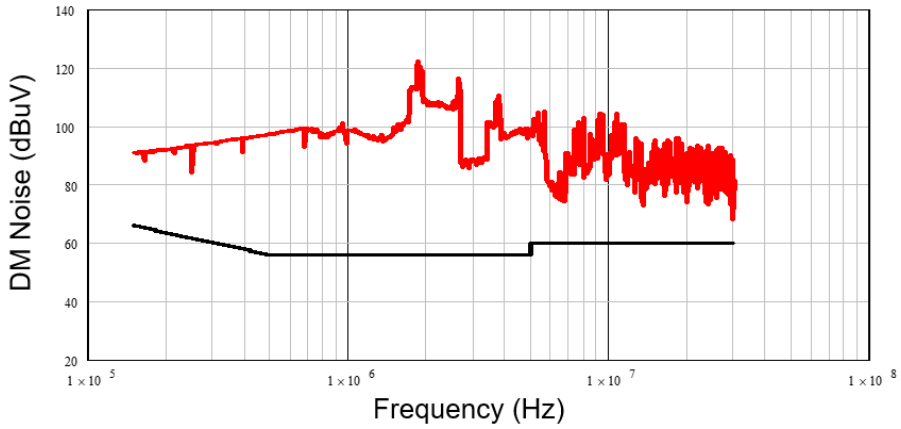


Fig. 4.2 Two-stage EMI filter structure

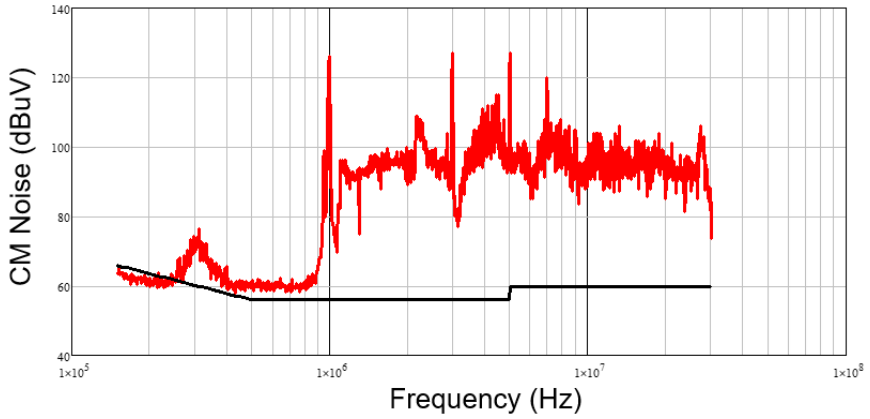
In today's power electronics products, people are always pursuing high efficiency, high power density and low cost. With the development of GaN devices, the switching frequency of power converters can be pushed 10 times higher. Therefore, the power density of power converters can be increased 5 to 10 times higher than traditional Si based design [24][36][48]. As demonstrated in Chapter 3, a high efficiency, high density 1 kW PFC converter is demonstrated. The peak efficiency is above 99% and the power density is 350W/in^3. In Chapter 2, a 1 kW DC-DC converter is demonstrated with 97% efficiency and 700W/in^3 power density. Those two converters can form a high efficiency, high density server power supply. Therefore, the traditional two-stage EMI filter is not suitable in this high density power converter design. A simpler, compact one-stage EMI filter is needed.

However, extra efforts are needed in order to use the one stage EMI filter to achieve the required attenuation. Fig. 4.3 (a) shows the measurement DM noise of this 1 kW server power supply. It can be seen that with two-phase interleaved structure, the fundamental frequency harmonic is canceled. The first peak is at 2 MHz. This can help increase the filter corner frequency and reduce filter size. Fig. 4.3 (b) shows the CM noise measurement result. It can be seen that the CM noise is very high. In order to reduce CM noise, several CM noise reduction technique is introduced in previous chapters. In Chapter 2, the shielding technique is applied to reduce the CM

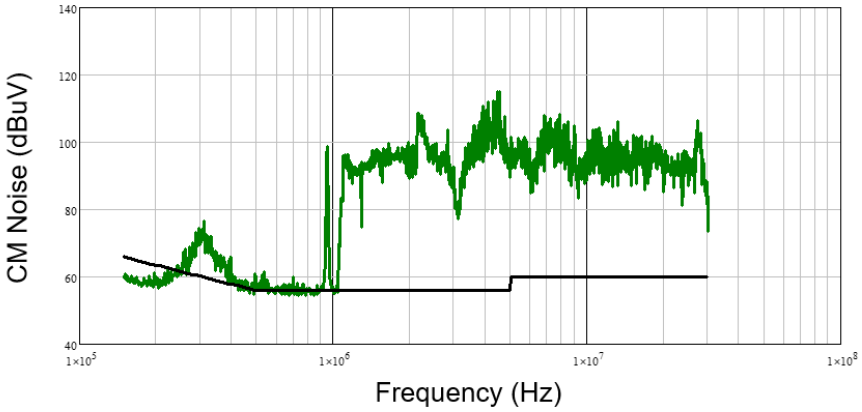
noise of DC-DC converter. As shown in Fig. 4.3 (c), with shielding technique, the CM noise of DC-DC converter has been greatly reduced. However, the remaining CM noise is still high. In Chapter 3, interleaving and balance technique is used to reduce the EMI noise of PFC converter. As shown in Fig. 4.3 (d), with balance technique, the CM noise can be greatly reduced. These EMI noise reduction techniques makes the idea of one-stage EMI filter become possible.



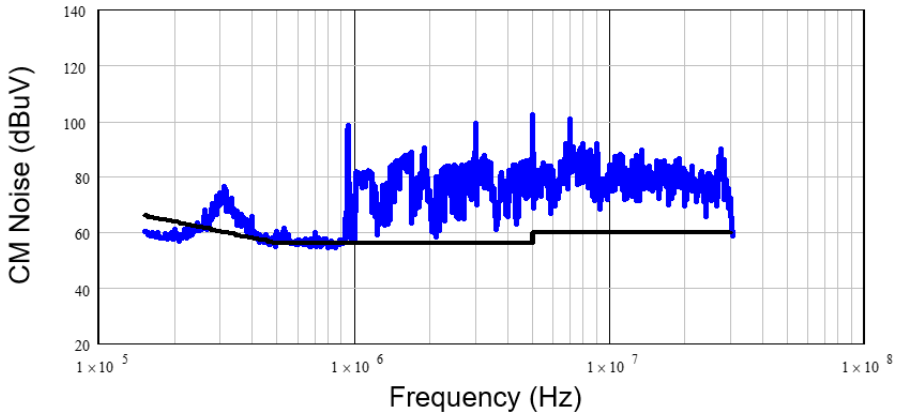
(a) DM noise measurement result



(b) CM noise measurement result



(c) CM noise with shielding technique



(d) CM noise with shielding and balance technique

Fig. 4.3 EMI noise measurement result for 1 kW server power supply

Theoretically, the EMI filter is a low-pass filter. The self parasitics and mutual coupling will impact the filter performance. Many researches has been done to reduce the self parasitics and mutual coupling [58]-[73]. In [67], the method of reducing mutual coupling between inductor and capacitor is analyzed. Self parasitics of capacitor is analyzed in [68]. In [69], the mutual coupling between two capacitors are analyzed. However, those methods is seldom used in the two-stage EMI filter. Because those parasitics and mutual coupling will not severely impact the performance

of two-stage EMI filter. However, in the one-stage EMI filter, the parasitics and mutual coupling will dominating the high frequency performance.

In this chapter, the self parasitics and mutual coupling of one-stage EMI filter is analyzed. The methods of reduction of self parasitics and mutual coupling is demonstrated. A compact and effective single stage EMI filter design is provided.

4.1 Single Stage EMI Filter

Fig. 4.4 shows the topology of one-stage EMI filter. It has two x-capacitors, two y-capacitors and one CM inductor. The leakage inductance of CM inductor will serve as differential mode (DM) inductor. Comparing with the two-stage EMI filter design, the one-stage EMI filter is more compact and simple. The designed parameter of this single stage EMI filter is: L_{DM} = 40 uH, C_X = 680 nF, L_{CM} = 1.5 mH, C_Y = 3.6 nF.

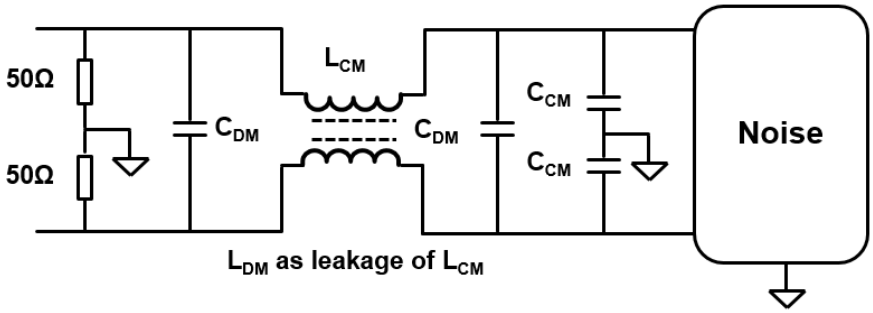
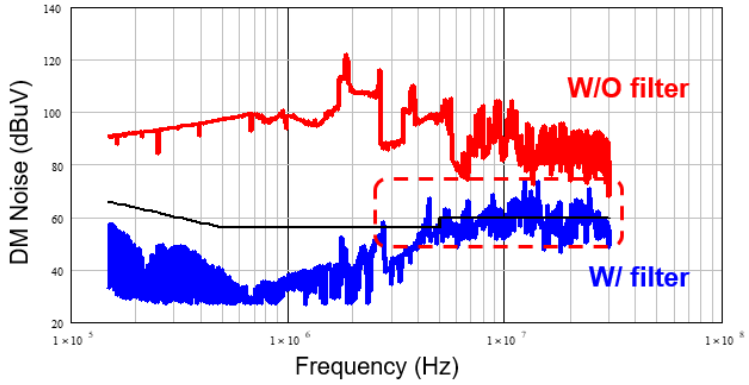
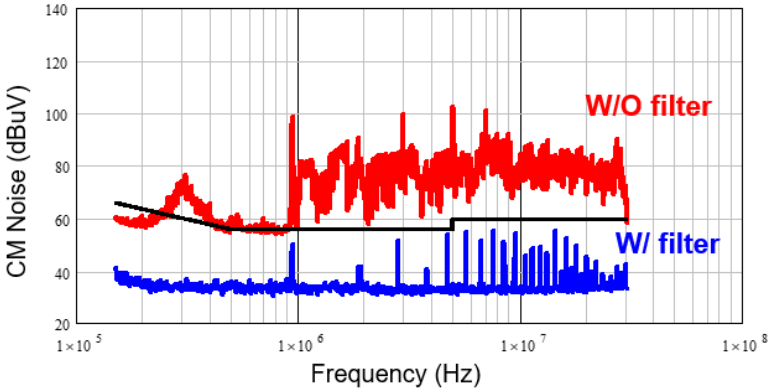


Fig. 4.4 One-stage EMI filter structure

The measured EMI noise with the single-stage EMI filter is shown in Fig. 4.5. It can be seen that the CM noise can pass the standard. At low frequency, the DM noise can pass the standard. However, the DM noise exceeds the standard at high frequency. This means that the preliminary design of DM filter needs to be improved.



(a) DM noise with single stage EMI filter



(b) CM noise with single stage EMI filter

Fig. 4.5 EMI noise measurement results

In the one-stage EMI filter, the leakage inductance of CM inductor serves as the DM inductor. The equivalent circuit for DM and CM filters are shown in Fig. 4.6 and Fig. 4.7. Two CM capacitors are in series for DM noise, so the capacitance is only one half of the single capacitor. Two DM inductors are in parallel for CM noise, so the equivalent inductance is only half of one DM inductance. DM capacitors work like balance capacitors for CM noise. CM inductor is like a short circuit for DM noise because the magnetic fluxes generated by the DM current in two coupled windings are cancelled. Because the CM noise can pass the standard, this chapter focuses on the DM filter.

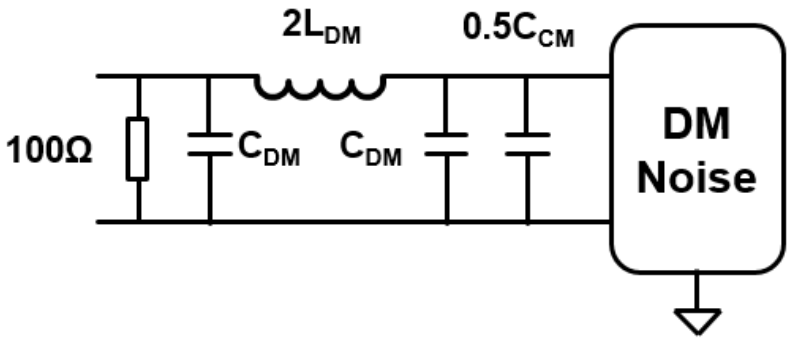


Fig. 4.6 Equivalent circuit for DM filter

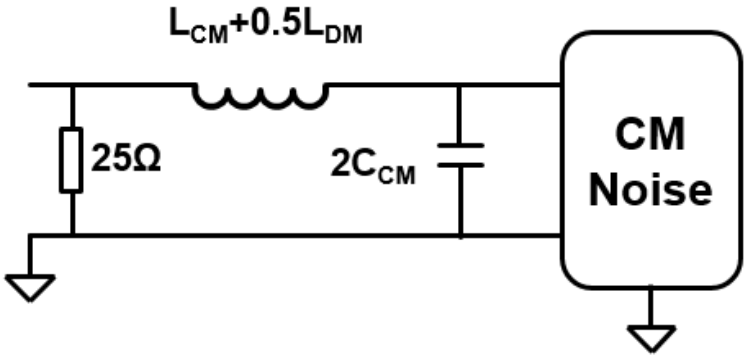


Fig. 4.7 Equivalent circuit for CM filter

4.2 Parasitic of DM Filter

Fig. 4.8 shows the insertion voltage gain for the ideal DM filter. Ideally, the one-stage DM filter serves as a low-pass filter. After the corner frequency, the attenuation is 60dB/dec. However, the real DM filter will not work like the ideal case. There are self-parasitics and mutual parasitics to impact the filter performance.

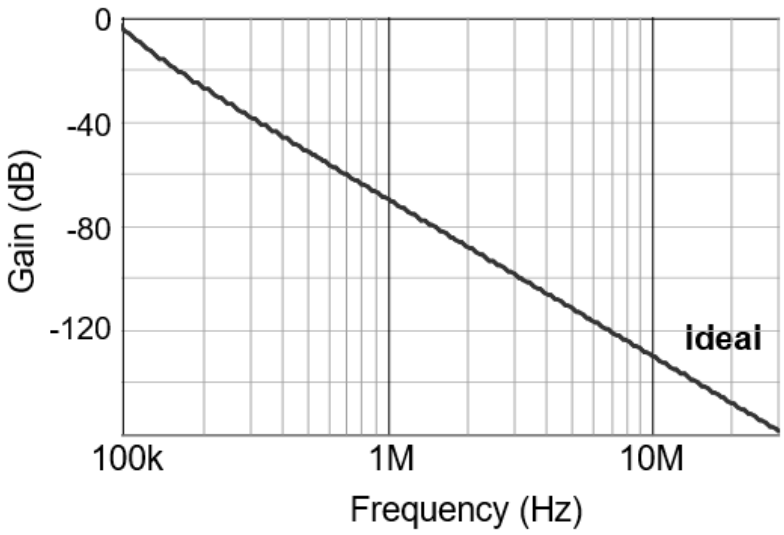


Fig. 4.8 Insertion voltage gain for ideal DM filter

Fig. 4.9 shows the DM filter with self parasitics. For the inductor, there are equivalent parallel capacitance (EPC) and equivalent parallel resistance (EPR). For the capacitor, there are equivalent series inductance (ESL) and equivalent series resistance (ESR). With those self parasitics, the filter performance on high frequency will be changed.

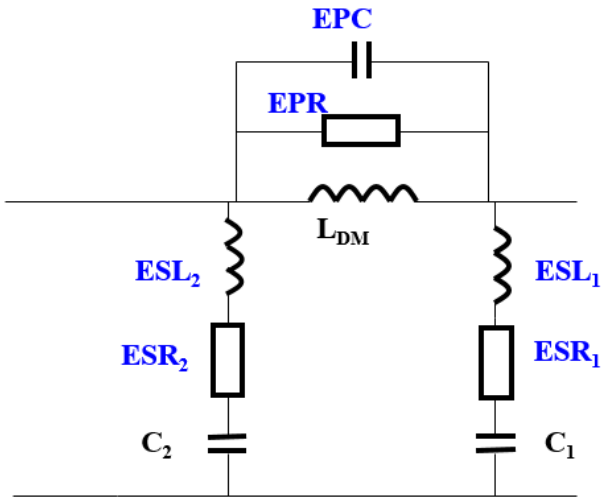


Fig. 4.9 DM filter with self parasitics

Besides the self parasitics, the filter will also be impacted by mutual parasitics. Fig. 4.10 shows the measured insertion voltage gain for the DM filter. It can be seen that the filter has much less attenuation on the high frequency. Fig. 4.11 shows the DM filter with self and mutual parasitics. M_1 and M_2 are mutual coupling between inductor and capacitor. M_3 is the mutual coupling between two capacitors. With such bad high frequency performance, the filter cannot achieve the required attenuation. Therefore, the reduction of self parasitics and mutual couplings is critical in the one-stage EMI filter design.

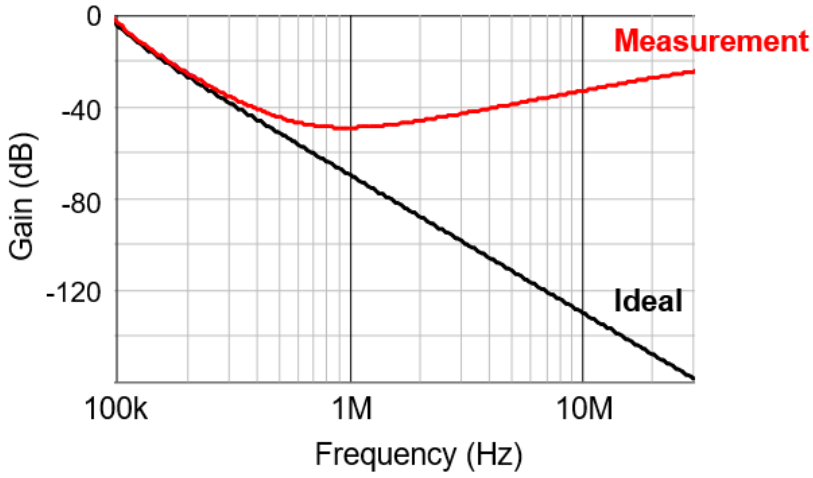


Fig. 4.10 Insertion voltage gain for actual DM filter

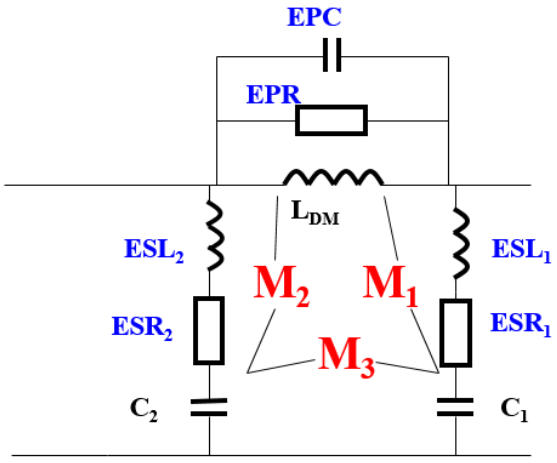


Fig. 4.11 DM filter with self and mutual parasitics

4.3 Near-field Analysis for Mutual Parasitic Cancellation

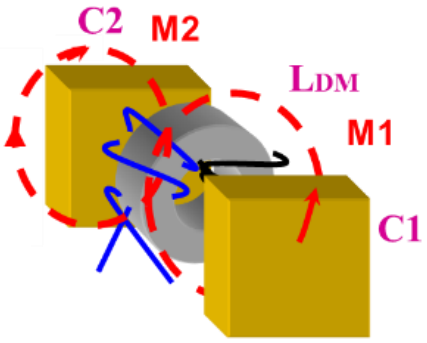


Fig. 4.12 Mutual coupling between inductor and capacitor

Among all the mutual couplings discussed in the previous section, the most important coupling is M_1 and M_2, which are the mutual coupling between inductor and capacitor. As shown in Fig. 4.12. For a compact EMI filter design, the inductor and capacitor are placed close to each other. This makes the near field coupling between inductor and capacitor very strong. In [63], the near field measurement method is used to analyze the DM inductor. The measurement setup is shown in Fig. 11. The Tektronix AFG3102 signal generator provides the sine wave signal with certain frequency. The signal is then go into the inductor through the 25W power amplifier. The near field probe is placed 5 mm above the inductor and the inductor is placed on a XY table. With the moving of XY table, the flux on the surface will be measured in X, Y and Z directions. 10 by 10 points is measured in this surface to visualize the near field flux of the inductor. The scope is used to monitor the flux amplitude measured by the near field probe.

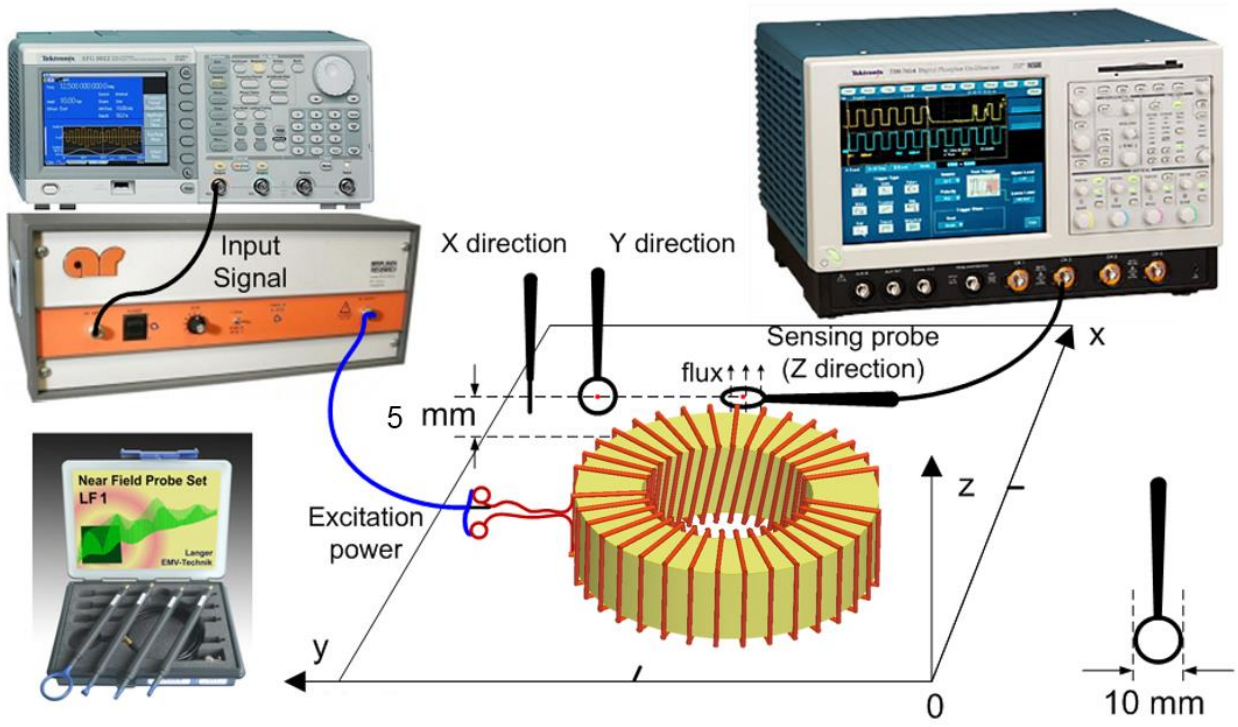
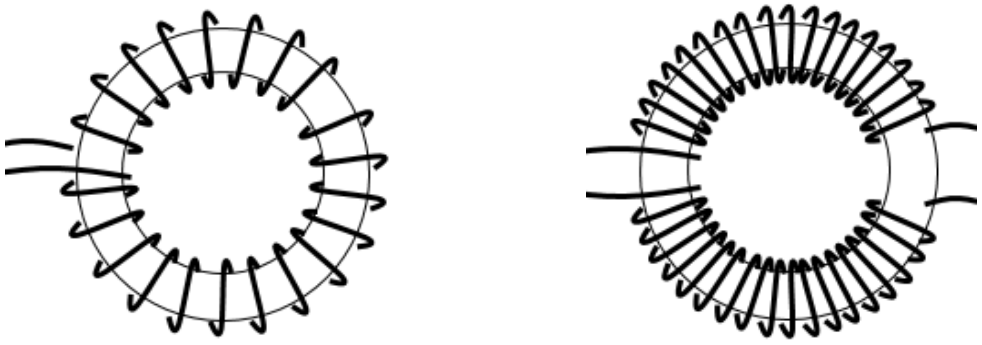


Fig. 4.13 Near-field flux measurement setup

In this work, same measurement method is used to measure the DM flux of a CM inductor. For the DM inductor, the windings are evenly distributed on the magnetic core, as shown in Fig. 4.14 (a). However, for the CM inductor, the windings are divided into two groups, as shown in Fig. 4.14 (b). This makes the CM inductor has different DM near field flux with the DM inductor.



(a) DM inductor structure (b) CM inductor structure

Fig. 4.14 DM inductor structure and CM inductor structure

The measurement result is shown below. First the excitation frequency is 1 MHz, which is a low frequency for this EMI filter inductor. Fig. 4.15 (a), (b) and (c) shows the measurement results in X, Y and Z directions. The X and Y direction measurement result can be combines as XY plane ($\sqrt{x^2+y^2}$), as shown in Fig. 4.15 (d). Because the winding is divided into two groups, the field shows two poles. The flux is going from one pole to another pole. The Y direction shows the maximum value at the center area. This matches out expectation. Fig. 4.16 shows the demonstration of flux flow direction.

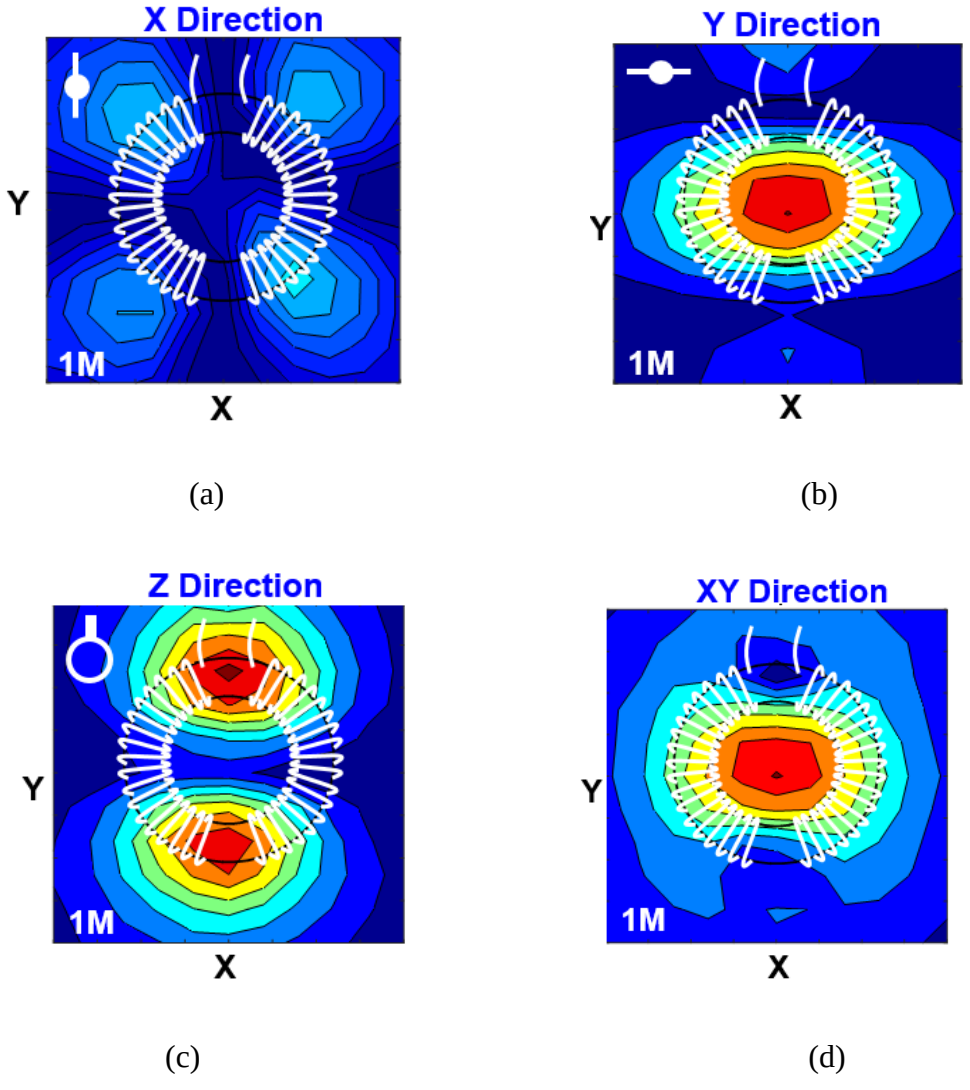


Fig. 4.15 Near-field flux measured with 1MHz excitation

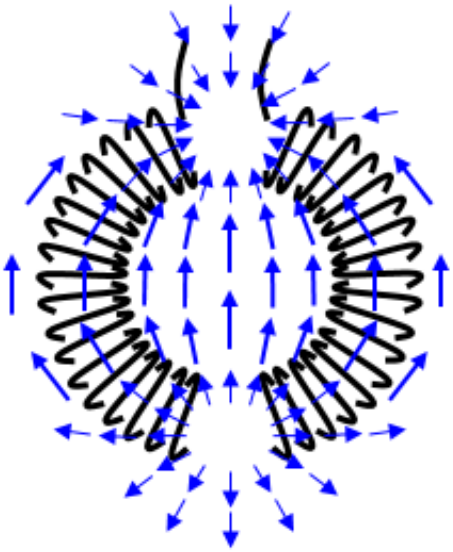
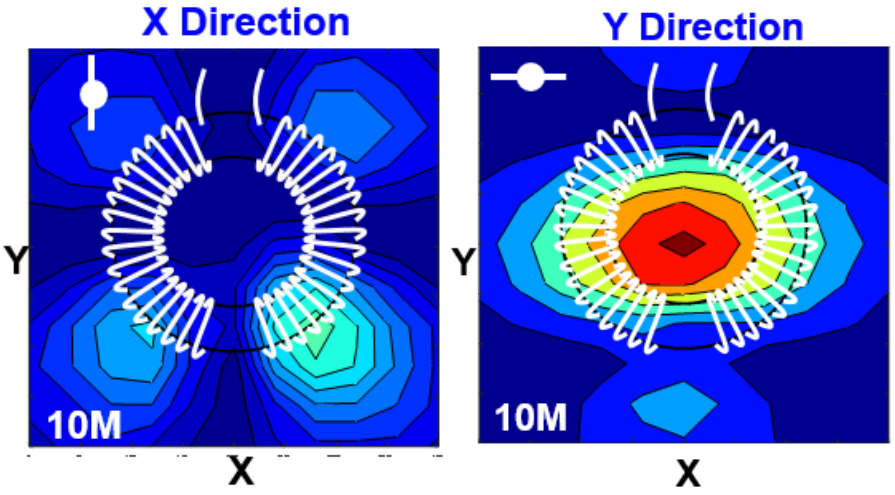


Fig. 4.16 Flux flow direction of 1 MHz excitation

Then, the excitation frequency is increased to 10 MHz. The measurement result is shown in Fig. 4.17. There is not much difference between the 10 MHz result and 1 MHz result. However, it is notices that the flux in one pole becomes weaker. The flux flow direction is shown in Fig. 4.18. The flux still flows from one pole to the other pole.



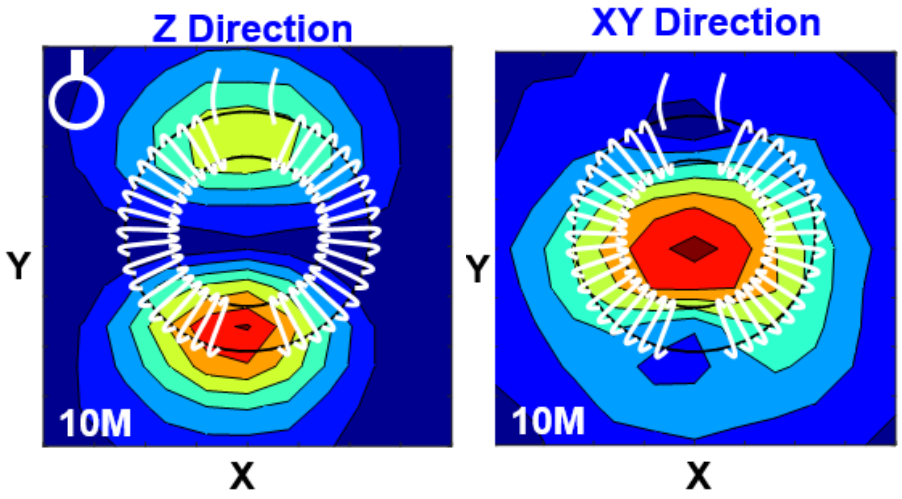


Fig. 4.17 Near field measurement result of 10 MHz

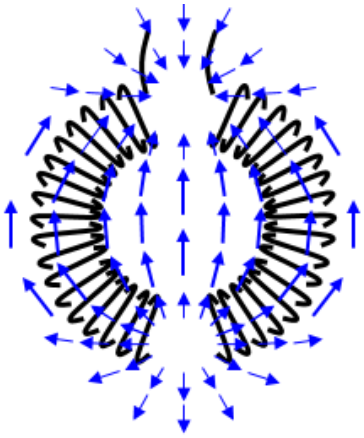


Fig. 4.18 Flux flow direction of 10 MHz excitation

Next, the excitation frequency is set to 15 MHz. The measurement result is shown in Fig. 4.19. Comparing with the 1 MHz and 10 MHz result, at 15 MHz, the pole on top becomes very weak. Fig. 4.20 shows the flux flow direction. The flux in more evenly distributed at top.

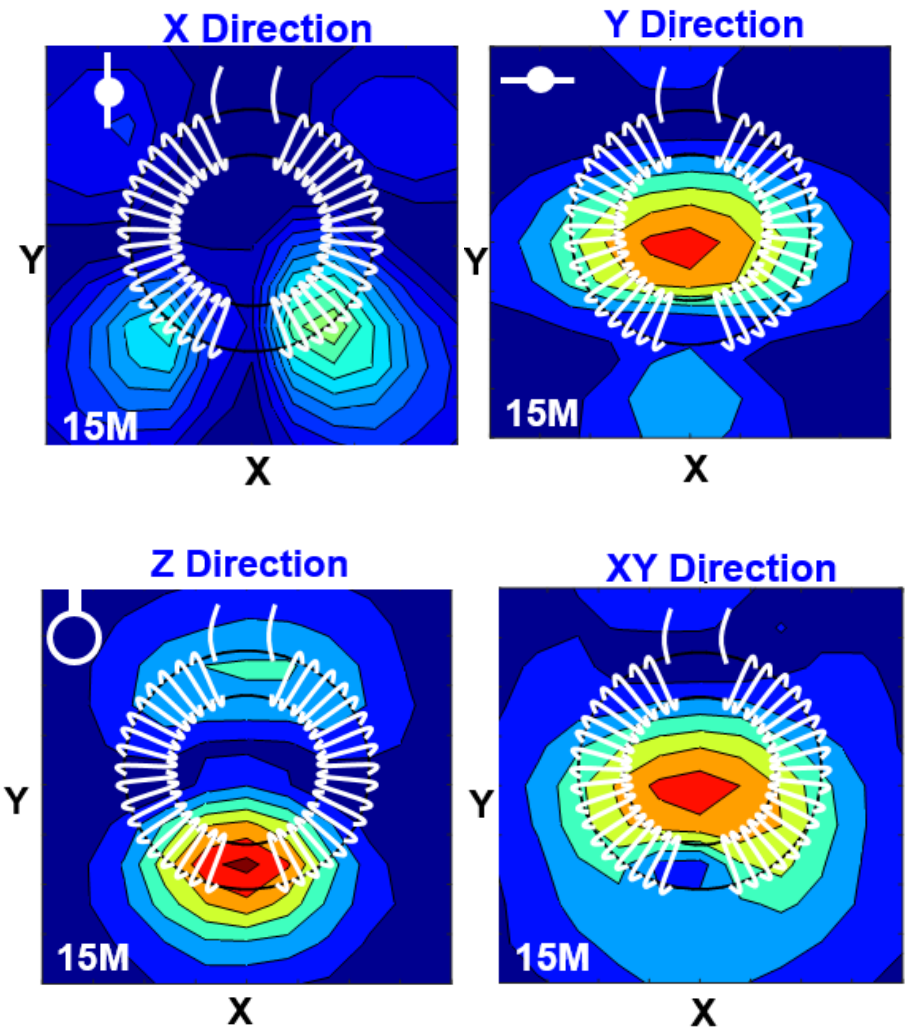


Fig. 4.19 Near field measurement result of 15 MHz

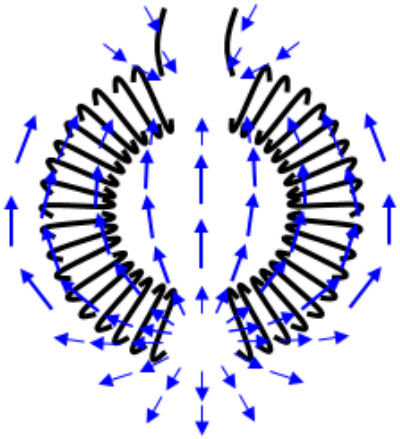


Fig. 4.20 Flux flow direction of 15 MHz excitation

Finally, the excitation frequency is increased to 25 MHz. The measurement result is shown in Fig. 4.21. It can be seen that this result is clearly different from low frequency measurement results. Instead having two poles, the flux now has three poles. The flux first comes from the bottom pole and then split to go to two top poles. Fig. 4.22 shows the flux flow direction.

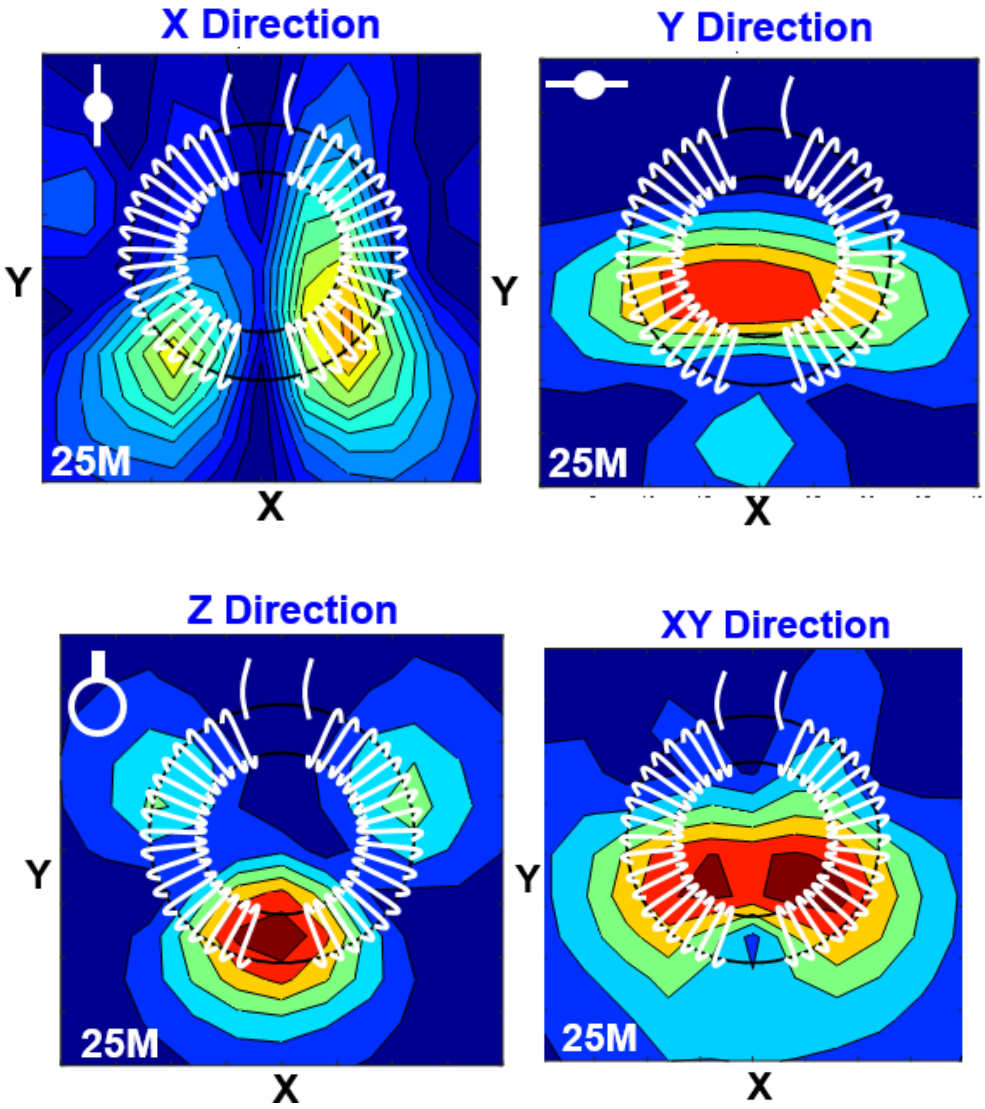


Fig. 4.21 Near field measurement result of 25 MHz

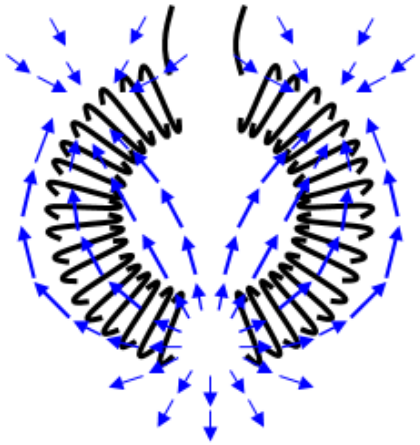


Fig. 4.22 Flux flow direction of 25 MHz excitation

Based on the previous analysis, a better EMI filter performance can be achieved by better layout design. Fig. 4.24 shows the traditional EMI filter layout. The inductor is vertically placed on the board. The near-field flux of inductor will generate mutual flux through capacitor. In order to reduce the mutual coupling between inductor and capacitors, the inductor is placed horizontally. Fig. 4.23 shows different capacitor positions with horizontal inductor. There are two positions of the capacitors, the red position and yellow position. For the red position, it can be seen that strong Y-direction flux flows through the capacitor. Therefore, the mutual coupling will be strong. For the yellow position, although the Y-direction flux is strong, the flux is in parallel with the capacitor. There is no mutual coupling between inductor and capacitors. Therefore, the yellow position is better to reduce the mutual coupling between inductor and capacitors.

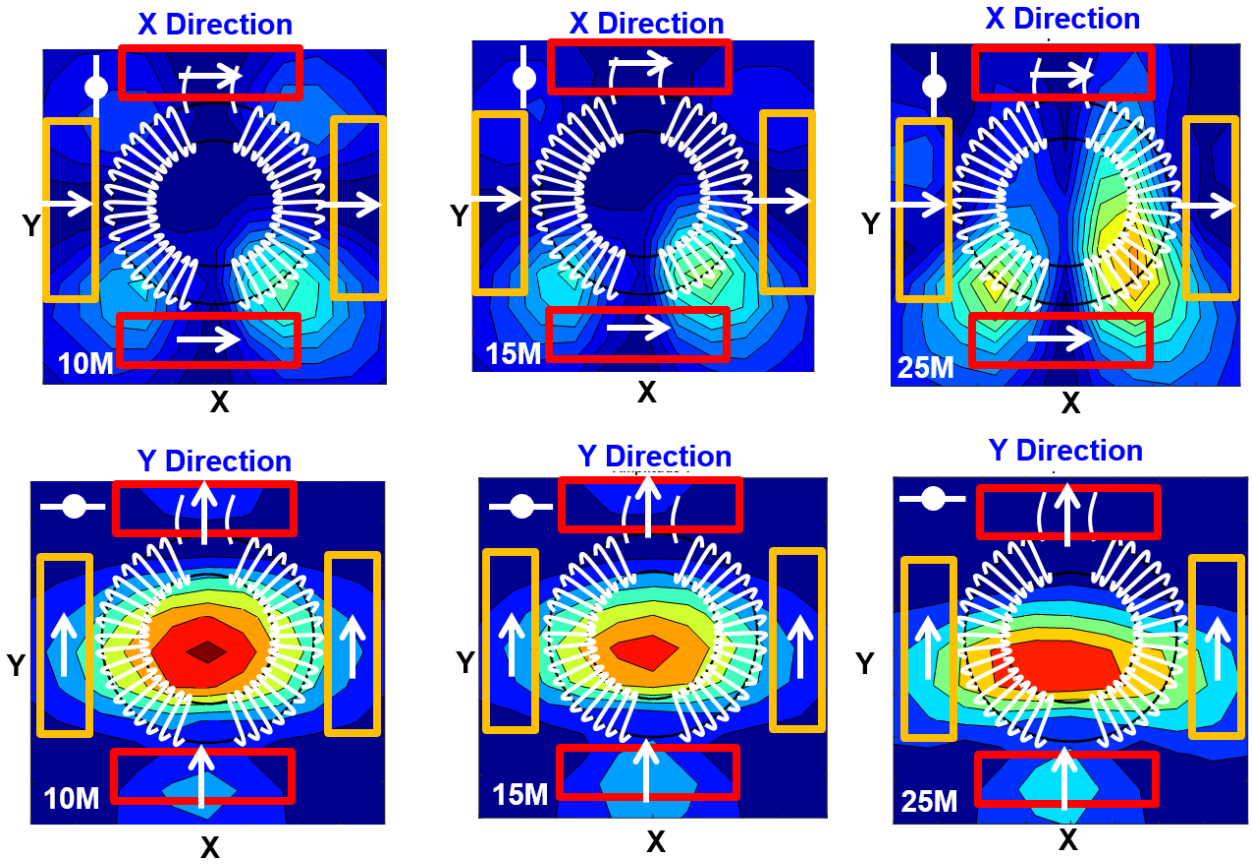


Fig. 4.23 Different capacitor position with horizontal inductor

Fig. 4.25 shows an improved EMI filter design. The inductor is laid down on the board and the capacitors are in the red position. And Fig. 4.26 shows a second improved design. The inductor rotates 90 degree, and the capacitors are in the yellow position.

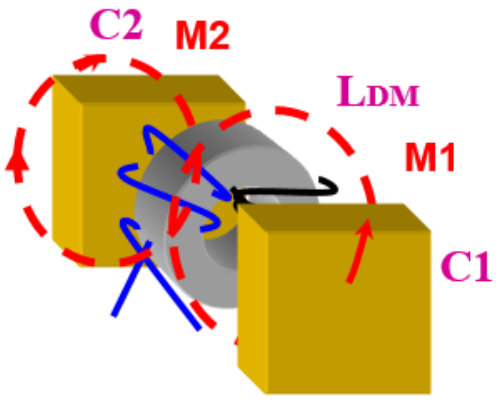


Fig. 4.24 Traditional EMI filter layout

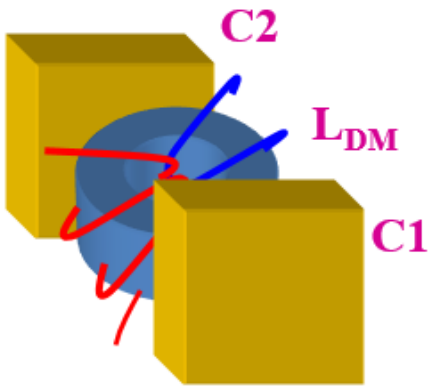


Fig. 4.25 Position 1

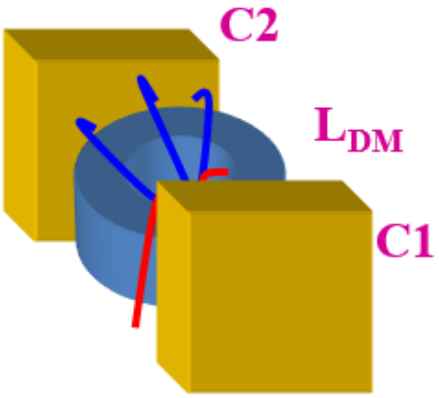


Fig. 4.26 Position 2

Fig. 4.27 shows the DM noise measurement result with those three different filer layouts. The traditional design has poor performance at high frequency. The improved design 1 has better high frequency performance than traditional design. But it still cannot pass the standard at high frequency. The improved design 2 pass the standard at both low and high frequency but with little margin.

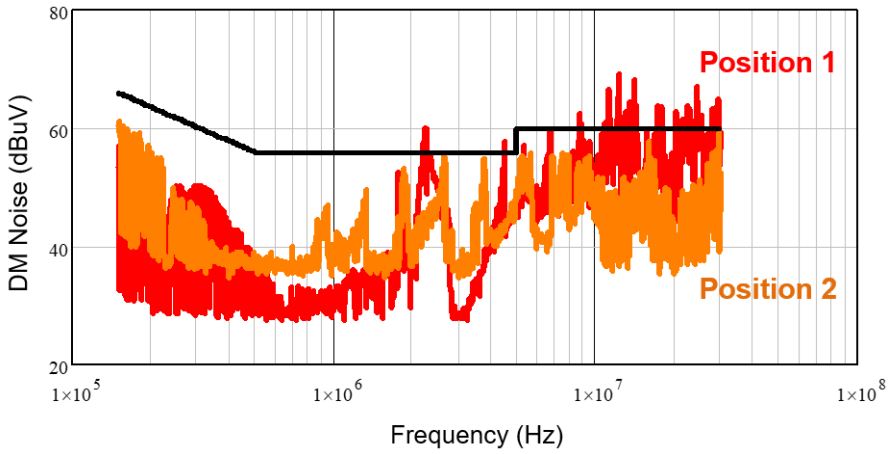


Fig. 4.27 DM noise measurement result

Fig. 4.28 shows the insertion voltage gain for single stage EMI filter with $M_{1,2}$ cancellation. The improved filter has better performance than the original filter at high frequency. Hence, the high frequency DM noise is attenuated.

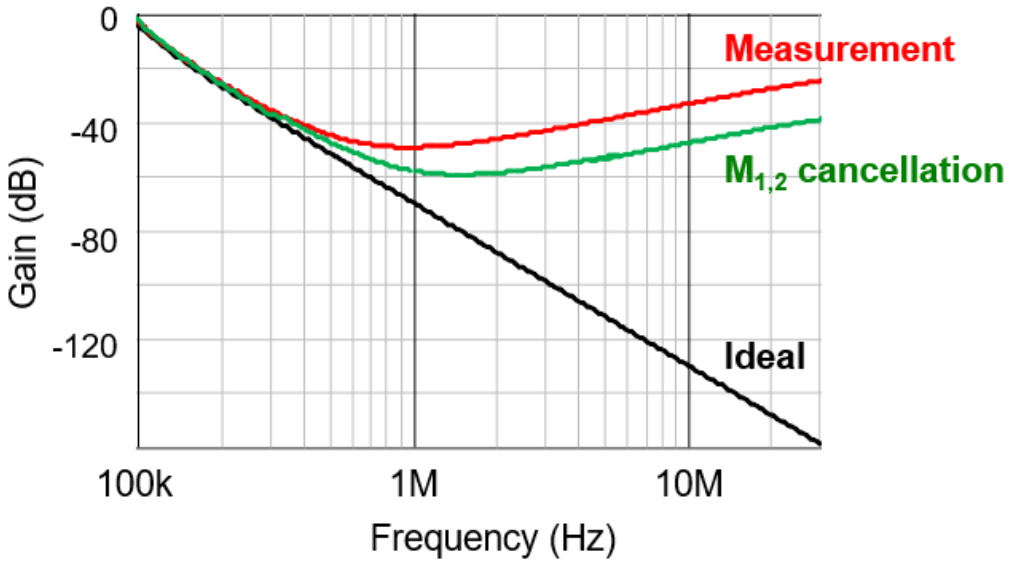


Fig. 4.28 Insertion voltage gain for filter with $M_{1,2}$ cancellation

4.4 Reduction of ESL of Capacitor Branch

The ESL in the capacitor branch will reduce the high frequency attenuation ability of the filter. In [68], a method is analyzed to reduce the ESL of capacitor branch based on circuit network theory.

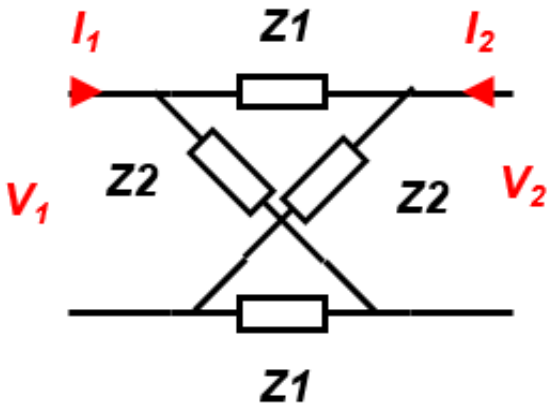


Fig. 4.29 Circuit network 1

For the circuit network shown in Fig. 4.29, the port voltage and current can be described by the following equation with Z matrix.

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \begin{pmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \end{pmatrix} \tag{4-1}$$

Then the Z matrix can be calculated as:

$$\mathrm{Z} = \begin{pmatrix} \frac{Z_1 + Z_2}{2} & \frac{Z_2 - Z_1}{2} \\ \frac{Z_2 - Z_1}{2} & \frac{Z_1 + Z_2}{2} \end{pmatrix} \tag{4-2}$$

Another circuit network can be created with same Z matrix, as shown in Fig. 4.30.

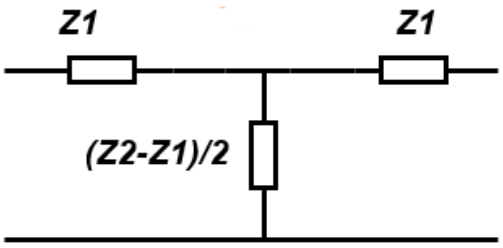


Fig. 4.30 Circuit network 2

Because the circuit network 1 and circuit network 2 have same Z matrix, they have same performance on two ports. Therefore, circuit network 1 is equivalent to circuit network 2. From circuit network 1 to circuit network 2, the impedance Z_1 is subtracted by Z_2 and formed the impedance $(Z_2-Z_1)/2$. Based on this circuit network transformation, the ESL of capacitor branch can be cancelled.

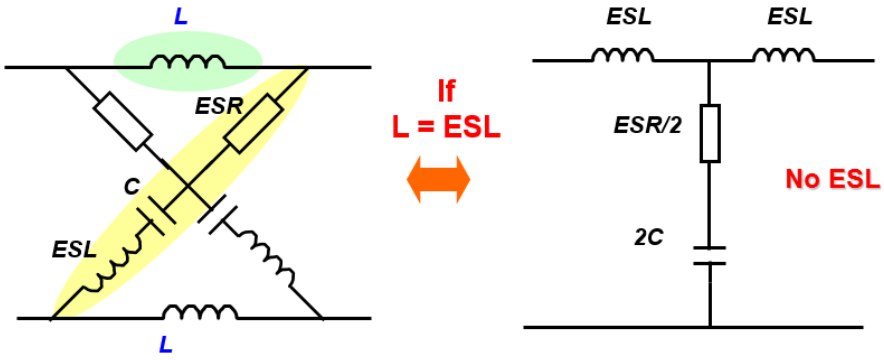


Fig. 4.31 ESL cancellation of capacitor

As shown in Fig. 4.31, two capacitors are diagonally positioned, just as circuit network 1. The two cancellation inductors are placed on the top and bottom line. According to the network theory, if the value of cancellation inductor L is equal to the ESL of capacitor, the shunt branch in the equivalent circuit will have no inductance.

The ESL of capacitor is usually very small at nH level. For example, for a 275 Vac 0.32 uF capacitor, the ESL is only 9 nH. Such small inductance can be easily formed through PCB

windings, as shown in Fig. 4.32. The two film capacitors are placed parallel. The cancellation inductor is realized using PCB winding. The calculation of the PCB winding inductance can be found in [74]:

$$L = \frac{\mu_0}{4\pi}\left[4l_1 \ln\left(\frac{2l_1}{w}\right) + 4l_2 \ln\left(\frac{2l_2}{w}\right) - 4l_1 \sinh^{-1}\left(\frac{l_1}{l_2}\right) - 4l_2 \sinh^{-1}\left(\frac{l_2}{l_1}\right)\right. \quad (4\text{-}3)$$

$$\left. + 8(l_1^2 + l_2^2)^{\frac{1}{2}} - 2(l_1 + l_2)\right]$$

Fig. 4.32 ESL cancellation implementation into PCB

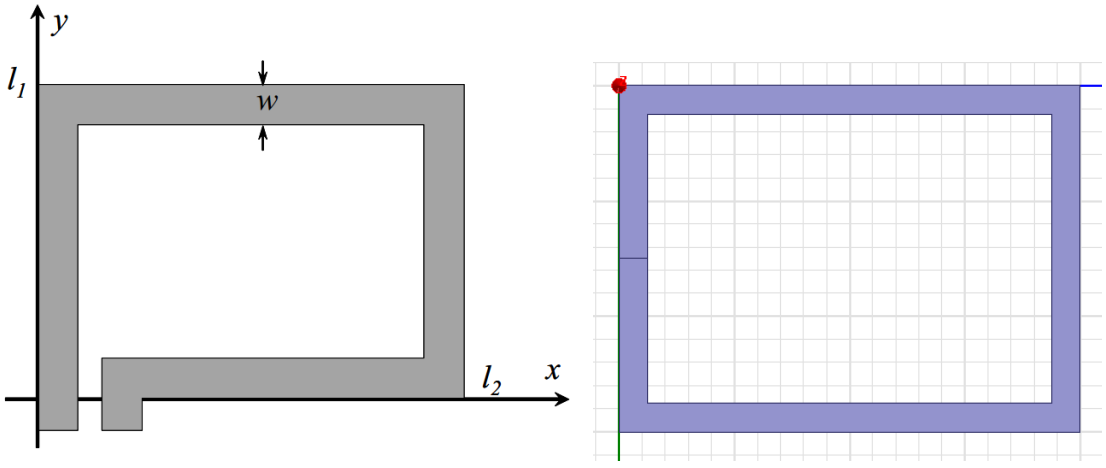


Fig. 4.33 Calculation and simulation of PCB winding inductance

The calculation can also be verified by FEA simulation, as shown in Fig. 4.33. Table 4-1 shows the results comparison between calculation and FEA simulation. It can be seen that with different dimension, the inductance value matches very well.

Table 4-1 Comparison between calculation and FEA simulation

	Calculation	FEA simulation
Inductance	9.9 nH	9.5 nH

Fig. 4.34 shows the insertion voltage gain for the filter with ESL cancellation method. It can be seen that with the ESL cancellation method, the high frequency performance can be improved. However, the filter performance around 2 MHz is not improved.

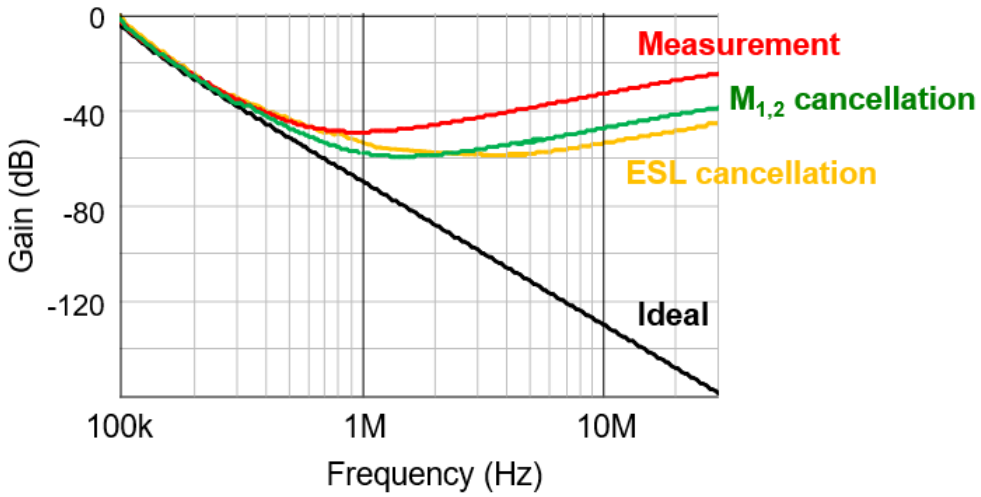


Fig. 4.34 Insertion voltage gain for filter with ESL cancellation

Fig. 4.35 shows the DM noise measurement result. It can be seen that the high frequency DM noise can be attenuated as analyzed from the insertion voltage gain. However, because the DM filter performance is not improved around 2 MHz, the DM noise around 2 MHz is not reduced, as shown in Fig. 4.35.

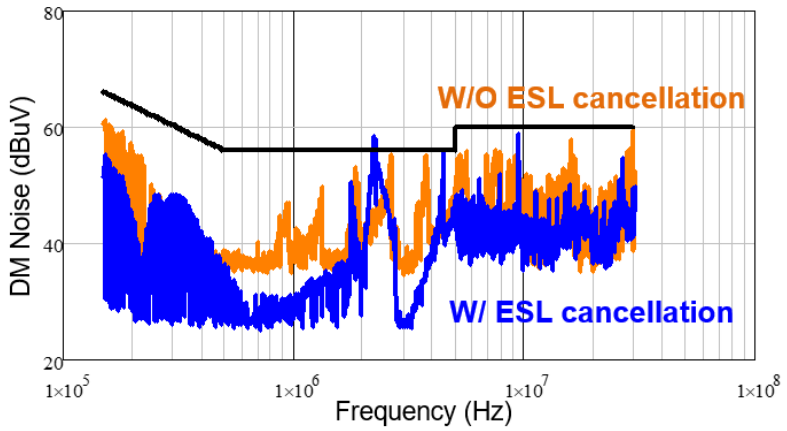


Fig. 4.35 DM noise measurement result with ESL cancellation

4.5 Reduction of Mutual Coupling between Two Capacitors

Film capacitors are very popular for DM filters. There are two methods of producing film capacitors: the wound technology and stacked-film technology. The wound technology is shown in Fig. 4.36. Capacitors are made by individually rolling the metallized films or the film/foils into cylindrical rolls and then covering them with an insulating sleeve or coating. The stacked-film technology is shown in Fig. 4.37. Large rings of metallized film are wound onto core wheels with diameters up to 60 cm. In this way the "master capacitors" are produced under well-defined and constant conditions [75].

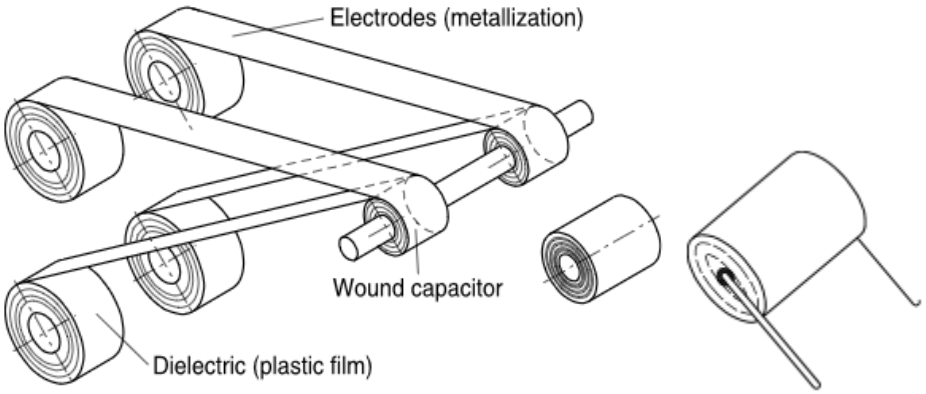


Fig. 4.36 Wound technology

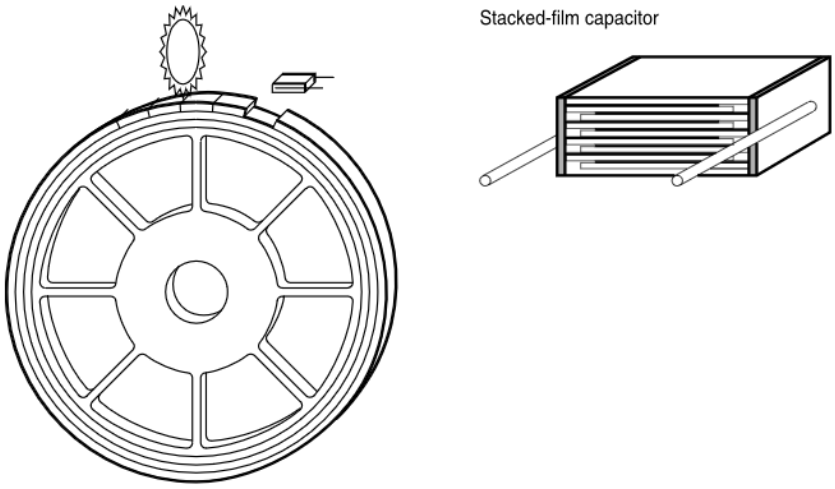


Fig. 4.37 Stacked-film technology

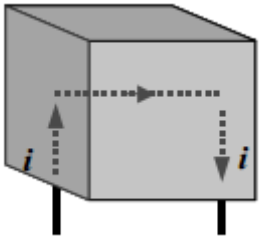


Fig. 4.38 Current flow path in the film capacitor

Fig. 4.38 shows the current flow path in the film capacitor. The current flows in from the wire lead and metal contact layer on one end of the capacitor. Then the current flows through the electrodes and dielectric films. Then the current reaches the metal contact layer and wire lead on the other side of the capacitor. Therefore the current loop inside the capacitor is shown in Fig. 4.38. This loop will coupled with external flux and then generate mutual coupling.

M_3 represents the mutual coupling between two capacitors, as shown in Fig. 4.11. The flux linkage is shown in Fig. 4.39. The mutual flux Φ_{M3} couples the current loops of C_1 and C_2. Based on the current direction, the two capacitors are positively coupled. [70] provides a method to reduce the mutual coupling between two capacitors.

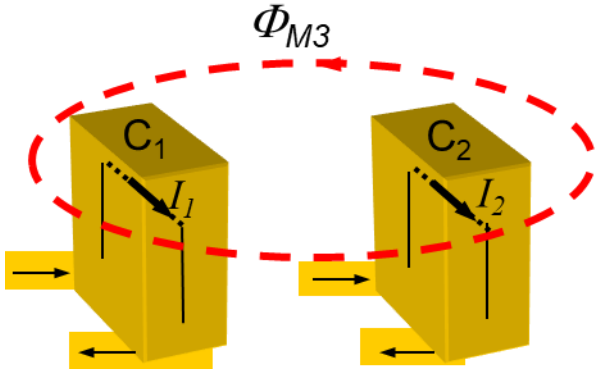


Fig. 4.39 Flux linkage between two capacitors

In order to reduce the mutual coupling between the two capacitors, an additional inductor is added in capacitor C_1, as shown in Fig. 4.40 [70]. The original terminals of C_1 is point A and point B. The additional inductor has two terminals, point C and point D. Point B of C_1 is connected with point D of the additional inductor L_M. Therefore, the current flows in at point C and flows out at point A. The current direction in L_M is opposite from C_1. Hence, the flux generated by L_M has opposite direction as the flux generated by C_1. Thus, the additional inductor and C_2 are negatively coupled. The circuit analysis is shown in Fig. 4.41. If M_A equals to M_3, the mutual coupling between two capacitors can be minimized.

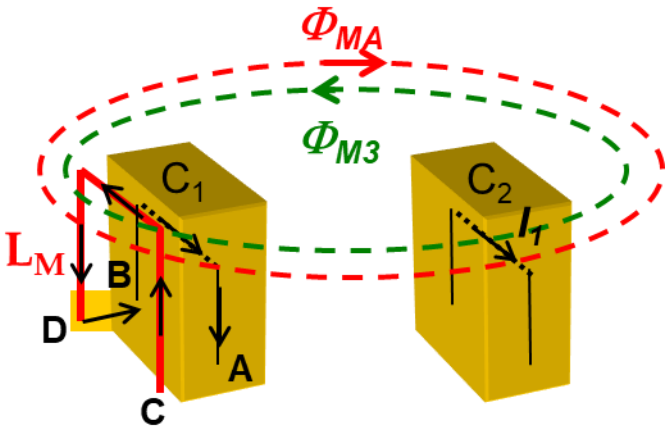


Fig. 4.40 Cancellation of M_3 using additional inductor

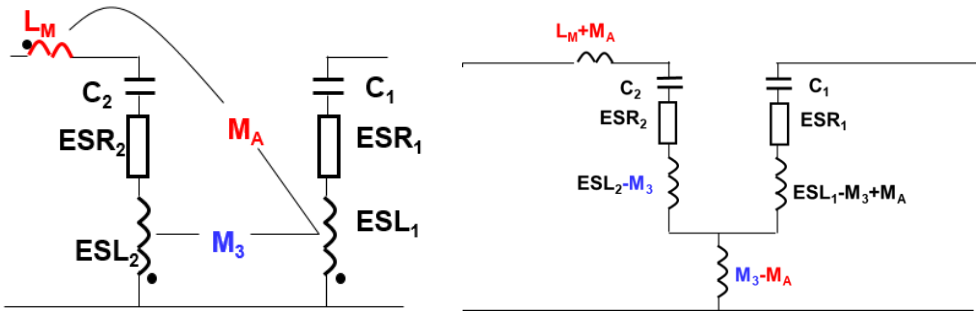


Fig. 4.41 Equivalent circuit of M_3 cancellation method

Fig. 4.42 shows the insertion voltage gain of filter with M_3 cancellation method. It shows that the filter can have better attenuation from 2 MHz to 30 MHz.

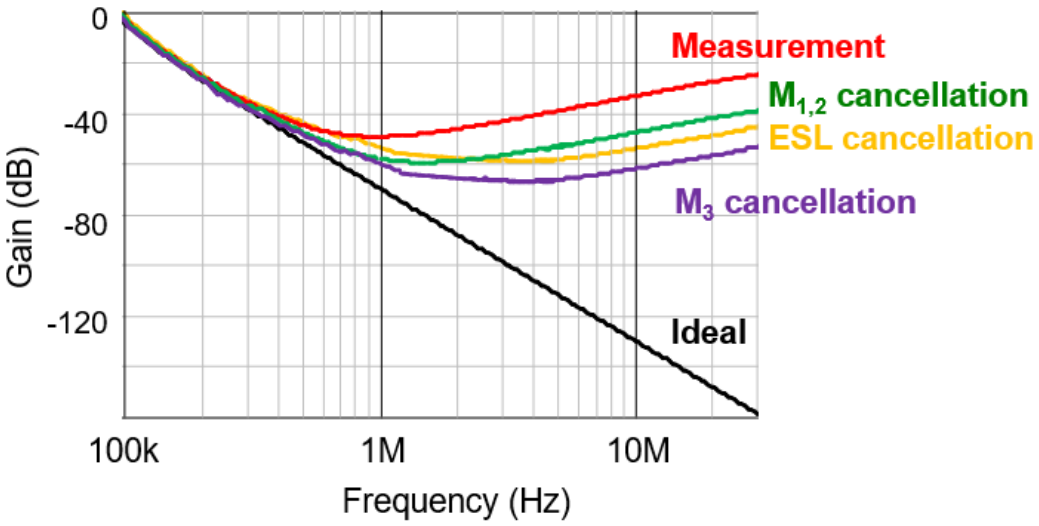


Fig. 4.42 Insertion voltage gain of filter with M_3 cancellation

Fig. 4.43 shows the DM noise measurement result. As predicted from the insertion voltage gain. The DM filter is attenuated at high frequency.

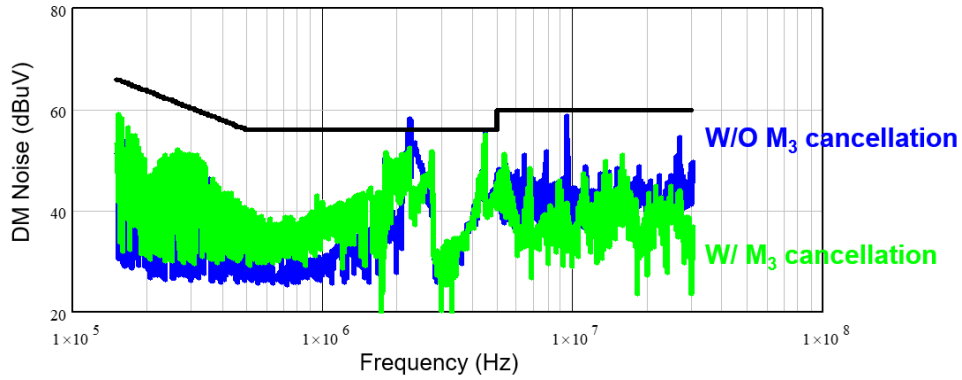


Fig. 4.43 DM noise measurement result with M_3 cancellation

4.6 Single Stage EMI Filter Demonstration in 1 kW Server Power Supply

With all the proposed analysis, a 1 kW server power supply with single stage EMI filter is demonstrated. The EMI filter uses the proposed single stage EMI filter. The volume of this single stage EMI filter is only 20% of the traditional two-stage EMI filter. The PFC stage uses the two-phase interleaved totem-pole structure, as analyzed in Chapter 3. With GaN devices, the switching frequency is above 1 MHz. With the proposed PCB winding inductor structure with balance technique, the PFC converter can achieve high efficiency, high density, low EMI noise and automated manufacturer. The DC-DC converter is an LLC converter with matrix transformer. Shielding method is applied to significantly reduce CM noise. All these EMI noise reduction methods make the single stage EMI filter become possible.

Fig. 4.44 shows the DM filter performance of this single stage EMI filter. With all the mutual coupling reduction and self-parasitic reduction methods, the single stage EMI filter can achieve the required attenuation.

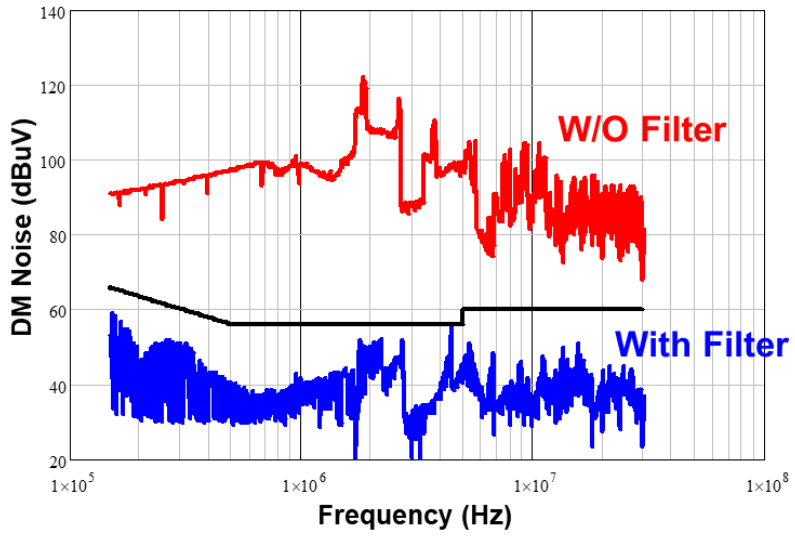


Fig. 4.44 DM filter performance

Fig. 4.45 shows the CM filter performance of this single stage EMI filter. With the balance and shielding technique, the CM noise has been greatly reduced. This makes the design of CM filter very simple. It can be seen that the single stage EMI filter can achieve the required attenuation.

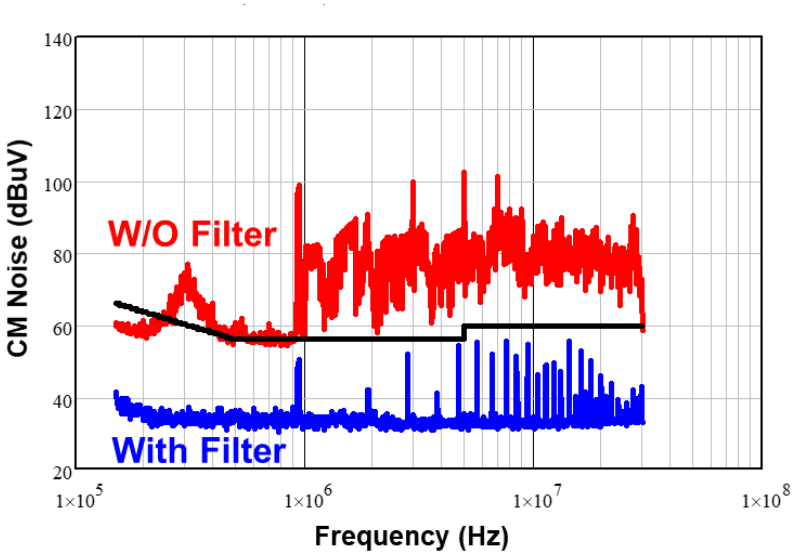


Fig. 4.45 CM filter performance

4.7 Conclusions

Traditionally, two-stage EMI filter is applied in the 1 kW server power supply. The two-stage EMI filter is bulky and expensive. With the GaN devices, the switching frequency of server power supply is increased to above 1 MHz. This can greatly reduce the converter volume and improve the power density. The bulky two-stage EMI filter is not suitable for this high density converter design. In order to use simple one-stage EMI filter, several EMI noise reduction method is applied. For the PFC converter, the balance technique is applied to reduce CM noise. Interleaving is applied to reduce DM noise. For the isolated DC-DC converter, shielding technique is applied to reduce CM noise through the transformer. With these techniques, the EMI noise of the converter has been greatly reduced. Therefore, one-stage EMI filter can be applied to achieve desired attenuation.

However, the traditional one-stage EMI filter cannot meet the EMI requirements. The self parasitics and mutual coupling will impact the high frequency performance of EMI filter. This impact is more severe in one-stage EMI filter than in two-stage EMI filter. In this chapter, the self parasitics and mutual coupling of EMI filter components are analyzed. Near field measurement is applied to visualize the flux near filter components. A better filter arrangement is proposed to reduce the mutual coupling between inductor and capacitors. The method to reduce the self parasitics and mutual coupling between capacitors are then analyzed. A simple and compact one-stage EMI filter is demonstrated on a 1 kW server power supply.

Chapter 5. Conclusions and Future Work

For today's power electronics products, with given quality and reliability, high efficiency, high power density and low cost are getting more and more attention. With recent advances made in wide-bandgap (WBG) devices, the design of power converters can be dramatically changed. With much faster switching speed and lower switching loss of WBG devices, the switching frequency of power converters can be increased 10 times higher than Si MOSFET design. The power density of converters can be dramatically increased. This brings challenges to the EMI design. With fast switching speed, the dv/dt is much higher, which will lead to high common mode noise. The PCB winding transformer is high efficiency and high density. But the inter-winding capacitance is very large. Therefore, the EMI noise will be larger. Conventional EMI filter design uses two-stage structure. It is very bulky and expensive. With high density power converters, the two-stage EMI filter will occupies a lot volume and greatly reduce the system power density.

To solve these issues, this dissertation proposes several solutions. In order to reduce the CM noise of isolated converters, shielding method is proposed. The PCB winding transformer suffers from large inter-winding capacitance. A novel shielding method is proposed to help reduce the CM noise so that it can be used in off-line power supplies. The design methodology of shielding is analyzed. With the proposed shielding method, the CM noise can be reduced more than 20 dB. More importantly, the shielding remains effective at very high frequency up to 30 MHz. The proposed shielding method can be implemented to different converter topologies.

In the PFC converter, in order to achieve high efficiency, CRM is applied. However, with CRM operation, the switching frequency has a wide range and the inductor current ripple is large. This dissertation proposes a novel PCB integrated coupled inductor structure to solve these issues.

Negative coupled inductor is applied to 1 kW server PFC converter. It can greatly reduce the switching frequency to reduce switching related loss. It can help achieve ZVS to reduce turn-on loss. A novel inductor structure is proposed that for the first time, the CRM PFC inductor can be integrated into PCB with similar efficiency as litz wire inductor. The PCB winding inductor has much higher power density and good manufacturability. Furthermore, balance technique can be implemented into PCB winding inductor to reduce CM noise of PFC converter. With PCB winding, the parasitic is easy to control and balance technique has better performance. It can achieve more than 20 dB attenuation. Then the positive coupled inductor is applied to 6.6 kW OBC PFC. The difference of negative coupling and positive coupling is analyzed. The positive coupled inductor can help reduce the switching frequency for 6.6 kW OBC PFC converter. The inductor is also integrated into PCB motherboard. However, due to large inductor size, the EPC of the inductor is large. This introduces extra loss. A new design methodology is proposed to optimize the inductor. With the improved inductor design, the PFC converter has better efficiency. Balance technique is also applied to help reduce CM noise.

For 1 kW server power supply, two-stage EMI filter is a popular solution. However, it is bulky, expensive and not suitable for today's high density power converters. This dissertation proposes the design of one-stage EMI filter. Thanks to the previous EMI noise reduction method, one-stage EMI filter can have the opportunity to achieve the required EMI attenuation. However, the parasitics and mutual coupling will severely impact the one-stage EMI filter. This dissertation analyzes the self parasitics and mutual coupling. The near field measurement method is applied to visualize the flux near filter components. The method to reduce the self parasitics and mutual coupling between filter components are demonstrated. Finally, a simple, effective one-stage EMI filter is demonstrated in the 1 kW server power supply system.

With the switching frequency of power converters above MHz, new magnetic materials are desperately need. Most today's magnetic materials are suitable for low frequency. They will suffer from high core loss at high frequency. The materials limit the magnetic design to be more efficient and more compact.

The PCB winding inductor has been applied to 1 kW server PFC and 6.6 kW OBC PFC converter. The PCB winding inductor performs well in low power applications. But in higher power, the PCB winding inductor faces some issues. Further efforts need to be spend on how to design PCB winding inductors at high current condition. What is the limitation of PCB winding inductor should be investigated.

The balance technique can achieve good CM noise reduction at low frequency. But at high frequency, the balance technique is not so effective. It is meaningful to investigate how to improve the high frequency performance of balance technique.

This dissertation only studies the conducted EMI noise. The radiated EMI noise is also an important topic. As the switching frequency goes beyond MHz, the radiated EMI noise would become severe. It is worth to take effort to study the radiated EMI noise for high frequency converters.

Reference

[1] International Electrotechnical Vocabulary IEV 161-01-07.

[2] International Electrotechnical Vocabulary IEV 161-01-06.

[3] Agilent Technologies: “AN150 Spectrum Analysis Basics”.

[4] EN55022: Information Technology Equipment - Radio Disturbance Characteristics – Limits and Methods of Measurements.

[5] Wang S. Characterization and Cancellation of High-Frequency Parasitics for EMI Filters and Noise Separators in Power Electronics Applications [Ph.D. Dissertation]. Blacksburg: Department of Electrical and Computer Engineering, Virginia Tech, 2005.

[6] Shuo Wang; Lee, F.C., "Common-Mode Noise Reduction for Power Factor Correction Circuit With Parasitic Capacitance Cancellation," *Electromagnetic Compatibility, IEEE Transactions on* , vol.49, no.3, pp.537,542, Aug. 2007.

[7] Shuo Wang; Pengju Kong; Lee, F.C., "Common Mode Noise Reduction for Boost Converters Using General Balance Technique," *Power Electronics, IEEE Transactions on* , vol.22, no.4, pp.1410,1416, July 2007.

[8] Pengju Kong (2009). Common mode EMI noise reduction techniques in switch mode power supplies (Doctoral Dissertation).

[9] Pengju Kong; Shuo Wang; Lee, F.C., "Improving balance technique for high frequency common mode noise reduction in boost PFC converters," *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE* , vol., no., pp.2941,2947, 15-19 June 2008.

[10] Pengju Kong; Shuo Wang; Lee, F.C., "Common Mode EMI Noise Suppression for Bridgeless PFC Converters," *Power Electronics, IEEE Transactions on* , vol.23, no.1, pp.291,297, Jan. 2008.

[11] Pengju Kong; Shuo Wang; Lee, F.C.; Chuanyun Wang, "Common-Mode EMI Study and Reduction Technique for the Interleaved Multichannel PFC Converter," *Power Electronics, IEEE Transactions on* , vol.23, no.5, pp.2576,2584, Sept. 2008.

[12] Rockhill A, Lipo T A, Julian A L. High Voltage Buck Converter Topology for Common Mode Voltage Reduction. Proceedings of IEEE APEC 1998:940-943.

[13] Crebier J, Ferrieux J. PFC Full Bridge Rectifiers EMI Modeling and Analysis-common Mode Disturbance Reduction. IEEE Transactions on Power Electronics 2004,19(2):378-387.

[14] Wu H, Chen X, Zhou M, Zeng J, Ying J. A Novel Control Method of Interleaved Two-Transistor Forward Converter. Proceedings of IEEE PESC 2007:2812-2818.

[15] Wu X, Poon F, Lee C M, Pong M H, Qian Z. A Study of Common Mode Noise in Switching Power Supply from a Current Balancing Viewpoint. Proceedings of IEEE PEDS 1999(2):621-625.

[16] Hofsajer I W, Fricker K, Crosato M O. Reduction of EMI in Planer Transformers by Charge Balancing. IEEE Electronics Letters 2002,38(25):1712-1714.

[17] Cochrane D, Chen D, Boroyevic D. Passive Cancellation of Common-mode Noise in Power Electronic Circuits. IEEE Transactions on Power Electronics 2003,18(3):756-763.

[18] Crosato M O, Hofsajer I W. Minimising Conducted Common Mode EMI by Charge Balancing in a Nonisolated DC-DC Converter. Proceedings of IEEE PESC 2004(4):3146-3151.

[19] Shoyama M, Li G, Ninomiya T. Balanced Switching Converter to Reduce Common-Mode Conducted Noise. IEEE Transactions on Industrial Electronics 2003,50(6):1095-1099.

[20] Chan Woong Park, "Method and apparatus for substantially reducing electrical earth displacement current flow generated by wound components without requiring additional windings," U.S. Patent 7109836 B2, 2006.

[21] S. Lin, M. Zhou, W. Chen, and J. Ying, “Novel methods to reduce common-mode noise based on noise balance,” in Proc. 2006 IEEE Power Electron.Spec. Conf., pp. 2728–2733.

[22] Lee, F.C.; Barbosa, P.; Peng Xu; Jindong Zhang; Yang, B.; Canales, Francisco, "Topologies and design considerations for distributed power system applications," *Proceedings of the IEEE* , vol.89, no.6, pp.939,950, Jun 2001.

[23] M. M. Jovanovic "Technology drivers and trends in power supplies for computer/telecom", *Proc. APEC*, 2006.

[24] X. Huang, J. Feng, W. Du, F. C. Lee and Q. Li, "Design consideration of MHz active clamp flyback converter with GaN devices for low power adapter application," *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2016, pp. 2334-2341. G. Huang, A. J. Zhang, and Y. Gu, "LLC series resonant DC-to-DC converter," U.S. Patent 6 344 979, Feb. 5, 2002.

[25] Y. Yang, D. Huang, F. C. Lee and Q. Li, "Transformer shielding technique for common mode noise reduction in isolated converters," *2013 IEEE Energy Conversion Congress and Exposition*, Denver, CO, 2013, pp. 4149-4153.

[26] B. Yang , Y. Ren and F. C. Lee "Integrated magnetic for LLC resonant converter", *Proc. IEEE APEC*, pp.346 -351 2002.

[27] B. Yang , F. C. Lee , A. J. Zhang and G. Huang "LLC resonant converter for front end dc/dc conversion", *Proc. IEEE APEC*, pp.1108 -1112 2002.

[28] Bo Yang, "Topology investigation for front end DC/DC power conversion for distributed power system," Ph.D. dissertation, Dept. ECE, Virginia Tech, Blacksburg, VA, USA, 2003.

[29] Y. Gu , Z. Lu , L. Hang , Z. Qian and G. Huang "Three-level LLC series resonant DC/DC converter", *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp.781 -789 2005.

[30] D. Fu , Y. Liu , F. C. Lee and M. Xu "A novel driving scheme for synchronous rectifiers in LLC resonant converters", *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp.1321 -1329 2009.

[31] Xinke Wu, Guichao Hua, Junming Zhang, and Zhaoming Qian, "A new current-driven synchronous rectifier for series–parallel resonant (LLC) DC–DC converter," IEEE Trans. Ind. Electron., vol. 58, no. 1, pp. 289–297, Jan. 2011.

[32] Xinke Wu, Chen Hu, Junming Zhang, and Chen Zhao, "Series–parallel autoregulated charge-balancing rectifier for multioutput light-emitting diode driver," IEEE Trans. Ind. Electron., vol. 61, no. 3, pp. 1262–1268, Mar.2014.

[33] Edward Herbert, "Design and Application of Matrix Transformers and Symmetrical Converters," a tutorial presented at the High Frequency Power Conversion Conference '90, Santa Clara, CA, May 11, 1990.

[34] K. Kit Sum, D. Trevor Holmes, "Novel Low Profile Matrix Transformers for High Density Power Conversion," Power Conversion and Intelligent Motion, September, 1988.

[35] D. Reusch and F. C Lee "High frequency bus converter with low loss integrated matrix transformer", *Proc. IEEE APEC 2012*, pp.1392 -1397.

[36] Daocheng Huang; Shu Ji; Lee, F.C., "LLC Resonant Converter With Matrix Transformer," *Power Electronics, IEEE Transactions on* , vol.29, no.8, pp.4339,4347, Aug. 2014.

[37] International Rectifier. (Feb. 2010). GaNpowIR—An introduction [On-line]. Available: http://www.IRF.com.

[38] Efficient Power Conversion. EPC1015—Enhancement mode power transistor [Online]. Available: www.EPC.com.

[39] N. Dai and F. C. Lee "Edge effect analysis in a high-frequency transformer", *Proc. 25th Annu. IEEE Power Electron. Spec. Conf., Rec.*, pp.850 -855 1994.Laszol Huber, Yungtaek Jang, Milan M. Jovanonic, "Performance Evaluation of Bridgeless PFC Boost Rectifiers," IEEE Transaction on Power Electronics, May 2008.

[40] Y. Yang, D. Huang, F. C. Lee and Q. Li, "Analysis and reduction of common mode EMI noise for resonant converters," *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, Fort Worth, TX, 2014, pp. 566-571.

[41] Y. Yang, M. Mu, Z. Liu, F. C. Lee and Q. Li, "Common mode EMI reduction technique for interleaved MHz critical mode PFC converter with coupled inductor," *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, 2015, pp. 233-239.

[42] L. Huber, Y. Jang and M. M. Jovanovic, "Performance Evaluation of Bridgeless PFC Boost Rectifiers," in *IEEE Transactions on Power Electronics*, vol. 23, no. 3, pp. 1381-1390, May 2008.

[43] L. Zhou, Y. Wu, J. Honea and Z. Wang, "High-efficiency True Bridgeless Totem Pole PFC based on GaN HEMT: Design Challenges and Cost-effective Solution," *Proceedings of*

PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2015, pp. 1-8.

[44] X. Huang, Z. Liu, Q. Li, and F C. Lee, "Evaluation and application of 600 V GaN HEMT in cascode structure," IEEE Trans. Power Electron., vol. 29, no. 5, pp. 2453–2461, May 2014.

[45] X. Huang, Q. Li, Z. Liu, and F C. Lee, "Analytical loss model of high voltage GaN HEMT in cascode configuration," IEEE Trans. Power Electron., vol. 29, no. 5, pp. 2208–2219, May 2014.

[46] Z. Liu, X. Huang, F. C. Lee, and Q. Li, "Package parasitic inductance extraction and simulation model development for the high-voltage cascode GaN HEMT," IEEE Trans. Power Electron., vol. 29, no. 4, pp. 1977–1985, April 2014

[47] X. Huang, W. Du, F. C. Lee, Q. Li, Z. Liu, "Avoiding Si MOSFET avalanche and achieving zero-voltage switching for cascode GaN devices," IEEE Trans. Power Electron., vol. 31, no. 1, pp. 593–600, Jan. 2016.

[48] Z. Liu, F. C. Lee, Q. Li and Y. Yang, "Design of GaN-Based MHz Totem-Pole PFC Rectifier," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 799-807, Sept. 2016.

[49] P. Wong, P. Xu, P. Yang, and F. C. Lee, "Performance improvements of interleaving VRMs with coupling inductors," IEEE Trans. Power Electron., vol. 16, no. 4, pp. 499–507, Jul. 2001.

[50] Fei Yang; Xinbo Ruan; Yang Yang; Zhihong Ye, "Interleaved Critical Current Mode Boost PFC Converter With Coupled Inductor," Power Electronics, IEEE Transactions on, vol.26, no. 9, pp. 2404, 2413, Sept. 2011.

[51] Xiucheng Huang; Lee, F.C.; Qiang Li; Weijing Du, "MHz GaN-based interleaved CRM bi-directional buck/boost converter with coupled inductor," *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*, pp. 2075, 2082, 15-19 March 2015.

[52] M. Mu and F. C. Lee. "Design and optimization of a 380V-12V high-frequency, high-Current LLC converter with GaN devices and planar matrix transformers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 854-862, Sep. 2016.

[53] Dianbo Fu; Lee, F.C.; Shuo Wang, "Investigation on transformer design of high frequency high efficiency dc-dc converters," *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, pp. 940, 947, 21-25 Feb. 2010.

[54] Pengju Kong; Shuo Wang; Lee, F.C.; Chuanyun Wang, "Common-Mode EMI Study and Reduction Technique for the Interleaved Multichannel PFC Converter," Power Electronics, IEEE Transactions on, vol. 23, no. 5, pp. 2576, 2584, Sept. 2008.

[55] Y. Yang, Z. Liu, F. C. Lee and Q. Li, "Multi-phase coupled and integrated inductors for critical conduction mode totem-pole PFC converter," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, 2017, pp. 1804-1809.

[56] J. S. Lai, L. Zhang, Z. Zahid, N. H. Tseng, C. S. Lee and C. H. Lin, "A high-efficiency 3.3-kW bidirectional on-board charger," *2015 IEEE 2nd International Future Energy Electronics Conference (IFEEC)*, Taipei, 2015, pp. 1-5.

[57] J. S. Lai, L. Zhang, Z. Zahid, N. H. Tseng, C. S. Lee and C. H. Lin, "A high-efficiency 3.3-kW bidirectional on-board charger," *2015 IEEE 2nd International Future Energy Electronics Conference (IFEEC)*, Taipei, 2015, pp. 1-5.

[58] W. Shuo, *et al.*, "Parasitic Effects of Grounding Paths on Common-Mode EMI Filter's Performance in Power Electronics Systems," *Industrial Electronics, IEEE Transactions on*, vol. 57, pp. 3050-3059, 2010.

[59] W. Shuo, *et al.*, "Design of Inductor Winding Capacitance Cancellation for EMI Suppression," *Power Electronics, IEEE Transactions on*, vol. 21, pp. 1825-1832, 2006.

[60] W. Shuo, *et al.*, "A Study of Integration of Parasitic Cancellation Techniques for EMI Filter Design With Discrete Components," *Power Electronics, IEEE Transactions on*, vol. 23, pp. 3094-3102, 2008.

[61] C. Rengang, *et al.*, "Improving the Characteristics of integrated EMI filters by embedded conductive Layers," *Power Electronics, IEEE Transactions on*, vol. 20, pp. 611-619, 2005.

[62] J. D. van Wyk, *et al.*, "Integrating active, passive and EMI-filter functions in power electronics systems:a case study of some technologies," *Power Electronics, IEEE Transactions on*, vol. 20, pp. 523-536, 2005.

[63] W. Ruxi, *et al.*, "High power density EMI filter design with consideration of self-parasitic," in *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, 2012, pp. 2285-2289.

[64] T. De Oliveira, *et al.*, "PEEC-models for EMC filter layout optimization," in *Integrated Power Electronics Systems (CIPS), 2010 6th International Conference on*, 2010, pp. 1-6.

[65] T. De Oliveira, *et al.*, "Automatic layout optimization of an EMC filter," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, 2010, pp. 2679-2685.

[66] S. P. Weber, et al., "Predicting parasitics and inductive coupling in EMI-filters," in Applied Power Electronics Conference and Exposition, 2006. APEC '06. Twenty-First Annual IEEE, 2006, p. 4 pp.

[67] Shuo Wang, Rengang Chen, J. D. Van Wyk, F. C. Lee and W. G. Odendaal, "Developing parasitic cancellation technologies to improve EMI filter performance for switching mode power supplies," in *IEEE Transactions on Electromagnetic Compatibility*, vol. 47, no. 4, pp. 921-929, Nov. 2005.

[68] S. Wang, F. C. Lee and W. G. Odendaal, "Cancellation of capacitor parasitic parameters for noise reduction application," in *IEEE Transactions on Power Electronics*, vol. 21, no. 4, pp. 1125-1132, July 2006.

[69] W. Shuo, *et al.*, "Improvement of EMI filter performance with parasitic coupling cancellation," *Power Electronics, IEEE Transactions on*, vol. 20, pp. 1221-1228, 2005.

[70] W. Shuo, *et al.*, "Effects of parasitic parameters on EMI filter performance," *Power Electronics, IEEE Transactions on*, vol. 19, pp. 869-877, 2004.

[71] M. Hartmann, *et al.*, "EMI Filter Design for a 1 MHz, 10 kW Three-Phase/Level PWM Rectifier," *Power Electronics, IEEE Transactions on*, vol. 26, pp. 1192-1204, 2011.

[72] J. Aime, *et al.*, "Determination of the layout influence on the effectiveness of a three-phase common mode filter by using equivalent circuits and PSpice," in *Industrial Electronics, 2008. ISIE 2008. IEEE International Symposium on*, 2008, pp. 1-6.

[73] C. Wei, *et al.*, "Near Field Coupling Effects on Conducted EMI in Power Converter," in *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, 2006, pp. 1-6.

[74] Bueno, M.A.; Assis, A.K.T. A New Method for Inductance Calculations. *J. Phys. D: Appl. Phys*. 1995, *28*, 1802.

[75] Film Capacitors - General technical information – EPCOS, 2015