



Enabling Solutions for Embedded & RISC-V Development

June 21, 2018



Agenda

- Introduction
- Ashling Background
- RiscFree™ IDE

Ashling Vision & Mission

Ashling is a global world-class technology partner offering integrated solutions, tools, and design services that are at the heart of the embedded environment

Our vision is to build on ubiquitously available open source technology with embedded tools, IP and services with customized support enriching and enabling the ecosystem.

Value Proposition

- 25 Years of Success due to focus on:
 - ARC customers (Ashling is Exclusive Service Provider, 14 years)
 - NXP Security Group Close relationship (10 years)
 - MIPS Embedded Partnership (10 years)
- 400+ Worldwide Customers in 18 countries
- Unique Vertical Experience in
 - Healthcare
 - Identification
 - Cryptography
 - Automotive
 - Semiconductor

Corporate Information

- Ashling is a NeST Group company (\$550M)

- Engineering count 1200+

- Software Engineers 850+
- Embedded Software Engineers 250+
- Electrical Engineers 80+
- Mechanical Engineers 25+

Locations

San Jose,
California

Portland,
Oregon

Limerick,
Ireland

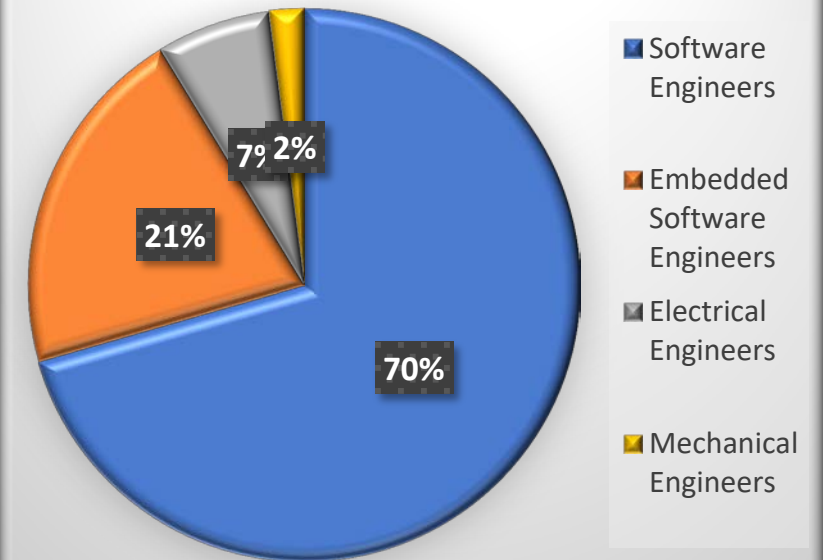
Leeds,
UK

Frankfurt,
Germany

Kochi,
India

Chennai,
India

Engineering Headcount



Ashling's Unique Business Model

- Tools-as-a-Service **TaaS™** where IP belongs to customer
- Comprehensive Ecosystem for RISC-V environment
- Engagement with Customer as Partner
- Open-System Environment allows
 - Premier Partnership
 - Ideal Growth Environment
 - Commercial Gaps closure
- Security expertise due to long-term partnership

Partners & Clients

SanDisk® NXP SHARP Alcon®

MICROCHIP Boston Scientific TEXAS INSTRUMENTS

DELPHI RENESAS SYNOPSYS®

United Technologies OKI MIPS

BROADCOM® ultra soc




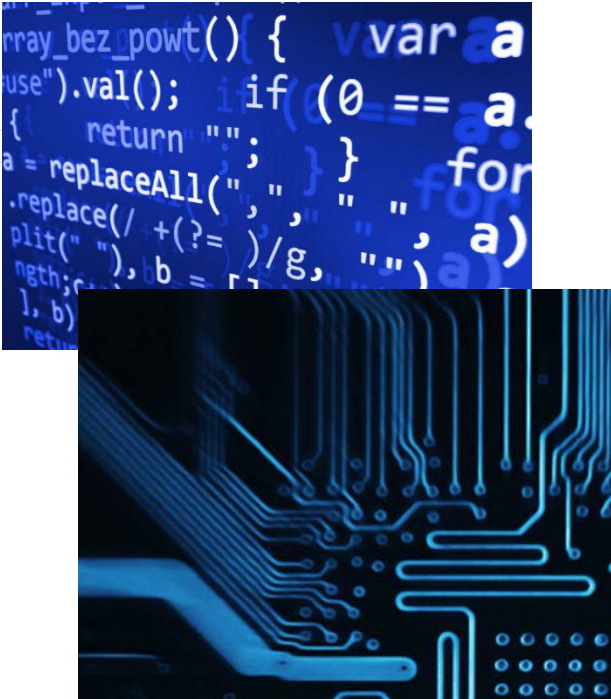
imperas

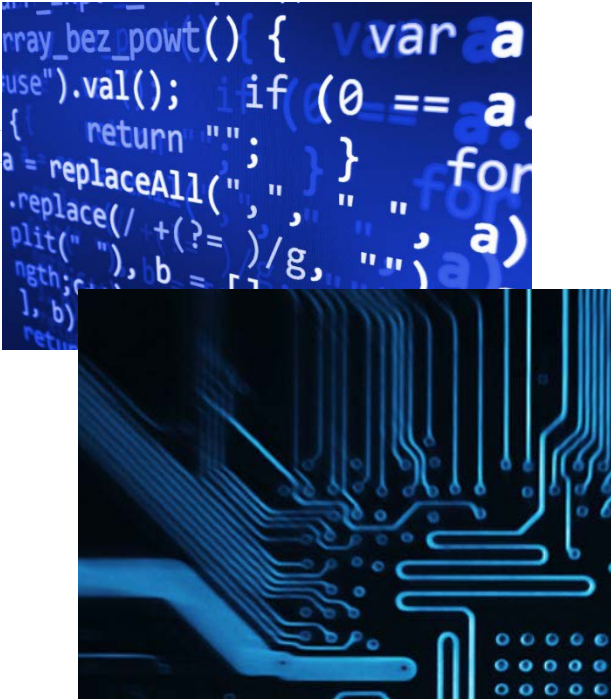

SiFive

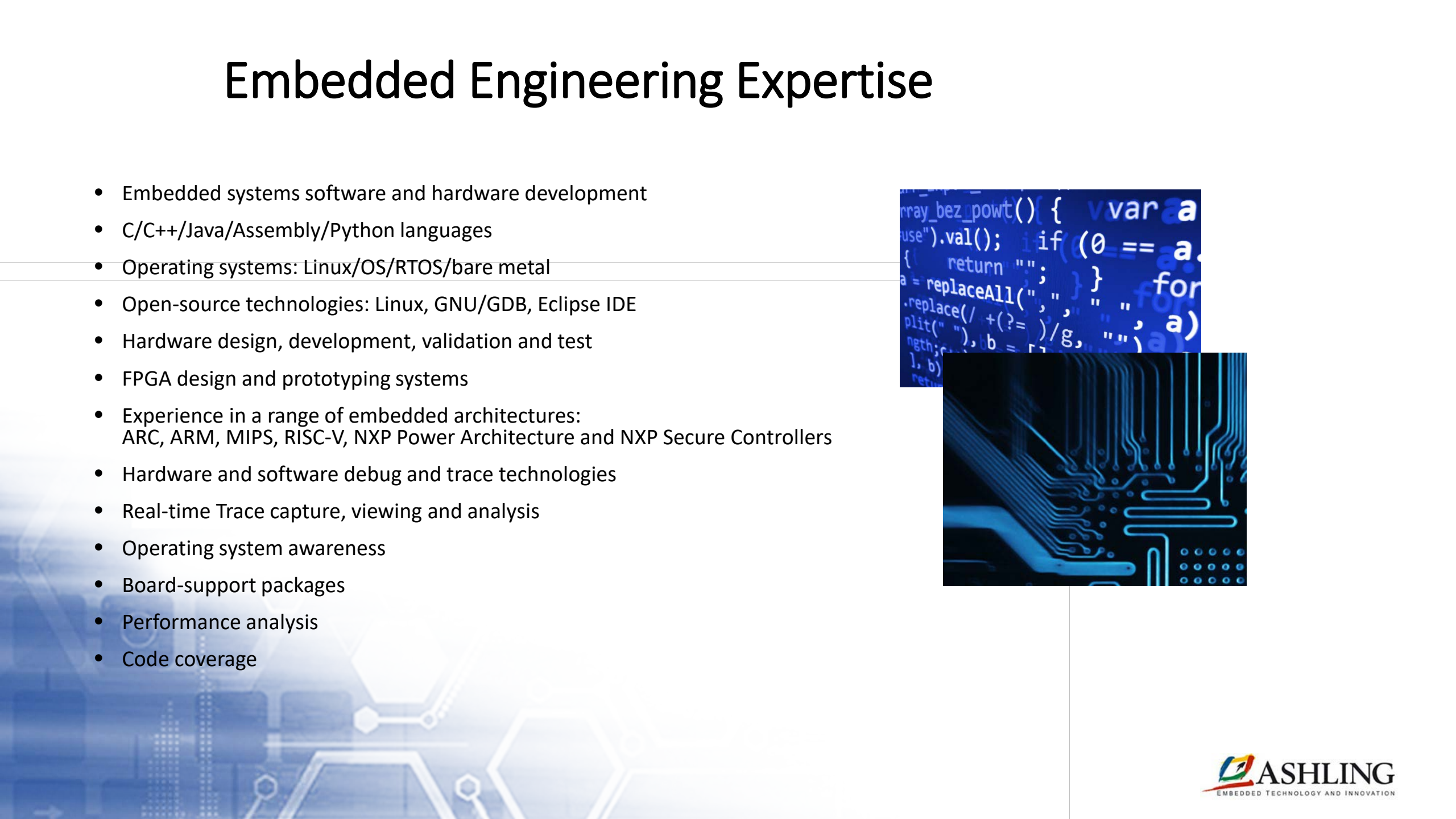
Microsemi®

Embedded Engineering Expertise

- Embedded systems software and hardware development
- C/C++/Java/Assembly/Python languages
- Operating systems: Linux/OS/RTOS/bare metal
- Open-source technologies: Linux, GNU/GDB, Eclipse IDE
- Hardware design, development, validation and test
- FPGA design and prototyping systems
- Experience in a range of embedded architectures:
ARC, ARM, MIPS, RISC-V, NXP Power Architecture and NXP Secure Controllers
- Hardware and software debug and trace technologies
- Real-time Trace capture, viewing and analysis
- Operating system awareness
- Board-support packages
- Performance analysis
- Code coverage



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Ashling Debug Tools

Broad capability

- High Speed JTAG Debug Probes
- Eclipse-based IDE/Source Debuggers
- Real-Time Trace Probes
- High Capacity, High Speed Debug and Trace Systems
- Non-intrusive Code Coverage Analysis Tools
- Non-intrusive Performance Analysis Tools



Ashling Ecosystem for RISC-V

- RISC-V Development Tools
- RISC-V SOC (System-on-chip) & IP design services
- IoT and Embedded Cloud Development
- Embedded Development and Engineering Services

RISC-V Development Tools

- Fully featured Eclipse based IDE which supports the complete software development cycle including edit, build, debug, test and verification on both virtual and hardware platforms
- Includes:
 - GCC and LLVM compilers.
 - QEMU RISC-V Simulator
 - RTOS awareness
 - Hardware debug and trace support via JTAG and Trace debug probes
 - Imperas Virtual Platforms/Processor Models support
- Use the same tool-chain from simulation (using the Imperas models) to device/board bring-up with actual silicon

RISC-V SoC & IP Design Services

We offer RISC-V processor IP and tools for developing and verifying RISC-V cores, SoCs, and subsystems while achieving the highest levels of quality, performance and innovation.

■ RISC-V IP CORES

- Differentiate yourself with proprietary enhancements and customizations
- Make product and business decisions independently of proprietary IP companies (by owning your own source code to processor cores)

■ RISC-V VERIFICATION TOOLS

- Ensure the verification of RISC-V cores as safe to use through rigorous independent verification.
- Any bug can be quickly detected and fixed.
- Verified RISC-V core can be up and running software in minimal time

■ RISC-V ACCELERATION

- Enable highest possible levels performance/watt by using dedicated hardware accelerators .
- Differentiate using proprietary accelerators.
- Focus on your problem and leave the risky, time consuming infrastructure details to the tool suite.
- Save considerable time by replacing multiple processor ecosystems with one used for all domain-optimized processors.

Embedded Development & Engineering Services

- We have a team of 800+ engineers with a vast range of embedded product development experience.
- We offer a wide range of expertise and skills in Automotive, Medical, Industrial Control, Consumer Electronics, Security and other industries.



Thank you!

Please visit our website at www.ashling.com

Case Studies

A sample of development projects completed by Ashling

- Healthcare
- Identification
- Cryptography
- Automotive
- Semiconductor

Healthcare – Software Validation

- **Customer requirement:**

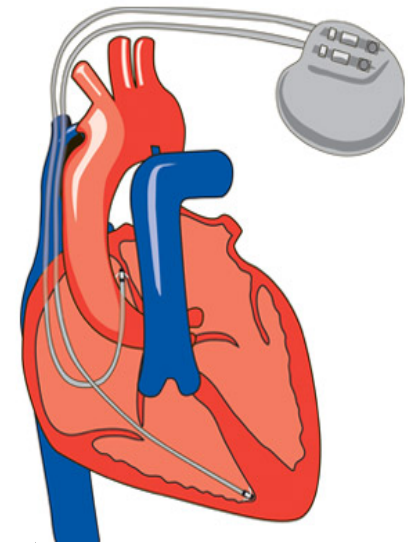
A US medical devices company required a mechanism to validate and certify software running in real-time on a bespoke microcontroller in an SoC device implanted in the human body

- **Solution developed by Ashling**

- Hardware for non-intrusive data capture enabling real-time tra
- Software integrated with IDE to manage user setup and display captured trace data

- **Key Customer Benefits**

- FDA certification achieved
- Time-To-Market requirements exceeded



Healthcare – Remote Access

- **Customer requirement:**

A US medical devices company making eye surgery equipment required a mechanism to provide remote programmatic access to their existing automated surgical equipment

- **Solution developed by Ashling**

- A set of dedicated APIs
- A software package providing remote access and programming support to embedded devices

- **Key Customer Benefit**

- Efficient firmware update mechanism



Identification – Smart Card COS Test

- **Customer requirement:**

A system to develop and test a smart card Operating System, Applications and Cryptographic libraries before availability of first silicon

- **Solution developed by Ashling**

- Windows-based PC/SC software driver
- PC/SC compliant contact and contactless card-reader simulator
- Seamless integration with Instruction Set Simulator (ISS) and Software Development tool-chain

- **Key Customer Benefits**

- System-level simulation
- Faster Time-To-Market



Identification – Smart Card IC Emulator

Customer requirement:

A high performance emulation system for smart card ICs

▪ Solution developed by Ashling

- A dedicated configurable hardware emulation platform with contact and contactless probes to support multiple smart card controller ICs
- A fully featured software debugger
- Hardware based real-time trace, code coverage analysis, and non-intrusive performance analysis

▪ Key Customer Benefits

- Seamless integration of real-time trace, non-intrusive performance analysis and code coverage analysis
- Single debug solution for an entire smart card IC family



Cryptography – Demo Software

- **Customer requirement:**

A mechanism to demonstrate the cryptographic capabilities of secure microcontrollers

- **Solution developed by Ashling**

- A software demonstration package illustrating the cryptographic performance of smart card based secure microcontrollers targeting Electronic Ticketing, Passport and Transaction applications
- Real-time measurement of cryptographic parameters when the smart card is presented to an external hardware card reader

- **Key Customer Benefits**

- Comprehensive demo presenting results with multiple layers of complexity
- Adaptable to different customer audiences based on level of technical knowledge



Automotive – Safety Critical Application

- **Customer requirement:**

To provide documented evidence that Engine Management code is fully tested and meets the safety-critical requirements of Automotive Industry Standards

- **Solution developed by Ashling**

- A high-end debug and trace probe for embedded code development in powertrain applications
- A full-featured Source Debugger with non-intrusive Real Time Trace and Performance Analysis to
 - record, display and log code coverage to help identify redundant code
 - provide proof that the code meets response and performance criteria necessary for product acceptance

- **Key Customer Benefits**

- Proof of compliance with automotive safety standards
- Code efficiency maximized by precise analysis of code execution parameters



Automotive – Secure Gateway

- **Customer requirement:**

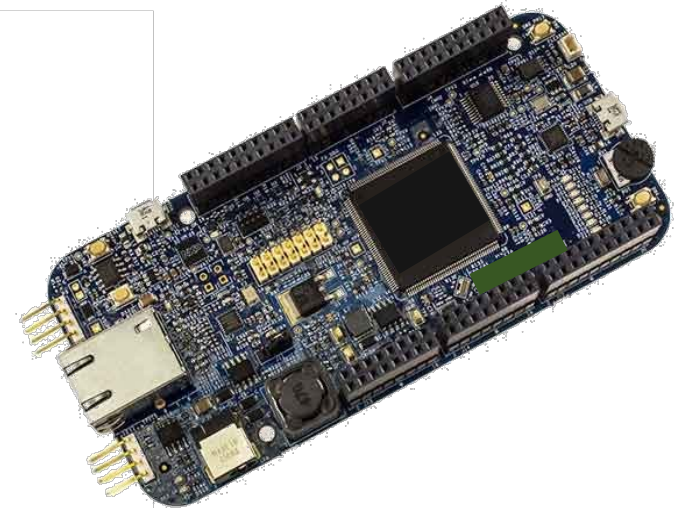
- A Secure Gateway demo platform based on the Power architecture with a dedicated tamper-resistant Secure Element device

- **Solution developed by Ashling**

- “Arduino” format demo platform consisting of Power based Gateway and “Arduino Shield” with the Secure Element linked to the Power device via an SPI interface
- Secure Element (essentially a secure microcontroller) contains all Cryptographic data e.g. symmetric and asymmetric keys and other confidential data

- **Key Customer Benefits**

- Prevents hacker access/control of the vehicle
- Creates a secure “firewall” between the internal vehicle networks and the outside world
- Allows secure, authenticated “over-the-air” firmware updates



Semiconductor – Reference Design

- **Customer requirement:**

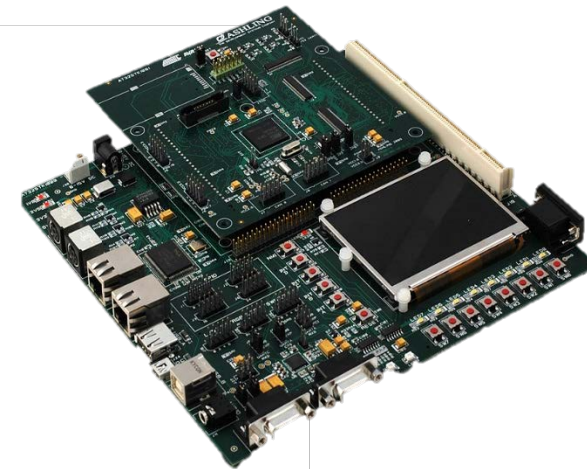
A reference design board for a 32-bit microcontroller

- **Solution developed by Ashling**

- A reference platform board (mother and daughter) including display, flash memory, SDRAM and Linux port
- Support for all major interfaces: USB, RS232, Ethernet, CF/MMC/SD, audio, CAN, NEXUS

- **Key Customer Benefit**

- Single reference design showcasing all functionality and capability



Semiconductor – Development Board

- **Customer requirement:**

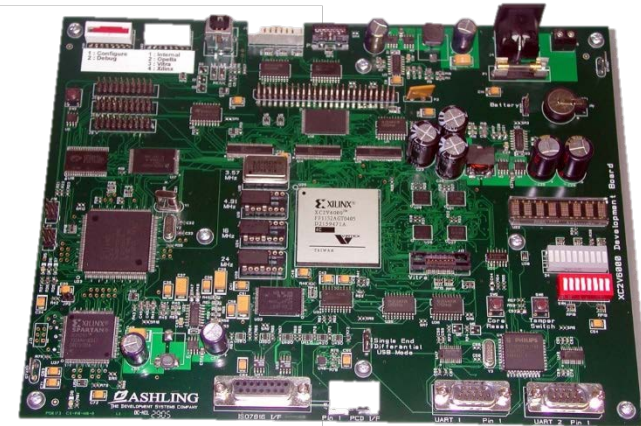
A development board for a smart card secure microcontroller

- **Solution developed by Ashling**

- Board design based on Xilinx FPGA
- ISO7816 smart card interface
- Interfaces to contact and contactless card readers
- EJTAG and PDTrace connectors to support external debug and trace tools

- **Key Customer Benefit**

- Flexible development platform supporting multiple smart card devices

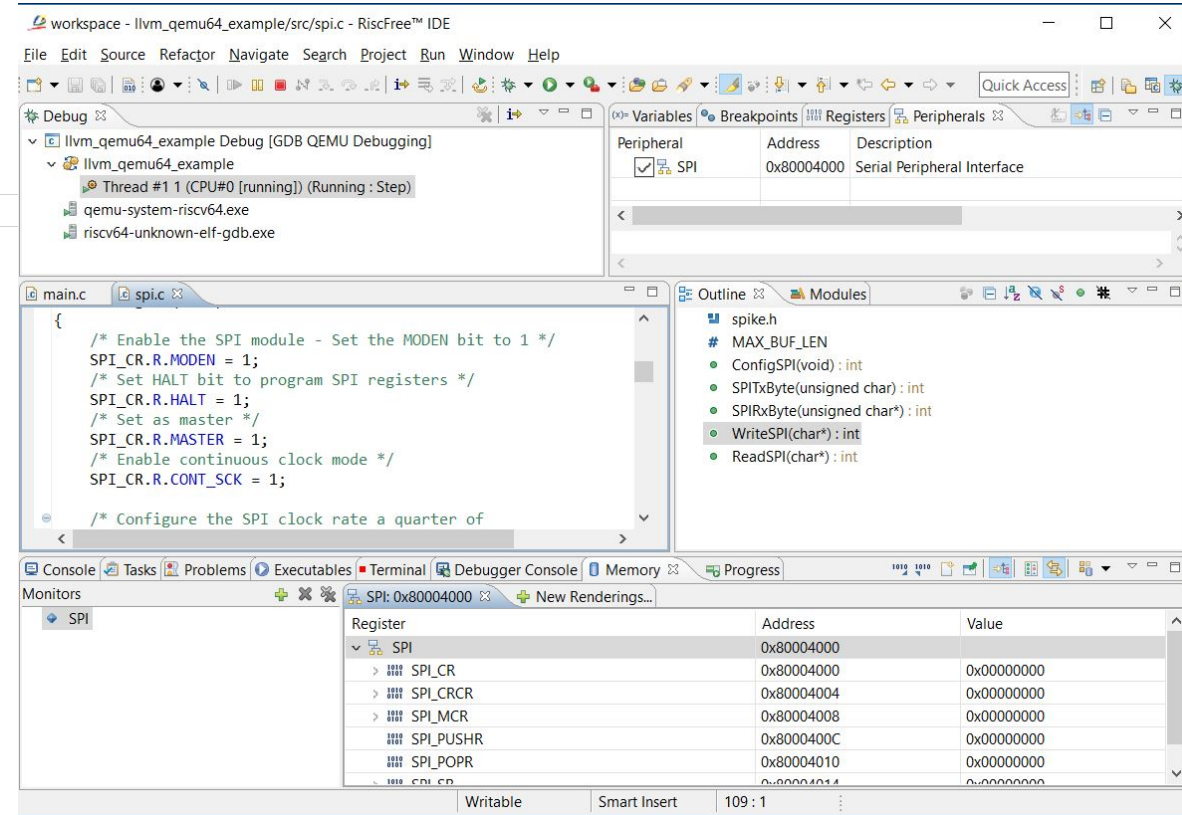


Ashling Tools for RISC-V Cores

RiscFreeTM IDE

RiscFree™ IDE Overview

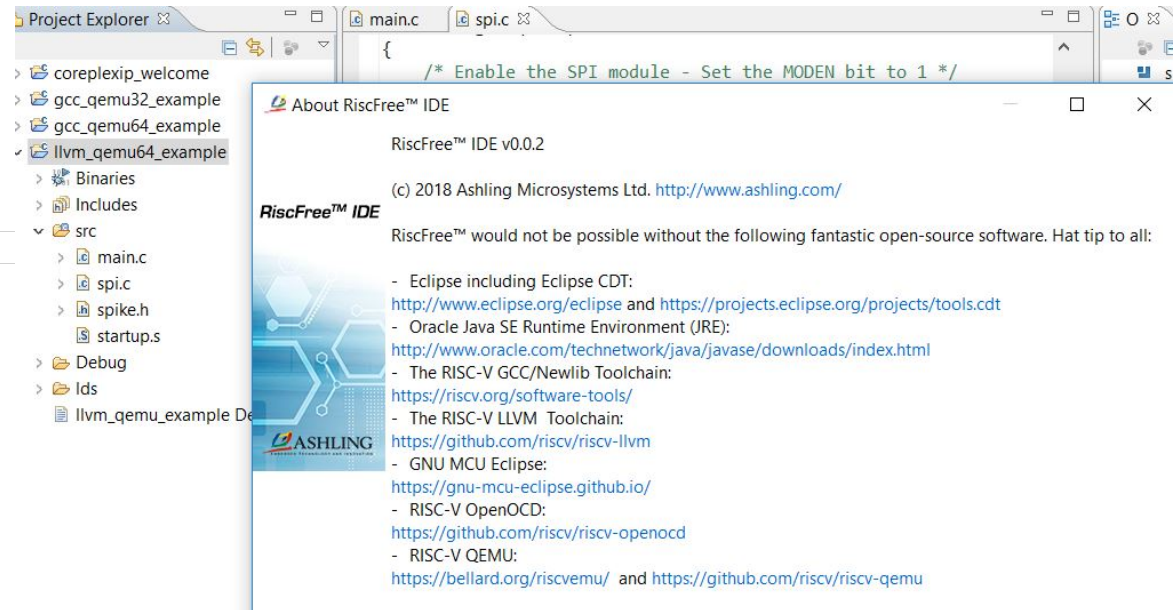
- RiscFree™ is an Eclipse based Integrated Development Environment (IDE) for RISC-V development
- Provides a complete, seamless environment for RISC-V software development including support for writing, building, simulating and hardware debugging
- Includes a single-shot installer that installs and automatically configures all the component tools to work “out-of-the-box” allowing you to begin developing your RISC-V application immediately



RiscFree™ IDE Overview (cont'd)

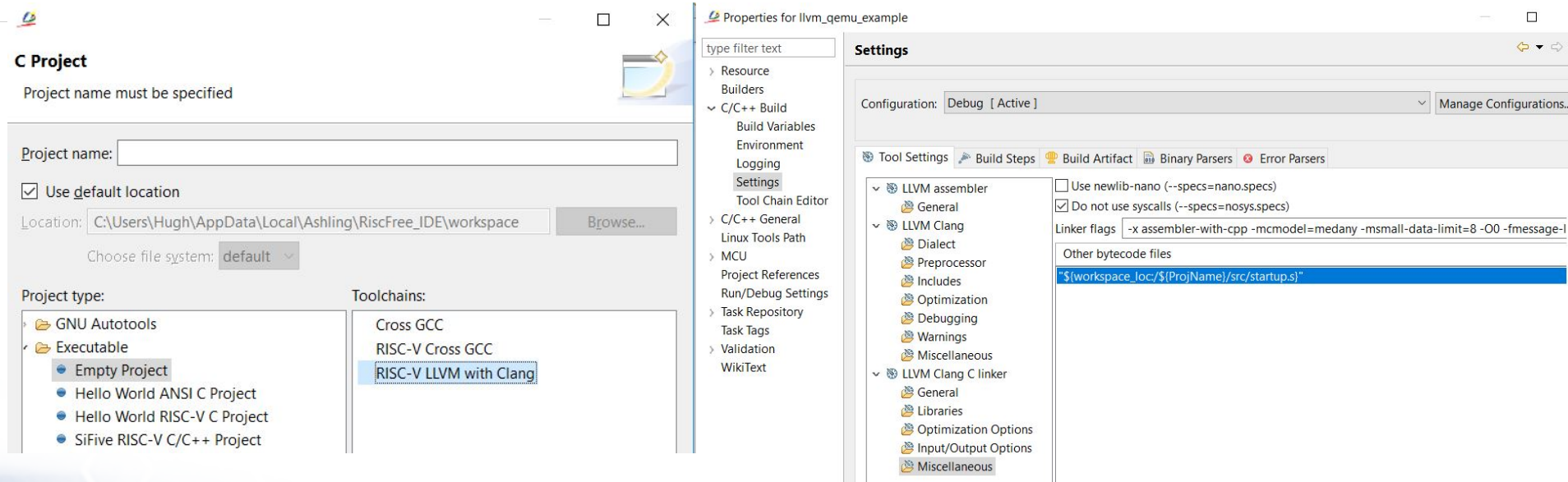
RiscFree™ includes:

- IDE based on latest Eclipse “Oxygen” release
- RISC-V GCC and LLVM compiler toolchains with full build-tool support
- QEMU RISC-V simulator with examples
- High-level RISC-V peripheral viewer
- OpenOCD hardware debug support
- Integrated RXTX serial terminal
- SiFive project wizard, examples and RISC-V device peripheral files



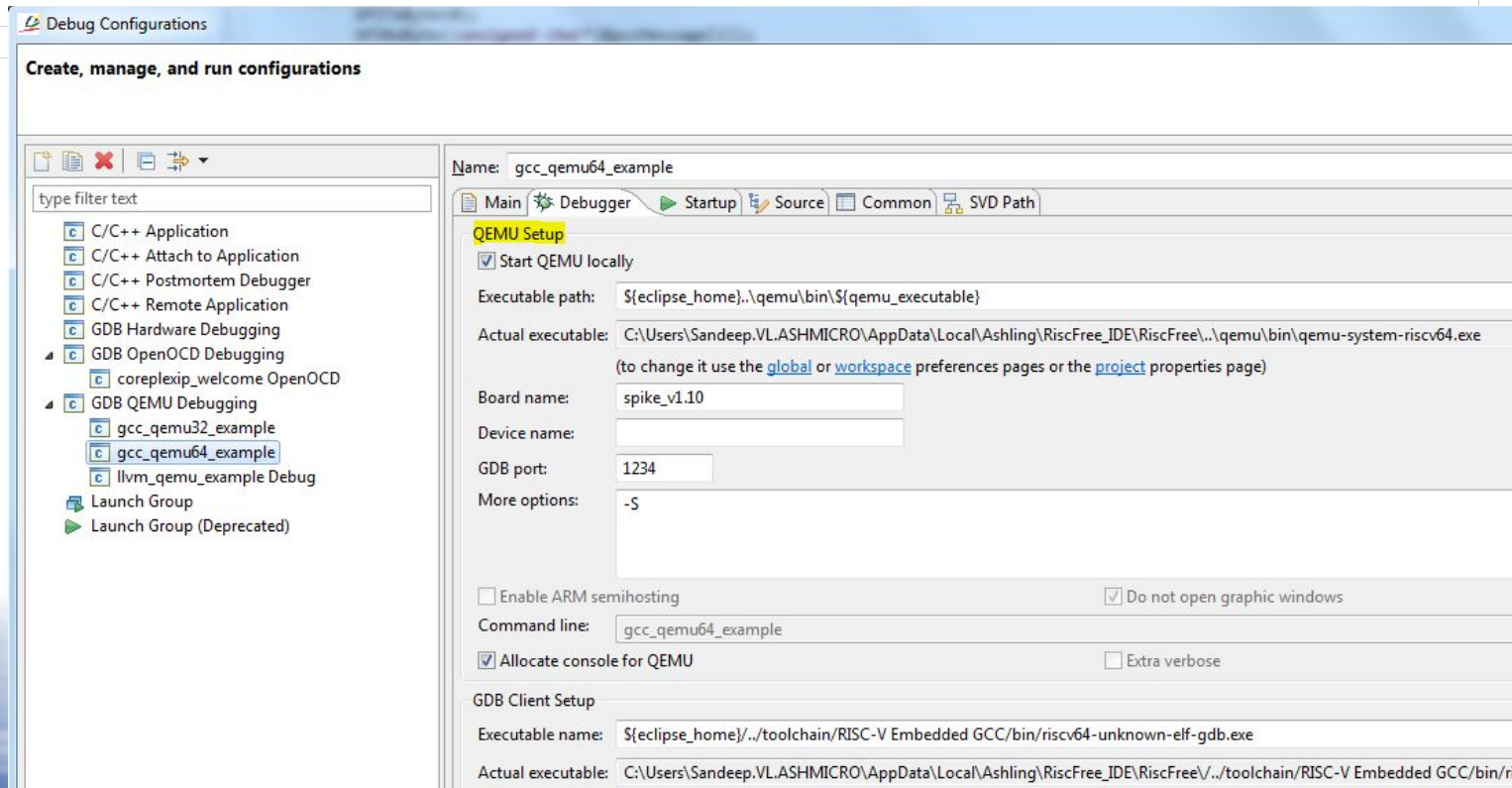
RiscFree™ Compiler Tool-chains

- RISC-V GCC and LLVM compiler toolchains with full build tool support
 - Choose/switch tool-chains on a project basis as you wish



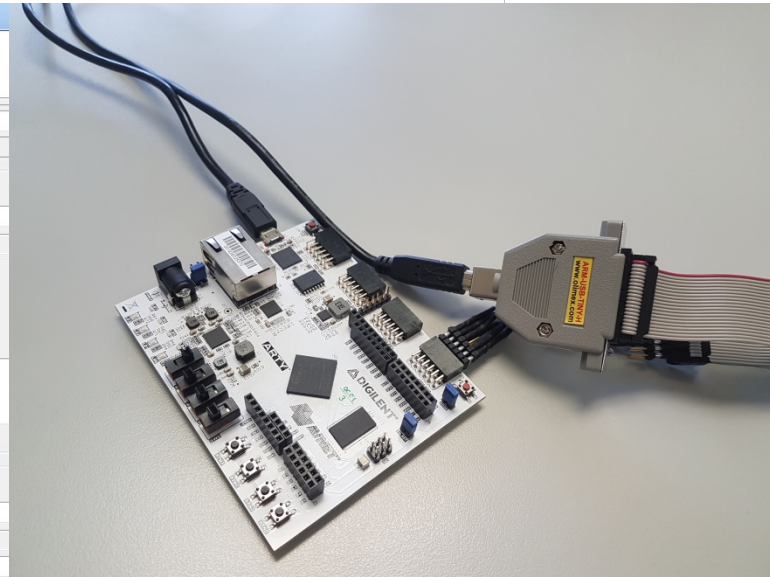
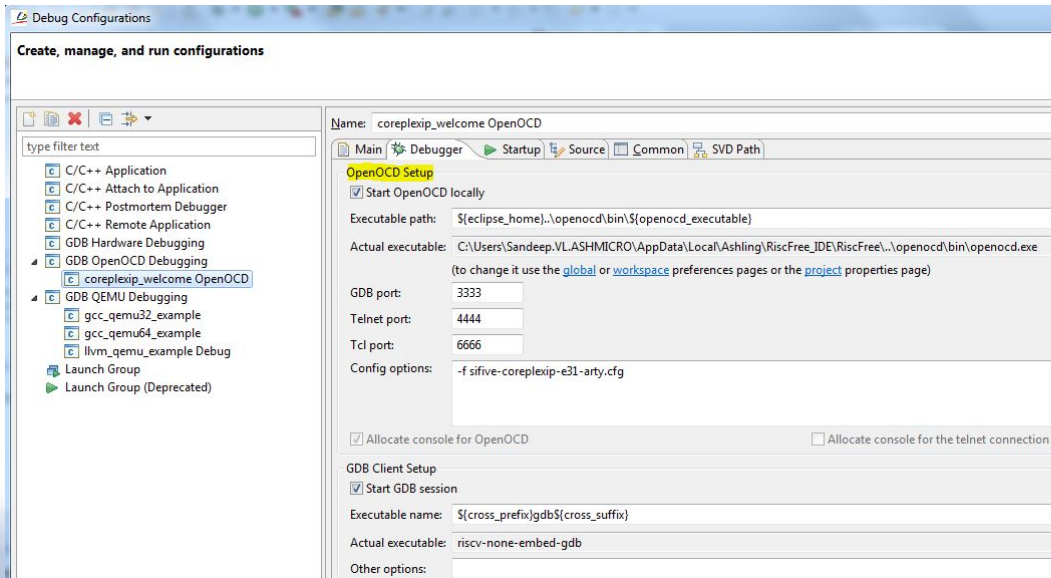
RiscFree™ QEMU Simulator Support

- QEMU ISA simulator for 32-bit/64-bit RISC-V cores using QEMU “Spike” virtual machine
 - Allows debugging without hardware
 - Setup and invocation fully integrated into *RiscFree™* Debug Configuration



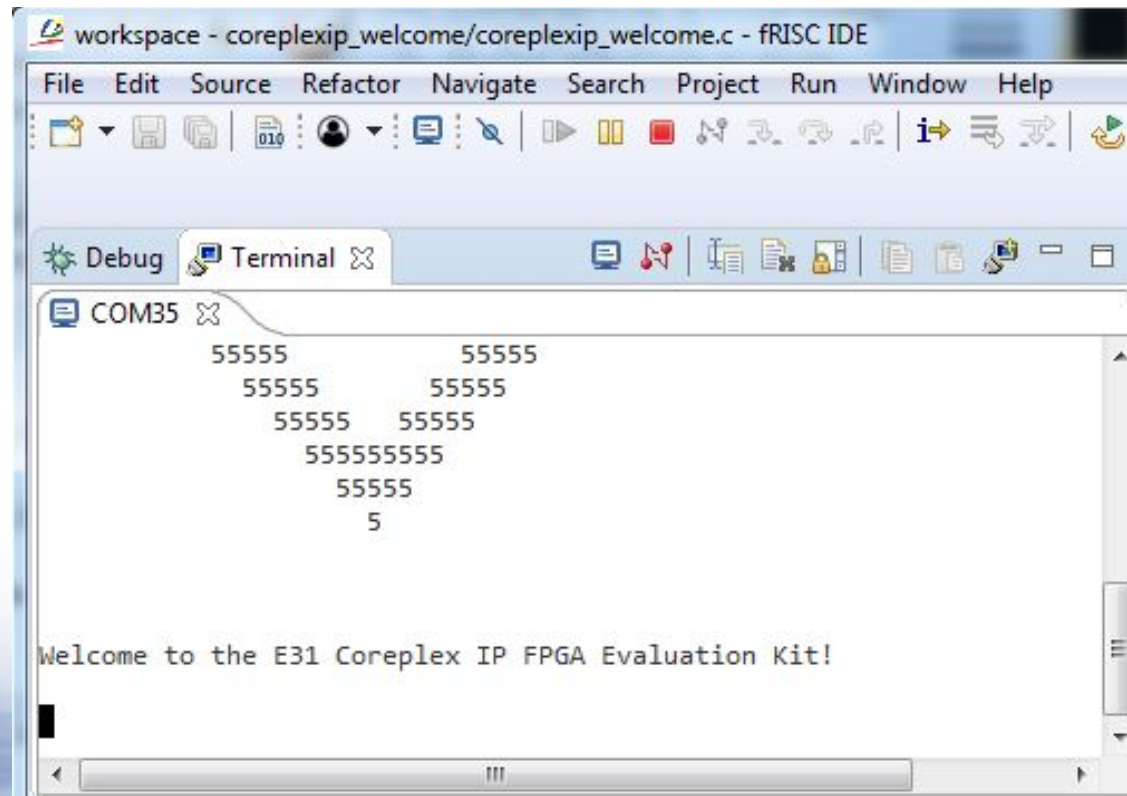
RiscFree™ OpenOCD Support

- OpenOCD support
 - Allows JTAG hardware debugging on reference boards or your RISC-V powered product
 - Setup and invocation fully integrated into *RiscFree™* Debug Configuration
 - For example: below shows use of a JTAG probe to debug the SiFive's E31 RISC-V core running on the Arty board



RiscFree™ RXTX Serial Terminal

- Integrated RXTX Serial Terminal (Eclipse Oxygen)
 - Interact with and view target UART outputs all from within your IDE
 - Requires Serial/USB interface to your target board's UART



RiscFree™ SiFive Wizard and Registers

- Project Creation Wizard and Registers

Project settings
Select the SiFive board and define project options.

Board:

Content:

Use system calls:

Trace output:

Check some warnings ☒

Check most warnings ☐

Enable -Werror ☐

Use -Og on debug ☐

Use newlib nano ☒

Main Debugger Startup Source Common SVD Path

SVD file (used by the peripheral registers viewer)

File path: C:\Users\Hugh\AppData\Local\Ashling\RiscFree_IDE\xsvd\e31arty-xsvd.json

Variables Breakpoints Registers Modules Peripherals

Peripheral	Address	Description
<input checked="" type="checkbox"/> clint	0x02000000	Core Complex Local Interruptor (CLINT) Peripheral
<input checked="" type="checkbox"/> gpio	0x20002000	General Purpose Input/Output Controller (GPIO) Peripheral
<input type="checkbox"/> plic	0x0C000000	Platform-Level Interrupt Controller (PLIC) Peripheral
<input type="checkbox"/> pwm0	0x20005000	Pulse-Width Modulation (PWM) Peripheral
<input type="checkbox"/> spi0	0x20004000	Serial Peripheral Interface (SPI) Peripheral
<input type="checkbox"/> uart0	0x20000000	Universal Asynchronous Receiver/Transmitter (UART) Peripheral

No details to display for the current selection.

main.c main.c Memory

Monitors

gpio: 0x20002000

Register	Address	Value
gpio	0x20002000	0x0000
value	0x20002000	0x0000
inputen	0x20002004	0x0000
outputen	0x20002008	0x0000
port	0x2000200C	0x0000
pue	0x20002010	0x0000
ds	0x20002014	0x0000



Thank you!

Please visit our website at www.ashling.com