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Driving Innovation in Microsystem Packaging /// EPS.IEEE.ORG

PRESIDENT'S COLUMN

Avram Bar-Cohen, PhD, Principal Engineering Fellow, Raytheon—Space and Airborne Systems, Arlington, VA

"…Oh the Times They Are a Changing…"

"…Then you better start swimming or you'll sink like a stone, for the times they are a-changing…"

Bob Dylan, 1964

As we enter 2018, the electronics industry is once again experiencing tremendous expansion and revolutionary change, repositioning electronic packaging as a value creator and product differentiator for broad domains of the semiconductor industry. With growing frequency, packaging is driving change in the microelectronic industry, building on innovations in 2.5D and 3D packaging, compound semiconductor materials, and heterogeneous integration to lay the groundwork for the approaching inflection in IoT technology, a new generation of telecommunication hardware, and the introduction of new computational modalities, from quantum to neuromorphic computing. To keep pace with these changing times, your Society has definitely "started swimming"…..changing its name to the Electronic Packaging Society; electing a new President—yours truly; and refreshing its Board of Governors.

While the IEEE CPMT (*Components, Packaging, and Manufacturing*) Society has been our professional home since 1994, it is sobering to realize that this professional community was born in 1954 as the *Professional Group on Production Techniques* of the IRE and has undergone several name changes in the ensuing years. When I joined IEEE in the 1980's, we were the IEEE *Components, Hybrids, and Manufacturing Society* and had earlier been called the IEEE *Parts, Materials, and Packaging Group* (1965) and the IEEE *Product Engineering and Production Group* (1964). On 5 November 2016, the CPMT BoG voted to rename our Society the IEEE *Electronics Packaging Society* and the change was approved by the IEEE Board in June 2017. The change is motivated by the growing prominence of packaging in the electronics industry and will allow EPS to

- Take ownership of, i.e. Brand, Packaging and Interconnection across all scales and applications;
- Drive industry appreciation for the strategic value of packaging, and
- Gain further recognition within IEEE and the industry as the primary source of packaging science and technology

In my more than 30 years of involvement in CPMT/EPS, I have had the privilege of serving on the BOG and as the Editor-in-Chief of our Transactions, founding and continuing to participate in the governance of the ITHERM Conference, and speaking to many Chapters and student sections as a CPMT/EPS Distinguished Lecturer. Building on that foundation, I am excited to serve as the first President of the Society—under its new name—and to help EPS members, our community, and the industry we serve—negotiate the rapidly changing technological landscape. In the next 2 years your BOG and I will be devoting particular attention to:

- Continuing to enhance the EPS flagship Conferences and regional symposia and workshops,
- Strengthening EPS Chapters and Student Branches (around the world,
- Developing a pathway to future Society and community leadership for young packaging professionals and other underrepresented groups, and
- Supporting the development of the Heterogeneous Integration Roadmap.

Helping in this work will be the new Officers and Directors: Ravi Mahajan (Intel) as VP of Publications, Andrew Tay (SUTD in Singapore) as Director of Student Programs, Jean Trewhella (Global Foundries) as the Junior Past President, and Jie Xue as the Senior

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NEWSLETTER SUBMISSION DEADLINES

1 March 2018 for Spring issue 2018

1 July 2018 for Summer issue 2018

30 August 2018 for Fall issue 2018

1 November 2018 for Winter issue 2019

Submit all material to d.manning@ieee.org

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2019 Term End: Regions 1-6, 7, 9—Li Li; Regions 1-6, 7, 9—David McCann; Regions 1-6, 7, 9—Kitty Pearsall; Regions 1-6, 7, 9—Subramanian S. Iyer; Region 8—Thomas Brunschwiler; Region 8—Gilles Poupon

2020 Term End: Regions 1-6,7,9—Alan Huffman, Sam Karikalan, Xuejun Fan and Jeff Suhling; Region 8—Grace O'Malley; Region 10—Yoichi Taira

Publications

Transactions on Components, Packaging and Manufacturing Technology

Managing Editor:
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Distinguished Lecturers

Program Director: Beth Keser, bkeser@qti.qualcomm.com

Lecturers: Mudasir Ahmad, Muhannad Bakir, Ph.D., Avram Bar-Cohen, Ph.D., Karlheinz Bock, Ph.D., Bill Bottoms, Ph.D., Chris Bower, Ph.D., Moises Cases, William T. Chen, Ph.D., Xuejun Fan, Ph.D., Paul D. Franzon, Ph.D., Philip Garrou, Ph.D., R. Wayne Johnson, Ph.D., Beth Keser, Ph.D., John H. Lau, Ph.D., Ning-Cheng Lee, Ph.D., S. W. Ricky Lee, Ph.D., Johan Liu, Ph.D., Ravi Mahajan, PhD., James E. Morris, Ph.D., Kyung W. Paik, Ph.D., Mervi Paulasto-Kröckel, Ph.D., Michael Pecht, Ph.D., Eric D. Perfecto, Karl J. Puttlitz, Ph.D., Dongkai Shangguan, Ph.D., Nihal Sinnadurai, Ph.D., Ephraim Suhir, Ph.D., Rao Tummala, Ph.D., Walter Trybula, Ph.D., E. Jan Vardaman, Paul Wesling, CP Wong, Ph.D., Jie Xue, Ph.D., Kishio Yokouchi, Ph.D.

Chapters and Student Branch Chapters

Refer to eps.ieee.org for EP Society Chapters and Student Branch Chapters list

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President's Column (*Continued from page 1*)

Past President. They will be joined by the newly elected Members-at-Large: for the Americas—Alan Huffman, Sam Karikalan, Xuejun Fan, and Jeff Suhling; for Africa, Europe, and the Middle East- Grace O'Malley, and for Asia and the Pacific region—Yoichi Taira. It is my great pleasure to add my congratulations and personal welcome to all the new Officers, Directors, and Members-at-Large.

I would also like to acknowledge the ongoing contributions by the returning members of the BOG who have "re-upped" and will continue to serve you in 2018-2019. These include Vice Presidents: Patrick Thompson—Technology, Chris Bailey—Conferences, Beth Keser—Education, and Thomas Reynolds—Finance, as well as the returning Program Directors: Jeffrey C. Suhling—Membership, Kitty Pearsall—Chapters, Eric Perfecto—Awards, William T. Chen—Industry, Toni Mattila—Region 8, and Yasumitsu Orii—Region 10, and the continuing Members at Large: for the Americas—Philip Garrou, Eric Perfecto, Li Li, David McCann, Kitty Pearsall, and Subramanian S. Iyer, for Africa, Europe, and Middle East - Karlheinz Bock, Thomas Brunschwiler, and Gilles Poupon; and for Asia and the Pacific region—C. Robert Kao, Andrew Tay, and Suresh Subramanyam.

It gives me great pleasure to use this opportunity to extend our collective thanks to Jean Trewhella for her stellar and steadfast leadership as President of CPMT for 2016–2017 and wish her well in her future professional activities.

Thank you all for the confidence you have placed in me and I look forward to working with each and everyone of you to strengthen and expand EPS and drive innovation in the microelectronic industry.

ABC
January 2018

EPS NEWS

Willam Chen Receives 2018 IEEE Electronics Packaging Award

Fellow of ASE Group Sunnyvale, California, USA

"For contributions to electronic packaging from research and development through industrialization, and for his leadership in strategic roadmapping efforts."

The IEEE Electronics Packaging Award, sponsored by the IEEE Electronics Packaging Society, recognizes meritorious contributions to the advancement of components, electronic packaging or manufacturing technologies. The technical field for this award includes all aspects of device and systems packaging, including packaging of microelectronics, optoelectronics, RF/wireless and micro-electro-mechanical systems (MEMS), enhancement of technology, impact on the relevant technical community and the profession, benefit to society, and the quality of the nomination.

The 2018 Award will be presented to William Chen at the 68th Electronic Components and Technology Conference (ECTC), May 2018.

William T. Chen is a visionary strategist, lead mentor for innovation, and hands-on engineer. His leadership has led to industrialization of game-changing packaging technologies by enabling miniaturization, cost reduction, and performance enhancements for today's pervasive all-powerful electronic devices. They include development of copper wirebonds replacing gold interconnects, saving industry hundreds of millions of dollars a year and 2.5D packaging high-volume implementation, setting the standard for myriad interconnects in a small package space for applications including high-performance logic and memory. His strategic vision on fan-out wafer-level packaging is critical for meeting future demand for smaller, thinner, and faster electronic systems. Early in his career he pioneered the use of predictive verified modeling integrating micromechanics, materials science, and finite element crucial for generations of electronics products.

William T. Chen (M'92, SM'03, F'06) received his engineering education at University of London (B.Sc), Brown University (M.Sc) and Cornell University (PhD). He joined IBM Corporation at Endicott New York in 1963.

At IBM he worked in a broad range of IBM microelectronic packaging products. He received IBM Division President Award for his leadership and innovation in Predictive Modelling on IBM products. He was elected to the IBM Academy of Technology for his contributions to IBM Products and Packaging Technologies. He retired from IBM in 1997. He joined the Institute of Materials Research and Engineering (IMRE) in Singapore, to initiate research in microelectronic packaging materials and processes. He was appointed to the position Director of the Institute (IMRE) steering the growth in people, funding and research facilities and research direction for IMRE to become the leading materials science and engineering research center in the ASEAN region. In 2001 he joined ASE Group, where he holds the position of ASE Fellow and Senior Technical Advisor. In this assignment he has responsibilities for guidance to technology strategic directions for ASE Group.

He served as President of the IEEE CPMT Society. He is the Co-Chair of the ITRS Assembly and Packaging Roadmap Technical Working Group. He is chair of the Semicon West Packaging Committee. He has been elected to a member of the iNEMI Board. He is a member of the Technology Committee of GSA.

He has been elected to Fellow of IEEE and Fellow of ASME. He has served as an Associate Editor of ASME Journal of Electronic Packaging, and IEEE T-CPMT.

William Chen joins the following past recipients of this Award.

2017—Paul Ho and King-Ning Tu

"For contributions to the materials science of packaging and its impact on reliability, specifically in the science of electromigration."

2016—Michael Pecht
"For visionary leadership in the development of physics-of-failure-based and prognosticsbased approaches to electronic packaging reliability."

2015—Nasser Bozorg-Grayeli
"For contributions to the advancement of microelectronic packaging technology, manufacturing, and semiconductor ecosystems."

2014—Avram Bar-Cohen
"For contributions to thermal design, modeling, and analysis, and for original research on heat transfer and liquid-phase cooling."

2013—John Lau
"For contributions to the literature in advanced solder materials, manufacturing for highly reliable electronic products, and education in advanced packaging."

2012—Mauro J Walker
"For advancing electronic manufacturing, technology and packaging worldwide through technical innovation and cooperative leadership in industry, government, academia, and professional organizations."

2011—Rao R. Tummala
"For pioneering and innovative contributions to package integration research, cross-disciplinary education and globalization of electronic packaging."

2010—Herbert Reichl
"For contributions to the integration of reliability in electronics systems, and leadership in research and education in electronics packaging."

2009—George G. Harman
"For achievements in wire bonding technologies."

2008—Karl Puttlitz Sr. and Paul A. Totta
"For pioneering achievements in flip chip interconnection technology and for semiconductor devices and packages."

2007—Dimitry Grabbe
"For contributions to the fields of electrical/electronic connector technology, and development of multi-layer printed wiring boards."

2006—C. P. Wong
"For contributions in advanced polymeric materials science and processes for highly reliable electronic packages."

2005—Yutaka Tsukada
"For pioneering contributions in micro-via technology for printed circuit boards, and for extending the feasibility of the direct flip-chip attachment process."

2004—John W. Balde
"For lifetime contributions to tantalum film technology and the introduction of new electronic packaging technology to development and manufacturing."

For additional information on this and other IEEE Techni-cal Field Awards and Medals, to view complete lists of past recipients or to nominate a colleague or associate for IEEE Technical Field Awards and Medals, please visit http://www. ieee.org/awards

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EPS Officers and Program Directors For 2018–2019

The Electronics Packaging Society Board of Governors appointed its Officers and Program Directors for the two-year term of 1 January 2018 through 31 December 2019. The following individuals were appointed:

President

Dr. Avram Bar-Cohen is an internationally recognized leader in thermal science and technology, Life Fellow of IEEE, and an honorary member of ASME, currently serving as a Principal Engineering Fellow at Raytheon Corporation—Space and Airborne Systems. His publications, lectures, short courses, and research, as well as his US government and professional service in IEEE and ASME, have helped to create the scientific foundation for the thermal management of electronic components and systems. His current efforts focus on embedded cooling, including on-chip thermoelectric and two-phase microchannel coolers for high heat flux electronic components, thermal control of directed energy systems, and studies of wireless power beaming.

Bar-Cohen served on the Board of Governors of the IEEE CPMT Society, has represented the Society as a Distinguished Lecturer for more than 15 years, and is a past Editor-in-Chief of the CPMT Transactions (1995–2005). In 2014 he was honored by the IEEE with the prestigious CPMT Field Award and had earlier been recognized with the CPMT Society's Outstanding Sustained Technical Contributions Award (2002), the ITHERM Achievement Award (1998) and the THERMI Award (1997). Bar-Cohen received the Luikov Medal from the International Center for Heat and Mass Transfer in Turkey (2008) and ASME's Heat Transfer Memorial Award (1999), Edwin F. Church Medal (1994), and Worcester Reed Warner Medal (1990).

Bar-Cohen recently completed his service (2010–2016) as a Program Manager in the Microsystem Technology Office at the US Defense Advanced Projects Agency in Virginia. From 2001 to 2010 he served as the Chair of Mechanical Engineering and Distinguished University Professor at the University of Maryland and is currently on a leave-of-absence from that institution. From 1998 to 2001 he directed the University of Minnesota Center for the Development of Technological Leadership and held the Sweatt Chair in Technological Leadership. He is a past member of ASME's Board on Professional Development and Board on Research and Technology Development, served a 3-year term as ASME VP of Research (1998–2000) and is also a past President of the Assembly of International Heat Transfer Conferences (2010–2014).

Bar-Cohen is the Editor-in-Chief of WSPC's Encyclopedia of Thermal Packaging and the co-editor of WSPC's "Advanced Integration and Packaging" book series. He has co-authored Dielectric Liquid Cooling of Immersed Components (WSPC, 2013), Design and Analysis of Heat Sinks (Wiley, 1995), and Thermal Analysis and Control of Electronic Equipment (McGraw-Hill, 1983), and has edited/co-edited another 28 books in this field. He has authored/co-authored more than 400 journal papers, refereed proceedings papers, and chapters in books and has delivered some 100 keynote, plenary and invited lectures at major technical conferences and institutions. He holds 8 US and 3 Japanese patents and has advised to completion 70 master's and PhD students at the University of Maryland, the University of Minnesota, and the Ben Gurion University (Beer Sheva, Israel), where he began his academic career in 1972.

Vice President, Technology

Patrick Thompson earned his BS, MS and PhD degrees in Chemical Engineering at the University of Missouri-Rolla. He has more than 25 years of experience in advanced packaging research, development and transfer to manufacturing, contributing to technologies ranging from flip chip fabrication and packaging, flip chip on board and chip scale packages, to multi-chip packaging, MEMS, optoelectronic packaging, and high performance portable packaging. He has led teams at Bell Labs, AMI Semiconductors, and Motorola (now Freescale). Since 2001, he has been a Senior Member of the Technical Staff at Texas Instruments, where he currently leads fine pitch Cu pillar interconnect and TSV packaging technology development.

Pat is active in industry-consortia and industry-university partnerships, including mentoring SRC custom projects and PhD students.

Pat has five patents and over two dozen publications. He has presented packaging tutorials and given invited talks at leading packaging conferences. He is a member of the Electronic Components and Packaging Technology Conference technical program committee, where he has held multiple positions, including General Chair of the 2006 ECTC, and is now the Financial Chair. He has served at both the local and Society level of the EPS holding positions including Member-at-Large of the Board of Governors, Administrative Vice President, and Technical Vice President of the EPS.

Pat has applied his interest in professional education and training and industry-academia interactions in EPS as a member, and current chair of the Awards Committee. He instituted the EPS Student Travel Award, and leads the search for and recognition of outstanding packaging professionals through the EPS major awards. He is also a member of the ECTC Advisory Committee and the EPS Field Award search team.

Vice President, Conferences

Chris Bailey is Professor of Computational Mechanics and Reliability at the University of Greenwich, London, United Kingdom. I received my PhD in Computational Modelling from Thames Polytechnic in 1988, and an MBA in Technology Management from the Open University in 1996. Before joining Greenwich in 1991, Chris worked for three years at Carnegie Mellon University (USA) as a research fellow in materials engineering.

One of Chris's main achievements with regards to EPS was helping to establish the Region 8 flagship conference ESTC (Electronics System-integration Technology Conference). He was the Programme Chair for the first conference held in Dresden, and was the General Chair for the 2008 conference in London. In 2007 he was the local chair for the IEEE EPS sponsored EuroSime conference held in London, and since 2009 has worked with the EuroSime team as co-editor of the proceedings and track chair for multi-physics modelling.

Since 2010 Chris has served as a member of the EPS Board of Governors. During his first term on the BoG, he also took on the role of Strategic Director for Student Programs with the aim of supporting students involved in EPS activities worldwide. Particular achievements include arranging financial support for student attendees at the International Spring Seminar on Electronics Technology (ISSE) as well as promoting student membership at events such as ECTC, EPTC and ESTC.

Other EPS activities that Chris has been involved with include membership of technical committees for EPTC (Singapore), Eurosime (Europe), ISSE (Europe) and ICEP/HDP (China) where he is a regular attendee and presenter. He has also worked closely with others in Europe to help promote closer co-operation between EPS and IMAPS for the benefit of the whole community.

His research has resulted in over 250 publications. He is currently an Associate Editor for the EPS Transactions and has been a guest editor on the journal of Soldering and Surface Mount Technology. He is also a committee member of the Innovative Electronics Manufacturing Research Centre (IeMRC) in the UK and has participated in a number of UK Government sponsored overseas missions to promote collaboration and review electronic packaging technologies. Recently he became a member of the working group writing a new IEEE standard for Prognostics and Health Management for Electronic Systems.

Vice President, Publications

Ravi Mahajan is an Intel Fellow and the Co-director of pathfinding and assembly and packaging technologies for 7-nanometer (7 nm) silicon and beyond in the Technology and Manufacturing Group at Intel Corporation. He is responsible for planning and carrying out multi-chip package pathfinding programs for the latest Intel process technologies. Ravi also represents Intel in academia through research advisory boards, conference leadership and participation in various student initiatives.

Ravi has led efforts to define and set strategic direction for package architecture, technologies and assembly processes at Intel since joining the company's Assembly and Test Technology Development organization in 2000, spanning 90 nm, 65 nm, 45 nm, 32 nm, 22 nm and 7 nm silicon. Earlier in his Intel career, he spent five years as group manager for thermal mechanical tools and analysis. In that role, Mahajan oversaw a Thermal-Mechanical Lab chartered with delivering detailed thermal and mechanical characterization of Intel's packaging solutions for current and future processors.

A prolific inventor and recognized expert in microelectronics packaging technologies, Mahajan holds more than 30 patents, including the original patent for a silicon bridge that became the foundation for Intel's Embedded Multi-Die Interconnect Bridge technology.

His early insights also led to high-performance, cost-effective cooling solutions for high-end microprocessors and the proliferation of photo-mechanics techniques used for thermo-mechanical stress model validation. Ravi has written several book chapters and more than 30 papers on topics related to his area of expertise.

Ravi joined Intel in 1992 after earning a bachelor's degree from Bombay University, a master's degree from the University of Houston, and a Ph.D. from Lehigh University, all in mechanical engineering. His contributions during his Intel career have earned him numerous industry honors, most recently the SRC's 2015 Mahboob Khan Outstanding Industry Liaison Award, the 2016 THERMI award from SEMITHERM and the 2016 Allan Kraus Thermal Management Medal from the American Society of Mechanical Engineers. He has also been nominated as an IEEE EPS Distinguished Lecturer. He is one of the founding editors for the Intel Assembly and Test Technology Journal (IATTJ) and currently Co-Editor for Special Topics of IEEE T-CPMT. Additionally he has been long associated with ASME's InterPACK conference and was Conference Co-Chair of the 2017 Conference. Ravi is a Fellow of two leading societies, ASME and IEEE. He was named an Intel Fellow in 2017.

Vice President, Education

Beth Keser, Ph.D., a recognized global leader in the semiconductor packaging industry with over 19 years of experience, received her B.S. degree in Materials Science and Engineering from Cornell University and her Ph.D. from the University of Illinois at Urbana-Champaign. Beth's excellence in developing revolutionary electronic packages for semiconductor devices has resulted in 15 patents, 8 patents pending, and over 40 publications in the semiconductor industry. Based in Munich, Germany, Beth leads the Wireless Packaging Solutions Department at Intel Corporation in the iCDG Business Unit.

Previously, Beth led Qualcomm's Fan-Out and Fan-In Wafer Level Packaging Technology Development and NPI Group for over 7 years where her team qualified over 50 products resulting in over 7 billion units shipped—technology consumers around the world enjoy in cell phones today.

Before joining Qualcomm in 2009, Beth was instrumental in developing 2 packaging technologies during her career at Motorola and Freescale Semiconductor. Beth led the Wafer-Level Chip Scale packaging team at Motorola, which included directing the activities of process engineering, package characterization, package reliability, and mechanical modeling. In addition, Beth was the lead technologist and manager of the Redistributed Chip Packaging Technology (RCP). She led the team that developed this technology for 6 years and filed 6 patents on this technology.

Beth has been IMAPS Device Packaging Conference Technical Chair 2006–2009, IMAPS Flip Chip/CSP Sub-committee member 2000–2009 and chair 2005–2008, and SMTA's International WLP Conference WLP Track Chair 2010–2011. Beth has taught a Professional Development Course on Fan-Out Wafer Level Packaging at conferences since 2015.

Beth is an IEEE Senior Member whose volunteer activities and professional society responsibilities include: ECTC Executive Committee 2010–17, ECTC Advanced Packaging Sub-committee member 2000–present, and has co-authored 16 papers (2000–1, 2003, 2007–8, and 2011–17) at ECTC. Beth is also an IEEE EPS Distinguished Lecturer who chaired IEEE EPS's 65th Electronic Component and Technology Conference.

Vice President, Finance

Thomas G. Reynolds III received his PHD from Brown University in 1972 where he worked on synthetic inorganic chemistry of electronic materials. His MS (1966) and BS (1964) were from the University of Virginia in Materials Science and Mechanical Engineering respectively. Tom has worked in the field of electronic ceramic materials and other advanced technologies for more than 35 years.

Retiring in 2003, from 1992 Tom was the Director of Technology at Murata Electronics N.A., Inc. He has worked in the areas of leading edge designs in decoupling capacitors, hard disk drive activation, LTCC modules, and integrated passive components. He has acted as liaison between American designs and Asian development activities, as well as in merger and acquisition analysis. Prior to joining Murata, Dr. Reynolds worked for Philips Electronics for 18 years in both the US and Europe, developing processes and methods for electronic (dielectric) ceramics, and from 1968 to 1973 he was staff scientist at Texas Instruments.

Tom has been involved with EPS and ECTC (Electronic Components Technology Conference) for more than 19 years. He was General Chair for ECTC in 2000 and was active for several years following this as Finance Chairman. He is also a Senior Member of IEEE. Tom has been a member of the EPS Board of Governors since 2004 and VP of Finance since 2006. In addition he is currently serving as Treasurer of the ECTC.

Additional activities and responsibilities include Treasurer of the Ft Walton Sail & Power Squadron of the United States Power Squadron and he was Commodore of the Ft Walton Yacht Club in 2006. Tom also served on the Board and the Finance Committee of that Club from 2007–2010. Tom is also a Founding Member of the Florida Commodores Association—an association of more than 250 with the goal of fostering communication, guidance and mentoring of past present and future leaders. Tom is also a member of the Institute for Senior Professionals (North West Florida State College), an association of business, professional, medical and military professionals to advise and serve the local community based on their experience and expertise.

Program Director, Membership Programs

Jeffrey C. Suhling received a B.S. degree in Applied Mathematics and Physics, and M.S. and Ph.D. degrees in Engineering Mechanics from the University of Wisconsin, Madison, WI. He joined faculty of the Department of Mechanical Engineering at Auburn University in 1985, where he currently holds the rank of Quina Distinguished Professor. Dr. Suhling co-established the NSF Center for Advanced Vehicle and Extreme Environment Electronics (CAVE3) in 1998, and served as Center Director from 2002–2008. CAVE3 is a government and industry sponsored research center involving over 20 member companies, 15 faculty, and 35 graduate students that specializes

in reliability of electronic packaging in harsh environments. In 2008, he was appointed Department Chair of the Department of Mechanical Engineering, which is the largest program at the University with over 1000 undergraduate students and 150 graduate students. He was selected "Outstanding Mechanical Engineering Faculty Member" by the undergraduate students during 1990, received the College of Engineering Birdsong Superior Teaching Award in 1994, and received the College of Engineering Senior Research Award in 2001. He has advised 75 graduate students at Auburn University, including 27 Ph.D. students and 48 M.S. students.

Dr. Suhling has been an active researcher in electronic packaging for over 25 years. His general areas of interest are in the mechanics and reliability of packaging. Specializations include silicon sensors for packaging stress and temperature measurements, stress effects in silicon devices, test chips, mechanical characterization of packaging materials including solders and polymers, solder joint reliability and aging effects, and finite element modeling. He has authored or co-authored over 375 technical publications, including 6 books and book chapters, 55 journal articles, and 325 conference proceedings papers. Six of his conference papers have been selected as the Best of Conference. These include Best Session Paper Awards at the 2005 and 2010 ECTC Conferences, as well as Best Paper Awards at the 1998 and 2002 IMAPS Annual Conferences, 2008 SMTA International, and 2013 InterPACK Conference. In addition, he and his co-authors have received Best Poster awards at the InterPACK 2007, InterPACK 2009, and InterPACK 2013 conferences.

Dr. Suhling is a member of IEEE/EPS, ASME, IMAPS, and SMTA. In IEEE, he has served on the ECTC Applied Reliability program committee for the past 10 years. He was appointed to the ECTC Professional Development Course (PDC) program committee in 2006, and has served as Assistant Chair from 2008—Present. He has also been active in the IEEE/EPS ITHERM Conference series, serving on the program committee for over 10 years. In ASME, Dr. Suhling served as Chair of the Electrical and Electronic Packaging Division (EPPD) during 2002–2003, and was on the EPPD Executive Committee from 1998–2003. Dr. Suhling was the Technical Program Chair of the InterPACK '07 Conference, and General Chair of the InterPACK '09 Conference. He was elected a Fellow of ASME in 2009, and was recognized with the ASME-EPPD Mechanics Award for outstanding contributions to electronic packaging research.

Program Director,
Chapter Programs

Kitty Pearsall received the BS degree in Metallurgical Engineering (1971) from the UT El Paso. Kitty received the MS and Ph.D. degree in Mechanical Engineering and Materials from the UT Austin in 1979 and 1983 respectively. Kitty worked for IBM from 1972 to 2013. In 2005 Kitty was appointed an IBM Distinguished Engineer and was elected to the IBM Academy of Technology. Kitty was a process consultant and subject matter expert working on strategic initiatives impacting component qualification and end quality of procured commodities. She engaged with worldwide teams implementing cross-brand, cross commodity processes/products that delivered high quality/high reliability end product.

Kitty received 4 IBM Outstanding Technical Achievement Awards; holds 9 US patents; 2 patents pending; and 8 published disclosures. She has numerous internal publications as well as 22 external publications in her field. Kitty is a licensed Professional Engineer (Texas since 1993). Kitty was the recipient of the UT Austin—Cockrell Engineering Distinguished Engineering Graduate Award in 2007 followed by induction into the UT Mechanical Engineering Dept. Academy of Distinguished Alumni in 2008. Kitty was awarded the Women in Technology Fran E. Allan Mentoring Award (2006) in recognition of her people development both in and outside of IBM. Currently Kitty is President of Boss Precision Inc. and works as an Independent consultant. This has included a one year engagement with Shainin Corporation.

Kitty is an active member in IEEE and EPS. She is a member of TMS, American Society of Metals, and WIE. Kitty has more than 22 years' experience with ECTC serving as a member of the ECTC Manufacturing Technology Committee (1993–2013) and as the Professional Development Course Chair since 2006. During Kitty's 10 years on the EPS Board of Governors she has served in many roles: Member at Large, Strategic Awards Director, VP of Education and currently Director of Chapter Programs. In each role Kitty made key contributions.

Kitty introduced the Regional Contribution Awards. She established the baseline for the EPS Distinguished Lecturer's (DLs) Program. The history of the DLs presentations to Universities, Research Centers, Conferences and EPS Chapters was charted to determine if the program was meeting its founding principal; i.e., primarily supporting the EPS chapters. Review of the data noted that this was not the case. Therefore Kitty focused on increasing Chapter usage which did improve over time. DL Budget tracking of planned versus actuals was initiated. Lastly, Kitty documented the roles and responsibilities of the VP Education and passed these on to the new VP. As Director of Chapter Programs Kitty is focusing on worldwide Chapter Communication as well as ensuring Chapters know their benefits and how to access them. First deliverable was a Worldwide Chapter Communication Survey highlighting best practices amongst them.

Program Director,
Awards Programs

Eric Perfecto has 28 years of experience at IBM working in the development of advanced packages for high-end systems. He holds an M.S. in Chemical Engineering from the University of Illinois and an M.S. in Operations Research from Union College.

Until 2000, Eric worked on the development and implementation of multi-level thin films on ceramic substrates, leading projects in photolithography, chemical etching, photosensitive polyimide, pattern electroplating and bonding metallurgies for C4 joining, wire-bonding and LGA. Later, he led the development of the thin film transfer technology including the joining materials and processes. He is currently the C4 Development Chief Technologist responsible for UBM and Pb-free solder implementation and yields improvements for server, ASICs and 3D applications. His technical interests include chip-package

interaction, electromigration, 3D interconnect, and design for manufacturing.

An author of more than 50 technical papers, Eric received two Best Conference Paper Awards (2006 ESTC and 2008 ICEPT-HDP) and the 1994 Prize Paper Award from CPMT Trans. on Adv. Packaging. He holds over 35 US patents and has been honored with two IBM Outstanding Technical Achievement Awards: one for the development and implementation of Cu-Polyimide structures, and the other for the development and implementation of 150 um pitch C4 technology.

Eric served as the 57th ECTC General Chair in Reno, the 55th ECTC Program Chair, the ECTC Materials and Processes Subcommittee Chair ('02-'03), and is currently the ECTC Publicity chair. He has achieved senior member status from IEEE, IMAPS and Society of Plastic Engineers, and is a member of the Society of Hispanic Engineers. Current volunteer activities include chairing the mentoring committee of the IBM East Fishkill Technical Vitality Council, and frequently serves as a judge at the Dutchess County Science Fair, NY.

Eric is currently an elected member of the Board of Governors of the EPS where he serves as the Program Director, Awards Programs. He is an Associate Editor for the EPS Transactions.

Program Director, Student Programs

Andrew Tay is currently a Senior Research Fellow at the Singapore University of Technology and Design. Prior to this he was a Professor in the Department of Mechanical Engineering, National University of Singapore (NUS). He obtained his B.E. (Hons I and University Medal) and PhD in Mechanical Engineering from the University of New South Wales, Australia. His research interests include thermo-mechanical failures, thermal management of electronics and EV battery systems, reliability of solar photovoltaic modules and fracture mechanics. To date he has published more than 250 technical papers, 4 book chapters, 7 keynote presentations, 11 invited presentations, 3 panel discussions, and co-edited 4 conference proceedings and two special issues of technical journals.

Dr Tay was the inaugural General Chair of the 1st and 2nd Electronics Packaging Technology Conference (EPTC) in 1997 and 1998. Since then, he has been in the organising committee of EPTC. In 2006 he was appointed the inaugural Chairman of the EPTC Board, charged with steering the development of EPTC, and is currently again serving as its Chairman. He has been in the Executive Committee of the Singapore Joint Reliability/EPS/ED Chapter since 2000 and was its Chairman from 2010–2011. He has been involved in the international advisory boards and program committees of more than 108 electronics packaging conferences worldwide including DTIP, ECTC, EMAP, EPTC, EuroSimE, HDP, ICEPT, IEMT, IMPACT, InterPack, ITHERM and THERMINIC.

Dr. Tay was an Associate Editor of the *ASME Journal of Electronics Packaging*, an editorial board member of several journals including *Microelectronics Journal* and *Finite Elements in Analysis and Design*, and a guest editor of a special issue on *Microelectronics Reliability*.

He has contributed significantly as a member of the IEEE EPS Education Committee from 1998 to 2007 where he helped to evaluate projects on web-based educational modules.

From 1998 to 2005, he coordinated the implementation of the Specialized Manpower Program in Electronics Packaging and Wafer Fabrication which was funded by the Singapore Economic Development Board. He has taught many professional short courses at packaging conferences. He has been awarded competitive research grants exceeding $14 Million for electronics packaging projects.

He has received the following major awards: 2012 IEEE CPMT Exceptional Technical Achievement and 2012 IEEE CPMT Regional Contributions Award, 2004 ASME Electronics & Photonics Packaging Division Engineering Mechanics Award, 2000 IEEE Third Millennium Medal, 2000 Special Presidential Recognition Award.

He has been an IEEE member since 1991, an ASME member since 1993, an ASME Fellow since 2004 and a Fellow of the Institution of Engineers (Singapore) since 2004.

Program Director, Industry Programs

William T. Chen received his engineering education at University of London (B.Sc), Brown University (M.Sc) and Cornell University (PhD). He joined IBM Corporation at Endicott New York in 1963.

He is the 2018 recipient of the IEEE Electronics Packaging Technical Field Award. Please refer to Dr. Chen's full bio under the 2018 Electronics Packaging Award.

Program Director, Region 8 Programs

Toni Mattila is a research scientist and docent at Aalto University in Helsinki, Finland where he leads a research team that focuses on the reliability of electronic devices. He received his Ph.D. degree in electrical engineering in 2005 and an M.Sc. degree in materials science and engineering in 1999 from the Helsinki University of Technology (HUT). Since 1996, he has been working with electronics production technologies and reliability of electronic devices both in industrial and academic settings. Before joining HUT in 1999 he worked in Tellabs and Nokia.

Toni's research has focused on electronics production technologies, soldering in electronics, failure mechanisms of electronic assemblies, MEMS technologies, and the development of improved methods for reliability assessment and lifetime prediction. Within the framework of his research Toni has been working in close cooperation with international electronics industry, research institutions and universities. His research has so far resulted in over fifty publications in scientific and technical journals and conferences. In addition, Toni has authored seven book chapters, held several professional tutorials during conferences and been a frequent speaker at conferences, seminars and technology fairs. He is also a frequent reviewer in several scientific journals, including EPS Transactions.

Since 2008, Toni has been Chairman of the EPS Finland Chapter. During this time he has, together with other board members, developed and revitalized local activities. More than 100 people attend seminars and events organized by the EPS Finland chapter annually. He has also established firm connections between the EPS chapters in Scandinavia. Toni is currently an elected member of the Board of Governors of the EPS.

Toni also works actively in the IEEE Finland Section, where he has been a member of the executive committee since 2008, and served in various positions. Other IEEE activities include, for example, a membership of technical committees for all three Electronics System Integration Technology Conferences (ESTC). In the past he has also acted in several other positions of trust. For example, he has been the chairman of a housing association for ten years.

Program Director, Region 10 Programs

Yasumitsu Orii received the B.S. in Material Science from the Osaka University, Japan and the Ph.D. from the Osaka University, Japan as well.

Dr. Yasumitsu Orii joined IBM Japan in 1986 and is a leading expert on Flip Chip organic packages, which have contributed to the performance improvements and miniaturization of such products as servers, laptop computers, and HDDs. The packaging technology is becoming more important for next generation server products as Moore's Law reaches its limits. His flip chip expertise extends into many related areas. Initially, he was a pioneer of flip chip on FPC (Flexible Printed Circuit) for HDDs, which allowed the read/write amplifier ICs to be mounted on the suspension and much closer to the GMR head. Later, he developed the C2 (Chip Connection) technology that supported low-cost 50-µm-pitch flip chip bonding for the commodity consumer electronics market and it was licensed to a company in Taiwan.

Currently he is a senior manager of IBM Research Tokyo Science & Technology division and a Senior Technical Staff Member as well as IBM Academy member is leading the next generation flip chip organic package, 3D-IC projects and Neuromorphic Computing at IBM Research Tokyo for IBM Servers and creating new technologies under a Joint Development Program involving many leading Japanese materials companies.

Dr. Yasumitsu Orii has served co-chair of IEEE EPS High Density Substrates & Boards and ECTC EPS Seminar since 2015 and he is the board member of IEEE EPS Japan Chapter. And he has contributed to ICSJ(IEEE CPMT Symposium Japan) as an invited speaker since 2012.

He received Best Paper Award at the 2008 ICEPS (International Conference on Electronics Packaging) , Outstanding Paper Award at the IMPACT 2011, JIEPS Annual Best Paper award in 2011 , IMAPS Sidney J. Stein International Award in 2012, JIEPS Annual technical award in 2014 and IMAPS Fellow award in 2015. And he had been the chair of Technical Program Committee in ICEPS 2009-2011 responsible for technical program editing and paper selection. He was the general chair of ICEP-IAAC(IMAPS All Asia Conference) 2012 in Tokyo.

Newly-Elected and Appointed Members of the Electronics Packaging Society Board of Governors

In 2017, EPS members elected new Members- at-Large to the EPS Board of Governors for the three-year term of 1 January 2018 through 31 December 2020.

Regions 1-6, 7 & 9

ALAN HUFFMAN (M: 2005, SM: 2007) is currently the Director of Engineering for Micross Advanced Interconnect Technology in Research Triangle Park, NC. He received the B.S degree in physics from The University of North Carolina at Chapel Hill in 1994. From 1994 to 2005 he was a Member of the Technical Staff at MCNC Research & Development Institute working on development and implementation of wafer level packaging technologies, reliability and failure mode analysis of flip chip devices, and optoelectronic and MEMS packaging. In 2005, he joined RTI International and was a Senior Research Engineer and Program Manager for WLP technology with RTI's Electronics and Applied Physics Division. His technical interests include wafer level packaging and flip chip process technology and fine pitch bump interconnect, 2.5D and 3D integration technology, characterization and process development for electronic materials used in WLP. He has authored or co-authored numerous papers and presentations on a number of advanced packaging topics, particularly on high density interconnect technologies and characterization of polymer material processes.

Member of IEEE and EPS since 2005, Elevated to Senior Member in 2007, Member of ECTC Interconnects technical sub-committee from 2005-2013, Chaired multiple ECTC technical sessions during this period

Member of ECTC Executive Committee 2011-present, 2016–17—Jr. Past General Chair, 2015–16—General Chair

2014–15—Vice General Chair, 2013–14—Program Chair, 2012–13—Asst. Program Chair, 2011–12—Web Administrator

10 year ECTC service recognition, May 2015, EPS Santa Clara Valley Chapter invited dinner meeting speaker, Sept 13, 2007, Appointed to CPMT Board of Governors in 2016 to fill Member-at-Large position

Member of ad hoc branding committee working on the society name change to IEEE Electronic Packaging Society

SAM KARIKALAN (M: 1995, SM: 2015) has 30 years of experience in the Semiconductor and Electronic Systems Industry. He is currently a Senior Manager of Package Engineering R&D at Broadcom Limited, responsible for Electrical, Thermal and Mechanical design analysis and optimization of IC Packages and co-design of IPs and Systems. Prior to Broadcom, Sam held in

technical or managerial positions at STATS ChipPAC, Primarion and Advanced Micro Devices, working on IC Package Design for Signal/Power Integrity and Electromagnetic Compatibility (EMC).

Before entering the semiconductor industry in 1998, Sam was a scientist at SAMEER-Centre for Electromagnetics in India, for over a decade, working on EMI/EMC Research & System Design and Radar technology. His current interests include Packaging Technologies for Performance Scaling, such as 2.5D/3D Integration, Design for Performance & Reliability, and Design for Test & Manufacturing. Sam holds a B.E. degree in Electronics & Communications Engineering from Bharathiar University, Coimbatore, India.

Sam has authored / co-authored 14 Conference/Journal papers on IC Packaging, Signal Integrity and EMI/EMC. He also has 20 issued US patents and several pending patents to his credit, on Interconnect design, 2.5D/3D Packaging and EMI/EMC. Sam has delivered few hundred hours of training lectures on Signal/Power Integrity and EMI/EMC at locations all across the globe, including two PDCs at the IEEE Electronic Components and Technology Conference (ECTC).

Sam has been a member of the IEEE for over 20 years and he is currently a Senior Member, with memberships in EP, EMC and MTT Societies. He has been very active in local chapters and sections in Singapore, Phoenix and Orange County (California), in various leadership roles, including the founding chairperson of the EPS Orange County chapter. Sam has received several awards for his contributions to the IEEE, including the 2014 IEEE CPMT Regional Contributions Award—Regions 1-6, 7, 9 (US, Canada, Latin America) and the 2012 Outstanding Leadership Award from the Orange County Section. Sam has been serving on the Technical Program Committee and the Executive Committee of the IEEE ECTC since 2006 and he is the General Chair of ECTC 2018.

XUEJUN FAN (M: 2002, SM: 2006) is a currently a professor in the Department of Mechanical Engineering at Lamar University, Beaumont, Texas. Over 25 years he has made many significant and distinguished contributions and outstanding achievements in several important fields encompassed by the IEEE EP Society. He is a well-known and internationally recognized expert in thermal and thermo-mechanical reliability, modeling and characterization of electronic materials, IC packaging and reliability, and LED packaging and system integration. He received the Outstanding Sustained Technical Contribution Award in 2017 and the Exceptional Technical Achievement Award in 2011. His papers received the Best Paper Award in IEEE Transactions on Components and Packaging and Technology in 2017 and 2008, respectively.

Dr. Fan received his PhD from Tsinghua University, Beijing, China in 1989. He became a full professor in 1991, at the age of 27, at Taiyuan University of Technology (TUT), China. He was one of the youngest professors in China at that time. Dr. Fan served as Associate Department Chair (1990–1993) and the Director of Institute of Applied Mechanics (1994–1997) at TUT. He was Visiting Professors at the University of Tokyo, Japan (1993–1994), and the University of British Columbia, Canada (1996–1997), respectively. He became a Member of Tech Staff and Group Leader at the Institute of Microelectronics (IME), Singapore (1997–2000), and then, Senior Member of Research Staff at Philips Research, Briarcliff Manor, New York (2001–2004), and Senior Staff Engineer at Intel Corporation (2004–2007), and a professor at Lamar University (2007–present).

Dr. Fan has published more than 220 papers, including over three books, 25 book chapters, and over 100 journal papers, and several patents. His publication h-index is 24. His first co-authored book "Mechanics of Microelectronics" has been adopted by some universities as textbooks. His book "Moisture Sensitivity of Plastic Packages of IC Devices' has been downloaded over 5000 times since its publication in 2011. His book on "Solid State Lighting Reliability: Components to System", has been downloaded over 40,000 times since its publication in 2012. Dr. Fan is a key contributing member for several white papers on solid state lighting reliability released by the Department of Energy (DOE), and a contributing member for a new JEDEC standard: JESD22-B111A: Board Level Drop Test Method of Components for Handheld Electronic Products, which is released in November 2016. Dr. Fan also serves as Associate Editor of IEEE Transactions on Components, Packaging and Manufacturing Technology.

Dr. Fan has been very actively leading and participating in many IEEE/EPS activities in last 15 years. He has served General Co-Chair (2012–present), Program Chair (2010), and Technical Chair/Co-Chair (2005–2010) for ICEPT since 2005. Dr. Fan has been serving ECTC technical committee since 2003, and attends ECTC planning meeting in Dallas and ECTC conference every year. Dr. Fan has been one of the founding members for EuroSimE, which has become one of the specialized EPS conference in modeling, simulation and characterization in heterogeneous system. Dr. Fan also serves as program /technical/ advisory committee members for EPTC, ESTC, IRPS, IEMT, EMPC, etc. Dr. Fan has been an ECTC PDC instructor since 2005. As IEEE Distinguished Lecturer, he has given numerous keynotes and tutorials around world each year on behalf of EPS. He has become a key liaison between EPS BoG and ICEPT Executive Committee, in which he has developed the fruitful partnership between EPS and China Electronics Packaging Technology Society. He is currently serving as co-Chair for Modeling/Co-Design in Heterogeneous Integration Roadmap Committee.

JEFFREY C. SUHLING (M: 2001, SM: 2017) has been a faculty member at Auburn University for 32 years. He currently holds the rank of Quina Distinguished Professor, and serves as Department Chair of the Department of Mechanical Engineering. Dr. Suhling co-established the NSF Center for Advanced Vehicle and Extreme Environment Electronics (CAVE3) in 1998, and served as Center Director from 2002–2008 before becoming Department Chair. Please refer to Dr. Suhling's full bio under the EPS Officers and Directors section.

Region 8

GRACE O'MALLEY (M: 2012) is Vice President of Global Operations for the International Electronic Manufacturing Initiative (iNEMl). Based in Limerick, Ireland, she supports the global iNEMl team and activities including managing collaborative projects, the iNEMl Roadmap process and interactions with the larger technical community in Europe. Grace's background is in electronics materials and manufacturing research. Prior to

iNEMI, she worked for Motorola in the US on the development and deployment of direct chip attach/flip chip capabilities and low-cost assembly processes in to production. She also spent approximately two years establishing and leading a multidisciplinary research team at Motorola's site in Jaguariuna, Brazil, supporting the volume manufacturing of cell phones, radios and cellular infrastructure for the Latin America markets. Grace started her career as a research engineer, focused on electronics packaging and board assembly, at the Tyndall National Institute, Cork, Ireland.

Grace has an honours bachelor's degree in electrical engineering from University College Cork, Ireland (1988), and a master of science in materials and manufacturing engineering from the Illinois Institute of Technology, Chicago, U.S.A. (1998). She has authored papers and presentations for a number of journals and conferences including IEEE-TCPMT and ECTC. She holds eight U.S. patents, and has been a member of IEEE for 25 years. A longtime supporter of EPS events, Grace recently worked on the organizing committee of the CPMT R2i-2017 Innovation Workshop in Dublin, Ireland; a one day event to connect researchers and their product ideas with industry and potential funding.

Region 10

YOICHI TAIRA (M: 1989) received his B.S. degree from Kyoto University and Ph.D. degree from University of Tokyo, both in Physics. From 1983 to1988, he was an Associate Professor with the Institute for Laser Science, University Electro-Communication, Tokyo. From 1988 to 2015, he was a Research Staff with IBM Research mostly in Tokyo. From 1989 to 1990, he was with IBM T.J. Watson Research Center. In 1998, he became an IBM Senior Technical Staff Member. Since 2015, he has been a Visiting Professor with Keio University. He is also involved in photonic packaging at IBM TJ Watson Research Center. He has been involved in various science and technology areas including technology research on various aspect of lasers including femtosecond laser technology, nonlinear optics, high power laser and UV lasers; VLSI design of memory and CPU; flat panel display technology including liquid crystal and organic light emitting materials; chip packaging including flip chip packaging, underfilling, chip cooling and chip stacking; high performance computer architecture including optical interconnects; nanometer precision fine molding technology, silicon photonic chip packaging and optically transparent adhesives He is the author of 5 books, more than 160 articles, and more than 60 inventions.

Some of the activities he is involved in for governing and administration of academic, society and related organizations include: Chair of IEEE EPS Japan Chapter; Auditor of Japan Institute of Electronics and Packaging (JIEP); General Chair of the 2017 Annual Meetings of Japan Institute of Electronics and Packaging; Chair of Optical Packaging Technology Committee in Japan Institute of Electronics and Packaging; Member of ECTC Materials and Processing Program Subcommittee

His technical interest includes: Laser science and it application to computer communication; Sensors using optics; Display technology; Precision assembly of electronics/opto-electronic components; Chip cooling and systems cooling; System and network architecture and technology; Technology enabling advanced packaging.

New IEEE EPS Senior Members

The members listed below were elevated to the grade of Senior Member between June and November 2017.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance.

Individuals may apply for Senior Member grade online at: www.ieee.org/web/membership/senior-members/index.html

Karlheinz Bock, Germany Section
Dominick Boesl, Germany Section
Martin Oppermann, Germany Section
Peter Ramm, Germany Section
Diane Titz, France Section
Steven Kosier, Twin Cities Section
Isaac Abothu, Seattle Section
Emil Davies-Venn, Phoenix Section
Daohui Li, United Kingdom and Ireland Section
Jin Yang, Oregon Section
Ning Ye, Santa Clara Valley Section
Tze Yang Hin, Malaysia Section
Liam Hsieh, Northern Virginia Section
Eng Hoo Leow, Malaysia Section
Bernard Lim, Malaysia Section
Dinesh Thanu, Phoenix Section
Cliff Tsay, Santa Clara Valley Section
Takefumi Yoshikawa, Kansai Section

Congratulations to the 2018 newly elevated IEEE Fellows

Listed below are new IEEE Fellows who are members of the EPS. See a list of all EPS members who are IEEE Fellows in the IEEE Fellows Directory.

The grade of Fellow recognizes unusual distinction in the profession and shall be conferred by the Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest. (Bylaw I-104:11) Nominees shall:

- have accomplishments that have contributed importantly to the advancement or application of engineering, science and technology, bringing the realization of significant value to society;
- hold Senior Member or Life Senior Member grade at the time the nomination is submitted;
- have been a member in good standing in any grade for a period of five years or more preceding 1 January of the year of elevation.

The year of elevation to the grade of Fellow is the year following approval by the Board of Directors conferring the grade of Fellow. Members elevated to the Fellow grade may use the title immediately following approval by the Board of Directors.

The IEEE Fellows, an elite global group with international recognition are called upon for guidance and leadership as the world of electrical and electronic technology, continues to evolve.

Kuan-neng Chen
“for contributions to 3D integrated circuit and packaging technologies”

Lang Klaus
“for leadership in heterogeneous integration and microelectronic packaging”

Xiaobing Luo
“for contributions to packaging of optoelectronic devices”

Jianmin Qu
“for contributions to design and reliability analysis for microelectronic packaging”

Heterogeneous Integration Roadmap—A Vision to the Future

We are entering the era of digital economy and myriad connectivity with data migration to the cloud, smart devices everywhere, Internet of Things to Internet of Everything, and the emergence of autonomous vehicles. Artificial Intelligence, big data analytics are undergirding each of the market segments.

The invention of transistor was on December 23rd 1947–70 years ago. Ten years later Integrated Circuits were invented starting the 50 years journey of innovation and advances in semiconductor technologies enabling ever lower cost and performance—well known as Moore’s Law Scaling. Today the economics of Scaling appears to be ending and the physical limits are within sight.

At this inflexion point of the plateauing of CMOS scaling advantage and explosive expansion of innovations and electronic products into global society, continued progress requires a different phase of electronics innovations. Heterogeneous Integration is and will be the key technology direction going forward. It is the “low hanging fruit” to initiate a new era of technological and scientific advances to continue and complement the progression of Moore’s Law Scaling into the distant future.

A Heterogeneous Integration Roadmap is urgently needed to focus on new materials and new devices, new architecture and designs, manufacturing processes and new methodologies to bring diverse components together into a System-in-Package (SiP) through Heterogeneous Integration. Let us read another quote from Moore’s 1965 paper “ It may prove to be more economical to build large systems out of small functions which are separately packaged and interconnected. The availability of large functions combined with functional design and construction

HIR Technical Working Groups

HI for Market Applications
- Mobile
- IoT and Wearable
- Medical and Health
- Automotive
- High Performance Computing & Data Center
- Aerospace & Defense

Heterogeneous Integration Components
- Single Chip and Multi Chip Packaging (including Substrates)
- Integrated Photonics
- Integrated Power Electronics
- MEMS & Sensor integration
- RF and Analog Mixed Signal

Design
- Co-Design & Simulation—Tools & Practice

Cross Cutting Topics
- Materials & Emerging Research Materials
- Emerging Research Devices
- Interconnect
- Test
- Supply Chain
- Security

Integration Processes
- SiP
- 3D + 2.5D
- WLP (fan in and fan out)

should allow manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically."

In summary the expanding digital economy: connectivity & network platforms, driving IoT to IoE, Smart Devices, Data to the Cloud, & Autonomous Vehicles are rapidly changing the electronics industry landscape. In the digital disruptive markets, each market has its own metric for performance, reliability, volume & cost tradeoffs. There is immense need for a comprehensive, pre-competitive technology roadmap addressing future vision, difficult challenges & potential solutions. This roadmap for the future is focused on system level integration & advanced packaging addressing expanding markets, enabling continued progress as the past 50 year following Moore's Law.

We firmly believe that Heterogeneous Integration Roadmap, founded with initiative from the three IEEE Societies—EPS, EDS & Photonics and in collaboration with SEMI & ASME EPPD, has expanded to embrace innovations wherever it arises and promote collaboration wherever possible to accelerate progress in this disruptive digital landscape. Heterogeneous Integration requires a diverse set of disciplines and addresses a broad spectrum of applications. We have developed a broad and inclusive worldview to comprehend this diversity and assembled a group of leading technical experts to develop the roadmap. The first version of the roadmap will be presented for public review and feedback in a Symposium to be held on February 22, 2018. In Santa Clara. Please check the EPS Web link for details.

If you would like to participate in the HIR activities, please contact Bill Chen wt-chen@ieee.org or Bill Bottoms bill_bottoms@3mts.com.

3D + 2.D Technical WG

Raja Swaminathan, TWG Chair and Ravi Mahajan, TWG Co-Chair, Intel Corporation

The (3D + 2.5D) TWG, composed of leading technologists from industry and academia[1], is has two primary objectives

a) **To define and proliferate a comprehensive, converged, physics based nomenclature for MCP[2] architectures.**

Although 2D and 3D MCP architectures have been in vogue for quite some time, currently there are no converged definitions for these architectures using a simple, over-arching physics (or structure) based approach. The TWG members who represent a wide spectrum of industry, academia, consultants and industry have come together and agreed that the current nomenclature (2.1D, 2.3D, 2.45D and 2.5D architectures) is not always rooted in physical or structural assumptions. The TWG is working on defining new nomenclatures and converged definitions to ensure standardization[3] moving forward.

b) **To define a complete set of metrics that describe the physical, electrical, mechanical and manufacturability attributes of MCP Architectures and describe their projected evolution**

It is possible to define a commonly accepted set of attributes that can be used to describe different MCP architectures. These attributes can be used to compare current capabilities and establish a scaling based roadmap for their evolution. Quantification of these attributes and a short term (five year horizon) and long term roadmap (10 year horizon) can be used to highlight challenges in meeting roadmap demand. More importantly this roadmap gives the packaging and micro-systems integration community a common set of goals that will streamline R&D efforts and provide a basis to track and compare progress.

[1]Current membership includes Debendra Mallik (Intel), Subu Iyer (UCLA), Steffen Kroehnert (Amkor), Peter Ramm (Fraunhofer), Markus Wimplinger (EV Group), Michael Alfano (AMD), Kaushik Mysore (AMD), Venky Sundaram (Georgia Tech), Tom DeBonis (Intel), Paul Franzon (North Carolina State University), Rozalia Beica (Dow Chemical), Kanad Ghose (Binghamton U), John Hunt (ASE), Jan Vardaman (TechSearch International)

[2]The term MCP is used in its broader context and is intended to cover on-package integration of multiple package and unpackaged chips.

[3]These definitions are not necessarily unique however they are expected to be complete and to cover all known architectures in a single framework.

2017 Regional Contributions Award

Shen Fu being Presented with the 2017 IEEE CPMT Regional Contributions Award—Region 10 (Asia and Pacific) at IMPACT 2017, by Dr. William Chen

"For contributions to the development of the IEEE CPMT Taipei Chapter and the successful establishment of a professional interactive platform among the chapters in Region 10, through international conferences."

Upcoming Webinars

January 31 2018 11:00 AM EST
"Multi-Die Heterogeneous Integration: Design Considerations and Technology Demonstrations" Presented by Muhannad Bakir

March 21, 2018 11:00 AM EST:
"A Moore's law for Packaging" Presented by Subu Iyer
Please visit the EPS website for more information: eps.ieee.org

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EPS CHAPTER NEWS

IEEE EPS Malaysia Chapter proudly present to you

2017 Semiconductor Advanced Packaging Workshop

The IEEE EPS Malaysia chapter has once again succeeded in its mission of constantly motivating local engineering community with technical knowledge sharing session from the internationally respected speakers. In year 2017, the team has fruitfully organized a 1-Day Semiconductor Advanced Packaging Workshop at Eastin Hotel, Penang and Sunway Resort Hotel,

Honorable speakers: Ms. E Jan Vardaman of TechSearch International Inc. (middle) & Mr. John Hunt of ASE (US) Inc. (right).

Attendees at Sunway Resort Hotel, Kuala Lumpur.

Attendees at Eastin Hotel, Penang.

Souvenir presentation to speakers as token of appreciation.

Kuala Lumpur scheduled respectively on September 26th and 27th. Approximately 120+ attendees- a diverse group of professionals from 30+ companies and local universities Malaysia wide, have gathered face-to-face in this bi-annual technical workshop at both venues.

It's our honor to have invited semiconductor packaging industry's notable speakers, presenting two topics of interest: (1) *Ms. E. Jan Vardaman (President, TechSearch International Inc.) on "Advanced Packaging Drivers: Smartphones, Big Data, and Automotive Electronics"* (2) *Mr. John Hunt (Senior Director, ASE (US) Inc.) on "Fan Out Packaging- Technology Overview and Evolution"*. They covered the introductory overview of advanced packaging technology trends, main market players and a prospective outlook on related future growth. Also, they discussed about the technology challenges and quality/reliability considerations span across package design and process domains.

In summary, this technical workshop was very informative, of all participants truly get inspired by the quality and quantity of late-breaking developments of emerging semiconductor packaging technologies. We would also like to thank EPS HQ for the continued commitment and support of Distinguished Lecturer program. So, what's next?—38th International Electronics Manufacturing Technology (IEMT) 2018 Conference. We are looking forward to seeing you next year in Malacca!!

PUBLICATION NEWS

5 Most Popular T-CPMT Articles according to 2017 usage statistics

3-D Printed Metal-Pipe Rectangular Waveguides
Mario D'Auria; William J. Otter; Jonathan Hazell; Brendan T. W. Gillatt; Callum Long-Collins; Nick M. Ridler; Stepan Lucyszyn
Publication Year: 2015, Page(s): 1339–1349

A Filtering Dual-Polarized Antenna Subarray Targeting for Base Stations in Millimeter-Wave 5G Wireless Communications
Hui Chu; Yong-Xin Guo
Publication Year: 2017, Page(s): 964–973

Design of Compact Bandpass Filters Using Quarter-Mode and Eighth-Mode SIW Cavities
Peng Li; Hui Chu; Ru-Shan Chen
Publication Year: 2017, Page(s): 956–963

3-D Integrated Electronic Microplate Platform for Low-Cost Repeatable Biosensing Applications
Muneeb Zia; Taiyun Chi; Jong Seok Park; Amy Su; Joe L. Gonzalez; Paul K. Jo; Mark P. Styczynski; Hua Wang; Muhannad S. Bakir
Publication Year: 2016, Pages: 1827–1833

Through Silicon Via (TSV) Defect Modeling, Measurement, and Analysis
Daniel H. Jung; Youngwoo Kim; Jonghoon J. Kim; Heegon Kim; Sumin Choi; Yoon-Ho Song; Hyun-Cheol Bae; Kwang-Seong Choi; Stefano Piersanti; Francesco de Paulis; Antonio Orlandi; Joungho Kim
Publication Year: 2017, Pages: 138–152

CONFERENCE NEWS

Heterogeneous Integration Roadmap Symposium

Introduction to our first edition
- https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html
- http://www.semi.org/en/heterogeneous-integration-roadmap

Moderators: Dr. William Chen, ASE (Chair, HIR), Dr. Bill Bottoms, 3MTS (Co-chair, HIR)

Program

- Presentations from HIR Technical Working Group chairs
- Overview from HIR International Roadmap Committee
- Panel Session including Open Discussion

Meeting Date: Thursday, February 22, 2018
Time: 9:00 AM to 4:30 PM
Cost: $40 IEEE members. students, unemployed, $50 non-members

Location: Texas Instruments Building E Conference Center, 2900 Semiconductor Dr. (off Kifer Rd), Santa Clara
Reservations: (URL)

Summary

The Heterogeneous Integration Roadmap (HIR), jointly sponsored by the IEEE EDS, EPS and Photonics Societies, SEMI and ASME EPPD, will introduce its first edition. HIR is founded on our belief that heterogeneous integration represents the low-hanging fruit to maintain the future progress no longer supported by CMOS scaling.

Everything in our lives is changing. In responding to these disruptive changes, we have selected representative applications for specific markets. They are:
- Mobile
- High Performance Computing
- IoT and Wearable
- Medical and Health
- Automotive

Most Popular Conference Papers Based on 2017 Usage

Electronic System-Integration Technology Conference (ESTC), 2016 6th

(held on 13–15 Sept. 2016)

Manufacturing supply chain challenges—globalization and IOT
Katherine Pearsall

Indoor air quality sensing indicators
Markus Tuomikoski; Sami Ihme; Arttu Huttunen; Marko Korkalainen; Samuli Yrjänä

Design of a GaN HEMT based inverter leg power module for aeronautic applications
Benoit Thollin; Fadi Zaki; Zoubir Khatir; Régis Meuret; Donatien Martineau; Clément Fita; Pierre-Olivier Jeannin; Johan Delaine; Pierre Lefranc; Laurent Mendizabal; René Escoffier; Farid Hamrani; Laurent Quellec; Eric Lorin

High frequency high voltage power conversion with silicon carbide power semiconductor devices
Saijun Mao; Tao Wu; Xi Lu; Jelena Popovic; Jan Abraham Ferreira

Electro-thermal-mechanical analyses on stress in silver sintered power modules with different copper interconnection technologies
R. Dudek; R. Döring; M. Hildebrandt; S. Rzepka; S. Stegmeier; S. Kiefl

Organic electronics application overview from automotive HMI to X-ray detectors
Romain Gwoziecki; Jean-Marie Verilhac; Antoine Latour; Amélie Revaux; Christophe Serbutoviez; Audrey Martinent

Electronics Packaging Technology Conference (EPTC), 2016 IEEE 18th

(held on Nov. 30 2016–Dec. 3 2016)

3D-printing and electronic packaging—current status and future challenges
C. Bailey; S. Stoyanov; T. Tilford; G. Tourloukis

Embedding of wearable electronics into smart sensor insole
M. Hubl; O. Pohl; V. Noack; P. Hahlweg; C. Ehm; M. Derleh; T. Weiland; E. Schick; H-H. Müller; D. Hampicke; P. Gregorius; T. Schwartzinger; T. Jablonski; J. -P. Maurer; R. Hahn; O. Ehrmann; K. -D. Lang; E. Shin; H. -D. Ngo

Development of Chip-to-Wafer (C2W) bonding process for high density I/Os Fan-Out Wafer Level Package (FOWLP)
Sharon Pei-Siang Lim; Ser Choong Chong; Mian Zhi Ding; Vempati Srinivasa Rao

Copper wire bond pad/IMC interfacial layer crack study during HTSL (high temperature storage life) test
Mingchuan Han; Miao Wang; Lidong Zhang; Beiyue Yan; Jun Li; Meijiang Song; Varughese Mathew

Molding process development for high density I/Os Fan-Out Wafer Level Package (FOWLP) with fine pitch RDL
Mian Zhi Ding; Ser Choong Chong; David Soon Wee Ho; Sharon Pei Siang Lim

Integration of MEMS/Sensors in Fan-Out wafer-level packaging technology based system-in-package (WLSiP)
André Cardoso; Steffen Kroehnert; Raquel Pinto; Elisabete Fernandes; Isabel Barros

Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), 2017 16th IEEE Intersociety Conference on

(held on May 30 2017–June 2 2017)

Electro-thermal reliability study of GaN high electron mobility transistors
B. Chatterjee; J. S. Lundh; J. Dallas; H. Kim; S. Choi

Microchannel cooling strategies for high heat flux (1 kW/cm^2) power electronic applications
Ki Wook Jung; Chirag R. Kharangate; Hyoungsoon Lee; James Palko; Feng Zhou; Mehdi Asheghi; Ercan M. Dede; Kenneth E. Goodson

Liquid cooled system for aircraft power electronics cooling
Debabrata Pal; Mark Severson

Micromesh-covered superhydrophobic surfaces for efficient condensation heat transfer
Rongfu Wen; Shanshan Xu; Ronggui Yang

Electronic Components and Technology Conference (ECTC), 2017 IEEE 67th

(held on May 30 2017–June 2 2017)

A Design Study of 5G Antennas Optimized Using Genetic Algorithms
Vincens Gjokaj; John Doroshewitz; Jeffrey Nanzer; Premjeet Chahal

First Demonstration of 28 GHz and 39 GHz Transmission Lines and Antennas on Glass Substrates for 5G Modules
Atom O. Watanabe; Muhammad Ali; Bijan Tehrani; Jimmy Hester; Hiroyuki Matsuura; Tomonori Ogawa; P. Markondeya Raj; Venky Sundaram; Manos M. Tentzeris; Rao R. Tummala

Heterogeneous Integration at Fine Pitch (≤10 µm) Using Thermal Compression Bonding
Adeel A. Bajwa; SivaChandra Jangam; Saptadeep Pal; Niteesh Marathe; Tingyu Bai; Takafumi Fukushima; Mark Goorsky; Subramanian S. Iyer

Latency, Bandwidth and Power Benefits of the SuperCHIPS Integration Scheme
SivaChandra Jangam; Saptadeep Pal; Adeel Bajwa; Sudhakar Pamarti; Puneet Gupta; Subramanian S. Iyer

Design and Demonstration of a Photonic Integrated Glass Interposer for Mid-Board-Optical Engines
Marcel Neitz; Markus Wöhrmann; Ruiyong Zhang; Mohamed Fikry; Sebastian Marx; Henning Schröder

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IEEE Xplore® Table of Contents Alert

Any technologist – **member or non-member** – is welcome to receive alerts when upcoming issues of our EPS *Transactions* are posted to the IEEE's Xplore database and all the papers are available for downloading. This is a handy way to scan the issue's Table of Contents and quickly learn about novel approaches to packaging, modeling, reliability, materials, assembly and other topics.

The website link is:ieeexplore.ieee.org/xpl/tocalerts_signup.jsp

If you already have an IEEE web account, you may sign in and select those journals you wish to track. If you don't have an account, all it takes is your name and email address! Then simply click the Alert Status box next to the journals you wish to monitor. You will receive an email each quarter when that journal is posted to Xplore.

Similarly, if you prefer to receive information by RSS feed, you may add our journals' feeds to your Reader. You'll get a listing of the papers in that issue, along with full abstracts and a link for downloading the paper. The RSS links are shown on this same web page.

Here are the journals we suggest you select for monitoring:

Transactions on Components, Packaging and Manufacturing Technology
Transactions on Semiconductor Manufacturing

ECTC

The 68th IEEE Electronic Components and Technology Conference

CALL FOR PAPERS

Sheraton San Diego Hotel & Marina • San Diego, California, USA • May 29 – June 1, 2018

Introduction

On behalf of the IEEE Electronic Components and Technology Conference (ECTC) Program Committee, it is my pleasure to invite you to submit an abstract for the 68th ECTC, to be held May 29 – June 1, 2018, at the Sheraton San Diego Hotel & Marina in San Diego, California, USA.

This premier international conference, sponsored by the IEEE Electronics Packaging Society (IEEE EPS, formerly the IEEE CPMT Society), covers a wide spectrum of electronic packaging technology topics, including components, materials, assembly, interconnect design, device and system packaging, wafer-level packaging, sensors and the Internet of Things (IoT), optoelectronics, silicon photonics, 2.5D and 3D integration technology, and reliability.

The ECTC Program Committee, with more than 200 experts from broad-ranging technical areas, is committed to creating an engaging technical program for all. ECTC typically attracts more than 1,400 attendees from over 25 countries. Last year's 67th ECTC in Orlando, Florida, had 1,439 attendees, with 337 papers and interactive presentations featured in 41 sessions. The 68th ECTC will continue with that tradition by being the premium venue to showcase all the latest developments in the electronic components industry where packaging has become a way to achieve device and system performance scaling.

The 68th ECTC program will include six parallel technical sessions in the mornings and afternoons over three days, along with other special topic panel discussions to present high-level trends and best practices in the industry. Professional Development Courses (PDCs) will also be offered by world-class experts, enabling participants to broaden their technical knowledge base.

The technical program and PDCs will be supplemented by Technology Corner Exhibits, which provide an opportunity for leading companies in the electronic components, materials, and packaging fields to exhibit their latest technologies and products. Last year's 67th ECTC featured a record number of 106 exhibitors.

As the Program Chair of the 68th ECTC, I invite you to submit an abstract between 250 and 750 words that describes the scope, content, and key points of your proposed technical paper at www.ectc.net. You are also welcome to submit proposals for PDCs. The deadline for abstract and proposal submission is October 9, 2017. Manuscripts conforming to the ECTC format are due by February 23, 2018, for inclusion in the Conference Proceedings. All abstracts and manuscripts must be original, free of commercial content, and non-confidential.

On behalf of the ECTC Program Committee, I look forward to seeing you at the Sheraton San Diego Hotel & Marina, San Diego, California, USA at the 68th ECTC, May 29 – June 1, 2018.

Chris Bower – 68th ECTC Program Chair
X-Celeprint, Inc., Research Triangle Park, North Carolina, USA

Major Topics

All submitted abstracts are rated by the ECTC technical subcommittee members. Highly rated abstracts are accepted for presentation at the ECTC conference. It is important that authors identify the subcommittees whose topic areas best fit their abstracts. Abstracts should include original and previously unpublished, non-confidential, and non-commercial information on new developments, technology, and knowledge in the areas including, but not limited to, those given below for each technical subcommittee.

Advanced Packaging: Fan-out & fan-in packages; Wafer & panel level processes; 2.5D, 3D, TSV & Interposer; Heterogeneous integration & SiP; Embedded & advanced substrates; Advanced flip-chip; CSP & PoP; MEMS, sensors & IoT; Power modules; Automotive; Bio, medical, flexible, wearable; High-performance computing.

Applied Reliability: Reliability of TSV, 2.5D, 3D, fan-out, WLCSP, WLFO, PLFO, SiP & MCM; Interconnect reliability in flip chip, wire bond and BGA; Product reliability including LED, IoT, and automotive; Reliability/life test methods & models; Failure analysis techniques & materials characterization; Drop/dynamic mechanical reliability; System level reliability; Automotive & harsh environment reliability.

Assembly and Manufacturing Technology: Embedded/hybrid package manufacturing; Wearable/IoT package assembly; Healthcare/fitness component assembly; Warpage management in board level assembly; Thin die/mold/package handling and assembly; Large package (SiP, SiM, MCP) integration and processing; Panel level manufacturing for fan-in, fan-out; Dicing and singulation technology.

Emerging Technologies: Wearable and implantable medical electronics including sensors/actuators, flexible, stretchable, disposable, dissolvable, self-healing packaging; Emerging MEMS & NEMS; 3D printing, self-alignment, emerging assembly, lab-on-chip & novel additive technologies; Packaging for autonomous sensors, photovoltaic, and heterogeneous integration; Security, anti-counterfeiting & smart electronics.

High-Speed, Wireless & Components: Electrical modeling, analysis, design, integration, and characterization of novel electronic packages, interconnects, components, modules, and systems; High-speed or wireless applications from digital to analog to RF, low to high power, DC to THz, nano to microscales, and beyond; Corresponding simulation and measurement methods.

Interconnections: Interconnections for fan-out & fan-in wafers & panels; Interconnects and TSV for 2.5D/3D, SiP, Si/glass/organic interposers, PoP & WLP; Flip chip, solder bumping, Cu pillar & thermocompression bonding technology; IMC interfaces, wirebonds & conductive adhesives; Interconnects for bio-medical, automotive, datacenters, cloud, network, and harsh environments.

Materials & Processing: Wafer & panel level packaging materials; Materials for harsh environments; Packaging substrates; Flexible, stretchable, bendable & wearable electronics; Battery materials; Wafer bond/debond materials; TSV; Emerging electronic materials & processes; Novel conductive and non-conductive adhesives; Solder metallurgy; Dielectrics and underfill; Molding compounds; Thermal interface materials; Optoelectronic materials; Advanced wire bonding.

Optoelectronics: Wafer & panel level photonic packaging; Photonic integrated circuits; Photonic interposers; Optical interconnects; Waveguide technology; Optical printed circuit boards; Optical sensors; Silicon and III-V photonics; Micro-optical systems; Photonic SiP; 3D photonics; Novel LEDs & high-power lasers; MicroLED; Visible light communication; Optoelectronic assembly, materials and reliability.

Thermal/Mechanical Simulation & Characterization: Component, board & system level modeling for microelectronics; 3D/2.5D; TSV; Interposer; SiP; WLP; BGA; Embedded actives/passives; Power modules; LEDs; MEMS; Thin wafer/die handling; Wire bonding & assembly processes; Modeling of fracture mechanics, fatigue, electro-migration, warpage, delamination, drop test & material attributes; Novel modeling including multi-scale and multi-physics; Novel characterization methodologies.

Interactive Presentations: Highly encouraged at ECTC, presenter and attendee often communicate more efficiently here than in oral presentations. Abstracts can relate to any electronics packaging topic. Interactive presentation session papers are published and archived in equal merit with the other ECTC papers.

Visit the ECTC website (www.ectc.net) for additional conference information.

Call for Professional Development Courses

See page two.

Abstract and Manuscript Submission

You are invited to submit an abstract between 250–750 words that describes the scope, content, and key points of your proposed paper via our website at www.ectc.net. Additional details on how to submit abstracts electronically can be found on the ECTC website under the "Author Information" tab. Submitted abstracts become the property of ECTC, and ECTC reserves the right to publish the abstracts accepted for the conference. ECTC also reserves the right to prohibit, limit, or reject any editing of submitted abstracts. Abstracts accepted for the conference may not be edited until manuscript submission. Abstracts must be received by **October 9, 2017**. Your submission must be cleared by management and co-authors as applicable and include the affiliation, contact telephone number, and email address for all authors, along with the mailing address for the presenting author. Please select two different program subcommittees in order of preference that should evaluate your submission for acceptance. Authors will be notified of paper acceptance with instructions for publication by December 11, 2017. At the discretion of the Program Committee, submitted abstracts may be considered for Interactive Presentation sessions.

Manuscripts conforming to the ECTC format are due in final form for publication in the Conference Proceedings by February 23, 2018. **Manuscripts not submitted by this date may be removed and replaced in the final program at the discretion of the Program Committee.** The submitted content must be original, previously unpublished, non-confidential, and without commercial content. All submitted manuscripts are checked for plagiarism and excessive self-duplication of previously published work through the IEEE CrossCheck system. For additional information regarding abstract and paper submission, please contact:

Christopher Bower – 68th ECTC Program Chair
X-Celeprint, Inc., Research Triangle Park, North Carolina, USA
Phone: +1-919-522-3230 • Email: cbower@x-celeprint.com

Special Paper Recognition

Best Paper Award: Each year the ECTC selects the best paper whose author(s) receive an ECTC personalized wall plaque and share a check for $2,500.

Best Interactive Presentation Award: Each year the ECTC selects the best Interactive Presentation paper whose author(s) receive an ECTC personalized wall plaque and share a check for $1,500.

Outstanding Paper Award: An outstanding conference paper is also selected for special recognition by the ECTC. The author(s) receive a personalized wall plaque and share a check for $1,000.

Outstanding Interactive Presentation Award: An outstanding Interactive Presentation paper is also selected for special recognition by the ECTC. The author(s) receive a personalized wall plaque and share a check for $1,000.

Intel Best Student Paper Award: Intel Corporation is sponsoring an award for the best paper submitted and presented by a student at ECTC. The winning student will be presented with a wall plaque and a check for $2,500. See next column for details.

Texas Instruments Outstanding Student Interactive Presentation Award: Texas Instruments is sponsoring an award for the best student interactive presentation at ECTC. The winning student will be presented with a wall plaque and a check for $500.

Technology Corner Exhibits

Reserve Your Space Early!

Exhibit your products or services to more than 1,400 engineers and managers from all areas of the microelectronics packaging industry. These include: materials & processes for semiconductor packaging, assembly and interconnect technologies, test & other equipment, market research, and research centers.

Two days: May 30 and 31, 2018

With 100 of 106 exhibition booths at the 68th ECTC reserved already, mostly by returning exhibitors from the 67th ECTC, applications are still being accepted for participation in the Technology Corner Exhibits. For information and an application contact Joe Gisler at gislerhj.ectc@mediacombb.net. Additional information is available at **www.ectc.net** under Technology Corner Exhibits.

Sponsorship Opportunities to Enhance Your Presence at ECTC

ECTC also offers excellent opportunities for promotion and visibility through sponsorships of the gala event, badge lanyard, USB flash drive proceedings, media, luncheons, refreshment breaks, program, and the student reception. Additional information is available at www.ectc.net under Sponsors. Please contact:

Wolfgang Sauter, Sponsorship Chair – GLOBALFOUNDRIES, USA
Phone: +1-802-922-3083 • Email: wolfgang.sauter@globalfoundries.com

Call for Professional Development Courses

Proposals are solicited from individuals interested in teaching educational, four-hour long Professional Development Courses (PDCs) on topics described on the previous page. From the proposals received, 18 PDCs will be selected for the 68th ECTC on Tuesday, May 29, 2018. Each selected course will be given a minimum honorarium of $1,000. In addition, instructors of the selected courses will be offered the speaker discount rate for the conference. Attendees of the PDCs will be offered Continuing Education Units (CEUs). These CEUs are recognized by employers as a formal measure of participation and attendance in "noncredit" self-study courses, tutorials, symposia, and workshops.

Using the format "Course Objectives/Course Outline/Who Should Attend," 200-word proposals must be submitted via the ECTC website at www.ectc.net by **October 9, 2017**. Authors will be notified of course acceptance with instructions by December 11, 2017. If you have any questions, contact:

Kitty J. Pearsall – Professional Development Courses Chair
Boss Precision, Inc., Austin, Texas, USA
Phone: +1-512-845-3287 • Email: kitty.pearsall@gmail.com

IEEE Electronics Packaging Society Travel Grant

IEEE Electronics Packaging (formerly IEEE Components, Packaging and Manufacturing Technology Society) is pleased to continue the IEEE EPS Travel Grant Program for the 68th ECTC. The goals of this award are to foster maximum student participation in ECTC and to recognize students with superior ECTC papers.

Description: Grants are available to apply towards actual travel expenses, including airfare, hotel, and meals. Grants will be awarded competitively, based on abstracts submitted by student authors. The student who is named as the primary author of each winning abstract will receive a travel grant.

Eligibility: The competition is open to all full-time graduate students enrolled at an accredited institution in a program of study within the scope of ECTC. The student must be listed as the primary author on the abstract. A maximum of two authors (one per paper) from any one institution will receive a travel grant.

Application Process: To apply, check the "IEEE EPS Society Travel Grant" box in the "Awards" section of the online abstract submission form. Pre-selected abstracts based on technical committee scores will be requested to submit an extended abstract.

Intel Best Student Paper Award

Intel Corporation is sponsoring an award for the best paper submitted and presented by a student at the ECTC. The winning student will be presented with a wall plaque and a check for $2,500.

Eligibility: To be considered for the award, the student must be a full-time student for at least one semester after the conference conclusion. The student must be the lead author and present the paper at the 68th ECTC. It is the convention at ECTC for the presenter to be listed as the first author. Finalists will be determined by review of the completed manuscripts by the judging committee. Manuscripts will be reviewed for relevance to the competition topics, technical content, and originality. The author of the best student paper will be notified after the conference and must submit an affidavit from the student's faculty advisor certifying that the student meets the eligibility requirements.

Application Process: To enter the Intel Best Student Paper Award competition, please check the "Intel Best Student Paper Award" box in the "Awards" section of the online abstract submission form.

Workshop Chair

Mihai Telescu
Université de Bretagne Occidentale, Brest (FRA)
Mihai.Telescu@univ-brest.fr

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Flavio G. Canavero
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Leibniz University Hannover, Hannover (GER)

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Michel S. Nakhla
Carleton University, Ottawa (CAN)

José E. Schutt-Ainé
University of Illinois, Urbana (USA)

Madhavan Swaminathan
Georgia Institute of Technology, Atlanta (USA)

Important Dates

Paper submission (2-4 pages):
January 19th, 2018

Notification of acceptance:
March 2nd, 2018

CALL FOR PAPERS
22nd IEEE WORKSHOP ON SIGNAL AND POWER INTEGRITY, 22-25 MAY 2018, BREST, FRANCE

Over the past two decades, the IEEE Workshop on Signal and Power Integrity (SPI) has evolved into a forum of exchange on the latest research and developments on design, characterization, modeling, simulation and testing for Signal and Power Integrity at chip, package, board and system level. The workshop brings together developers and researchers from industry and academia in order to encourage cooperation.

In view of the past years' success, the Committee is looking forward to the 22nd Edition which will be hosted in the charming region of Brittany, in Western France, in the city of Brest, bathed by the Atlantic Ocean. The SPI 2018 technical program will include both oral and poster sessions. A number of prominent experts will be giving tutorials on areas of emerging interest. The Conference Proceedings will be published with an ISBN code and will appear in IEEEXplore.

The SPI 2018 workshop is jointly organized by the Université de Bretagne Occidentale, the Ecole Nationale d'Ingénieurs de Brest and the Université de Savoie Mont Blanc.

https://spi2018.sciencesconf.org

Topics of Interest

- Modeling and simulation for SI/PI
- Coupled signal and power Integrity analysis
- Noise reduction and equalization techniques
- High-speed link design and modeling
- Power distribution networks
- RF/microwave/mixed signal systems
- 3D IC and packages (TSV/SiP/SoC)
- Nano-interconnects and nano-structures
- Electromagnetic theory and modeling
- Transmission line theory and modeling
- Macromodeling, reduced order models
- Electromagnetic compatibility
- Design methodology/flow measurements
- Jitter and noise modeling
- Stochastic/sensitivity analysis
- Electro-thermal modeling
- Chip-package co-design
- Novel CAD concepts
- Optical interconnects

Industry forum

Building on the success of previous editions, the **Industry Forum** is becoming an SPI tradition. This special session will be reserved to both invited and contributed talks from the industry. The objective is to present and discuss problems rather than solutions, for those aspects of Signal and Power Integrity (and related topics) that have no good solution yet, neither theoretical, nor in form of EDA tools. The explicit goal is to foster the discussion between industry, academia, and tool vendors, so that the three communities can cooperate in the future and focus on the most relevant problems.

7th ELECTRONICS SYSTEM-INTEGRATION TECHNOLOGY CONFERENCE

September 18-20, 2018

SECOND CALL FOR PAPERS

THE SINGLE LARGEST SEMICONDUCTOR PACKAGING CONFERENCE IN EUROPE

It is our pleasure to announce the **7th ESTC Conference**, the premier European scientific conference event in the field of microelectronics packaging and system integration. The conference will be held from 18th to 20th of September, 2018, at the Westin Bellevue Hotel in Dresden, Germany. This international event brings together both academics as well as the industry leaders to present and discuss state-of-the-art and the future trends in packaging and integration technologies. ESTC provides a perfect opportunity to learn about the latest developments in those fields. Save the date right now! This major event only takes place once every 2 years. ESTC is supported by IEEE-EPS in association with IMAPS-Europe. Read more at www.estc-conference.net. ESTC 2018 seeks original papers describing research and innovations in all areas of electronic packaging and system integration. You are invited to submit abstracts that provide non-commercial information of new developments and knowledge in areas like:

- Advanced packaging, 3D integration, embedded structures, wafer level packaging, TSVs, TEVs…
- Materials for interconnects and packaging, piezoelectric, dielectric and memory materials, nanomaterials…
- Optoelectronic systems packaging, fiber optical interconnects, optical sensors, LEDs and other photonic devices…
- Assembly and manufacturing technologies, wafer level processing…
- MEMS/NEMS and sensors packaging, bonding technologies, wafer bonding, micro-bonding…
- Design tools and modeling, thermal, mechanical and electrical modeling, signal and power integrity
- Power electronic systems packaging, power embedding, wide bandgap power semiconductor devices…
- Advanced technologies for emerging systems, allotropes of carbon, nano packaging, bio-electronics…
- Reliability of electronic devices and systems, characterization and test, failure diagnostic …
- Flexible printed and hybrid electronics, printed/jetted conductors, paper electronics, energy storage…

ABSTRACT SUBMISSION

You are invited to submit a 300 - 500 word abstract that describes the scope, content and key points of your proposed paper. Abstracts must include results and graphics. The official language of all presentations is English. Please visit www.estc-conference.net to find more information and to upload your abstract. Submission of abstracts will be open from December 1st 2017 and abstracts are due **February 15th 2018**. All abstracts must be submitted electronically at the conference website. All submitted abstracts will be reviewed by the committee to ensure high-quality of the conference. Authors will be notified of paper acceptance with instructions for publication by March, 30th 2018. If you have any questions, please contact: Karlheinz Bock, the General Chair of the 7th ESTC, via email karlheinz.bock@tu-dresden.de.

PUBLICATION OF PAPERS

All oral and poster presentation papers will be included in the conference proceedings and made available at the IEEE Xplore Digital Library (ieeexplore.ieee.org). In order to be included in IEEE Xplore, the paper must be original and not previously published, and avoid inclusion of commercial content.

ESTC 2018 Committee is proud to announce:

The **10% best ranked papers** of the conference will be invited to be published as journal publications in special sections of the **IEEE Transactions on Components, Packaging and Manufacturing Technology** after the conference. After an evaluation of the submitted full papers by the Technical Committee of ESTC authors of those papers will be informed and requested to adapt their full paper according to the transaction guidelines if necessary. Papers will then be grouped by topic of interest and published in the next upcoming issues of the journal.

Don't miss this opportunity to place a high ranked journal publication!

BEST PAPER AWARD

The ESTC Technical Committee will select the best paper presentation. The author(s) will receive a personalized ESTC award that comes with a 1.000 € prize money. The best poster paper will also be selected and the author(s) will receive a personalized ESTC award that comes with a 1.000 € prize money, too.

PROFESSIONAL DEVELOPMENT COURSES

In addition to abstracts for paper presentations, we call proposals from individuals interested in teaching Professional Development Courses (duration 4 hours) about the topics described in the Call for Papers. Up to four Professional Development Courses will be selected from the received proposals for Tuesday morning (September 18th, 2018) of the conference. Each selected course will be given an honorarium of 750 € if a minimum number of participants will sign in for the course. In addition, instructors of the selected courses will be offered the speaker discount rate for the conference. A 300 to 500 words proposal containing description of course objectives, course outline and who should attend, should be submitted to klaus-juergen.wolter@tu-dresden.de by February 15th, 2018.

IMPORTANT DATES

- **Website open for abstract submission: December 1st, 2017**
- **Abstract submission deadline: February 15th, 2018**
- **Notification of acceptance: March 30th, 2018**

General Chair:
Karlheinz Bock
Technische Universität Dresden, Germany

Executive Chair:
Thomas Zerna
Technische Universität Dresden, Germany

Technical Program Chair:
Steffen Kröhnert
Nanium S.A., Portugal

29th International Conference on Electrical Contacts together with 64th IEEE Holm Conference on Electrical Contacts

14-18 OCTOBER 2018 Hotel Albuquerque
Albuquerque, NM, USA

2018 Call for Papers Technical Areas

AUTOMOTIVE

Hybrid/Electric Power	Hot Plugging
Switching &Connectors	Environmental Effects

ELECTRONIC CONNECTORS

High Frequency	High-Speed Data
Telecommunications	Lubricants
Corrosion Inhibitors	

POWER CONNECTORS

Crimp Connections	Bolted Connections
Plating/Lubricants	Glowing Contacts
	Degradation Effects

CONTACT MATERIALS

Air and Vacuum	High Frequency Relays
Ultra Miniature Relays	Carbon Fiber
Degradation Mechanisms	Reed Relays
Material Development	Switching Performance
Electroplating	Lead Free

DEGRADATION MECHANISMS

Switching Performance	Environmental Effects
Welding	Reliability
Breakdown	Diagnostics
Fretting	

ARC INTERRUPTION

DC/AC Switching	Circuit Breakers
Vacuum Interrupters	Hybrid Switching
Micro-Arcing	High-Speed Film/Video
	Super-Conducting Limiters

MODELING

Fundamentals	Dielectric Breakdown
Arc Simulation	Dynamic Welding

NEW TECHNOLOGY

MEMS	Micro Switches
RF Connectors	Arc Fault Safety
Nanotechnology	Superconductors
High DC Voltage Switching	

ICEC/HOLM 2018

The 29th International Conference on Electrical Contacts together with the 64th IEEE Holm Conference on Electrical Contacts will be held from October 14-18, 2018 at the Hotel Albuquerque, Albuquerque, NM, USA.

Prior to this, the 4-day Intensive Course on Electrical Contacts will be held on October 10-13, 2018 in the same location. The course covers all aspects of Electrical Contacts, including:

- Contact fundamentals and materials
- Friction, wear, fretting and lubrication
- Electric arc fundamentals and dynamics
- Power and electronic connector technologies
- Guidelines for electrical and electronic connector design

IEEE uploads the ICEC/Holm Conference Proceedings to all relevant databases including the Engineering Index. Prospective authors should submit a brief abstract (200 words maximum) online before February 9, 2018. For abstract submissions and the latest information regarding the conference, please visit the Holm Conference Website at:

www.ieee-holm.org

IMPORTANT DATES

February 9, 2018	Abstract Deadline
February 23, 2018	Notification of Acceptance
April 20, 2018	Completed Paper Deadline
October 14, 2018	Conference Begins

CORRESPONDENCE ADDRESS

IEEE Meeting & Conference Management
64th IEEE Holm Conference (2018)
445 Hoes Lane
Piscataway, NJ 08854
tel: +1 800 810 4333 or
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Name: 2018 19th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)
Location: Toulouse, France
Dates: Apr 15, 2018–Apr 18, 2018

Name: 2018 IEEE 22nd Workshop on Signal and Power Integrity (SPI)
Location: Brest, France
Dates: May 22, 2018–May 25, 2018

Name: 2018 17th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)
Location: San Diego, CA USA
Dates: May 29, 2018–Jun 1, 2018

Name: 2018 IEEE 68th Electronic Components and Technology Conference (ECTC)
Location: San Diego, CA USA
Dates: May 29, 2018–Jun 1, 2018

Name: 2018 7th Electronic System-Integration Technology Conference (ESTC)
Location: Dresden, Germany
Abstract Submission Date: Jan 31, 2018
Dates: Sep 18, 2018–Sep 21, 2018

Name: 2018 IEEE Holm Conference on Electrical Contacts
Location: Albuquerque, NM USA
Abstract Submission Date: Feb 5, 2018
Dates: Oct 14, 2018–Oct 18, 2018

Name: 2019 IEEE 69th Electronic Components and Technology Conference (ECTC)
Location: Las Vegas, NV USA
Abstract Submission Date: Oct 19, 2018
Dates: May 25, 2019–Jun 2, 2019

Name: 2020 IEEE 70th Electronic Components and Technology Conference (ECTC)
Location: Lake Buena Vista, FL USA
Abstract Submission Date: Oct 18, 2019
Dates: May 26, 2020–May 29, 2020

Name: 2021 IEEE 71st Electronic Components and Technology Conference (ECTC)
Location: San Diego, CA USA
Abstract Submission Date: Oct 16, 2020
Dates: Jun 1, 2021–Jun 4, 2021

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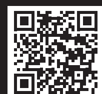

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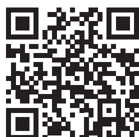

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