Equalization Techniques for Nonlinear Analog Circuits

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ABSTRACT

Technology advancement entails an analog design scenario in which sophisticated signal processing algorithms are deployed in mixed-mode and radio frequency circuits to compensate for deterministic and random deficiencies of process technologies. This article reviews one such approach of applying a common communication technique, equalization, to correct for nonlinear distortions in analog circuits, which is analogized as non-ideal communication channels. The efficacy of this approach is showcased by a few latest advances in data conversion and RF transmission integrated circuits, where unprecedented energy efficiency, circuit linearity, and post-fabrication adaptability have been attained with low-cost digital processing.

INTRODUCTION

The confluence of Moore's law and the maturation of the art of analog integrated circuit (IC) design has created a flurry of recent research and development work on digitally intelligent analog circuits. Exploiting high-density on-chip digital processing, the approach represents a trendy alternative to conventional hard-labored analog design methodology, in which the inescapable trade-off between linearity, circuit bandwidth, complexity, and power dissipation has limited the scaling progress of precision analog circuits in the past.

This trend is most observable in the area of analog-to-digital converters (ADCs), in which the readily available output bits provide a convenient digital means to infer component errors of the constituent imperfect analog circuits, and to devise correction schemes to mitigate the effect of these imperfections, all performed naturally in the digital domain [1]. On a parallel path, although treating a continuous-time radio frequency (RF) circuit is considerably more difficult than treating a discrete-time baseband ADC, the potential benefit and adaptability that can be harvested from such treatment seems to well offset the initial design effort involved. As a result, similar design approaches are making quick inroads in the RF and soon even millimeter-wave sectors [2, 3].

This article reviews the latest progress in these exciting areas of research. An analogy will first be drawn to relate analog circuit distortions to the non-idealities of a communication channel. Under certain assumptions, both impairments can be modeled as a transversal structure. It is then pointed out that a zero-forcing equalizer is sufficient to treat the linear/nonlinear analog distortions similar to receiver equalization in communications. Two variants of this approach, the parallel-path and split-path equalization techniques, are presented next, followed by a few design examples. The approach is last extended to treating RF transmitter nonlinearities and I/Q mismatches with an adaptive transmitter equalizer to obtain highly linear RF transmission at low power consumption with highly nonlinear analog circuit components.

COMMUNICATION CHANNEL VS. ANALOG CIRCUIT

In wireless communications, multipath signal transmission results in a phenomenon called intersymbol interference (ISI), in which successive transmitted symbols arrive at the receiver at the same time, causing difficulties in decoding the information. In such a scenario, the impulse response of the wireless channel becomes non-ideal, as shown in Fig. 1a, where it is modeled as a simple transversal structure.

In analog circuits, it is often necessary to realize in solid-state technology certain analog building blocks with precision (e.g., amplification), which is vital to the overall accuracy of the analog system constituting such building blocks. Figure 1d shows one example of such applications of an ADC that utilizes the pipeline conversion architecture. A pipelined ADC exploits the concurrency of pipelining to expedite the conversion process, in which multiple conversion stages operate in tandem to divide the job into subtasks, with each stage responsible for one subtask only. In the limiting case, an N-bit ADC can be divided into N pipelined stages with each stage resolving one bit. The unresolved part of the analog signal in a previous stage is passed on to the next one in the form of a residue signal, which needs to be provisioned and amplified to certain precision along the pipeline. The gains of the successive amplifications are shown in Fig. 1 as a_1, a_2, a_3, …, which all have an ideal value of exactly 2 in the 1-bit/stage architecture shown in the diagram. When these residue gains are realized perfectly, the partial decision bits from each

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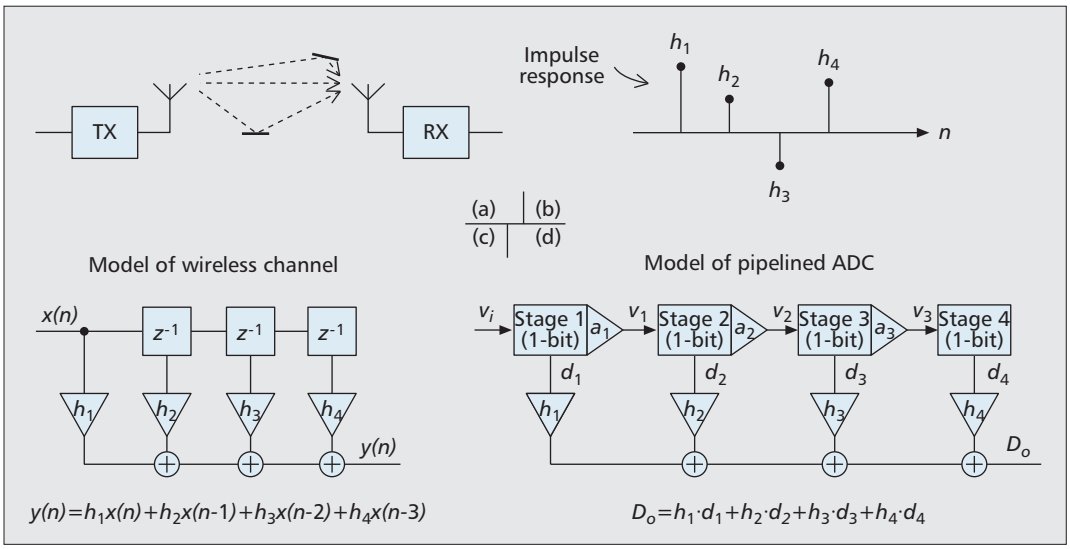


Figure 1. *Channel non-idealities in communications result in intersymbol interference in the time domain, whereas analog circuit non-idealities in multistep analog-to-digital converters lead to interstage interference in the code domain.*

A common technique to correct for the non-ideal channel response in a communication receiver is to perform receiver equalization, in which a known sequence of training symbols are transmitted to assist the receiver to estimate the channel. This inspires the parallel-path ADC architecture of digital background calibration.

stage can be assembled to form the overall quantization result of the input sample. The assembly process is typically no more than a binary-weighted sum of all bits with latency accounted for. In practice, component mismatch and insufficient gain accuracy of analog circuits cause the residue gain to vary from its ideal value of 2. Although this variation may not be as large and time-variant as the impulse response of a wireless channel, it can be significant for high-resolution applications. For example, if the target resolution is 12-bit, the residue gain error in the first pipeline stage must be controlled to within 2^{-11}, or 0.05 percent, of its nominal value, which is difficult to realize in monolithic forms without trimming.

While effort can be invested in the design of analog circuits to improve their raw accuracy in the first place, a trend in mixed-signal design is to increasingly utilize the on-chip processing capability readily available in nanometer complementary metal oxide semiconductor (CMOS) technology to perform digital post-processing of the raw circuit outputs to remedy various deterministic and random analog impairments. Due to the difficult trade-off between linearity, bandwidth, complexity, and power consumption in analog design, the digital-oriented alternative approach embodies potential for power saving and improved scalability for conventional analog circuits in scaled technologies. Thus, this design approach has been in the limelight of academic (in some cases, as well as industrial) research in recent years.

In the pipelined ADC example shown in Fig. 1d, it has been shown in [1] that an ideal quantization of an input sample can still be obtained by a proper weighted sum of all bits, $\Sigma h_j \cdot d_j$, as long as the bit weights h_1, h_2, h_3, and h_4 take the values 1, $(a_1)^{-1}$, $(a_1a_2)^{-1}$, and $(a_1a_2a_3)^{-1}$, respectively. The transversal structure of this formulation resembles the impulse response of the wireless channel model introduced earlier. It was pointed out in [1] that, omitting quantization noise, $\{d_j\}$ can be interpreted as a (non-)binary decomposition of the input sample V_i. Under certain conditions, even with non-ideal bit weights due to analog inaccuracies, the ideal binary code space of V_i is still fully spanned by $\{d_j\}$; that is, $\{d_j\}$ constitutes sufficient statistics of the ideal quantization of V_i. This argument can be related to a common principle in digital communications, which states that the received symbols in the presence of ISI form sufficient statistics of the transmitted symbols under certain conditions. Whereas the ISI in communications is modeled as a time-domain transversal structure, the interstage interference in a pipelined ADC is represented by a (binary) code-domain transversal structure, with both shown in Fig. 1. In addition, if the reversal of the multipath distortion in wireless receivers relies on estimating the impulse response of the channel, the reversal of the effect of the residue gain inaccuracies in a pipelined ADC can be reduced to estimating the bit weights $\{h_j\}$, which may be analogized as the "impulse response" in the code domain.

Equalizing A/D Converters

A common technique to correct for the non-ideal channel response in a communication receiver is to perform receiver equalization, in which a known sequence of training symbols are transmitted to assist the receiver to estimate the channel. This inspires the parallel-path ADC architecture of digital background calibration shown in Fig. 2a. Here, "calibration" means to estimate the error parameters such as the bit weights $\{h_j\}$ in Fig. 1d of a non-ideal analog circuit and devise error-correction schemes accordingly to eliminate the resulting distortions. In principle, conversion nonlinearities caused by component mismatch, amplifier gain error and nonlinearity, and offset can all be treated. In Fig. 2a, the main ADC under calibration is the communication "channel"; a digital post-proces-

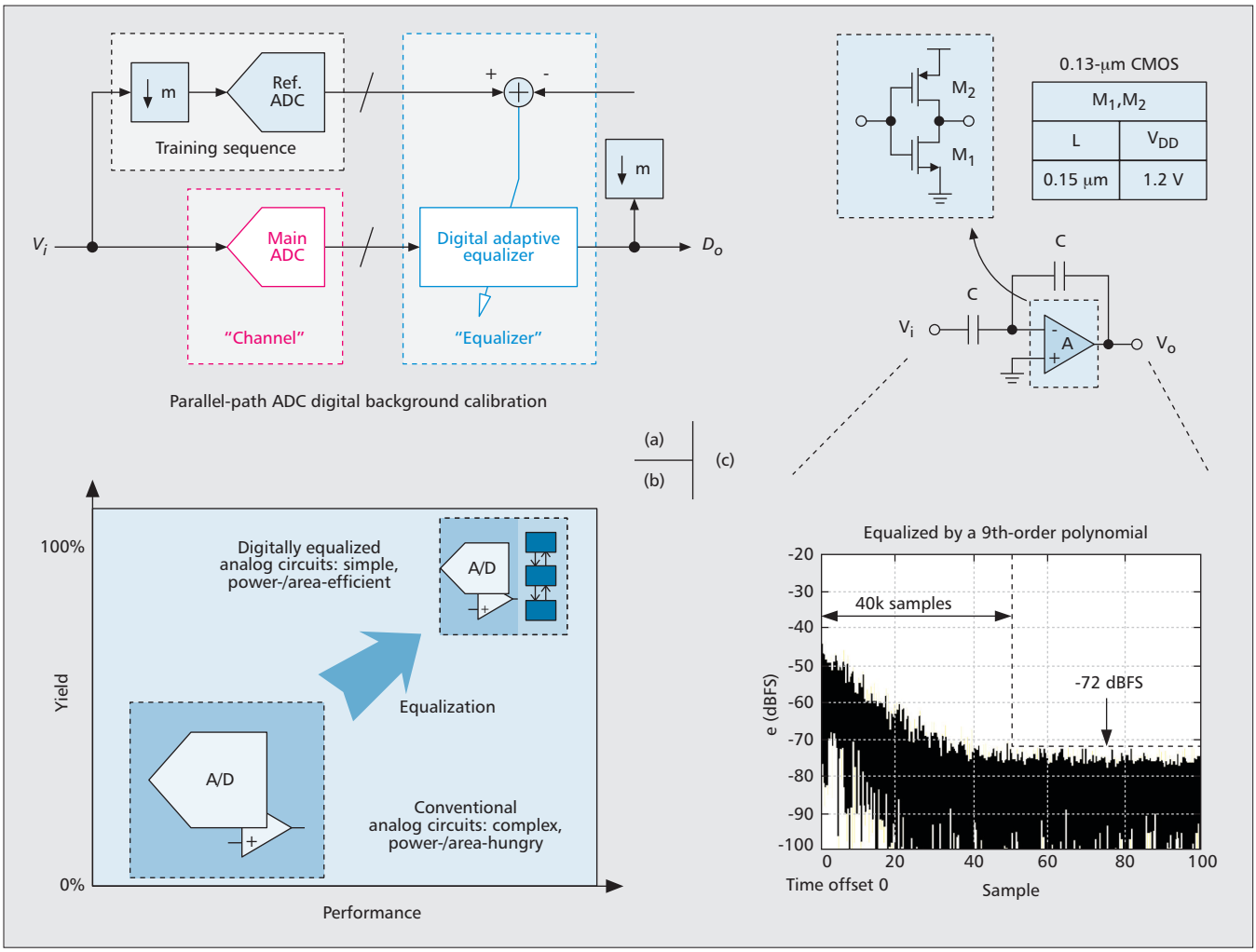


Figure 2. *Parallel-path digital background equalization of high-speed data converters.*

sor is the "equalizer" that attempts to eradicate the conversion errors in the ADC digital output stream, assisted by a parallel reference ADC that provides a "training sequence" continuously at a significantly lower rate compared to the main path. The down-sampling of the reference path is essential for this scheme in practice as otherwise the realization of the reference ADC would pose an issue. From a circuit standpoint, this architecture can also be understood as a seamless integration of two parallel ADCs, one fast but crude and the other precise but slow, to simultaneously accomplish speed and accuracy in a digitizing process. This approach was first shown to be viable in [1]. Similar work was independently reported in [4].

With the back-end digital calibration logic to take care of the analog imperfections, the main ADC circuits can then be made simple, fast, and energy efficient. As elucidated before, this would be otherwise impossible with the conventional design methodology of precision analog circuits. In contrast, while certain accuracy is required for the reference ADC, its conversion speed is greatly relaxed relative to the main path, and thus it can be realized with ease using a variety of conventional techniques. Another aspect of this design approach is related to the elevated variability in deeply scaled processes. It is known that analog circuits are typically orders of magnitude more sensitive to process variations than their digital counterparts. With the conventional verification methodology for analog design, a pessimistic bound of performance must be set to meet certain target yield specs in anticipation of severe process variations. Digital post-processing essentially mitigates the difficult trade-off between performance and yield by allowing self-healing or digital intelligence built into an otherwise inflexible analog circuit, resulting in superior and reliable performance from unreliable analog components with poor raw performance.

The efficacy of this technique can be better appreciated by the example shown in Fig. 2c of a capacitive amplifier employing a digital inverter as the gain element, which is calibrated by a 9th-order polynomial. The open loop gain of the inverter, which consists of two short-channel transistors biased in saturation in a 0.13-μm CMOS process, is no more than 20 dB. A SPICE simulation of the closed-loop response reveals a linearity of no more than 25 dB, which upon calibration is improved to over 72 dB, nearly sufficient for a 12-bit ADC. The zero-forcing nature of the equalization also results in swift adapta-

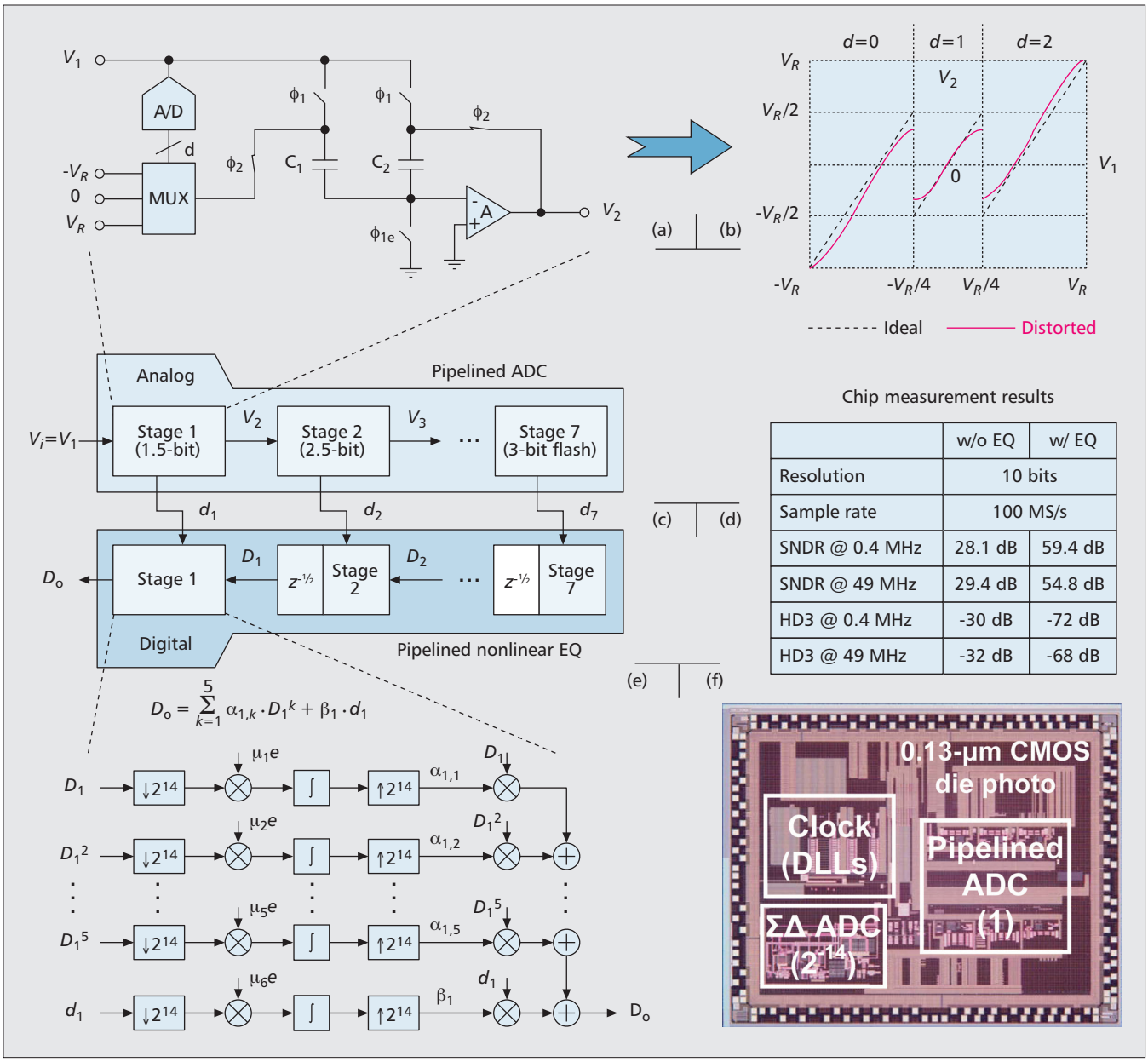


Figure 3. *Nonlinear adaptive digital equalization of high-speed pipelined ADCs and experimental results.*

tion of the error correction logic to accomplish the above-mentioned accuracy within merely 40,000 samples. This speed contrasts to the millions or even billions of training samples required for convergence by alternative background calibration techniques, such as the correlation-based schemes [5, 6].

A Digitally Equalized Pipelined ADC

As mentioned before, a pipelined ADC is probably the most popular multistep converter used in practice and has been identified as the first demonstration vehicle of the digital equalization technique for nonlinear analog circuits [7]. In switched-capacitor technology, a pipelined ADC can be realized by a compact circuit called the multiplier digital-to-analog converter (MDAC), shown in Fig. 3a. In the prototype, a pipelined ADC utilized a 1.5-bit front-end stage, followed by five 2.5-bit intermediate stages and a 3-bit last stage. Simple cascode pseudo-differential inverters were employed as residue gain amplifiers in each stage, resulting in a low gain of around 30 dB with highly nonlinear closed-loop characteristics. The nonlinearity of the residue amplifier translates into the distortion of the ADC transfer curves shown in Fig. 3b. A 5th-order nonlinear polynomial, illustrated in Fig. 3e, was identified as sufficient to treat the amplifier for 12-bit linearity due to the cascode gain stage used in the design, which compares to the example in Fig. 2c wherein a digital inverter was employed.

One practical issue emerges when a multistage equalization treatment is formulated for a pipelined ADC, in which a straightforward realization of simultaneous multistage error correction dictates geometrical complexity vs. the

A unique feature of this treatment is that upon training, the characteristics of the individual ADCs are uniformly aligned to that of the reference ADC, thus eliminating path-mismatch errors inherent in time interleaving.

number of the pipelined stages under calibration [1]. A reversely pipelined (relative to the analog circuits) nonlinear adaptive equalizer shown in Fig. 3c was introduced to solve this issue in the prototype. In addition, the 5th-order polynomial correction was applied only to the first two stages; the rest of the stages all employ a linear (i.e., first-order polynomial) correction scheme.

In the 0.13-μm CMOS prototype chip, the reference ADC was implemented by a sigma-delta ADC; and the relative down-sampling factor was 2^{14} between the reference and main paths. In experiments, the 3rd-order harmonic distortion (HD3) of the pipelined ADC clocked at 100 Msamples/s was measured to be –30 dB with a low-frequency full-scale sinusoidal input. It was improved to –72 dB when the digital equalizer was fully adapted within 50,000 reference samples. The measured peak integral nonlinearity (INL) was 34.6 least significant bits (LSBs) and 1.1 LSBs before and after equalization, respectively. This work was reported in [7].

"Split-ADC" Equalization

Parallel path equalization is proven to be effective in treating nonlinear distortions in pipelined ADCs. However, the architecture exhibits two undesirable features for practical applications:

- The nearly opposite performance specs for the main and reference ADCs dictate a system-level complexity in that two dramatically different ADCs need to be designed.
- The large down-sampling factor that eases the design of the reference path may turn out to be a limiting factor for the overall adaptation speed.

To minimize design complexity and accelerate convergence, the two ADCs in the parallel architecture can be made identical and clocked at the same speed. Although neither is ideal to begin with, the difference between their outputs captures the lumped effect of their individual conversion errors. A zero-forcing equalizer can again be used to simultaneously treat both ADCs; when their characteristics become ideal, the difference in their output disappears and the adaptation halts. This technique has led to the "split-ADC" equalization of algorithmic ADC [8, 9] and pipelined ADC [10]. Of course, the two ADCs under calibration can be wrong in exactly the same way, and the difference still drops to zero. In practice, decision trajectories can be artificially mutated by offsetting the comparator thresholds in the two ADCs incorporating architectural redundancy, thereby lowering the probability of convergence to the wrong states [8]. INL as high as 13 bits has been demonstrated in a 2.5-V 0.25-μm CMOS algorithmic ADC using the split-ADC equalization approach [8].

Lastly, a self-equalization architecture [11] was reported during the writing of this article, wherein an offset double conversion scheme was utilized to identify all capacitor mismatch errors in a 12-bit successive approximation (SA) ADC. The absence of a reference path results in the simplicity of this technique, yielding a highly efficient equalization treatment while avoiding a potential front-end mismatch issue in the split-ADC architecture [8, 11].

Other Converter Applications

Theoretically speaking, the advocated parallel-path equalization should work for any A/D conversion architectures including the flash type. However, more succinct and compact error models can often be derived for a multistep ADC than for a single-step one. This is mostly attributable to the built-in redundancy in these architectures to avoid a potential overflow/underflow problem due to circuit offsets in a multistep resolving process. Common multistep Nyquist-rate conversion architectures include pipeline, algorithmic, SA, and subranging types. The SA architecture is of particular interest in scaled processes due to its switching nature, low power, and benign digital compatibility. The linearity-limiting component in an SA ADC is usually its constituent DAC, especially for resolutions of 10 bits and above.

In [12], it was shown that the equalization technique is applicable to an SA ADC to correct its conversion nonlinearities provided that a sub-radix-2 digital-to-analog converter (DAC) is utilized, which compares to the binary search process realized by a conventional SA structure. Note that a sub-radix-2 conversion architecture implements a sub-binary search algorithm of the quantization process, which can be regarded essentially as a form of redundancy. The circuit schematic of an SA ADC is shown in Fig. 4b, where the ratio between adjacent DAC capacitors is chosen to be slightly less than two (as opposed to two in a binary counterpart). An experimental prototype of an 8-bit SA ADC was demonstrated in [13], which achieved a measured low-frequency spurious-free dynamic range (SFDR) of 65 dB in testing.

While technology advancement helps to improve the switching speed of digital as well as analog circuits, with both proven advantageous to the operation of SA ADCs, the sequential search process during which one bit is resolved in each step still imposes an inherent limit on the conversion throughput of the architecture. At high conversion speeds, time-interleaved SA ADC arrays provide a viable way to achieve high throughput with low power consumption. Unfortunately, it is well known that time-interleaved converter arrays are highly sensitive to path-mismatch problems such as gain error, offset, nonlinearity, and sampling aperture skew among many parallel analog signal paths that constitute the interleaving. It turns out that the inherent deficiencies of time interleaving can be mostly lifted when equalization is applied.

The block diagram of a prototype time-interleaved ADC array is shown in Fig. 4a, which aggregates the throughputs of 10 parallel ADCs, each clocked at 60 Msamples/s and utilizing an energy-efficient SA architecture. The raw output of each path is post-processed by an adaptive digital equalizer assisted by a single slow but accurate reference ADC, which continually updates the equalizers using a gradient-descent algorithm to track ambient variations. A unique feature of this treatment is that upon training, the characteristics of the individual ADCs are uniformly aligned to that of the reference ADC, thus eliminating path-mismatch errors inherent

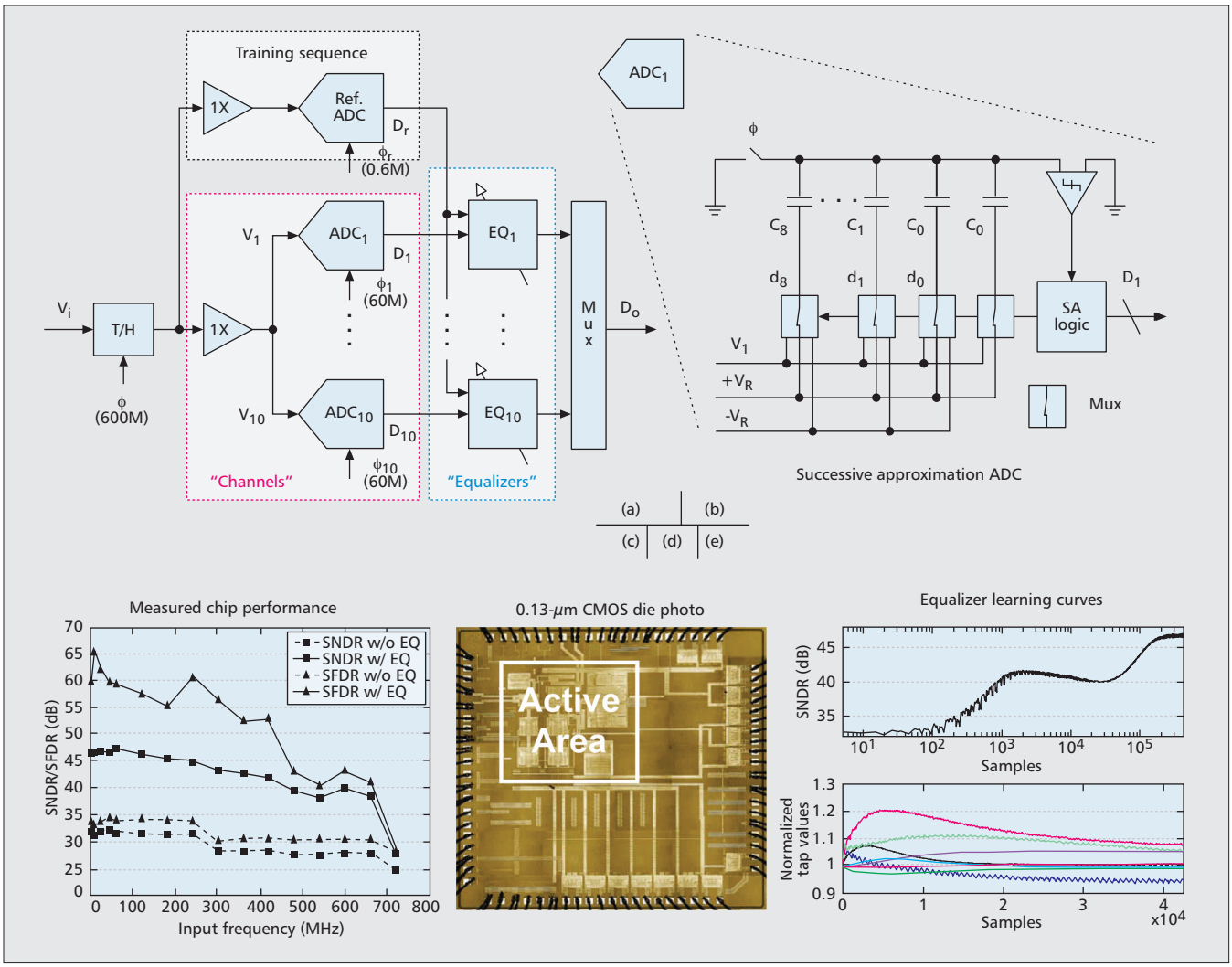
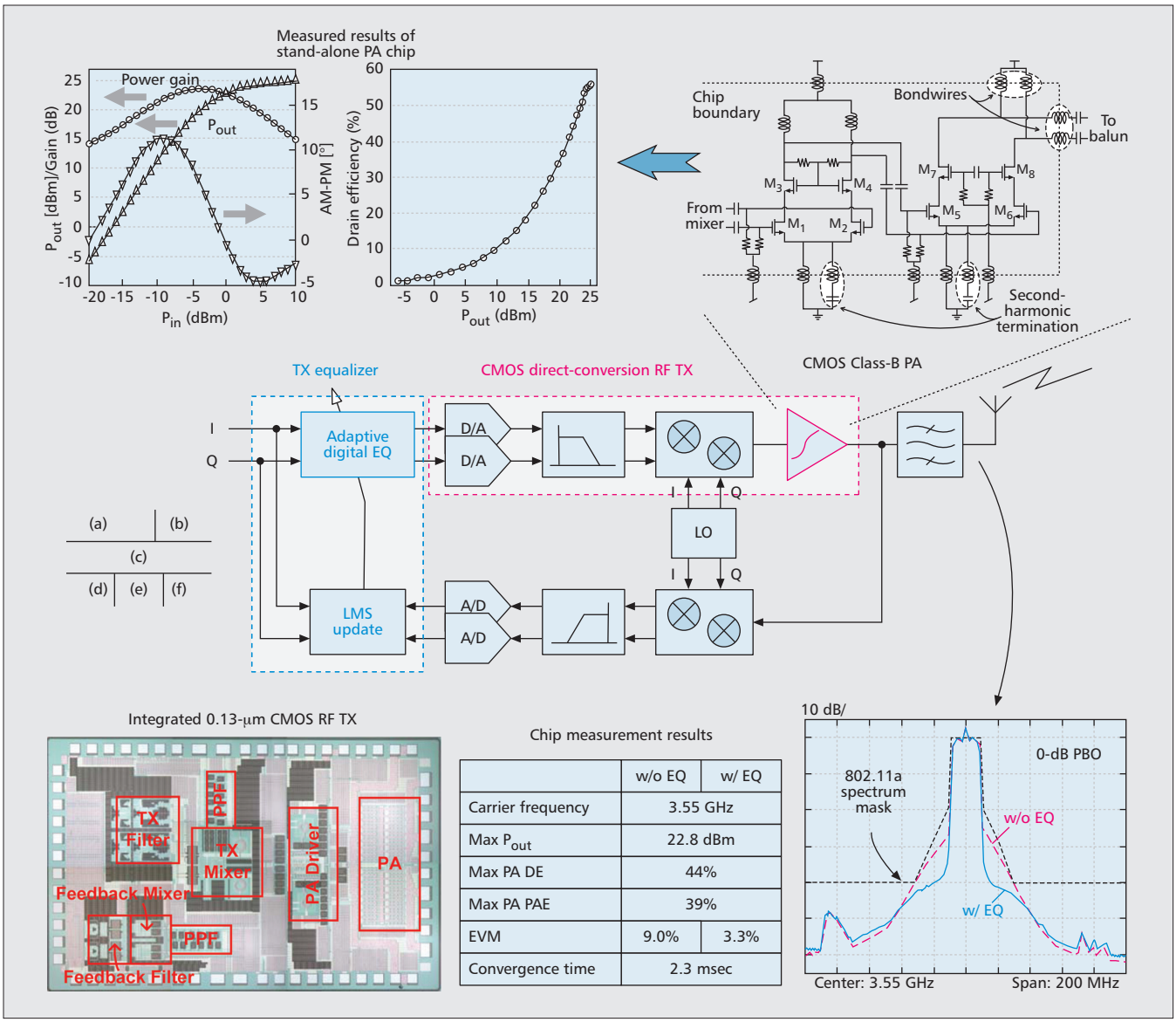


Figure 4. *Equalization of time-interleaved ADC array to a single reference path results in automatic inter-ADC mismatch correction and path alignment.*

in time interleaving. A front-end track-and-hold (T/H) stage is utilized to mitigate the sampling aperture skews among the 10 interleaved paths. The prototype chip was fabricated in a 0.13-μm CMOS process, and occupies an active area of 1.1 mm^2. All measurements were performed at 600 MS/s with a 1.2-V supply. When a 7.8-MHz sinusoidal input was applied, equalization resulted in a signal-to-noise plus distortion ratio (SNDR) improvement from 31.2 to 46.7 dB, and an SFDR improvement from 33.0 to 65.2 dB. The large spectral spurs due to path mismatch errors were largely eliminated. The measured peak INL was 1.7 LSBs and 0.23 LSBs at 8-bit level before and after calibration, respectively. Figure 4c shows the measured SNDR and SFDR vs. the input frequency. The SNDR was maintained above 40 dB up to 460 MHz. In the experiments, it took 200,000 reference samples (0.33 s) to train all 10 interleaved ADCs. The array SNDR during a typical adaptation process is shown in Fig. 4e. The peak-to-peak SNDR fluctuation was less than 0.5 dB in steady state due to continuous background tracking. The total power consumption including analog, digital, and clock distribution was 28 mW. The digital equalizers, which were implemented in software in the experiment, estimate to an additional 2.3 mW in power and 0.08 mm^2 in area. This work was recently reported in [13]. It is interesting to note that the split-ADC equalization scheme has recently been extended to treating time-interleaved ADC arrays as well [14].

Digitally Equalized RF Transmitter

Continuous-time analog circuits perhaps are arguably more difficult to compensate than their discrete-time counterparts such as converters. However, if treating ADC conversion errors resembles receiver equalization, certain continuous-time circuits, such as an RF transmit path, may well be compensated by transmitter equalization. This approach is illustrated in Fig. 5c, where a common direct-conversion CMOS RF transmitter (TX) is augmented by a feedback path and an adaptive digital equalizer. The baseband in-phase (I) and quadrature-phase (Q) digital data are preprocessed digitally to cancel out the effects of any I/Q mismatch and memoryless



	w/o EQ	w/ EQ
Carrier frequency	3.55 GHz	
Max P_{out}	22.8 dBm	
Max PA DE	44%	
Max PA PAE	39%	
EVM	9.0%	3.3%
Convergence time	2.3 msec	

Figure 5. *Transmitter adaptive equalization demonstrates the potential of highly linear and power-efficient CMOS radios with fully integrated nonlinear power amplifiers.*

nonlinearities of the whole transmit path including the severe amplitude and phase distortions of the RF power amplifier (PA). The digital preprocessor is fine-tuned by a least mean square (LMS) algorithm to precisely match to the potentially time-varying characteristics of the RF circuits. This tuning is performed continuously in the background by comparing the original transmitted data with a downconverted version of the actual radiated signal off the antenna (via the feedback path).

Digitally calibrated RF radios in CMOS technology are trendy perhaps mostly due to the fact that an efficient allocation of the spectrum resource for modern communication systems dictates the use of non-constant-envelop modulations that exhibit a high peak-to-average power ratio (PAPR). High PAPR stresses the TX linearity requirement, constraining designers to use linear and therefore power-inefficient analog/RF circuits, especially the most power-consuming component of a TX, the PA. A viable linearity/efficiency enhancement approach for highly integrated CMOS TX is baseband digital equalization, also known as adaptive predistortion, which allows the use of nonlinear PAs such as the Class-B type (a CMOS circuit schematic of a Class-B PA is shown in Fig. 5b) with superior peak and average efficiency characteristics. Wide signal bandwidths can be treated using digital equalization that is less susceptible to stability concerns in contrast to analog linearization schemes such as Cartesian feedback [15].

In a prototype 3.5-GHz CMOS TX chip implemented in a 0.13-μm CMOS technology, an integrated Class-B PA measured 44 percent drain efficiency (DE) and 22.8 dBm saturated output power, which compare favorably to linear Class-A PAs that usually achieve a peak DE in the range of 10–20 percent. However, the efficiency was achieved at the cost of a gross distortion to the transmitted signal shown in Fig. 5a, which displayed an in-band error vector magni-

tude (EVM) as high as 9.0 percent at 0 dB peak back-off (PBO) when a 20-MHz, 64-quadrature amplitude modulation (QAM), 64-subcarrier orthogonal frequency-division multiplexed (OFDM) signal with a 9.6-dB PAPR was transmitted. An RF transmitter that exhibits such linearity is normally of little practical value because an indoor wireless LAN protocol (e.g., 802.11a/g) typically stipulates an EVM spec of –25 dB (5.6 percent). In the experiment, an I/Q-addressed two-dimensional lookup table (2D LUT) was devised to compensate the TX distortions. A unique advantage of employing a 2D LUT compensation scheme is that the I/Q mismatch and memoryless TX nonlinearities, including the baseband circuits (i.e., the DAC and low-pass filter [LPF]) and RF signal paths (i.e., the upconversion mixer and PA), are all uniformly treated. As a result, the EVM was improved significantly to 3.3 percent when the equalizer converged within 2.3 ms. A die photo of the prototype chip is illustrated in Fig. 5d, which integrates the TX, Class-B PA, and feedback path. The digital equalizer was implemented in an Altera Stratix II field programmable gate array (FPGA) that was clocked at 80 MHz. This work was recently reported in [2], and more details of the digital equalizer can be found in [3].

One further remark on this work is about a known side effect of digital preprocessing compensation in which the baseband signal bandwidth may be significantly broadened. In our experiment, a 34-MHz cutoff frequency of the TX LPF and an 80-MHz DAC sample rate were found sufficient to satisfy the 802.11a spectrum mask without additional oversampling. The measured PA output spectra before and after equalization are shown in Fig. 5f. The 5th-order frequency response of the LPF is instrumental here to retain all desired spread spectrum and yet maintain the low oversampling ratio.

Conclusion

The art of analog design has evolved such that circuit linearity may be more efficiently procured using system-level techniques rather than device- or component-level ones. Among various research efforts inspired by this vision, a digital equalization approach addressing analog circuit distortions stemming from various physical origins, including the process variability in deeply scaled technologies, is presented. Several experimental chip results are showcased to demonstrate the efficacy of this approach and support the rationale behind the advocated research theme. Unprecedented analog linearity, energy efficiency, and scalability are likely outcomes of this approach in nanometer fabrication technologies in the years to come.

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