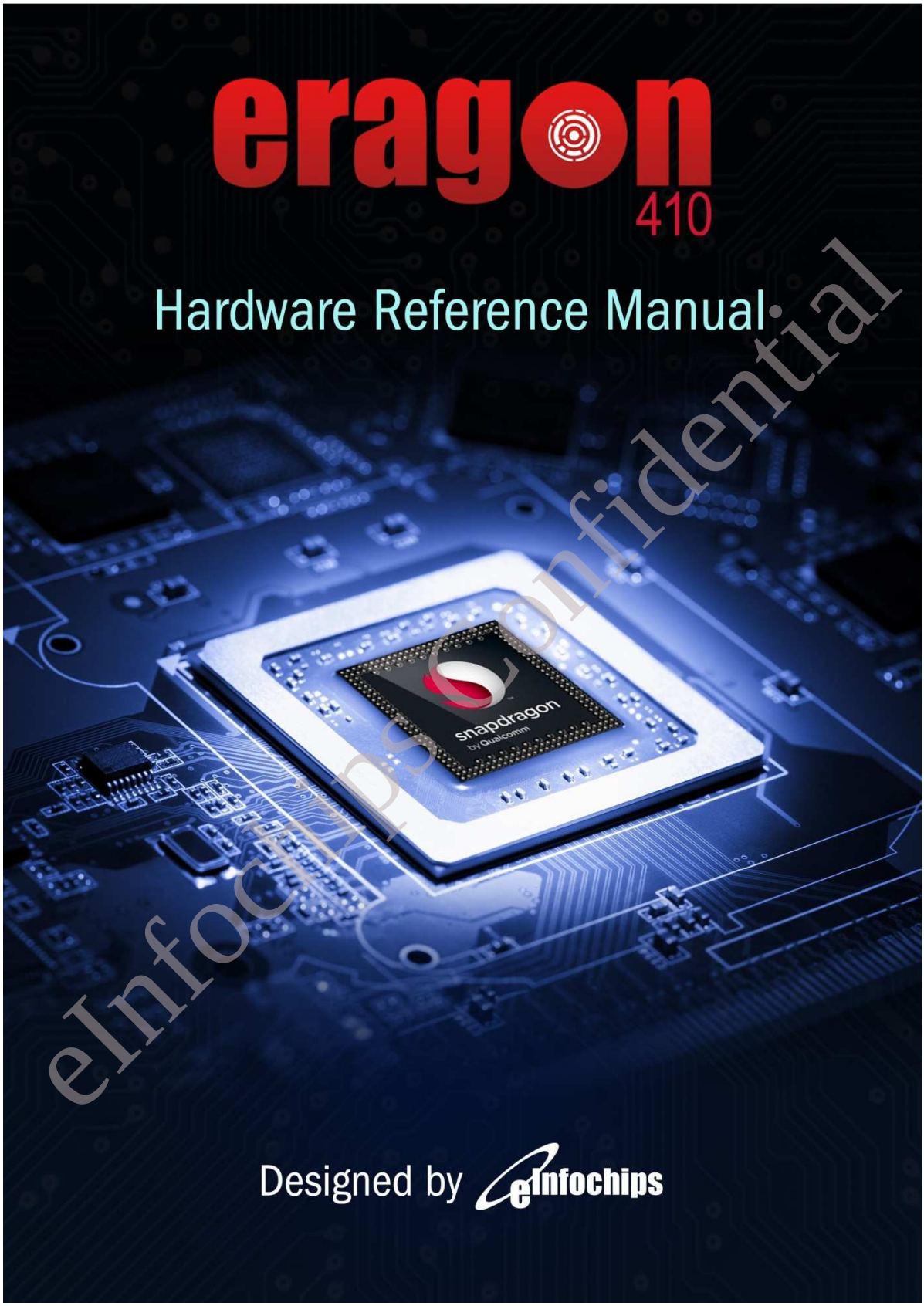
eragon 410

Hardware Reference Manual



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1 Document Details

1.1 Document History

Version	Author		Reviewer		Approver		Description Of Changes
	Name	Date	Name	Review Comment ID	Name	Date	
Release Ver. 1.0	*eInfochips*	*05-Dec-15*	*eInfochips*	*05-Dec-15*	*eInfochips*	*05-Dec-15*	*Initial release*
Release Ver. 1.1	*eInfochips*	*01-June-17*	*eInfochips*	*05-June-17*	*eInfochips*	*05-June-17*	*Release Update*

Table 1: Document History

1.2 Definition, Acronyms and Abbreviations

Definition/Acronym/Abbreviation	Description
AC	Alternate Current
BLE	Bluetooth Low Energy
BOM	Bill of Material
Bpp	Bits Per Pixel
BT	Bluetooth
CPU	Central Processing Unit
CSI	Camera Serial Interface
DC	Direct Current
DDR	Double Data Rate
DMIPS	Dhrystone MIPS

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DSI	Display Serial Interface
eI	eInfochips
GB	Giga Byte
GPIO	General Purpose Interface
GPS	Global Positioning System
HD	High Definition
HDMI	High Definition Multimedia Interface
HSIC	High-speed Serial Interface Connect
I/O	Input Output
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
Inc.	Incorporated
JTAG	Joint Test Application Group
KB	Kilo Byte
LAN	Local Area Network
LNA	Low Noise Amplifier
LPDDR	Lower Power DDR
MB	Mega Byte
Mbps	Mega Bits Per Second
MIPI	Mobile protocol working Alliance (not an Acronym)
MIPS	Million Instruction Per Second
MISO	Master In Slave Out
Mm	Millimeter
MMC	Multi Media Card

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MOSI	Master Out Slave In
MP	Mega Pixel
OTG	On The Go
PCIe	Peripheral Component Interface – Express
PLL	Phase Loop Locked
PMIC	Power Management IC
RAM	Random Access Memory
RF	Radio Frequency
RH	Relative Humidity
RoHS	Restriction of Hazardous Substances
Rx	Receive
SATA	Serial
SATA	Serial Advance Technology Attachment
SiP	System In Package
SMPS	Switched Mode Power Supply
SOM	System On Module
SPI	Serial peripheral Interface
Tx	Transmit
UART	Universal Asynchronous Interface
USB	Universal Serial Bus
VCO	Voltage Controlled Oscillator
WLAN	Wireless LAN

Table 2 : Definition, Acronyms and Abbreviations

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1.3 References

No.	Document	Version	Remarks
1	ERAGON 410_SOM Datasheet	1.0	

Table 3 : References

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3 Preface

This document provides an overview of the EIC-Q410-200 Nano SoM and ERAGON410 reference design based on Qualcomm's APQ8016 SoC. It provides detailed information about the hardware components and associated software release .

3.1 Intended Audience

This document is intended for technically qualified personnel.

3.2 Intended Use

The development platform supports a wide range of industry interfaces and offers a comprehensive hardware and software design. It comes with Android 5.1.1 and Linaro 15.07 software packages and sample demo applications for easy adaption.

This platform enables developers to evaluate and create solutions targeted at various market segments while customers and OEMs can build their products based on these designs directly or with customizations.

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4 Overview

The EIC-Q410-200 Nano SoM provides an ideal building block for simple integration with a wide range of products in target markets requiring rich multimedia functionality, powerful graphics processing and video capabilities, as well as high-processing power, in a compact, RoHS compliant, fan less, cost effective SoM with low power consumption.

The EIC-Q410-200 Nano SoM leverages cutting edge mobile computing for embedded and industrial product designs, based on the Qualcomm Snapdragon™ 410 (APQ8016) 1.2 GHz quad Krait™ CPU, high performance Adreno 306 GPU and a dedicated DSP for advanced A/V processing.

The SOM is equipped with full range of interfaces available in the Qualcomm Snapdragon APQ8016 SoC, which are routed to the 156 pin edge castellation connector.

The APQ8016 SOM supports two operating system

- Linaro Kernel (15.07)
- Android 5.1.1

The ERAGON410 Development kit is based on EIC-Q410-200 Nano SoM for the developers to quick start their application development and is ideal for rapid prototyping of end product. With support for almost all the peripherals, it reduces the design time of innovative applications and helps achieve early time to market. With variety of peripherals, this kit is targeted for wide range of applications supporting bulk storage, faster connectivity, higher through put and performance at lower power.

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4.1 ERAGON 410_Key Features

CPU • Qualcomm Snapdragon 410 • Quad-core ARM® Cortex® A53 at up to 1.2 GHz per core • 64-Bits capable • Qualcomm Adreno 306 400MHz GPU for PC-class graphics with support for advanced APIs, including OpenGL ES 3.0, OpenCL, DirectX, and content security • 1920 x 1080p video encoding/ decoding capability	**Operating System** • Linaro Kernel Release (15.07) • Android 5.1.1
Memory • **RAM:** Up to 16Gb LPDDR3 at up to 533 MHz • **Storage:** Up to 16GB eMMC v4.5	**Connectivity** • Gigabit Ethernet • WLAN 802.11 b/g/n 2.4GHz • Bluetooth 4.0 • GPS
Camera MIPI CSI Alliance for D-PHY, v0.65 and v0.9/v1.0. • 1xMIPI CSI 2 Lane Camera Interface. • 1xMIPI CSI 4 Lane Camera Interface.	**Display** • MIPI DSI for D-PHY v0.65, v0.81, v0.90 • Resolution: QXGA up to 1920 x 1080p, 24 bps.
Audio • **Input:** o 2x Analog mic • **Output:** o 1x Stereo Headset Output o 1x Speaker Output o 1x Earphone output	**Multimedia** • Up to 13Mp in-line JPEG encode at 15 fps, 60 fps WXGA view finder frame rate • Support for wide variety of pixel manipulation, camera modes, image effects, and post-processing techniques including defective pixel correction.
USB • 1x USB OTG • 2x USB 2.0 **Note**: The APQ8016 includes a single USB OTG channel. A USB Mux Switch on SoM, routes this single USB channel either to a USB HUB or to the USB OTG connector on Carrier card.	**Miscellaneous** • 4xI2C, 2xUART, 2xSPI • 7xGPIOs • JTAG
Power Input & Consumption Voltage In: +12VDC/3A	**Physical & Operating Characteristics** • **Dimension:** o 100mm x 72mm • **Storage Temperature Range:** o -20C to 70C • **Recommended Operating Temperature Range:** o 0C to 70C

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4.2 Applications

The EIC-Q410-200 Nano SoM is used in a wide range of products across many different target markets. Some of the typical applications are:

- Domestic Robot
- Digital signage
- Security & Surveillance
- Biometric Access Control Systems
- POS Terminal
- Home and Health Hub
- Human-machine interface
- Home energy management systems
- In-flight entertainment
- Intelligent industrial control systems
- Portable medical

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5 Getting Started

5.1 Prerequisites

Before power up the ERAGON 410 board for the first time user will need the following:

- ERAGON 410 board.
- The ERAGON 410 Boards compliant power supply.
- A HDMI or DSI LCD Display that supports a resolution of minimmum720P/30Hz.
- HDMI Bridge Board or LCD Bridge Board.
- FFC Cable for connecting Bridge Board to the ERAGON 410 Board.
- Standard Type-A HDMI-HDMI cable to connect the board to the Monitor.
- USB Mouse & Keyboard.

5.2 Starting the board for the first time

To start the board, follow these simple steps:

Step 1. Connect the ERAGON 410 Board to the HDMI Bridge Board or to the LCD Bridge Board using FFC cable provided along with kit.

Step 2. Connect the Standard HDMI Type A cable to the HDMI connector of HDMI Bridge board to the LCD Monitor which is compatible with the HDMI. User can also use the MIPI LCD Display for display purpose using the LCD Bridge Board.

Step 3. Connect the USB compatible keyboard and mouse to the USB connector of board.

Step 4. Ensure that the boot switch SW5 is set to '000', all in OFF position.

Step 5. Connect the compatible power supply to power connector J15 on carrier board.

Once User plug the power supply into a power outlet the board will start the booting process, and User should see Android boot up image on screen.

Please note that the first boot takes several minutes due to Androids initialization. Subsequent boot times should be faster.

Note: If User uses the HDMI port, User has to connect both FFC cable, DSI Data FFC Cable & another for Audio Application. While using only LCD Bridge Board User has to connect only DSI Data FFC cable.

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6 System Block Diagram

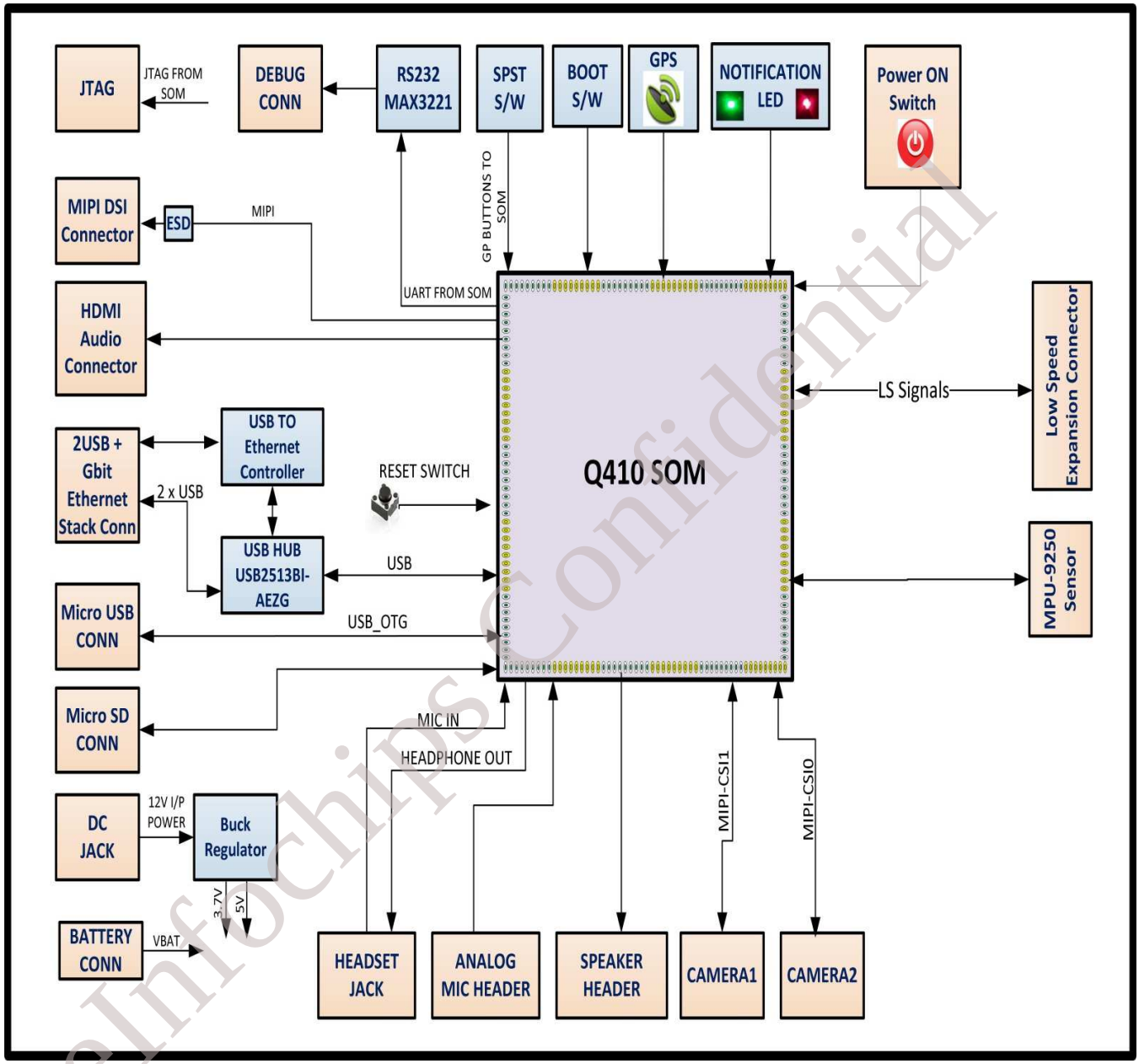

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Figure 1 – Functional Block Diagram

6.1 ERAGON410 BOARD IMAGE

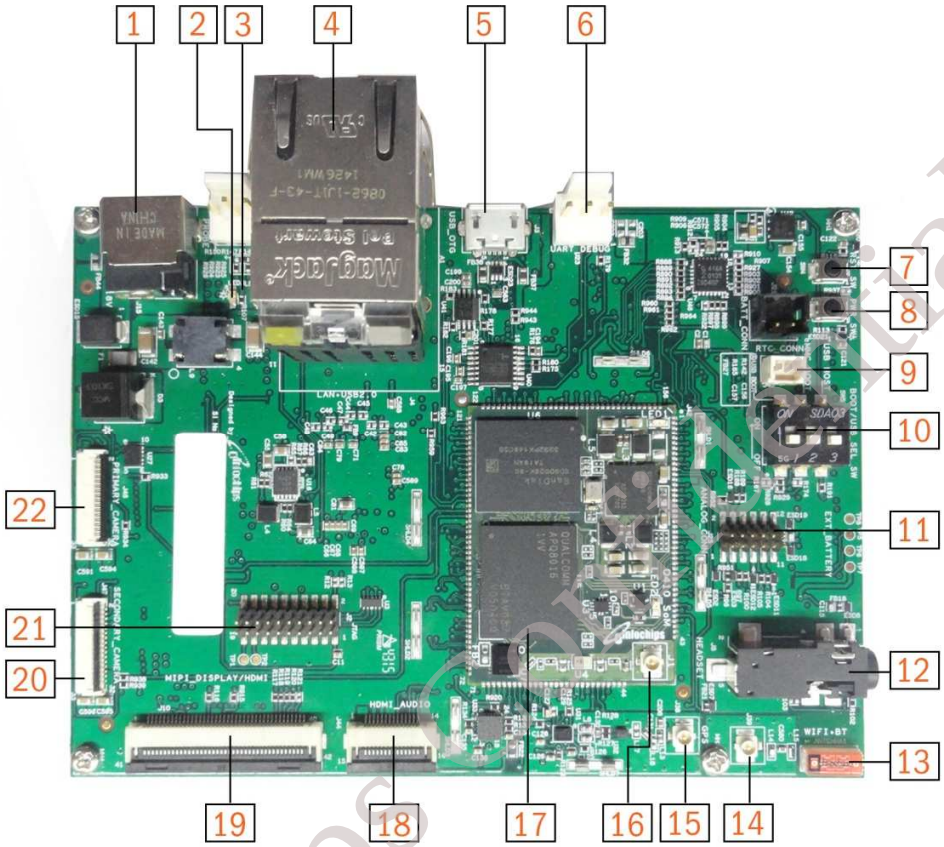

Figure 2 – ERAGON410 Top View of SOM + Carrier Board

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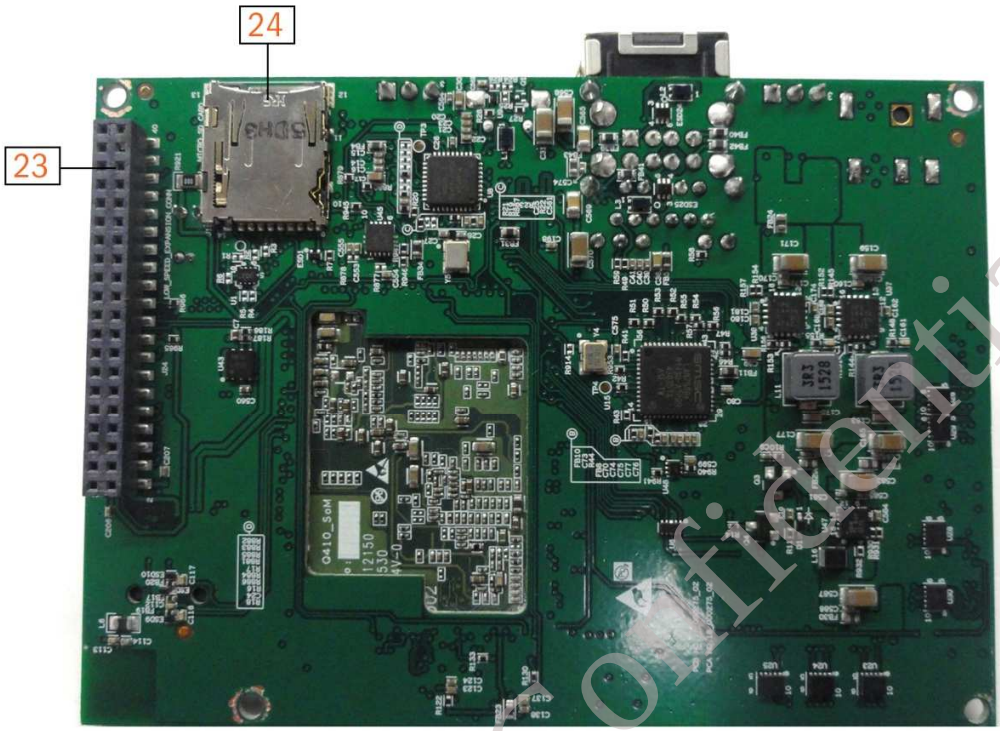

Figure 3 – ERAGON410 Bottom View of SOM + Carrier Board

The ERAGON 410 board offers a wide boost of interfaces and peripherals, including several high speed signals through its edge connector. The major parts of ERAGON 410 board are marked with labels in above figures and the name of it is, are listed in the below table.

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ERAGON 410 Component Details	
1	12V Power Supply Jack Connector
2	Status LED 1 (3.7V Power Indication)
3	Status LED 2 (5V Power Indication)
4	USB + Ethernet Connector(USBA Dual + RJ45)
5	micro USB OTG Connector
6	Debug UART Header
7	Fast boot Switch
8	Power On Switch
9	RTC Battery Coin Cell Header
10	Boot Configuration Switch
11	Analog Audio Connector
12	3.5mm Audio Jack
13	Wi-Fi + BT Chip Antenna
14	Wi-Fi + BT UFL Header On Carrier
15	GPS UFL Header
16	UFL Header on SOM
17	APQ8016 Processor
18	HDMI Audio Connector
19	MIPI DSI Connector
20	CSI Secondary Connector
21	JTAG Connector
22	CSI Primary Connector
23	Low Speed Expansion Connector
24	Micro SD Card Connector

Table 4 : ERAGON 410 COMPONENTS

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6.2 Major Blocks of ERAGON410 Board

6.2.1 Processor features and interfaces

- The Qualcomm APQ8016 is 1.2GHz, Quad-Krait processor. It has 4core(s), resulting in extremely efficient multi-tasking when compared to dual core processors.
- Four Krait application processors – advanced CPU architecture for high-end multimedia applications.
- ARM v7 compliant
- Powerful QDSP6 core (500 MHz) for application support (within the low-power audio subsystem)
- 128kB TCM/L2 memory

Memory Support Features

- Single channel SDRAM blocks, 32-bit wide/channel LPDDR2, DDR3 through EBI interface
- Support up to 16 GB total memory
- Secure Digital supports eMMC flash.
- There is SD card connector is also available for external storage devices.

Multimedia features

- Primary (via 4-lane MIPI_CSI) – supports CMOS and CCD sensors
  – Up to 13 MP in-line JPEG encode at 15 fps
  – 60 fps WXGA viewfinder frame rate
  – A wide variety of pixel manipulation, camera modes, image effects, and post-processing techniques are supported, including defective pixel correction.

Web technologies

- V8 JavaScript Engine optimizations
- Webkit browser JPEG hardware decode acceleration
- Webkit compositing engine 2D/VG GPU acceleration
- Networking Stack IP and HTTP tuning
- Flash 10.1 3D/GL-ES GPU acceleration

Messaging

- Short messaging services like text messages, text encoding for SMS
- Multimedia messaging services like combined video (MPEG4), still image (JPEG), voice tag (AMR), and text sent as a message

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6.2.2 Memory Interface

The ERAGON 410 Board uses a single embedded Multi Chip Package (eMCP) dual function LPDDR3/eMMC memory solution. The installed chip provides 8Gbyte of eMMC and 1Gbyte of LPDDR3. As the APQ8016 supports the single chip for both eMMC & DDR3, the board size is decreased.

- The LPDDR3 is a 32bits width bus implementation interfacing directly to the APQ8016 build-in LPDDR3 controller. The maximum DDR clock is 533Mhz
- The eMMC is an 8 bits implementation interfacing with APQ8016 SDC1 interface supports eMMC 4.5 specifications.

6.2.3 Micro SDHC

The ERAGON 410 board, micro SD slot signals are routed directly to the APQ8016 SDC2 interface from the Micro SD card connector(J1). The Connector is a push-push type with a dedicated support for card detect signal. The ERAGON 410 board uses Four Data Signals Starting from SDC2_DATA0_SOM to SDC2_DATA3_SOM, one SDC2_CMD_SOM for command, one SDC2_CLK_SOM Micro SD card Clock and One GPIO APQ GPIO_38 as the SD_CARD_DET_N.

Figure 4 – Micro SD card Connector

6.2.4 Wi-Fi/BT/RF

The ERAGON 410 board deployed Qualcomm's RF chip WCN3620 solution that integrates two different wireless connectivity technologies into a single device, the interfaces are:

- WLAN compliant with IEEE 802.11 b/g/n specifications for Wi-Fi.
- Bluetooth compliant with the BT specifications version 4.0 (BR/EDT + BLE), requirements for BT

For this purpose the board contain on chip antenna.

Figure 5 – Wi-Fi + BT Antenna

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6.2.5 Display Interface

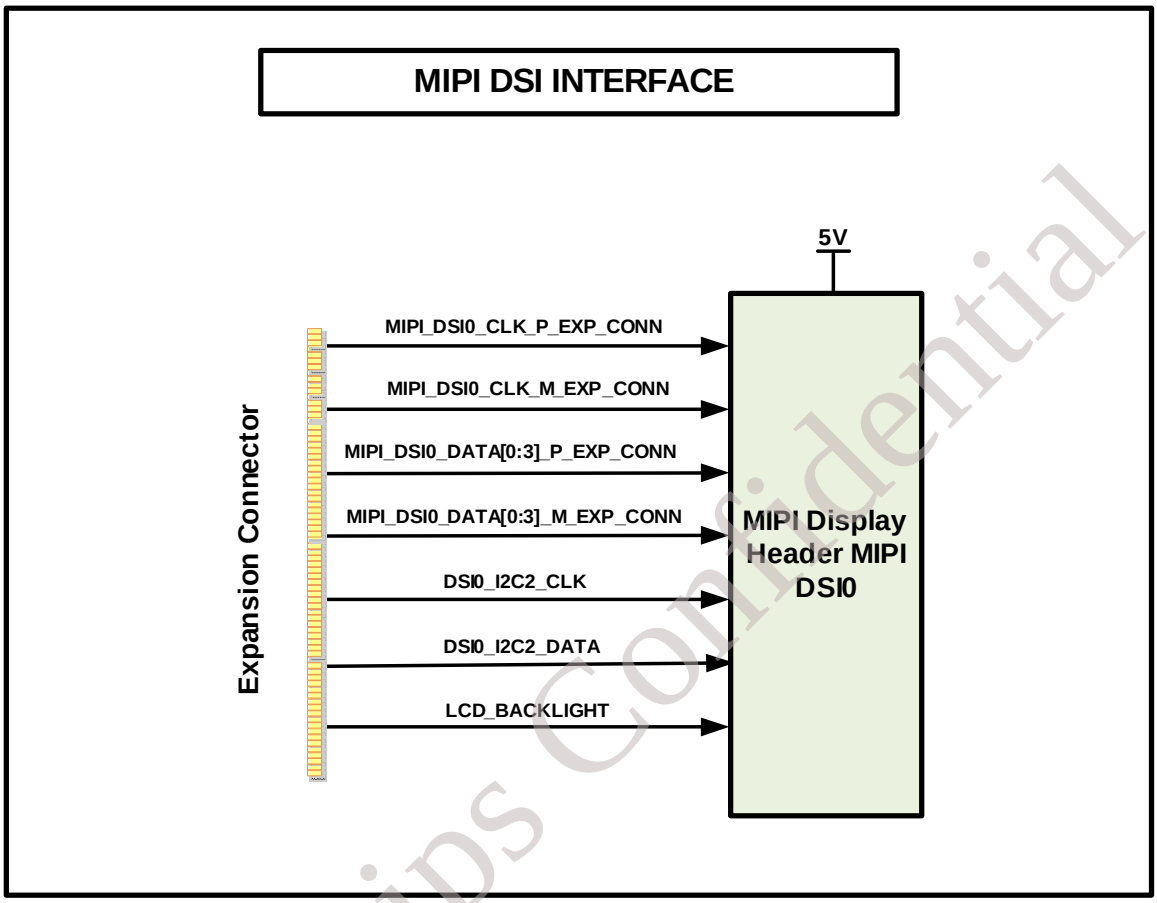

Figure 6 – Display Interface

6.2.5.1 HDMI

The Qualcomm APQ8016 Processor does not include a built-in HDMI interface. The ERAGON 410 has the built-in MIPI-DSI 4 lanes interface that is used as a source for the HDMI output. A DSI to HDMI Bridge Board performs this task and it supports a resolution from 480p to 720p at 30Hz.

While the ADV7533 on the DSI to HDMI Bridge board supports automatic input video format timing detection (CEA-861E) and an I2C channel from the APQ8016 allows the user to configure the operation of this Bridge Board. The BLSP2_I2C interface is used from the SoC that connects to the Bridgeboard.

This Bridge Board supports audio as well. The ERAGON 410 uses a single bit I2S2 interface from the APQ8016 chip which is mentioned in the below section.

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6.2.5.2 HDMI Audio Connector

The ERAGON 410 contains the 14 pin HDMI Audio Connector (Ref J44) on the board. A 3-wire (audio out only) I2S channel is routed directly from the APQ8016 SoC I2S interface pins to the DSI-HDMI bridge Board through HDMI Audio connector.

Figure 7 – HDMI Audio Connector

The pin specification of the HDMI Audio Connector is mentioned below:

Pin No.	Signal Name	Specification
1	VCC_3V3	3.3V Rail Supply Pin.
2	NC	Not Connected.
3	SYS_5P0	5V Supply Pin.
4	NC	Not Connected.
5	VCC_1V8	1.8V Supply Pin.
6	NC	Not Connected.
7,8	GND	Ground Pin.
9	APQ_19.2MHz_SYSCLK2	19.2MHz System Clock frequency.
10	DSI2HDMI_MI2S_SCK	I2S Clock Frequency.
11	HDMI_HPD_N	HDMI Hot Plug detect Pin.
12	DSI2HDMI_MI2S_WS	I2S Word Select Pin.
13	DSI2HDMI_MI2S_INT_N	I2S Interrupt Pin (Active Low).
14	DSI2HDMI_MI2S_DATA0	I2S Data Signal.

Table 5 : HDMI Audio Connector Pinouts

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6.2.5.3 MIPI DSI Connector

The ERAGON 410 implemented with a 40-pin four-lane MIPI_DSI interface connector (Ref J10). The signals from this connector are connected to HDMI Bridge board.

Figure 8 – MIPI DSI Connector

The pin specification of the DSI connector is mentioned below:

Pin No.	Signal Name	Specification
1	GND	Ground.
2	NC	Not Connected.
3	MIPI_DSI0_CLK_P_EXP_CONN	DSI Differential Clock Positive.
4	NC	Not Connected.
5	MIPI_DSI0_CLK_M_EXP_CONN	DSI Differential Clock Negative.
6	NC	Not Connected.
7	GND	Ground
8	SYS_5P0	5V Supply.
9	MIPI_DSI0_DATA0_P_EXP_CONN	DSI Data0 Differential Positive.
10	SYS_5P0	5V Supply.
11	MIPI_DSI0_DATA0_M_EXP_CONN	DSI Data0 Differential Negative.
12	GND	Ground.
13	GND	Ground.
14	NC	Not Connected.
15	MIPI_DSI0_DATA1_P_EXP_CONN	DSI Data1 Differential Positive.
16	DSI_RST_IN	DSI Reset Input.
17	MIPI_DSI0_DATA1_M_EXP_CONN	DSI Data1 Differential Negative.

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18	NC	Not Connected.
19	GND	Ground.
20	PMIC_MPP4_PWM	PMIC MPP4 GPIO for PWM.
21	MIPI_DSI0_DATA2_P_EXP_CONN	DSI Data2 Differential Positive.
22	GND	Ground.
23	MIPI_DSI0_DATA2_M_EXP_CONN	DSI Data2 Differential Negative.
24	NC	Not Connected.
25	GND	Ground
26	NC	Not Connected.
27	MIPI_DSI0_DATA3_P_EXP_CONN	DSI Data3 Differential Positive.
28	NC	Not Connected.
29	MIPI_DSI0_DATA3_M_EXP_CONN	DSI Data3 Differential Negative.
30	NC	Not Connected.
31	GND	Ground.
32	GND	Ground.
33	BLSP2_I2C_SCL	BLSP2 I2C Clock.
34	TOUCH_INT	Touch Interrupt.
35	BLSP2_I2C_SDA	BLSP2 I2C Data.
36	TOUCH_RST	Touch Reset.
37	GND	Ground.
38	TOUCH_GPIO	Touch GPIO.
39	GND	Ground.
40	NC	Not Connected.

Table 6 : MIPI DSI Connector Pinouts

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6.2.6 USB Ports

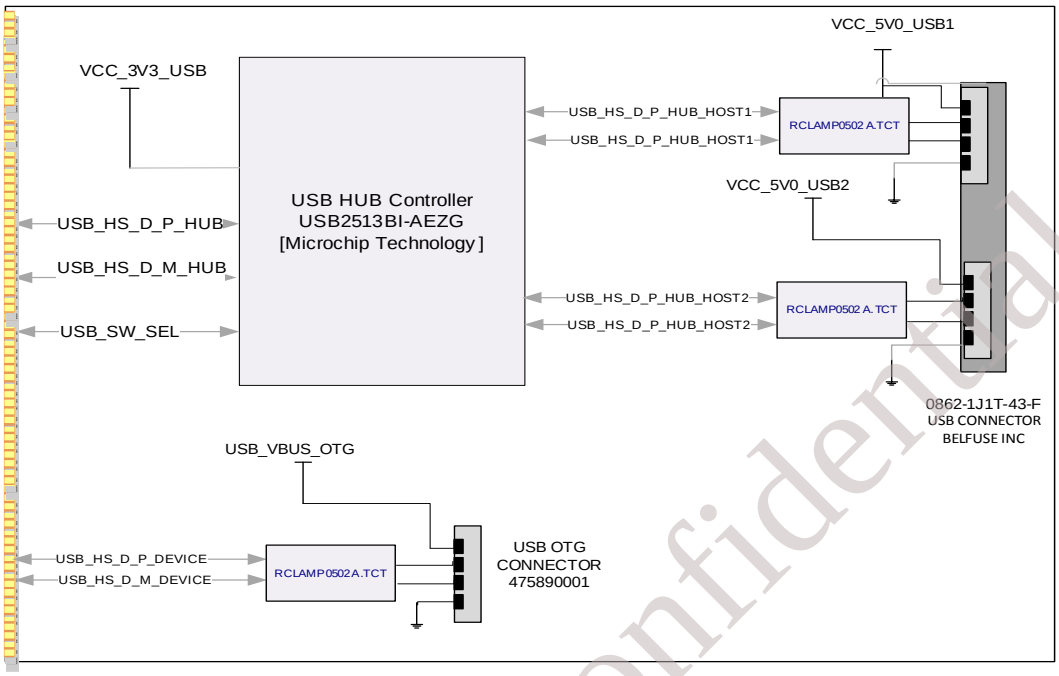

Figure 9 – USB Interfaces

6.2.6.1 USB-Host Ports

The ERAGON 410 Board has two USB host ports. The APQ8016 includes a single USB OTG channel. A USB Mux Switch TC7USB40MU, routes this single USB channel either to a USB HUB or to the USB OTG connector. The control of U3 switch is done via hardware or software. The control of U3 Switch via software is controlled by setting the GPIO (USB_SW_SEL_PM, GPIO_4 from the board PMIC) and the Control via hardware is done by setting the switch SW5 on the board. When the signal is logic low, '0', the USB data lines are routed to the Micro USB connector and the APQ8016 built-in USBOTG port is set to device mode. When 'USB_SW_SEL_PM' is logic level high, '1', the USB data lines are routed to a 3-port USB HUB and the APQ8016 built-in USBOTG port is set to host mode. The user can overwrite the software control by sliding switch 3 of Dip Switch (Ref SW5) to the 'ON' position. That action forces the USB–mux switch to route the built-in USBOTG data lines to the USB HUB. The overwrite option exists for the host mode only, User cannot hardware overwrite the mux to force device mode.

Figure 10 – USB Host to Device Change Switch

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Port 1 of the USB HUB (U8) is routed to a Type 'A' USB Host connector on USB stack (J4). A current limited USB Load switch sets the Power Current limit to 500mA. This port is named HOST2 in the board schematic.

Port 2 of the USB HUB (U8) is routed to a Type 'A' USB Host connector on USB stack (J4). A current limited USB load switch sets the Power Current limit to 500mA. This port is named HOST1 in the board schematic.

Port 3 of the USB HUB (U8) is routed to the USB to Ethernet convertor IC (U15) for the Ethernet Application. No current limited controller is implemented on the board for this channel.

6.2.6.2 USB-Device Port

ERAGON 410 Board contains a USB port to be implemented as an OTG port or a device port. The port is referenced as J3, a micro USB type B. If an application requires the use of the device port, USB_SW_SEL_PM signal must be set to low '0' and the user must verify that switch 3 of Dip Switch is set to the 'OFF' position.

Figure 11 – USB OTG Connector

Please note: The board can work in one mode at a time, Host mode or Device mode.

6.2.7 Audio Section

The ERAGON 410 board contains the headset, Speaker and MIC for the Audio. These sections are described below.

6.2.7.1 Headset

The ERAGON 410 Board Headset signals are routed from the inbuilt codec of PMIC PM8916 (U2) to the Connector J8.

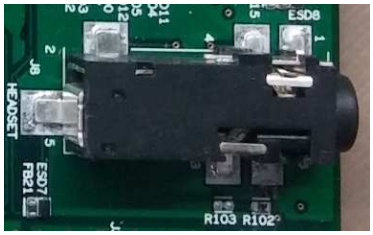

Figure 12 – Headset Connector

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The descriptions of the signals are given below:

- CDC_MIC2_P: Headphone Mic Output.
- CDC_HPH_R: Headphone PA Right Channel Output.
- CDC_HPH_L: Headphone PA Left channel Output.
- CDC_HS_DET: Headphone Detection.
- CDC_HPH_REF: Headphone Ground sensing.

6.2.7.2 FM Antenna

The FM_RX_ANT signal from the headset connector J8 is the path for the FM antenna to reach the WCN3620 (U7), an integrated three different connectivity technologies device:

- WLAN IEE802.11 b/g/n
- BT 4.0 (BR/EDR/BLE)
- Worldwide FM radio

6.2.8 Analog Audio Connector

The ERAGON 410 Board implements with 12Pin Analog audio connector (Ref J25).

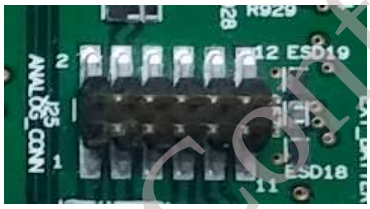

Figure 13 – Analog Audio Connector

The Signal Description is mentioned below:

Pin No.	Signal Name
1	CDC_MIC_BIAS1_CONN
2	CDC_MIC_BIAS1_CONN
3	CDC_MIC1_P_CONN
4	CDC_MIC1_M_CONN
5	GND_CFILT
6	GND_CFILT
7	SPKR_OUT_M_CONN
8	GND_CFILT
9	SPKR_OUT_P_CONN
10	GND_CFILT
11	CDC_EAR_P
12	CDC_EAR_M

Table 7 : Analog Audio Connector Pinouts

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6.2.8.1 Speaker

The speaker signals are routed from the PM8916 PMIC built-in Audio CODEC (U2) to the Analog audio connector (J25), the two signals are:

- SPKR_OUT_P_CONN - Speaker Amplifier Output Positive on Pin 9.
- SPKR_OUT_M_CONN - Speaker Amplifier Output Negative on Pin 7.

6.2.8.2 Mic

The microphone signals are rounded to the PM8916 PMIC Built-In CODEC (U2) to Analog Connector (J25) , the three signals are:

- CDC_MIC1_P_CONN - Primary mic1 on Pin 3.
- CDC_MIC3_P_CONN - Second mic3 on Pin 4.
- CDC_MIC_BIAS1_CONN - PMIC MIC bias on Pin 1, 2.
- GND_CFILT - Ground reference for PMIC bias on Pin 6.

6.2.8.3 EAR Piece

The Two signals CDC_EAR_P & CDC_EAR_M are routed for the application of ear phone, directly to the PMIC built-in Audio CODEC (U2) from the Analog Connector (J25).

- CDC_EAR_P - Earphone positive on Pin 11.
- CDC_EAR_M - Earphone Negative on Pin 12.

6.2.9 UART

The ERAGON 410 Board supports for two UART. One SoC UART is used for the Debug Console (J23) and another UART is provided on the Low Speed Expansion Connector (J24).

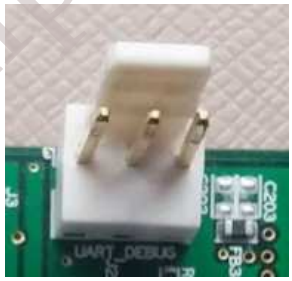

Figure 14 – Debug Connector

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6.2.10 JTAG

The ERAGON 410 Board contains 20 Pin JTAG Connector (J2) on the top side of the Board for the debug purpose.

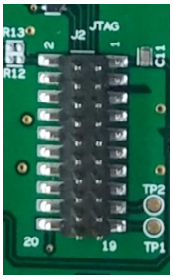

Figure 15 – JTAG Connector

The Signal Description of the JTAG Connector is mentioned below:

Pin No.	Signal Name
1	JTAG_CONN_VREF
2	Supply Voltage (Either SYS5P0 or VCC3V3)
3	JTAG_TRST_N
4	GND
5	JTAG_TDI
6	GND
7	JTAG_TMS
8	GND
9	JTAG_TCK
10	GND
11	Not Connected
12	GND
13	JTAG_TDO
14	GND
15	JTAG_SRST_N
16	GND
17	Test Point 1
18	GND
19	Test Point 2
20	JTAG_CONN_DET_N

Table 8 : JTAG Connector Pinouts

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6.2.11 Systems LEDs

The ERAGON 410 Board contains four LEDs for the indication purpose. Two LEDs mounted on the SOM board Reference LED1 and LED2. LED1 is used for the indication of VPH Power on the board and LED2 is used for reset indication. Two LEDs (LED3 and LED5) are mounted on the carrier board for the power supply indication of VPH_PWR and SYS_5P0, respectively.

6.2.12 Expansion Connector

The ERAGON 410 Board contains the one 40 pin Low Speed Expansion Connector. The Pinouts of the Low Speed Expansion Connector is given in the Section 7 .

6.2.13 GPS

The ERAGON 410 Board has a GPS antenna connector mounted on board (J38). The GPS Implementation is based on Qualcomm WGR7640 Chip (U31). This chip supports GPS, GLONASS and COMPASS. The Active Patch Antenna (AP.17F.07.0064A) needs to be connected on U.FL. Connector (J38) for GPS Application. Antenna other than mentioned can be implemented as per requirement but the performance might be different.

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7 Low Speed Expansion Connector

The ERAGON 410 Board has a Low Speed Expansion Connector (Ref J24).

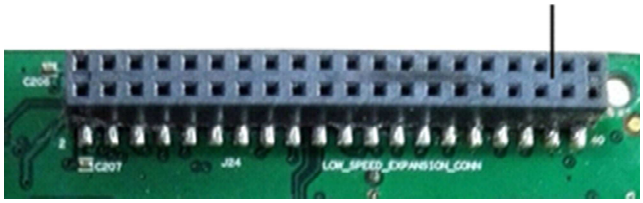

Figure 16 – Low Speed Expansion Connector

The Following table shows the Low Speed Expansion Connector pinouts.

Pin No.	Signal Name	Pin No.	Signal Name
1	VCC_1V8	21	BLSP5_SPI_CLK (1.8V Digital Logic)
2	VCC_3V3	22	BLSP5_SPI_CS_N (1.8V Digital Logic)
3	LS_EXP_GPIO_1	23	BLSP5_SPI_MISO (1.8V Digital Logic)
4	LS_EXP_GPIO_2	24	BLSP5_SPI_MOSI (1.8V Digital Logic)
5	LS_EXP_GPIO_3	25	BLSP6_I2C_SDA (1.8V Digital Logic)
6	LS_EXP_GPIO_4	26	BLSP6_I2C_SCL (1.8V Digital Logic)
7	LS_EXP_GPIO_5	27	BLSP2_I2C_SDA (1.8V Digital Logic)
8	LS_EXP_GPIO_6	28	BLSP2_I2C_SCL (1.8V Digital Logic)
9	LS_EXP_GPIO_7	29	PMIC_MPP3 (PMIC GPIO MPP3)
10	ALPS_INT_N	30	PMIC_MPP2 (PMIC GPIO MPP2)
11	GND	31	GND
12	GND	32	GND
13	BLSP1_UART_TX (1.8V Driven Logic)	33	MI2S_1_SCLK (1.8V Digital Logic)
14	BLSP1_UART_RX (1.8V Driven Logic)	34	MI2S_1_DATA0 (1.8V Digital Logic)
15	BLSP1_UART_CTS_N (1.8V Driven Logic)	35	MI2S_1_WS (1.8V Digital Logic)
16	BLSP1_UART_RTS_N (1.8V Driven Logic)	36	MI2S_1_DATA1 (1.8V Digital Logic)
17	BLSP3_SPI_CLK (1.8V Digital Logic)	37	GND
18	BLSP3_SPI_CS_N (1.8V Digital Logic)	38	GND
19	BLSP3_SPI_MISO (1.8V Digital Logic)	39	GND
20	BLSP3_SPI_MOSI (1.8V Digital Logic)	40	GND

Table 9 : Low Speed Expansion Connector Pinouts

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7.1 UART

The Four wire UART implementation that connects directly to the APQ8016 SoC. BLSP1 port is used for UART which is directly routed to the Low Speed Expansion Connector. This UART Signals are driven at 1.8V.

7.2 I2C

The ERAGON 410 Board contain the two I2C interfaces to be implemented on the Low Speed Expansion Connector (J24). These two I2C lines are operating on 1.8V voltage.

The ERAGON 410 board implements both interfaces, BLSP2_I2C and BLSP6_I2C that connects directly to the APQ8016 SoC. A 2K resistor is provided as pull-up for each of the I2C lines per the I2C specifications, these pull-ups are connected to the 1.8V voltage rail.

7.3 GPIO

The Low Speed Expansion connector (J24) on ERAGON 410 Board contains the 7 GPIO lines which are LS_EXP_GPIO_1 to LS_EXP_GPIO_7. These GPIO's are routed from IO Expander U46 to Low Speed Expansion Connector.

7.4 SPI

The ERAGON 410 Board has two SPI bus master to be provided on the Low Speed Expansion Connector (J24).The ERAGON 410 board implements a full SPI master with 4 wires, CLK, CS, MOSI and MISO all connect directly to the APQ8016 SoC. For this purpose BLSP3 & BLSP5 port are used. These signals are driven at 1.8V.

7.5 I2S

The ERAGON 410 Board has one I2S bus provided on the Low Speed Expansion Connector (J24). The I2s signals are CLK, WS and D0 & D1.These signals are driven at 1.8V.

7.6 Power Supplies

The two power rails and Ground Pins are provide on the Low Speed Expansion Connector(J24) in the ERAGON 410 Board.

- +1.8V
- +3.3V
- Ground

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8 MIPI CSI

The ERAGON 410 Board support CSI 2 Lane and CSI 4 Lane Interface. The CSI signals are directly routed from the APQ8016 SoC to the Camera Connectors. The board supports up to 13MP Camera. J46 Connector which is primary 4 Lane CSI Interface Camera connector & J47 Connector is a secondary 2 Lane CSI Interface Camera Connector present on the ERAGON 410 board. The Pinout and Signal Description of the Connectors is mentioned below Section.

8.1 Primary Camera

The Primary Camera Connector (J46) on the ERAGON 410 Board supports CSI 4 Lane Interface up to 13MP sensors.

Figure 17 – Primary Camera Connector

The Signal Description of the Camera connector is mentioned in the following table:

Pin No.	Signal Name	Specification
1	GND	Ground.
2	GND	Ground.
3	CAM_GPIO_2	Camera GPIO 2.
4	MCAM_PWDN	Primary Camera Power Down.
5	CAM_GPIO_1	Camera GPIO 1.
6	GND	Ground.
7	CAM_I2C_SDA	Camera I2C Data.
8	CAM_I2C_SCL	Camera I2C Clock.
9	CSI_MCLK	24MHz CSI Clock.
10	GND	Ground.
11	MCAM_RST_N	Primary Camera Reset (Active Low).
12	DP1P_CLK	CSI Differential Clock Positive.
13	DP1M_CLK	CSI Differential Clock Negative.
14	GND	Ground
15	DP1P_1	CSI Differential Data 1 Positive.
16	DP1M_1	CSI Differential Data 1 Negative.
17	GND	Ground.
18	DP1M_0	CSI Differential Data 0 Negative.
19	DP1P_0	CSI Differential Data 0 Positive.
20	GND	Ground.
21	DP1M_2	CSI Differential Data 2 Negative.

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22	DP1P_2	CSI Differential Data 2 Positive.
23	GND	Ground.
24	DP1P_3	CSI Differential Data 3 Positive.
25	DP1M_3	CSI Differential Data 3 Negative.
26	GND	Ground.
27	GND	Ground.
28	VPH_PWR	3.7V (VPH_PWR) Power Supply.
29		
30		
31		
32		
33		

Table 10 : Primary Camera Connector Pinouts

8.2 Secondary Camera

The Secondary Camera Connector (J47) on the ERAGON 410 Board supports CSI 2 Lane Interface up to 8MP sensors.

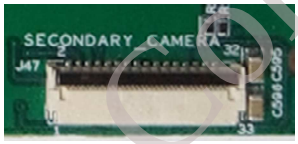

Figure 18 – Secondary Camera Connector

The Signal Description of the Camera connector is mentioned in the following table:

Pin No.	Signal Name	Specification
1	GND	Ground.
2	GND	Ground.
3	CAM_GPIO_2	Camera GPIO 2.
4	SCAM_PWDN	Secondary Camera Power Down.
5	CAM_GPIO_1	Camera GPIO 1.
6	GND	Ground.
7	BLSP6_I2C_SDA	BLSP6 I2C Data.
8	BLSP6_I2C_SCL	BLSP6 I2C Clock.
9	CSI1_MCLK	24MHz CSI1 Clock.

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10	GND	Ground.
11	SCAM_RST_N	Secondary Camera Reset (Active Low).
12	CSI_CLK_P	CSI Differential Clock Positive.
13	CSI_CLK_M	CSI Differential Clock Negative.
14	GND	Ground
15	CSI_D1_P	CSI Differential Data 1 Positive.
16	CSI_D1_M	CSI Differential Data 1 Negative.
17	GND	Ground.
18	CSI_D0_M	CSI Differential Data 0 Negative.
19	CSI_D0_P	CSI Differential Data 0 Positive.
20	GND	Ground.
21		
22		
23		
24		
25		
26		
27		
28	VPH_PWR	3.7V (VPH_PWR) Power Supply.
29		
30		
31		
32		
33		

Table 11 : Secondary Camera Connector Pinouts

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9 Power Management

ERAGON 410 Board has dedicated DC Jack for input supply and it has on board Buck Converters to generate required Power Supply.
The ERAGON 410 board uses three buck convertors, U37, U38 & U47 and two LDOs U42 & U43. U37 takes the power in to the board and generates 5V at 4A. This voltage feeds the USB HOST power limit switches and other peripherals and also used by buck convertor to generate the 3.3V at 2A using Buck Convertor (U47) . U38 takes the power in to the board and generates 3.7V at 4A. This voltage serves as the input Supply to the PMIC PM8916 (U2 placed on the ERAGON SoM). The PMIC PM8916 generates different voltages that required for the Processor, Memory on SoM & for the other peripherals on Carrier board.

9.1 DC Power Input

The ERAGON 410 board requires Input Supply (Range: 9V-18V) from a dedicated DC jack J15. Typical Power Adapter used is of 12V & 3A.

Figure 19 – DC Power Jack

9.2 Power Sequencing

Upon applying power to the ERAGON 410 board through a DC jack Connector (J15) both buck regulators will be enabled and will start regulating their target voltages. When the output of U38 on the carrier board is on, it will power on the on-board PMIC PM8916. This PMIC has four-buck regulators, one boost regulator and 20 LDOs. The sequencing of all power rails is set within the PM8916 configuration scheme during the production of this part. The user has no access to alter, modify or change the PMIC power up sequencing.

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10 DC Electrical Specifications

All AC & DC specifications mentioned in this datasheet are valid for the following voltage ranges.

Power Supply	MIN	TYP	MAX	Unit
Main Power Supply, DC VIN	9	12	18	V
Supply for SOM Component (Generated internally on the SOM)	3	3.6	4.5	V

Table 12 : Typical Voltage Ranges

Parameter	MIN	MAX	Unit	Group
VIH	1.17	-	V	EMMC JTAG, digital I/Os
VIL	-	0.63	V	
VOH	1.35	-	V	
VOL	-	0.45	V	

Table 13 : Digital I/O characteristics for VDD_P3 = VDD_P7 = 1.8V nominal

Parameter	MIN	MAX	Unit	Group
VIH	1.84	3.25	V	SD card Interface
VIL	-0.3	0.73	V	
VOH	2.22	2.95	V	
VOL	0	0.36	V	

Table 14 : Digital I/O characteristics for VDD_P2 = 2.95V nominal

Parameter	MIN	MAX	Unit	Group
VIH	1.27	-	V	USB Interface
VIL	-	0.85	V	

Table 15 : APQ8016 USB PHY specifications

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11 Switches

11.1 Power Button Switch

The push-button SW3 serves as the power-on/sleep button. Upon applying power to the board, the boot process will start. Once the board is running User can turn power-off by pressing the power button for a while moment. If the board is in a sleep mode, pressing the power button for more than 3 seconds will wake up the board.

Figure 20 – Power Button Switch

11.2 Reset Button Switch

The On-board SW4 Push-button has two different functions based on OS used.

- In Android, If Switch is pressed and Board is powered ON then Board will boot in fast boot mode.
- In Linux, if the switch is pressed and board is powered ON then Board will boot in fast boot mode and after power ON the board if the switch is pressed more than 10 second will cause a system reset.

Figure 21 – Reset Button Switch

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12 Boot Configuration Switch

The ERAGON 410 board contains Three Position Dip Switch marked SW5 located at the top side. For normal operation all three switched need to be set to the 'off' position.

Switch 1, 'FORCED USB BOOT', when set to 'on' position, will force boot over USB connection with a PC. This is only required for eMMC boot image upgrade.

Switch 2, 'SD BOOT', when set to 'on' position, will force the board to boot from SD card, to serve as the boot source for the ERAGON 410 board when set. User can use Micro SD as the main boot source or it can serve as a method for eMMC boot image upgrade.

Switch 3, 'USB HOST', is used to switch the USB Host mode. This switch is not a part of the boot configuration.

Figure 22 – Boot Configuration Switch

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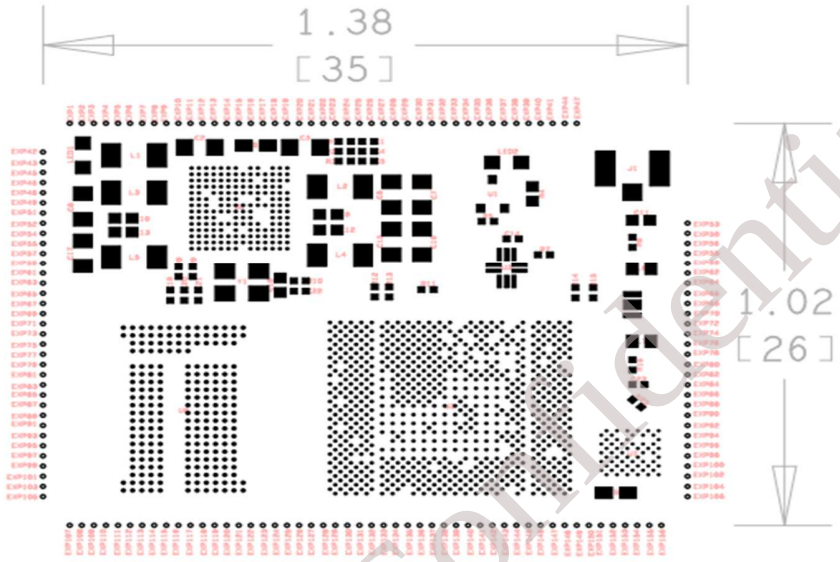
13 Mechanical Specification

13.1 SOM Board Dimensions



TOP View

Dimensions: Inches [Millimeters]

Note: For more details, refer dxf file.

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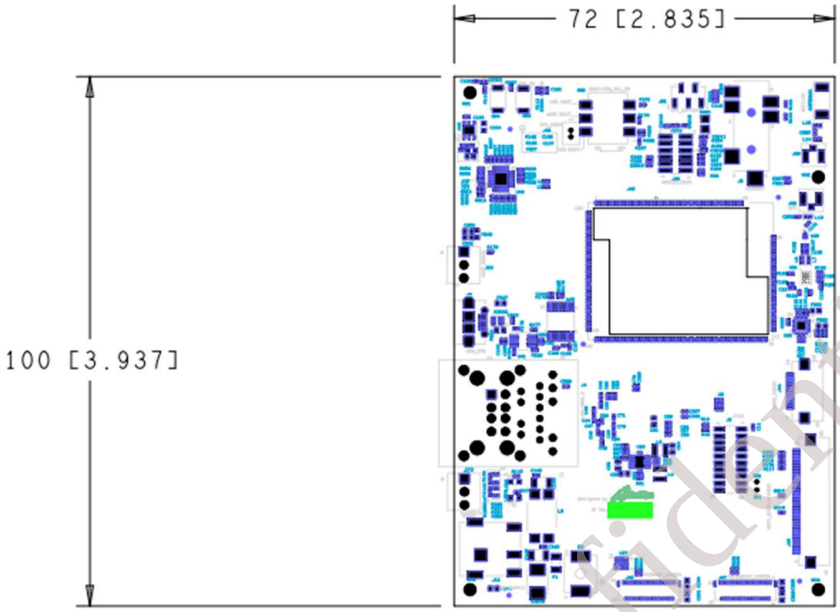
13.2 Carrier Board Dimension



TOP View

Dimensions: Millimeters [Inches]

Note: For more details, refer dxf file.

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14 Special Care when using ERAGON 410 Board

14.1 When using USB

Since the APQ8016 has a single USBOTG channel, care needs to be taken when the USB HOST function is to be used. Please verify that no cable is connected to the Micro USB type B connector (and to a host on the other side of the cable) as the hardware of the ERAGON 410 board will inform software about the presence of a request to configure the USBOTG to device mode.

Note: In APQ8016 Processor default, stage is USB Device that means by default USB used in Device Mode.

14.2 Development Device Notice

This device contains RF/digital hardware and software intended for engineering development, engineering evaluation, or demonstration purposes only and is intended for use in a controlled environment. This device is not being placed on the market, leased or sold for use in a residential environment or for use by the public as an end user device.

14.3 Anti-Static Handling Procedure

This device has exposed PCB and chips. Accordingly, proper anti-static precautions should be employed when handling the kit, including:

- Use a grounded anti-static mat
- Use a grounded wrist or foot strap

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15 Eragon410 – Daughter Boards

15.1 Q410 SOM Camera Interface Board-13MP

This board is add-on accessory to Eragon410. This is designed to interface various types of camera sensors to Eragon410 boards. This board supports camera sensors up to 13MP and connected to CSI interface of Eragon 410 at Primary Camera Connector (J46) on the Board. It uses SONY-IMX135 (13MP) Sensors. This board has three LDOs (U2, U3 & U4) to generate supplies VCC_2V8, VCC1V8 &VCC1V1. The camera control and configuration mechanism uses I2C interface. It has mating connector (J1) for Primary Camera Connector (J46) of the ERAGON 410 Board and camera connector (J2).

Figure 23 – Camera Interface Board – 13MP

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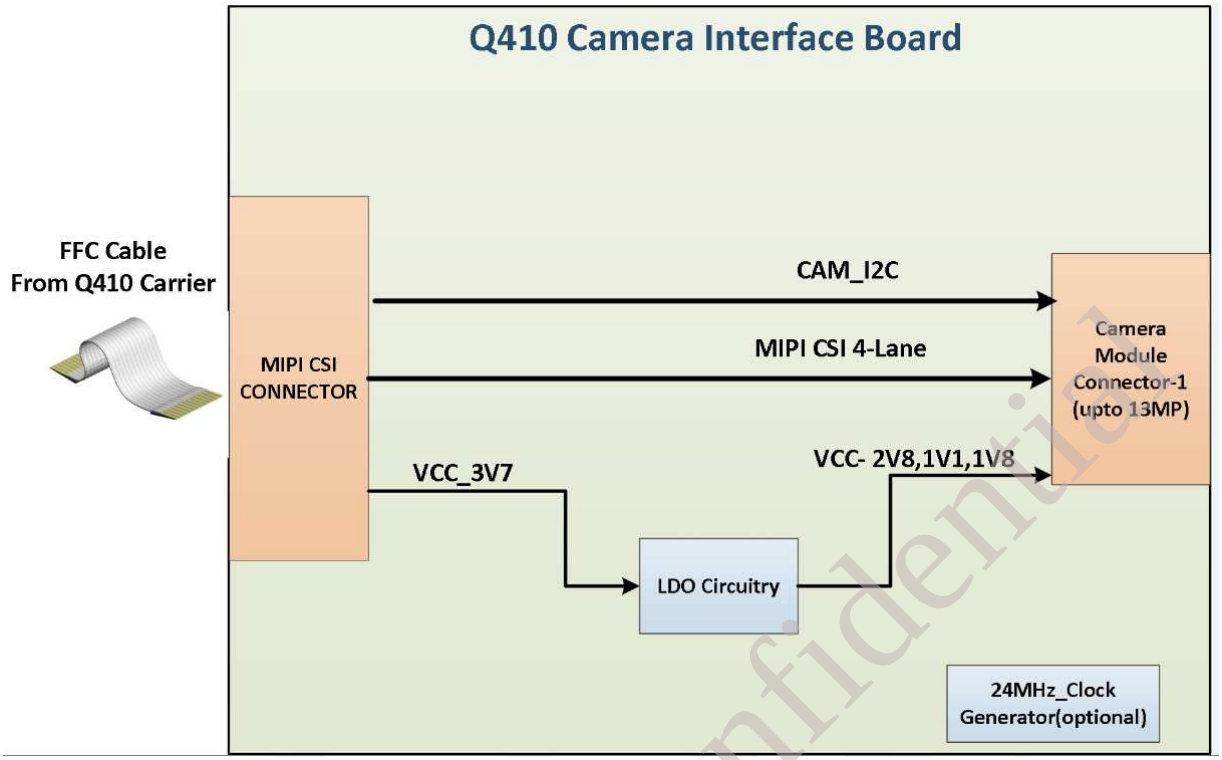

Figure 24 – Functional Block Diagram

The pin specification of the Primary Camera Connector (J2) is mentioned below:

Pin No.	Signal Name	Specification
1	GND	Ground.
2	VCC	VCC_2V8
3	VCC	VCC_1V1
4	VCC	VCC_1V8
5	NC	
6	GND	Ground.
7	VCC	VCC_2V8
8	GND	Ground.
9	CAM_I2C_SDA	Camera I2C Data.
10	CAM_I2C_SCL	Camera I2C Clock.
11	MCAM_RST_N	Primary Camera Reset (Active Low).
12	MCAM_PWDN	Primary Camera Power Down.
13	GND	Ground.

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14	CSI0_MCLK	24MHz CSI Clock.
15	GND	Ground.
16	MIPI_DATA3_P	CSI Differential Data 3 Positive.
17	MIPI_DATA3_M	CSI Differential Data 3 Negative.
18	GND	Ground.
19	MIPI_DATA2_P	CSI Differential Data 2 Positive.
20	MIPI_DATA2_M	CSI Differential Data 2 Negative.
21	GND	Ground.
22	MIPI_DATA1_P	CSI Differential Data 1 Positive.
23	MIPI_DATA1_M	CSI Differential Data 1 Negative.
24	GND	Ground.
25	MIPI_CLK_P	CSI Differential CLK Positive.
26	MIPI_CLK_M	CSI Differential CLK Negative.
27	GND	Ground.
28	MIPI_DATA0_P	CSI Differential Data 0 Positive.
29	MIPI_DATA0_M	CSI Differential Data 0 Negative.
30	GND	Ground.

Table 16 : Camera Connector Pinouts

15.2 Q410 SOM Camera Interface Board-5MP

This board is add-on accessory to Eragon410. This is designed to interface various types of camera sensors to Eragon410 boards. This board supports camera sensors up to 5MP and connected to CSI interface of Eragon410 at Primary Camera Connector (J47) on the Board. It uses Omni Vision camera sensors OV5640 (5MP). This board has three LDOs (U1,U2 & U3) to generate supplies VCC_2V8, VCC_1V8 &VCC_1V5.The camera control and configuration mechanism uses I2C interface. It has mating connector (J1) for Secondary Camera Connector (J47) of the ERAGON 410 Board and camera connector (J2).

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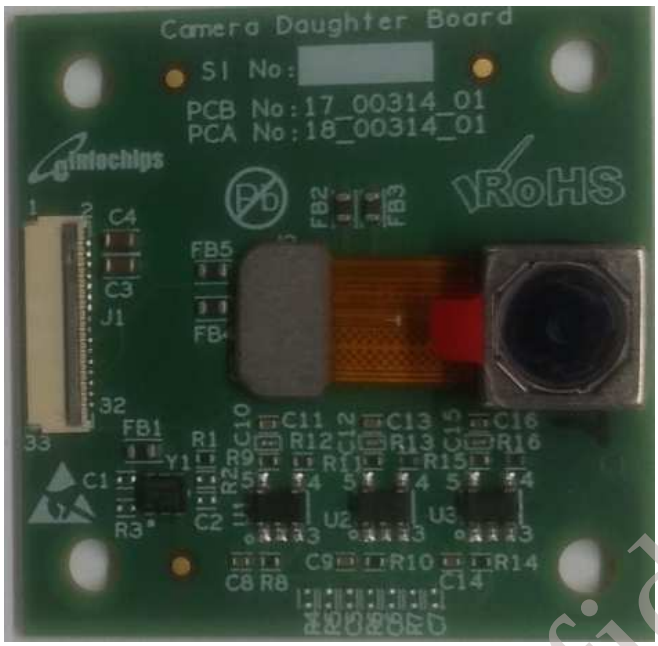

Figure 25 – Camera Interface Board – 5MP

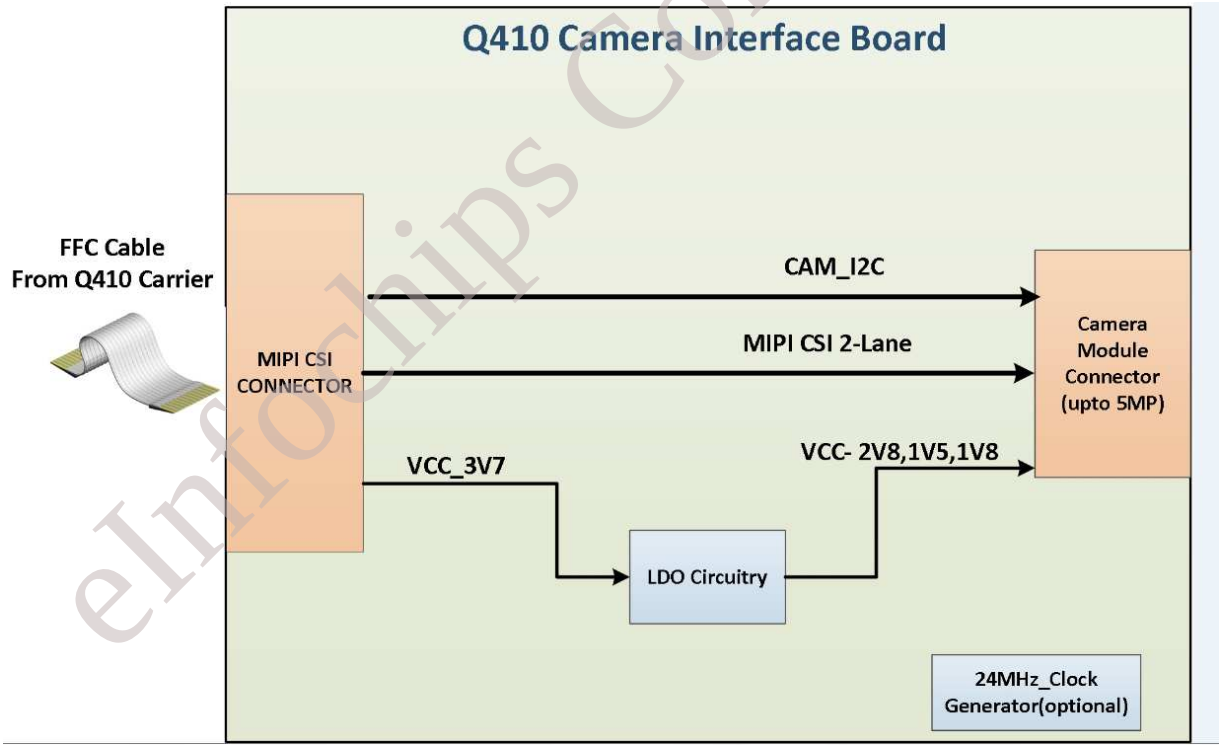

Figure 26 – Functional Block Diagram

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The pin specification of the camera connector (J2)is mentioned below:

Pin No.	Signal Name	Specification
1	VCC	VCC_2V8
2	VCC	VCC_2V8
3	CAM_I2C_SCL	Camera I2C Clock.
4	CAM_I2C_SDA	Camera I2C Data.
5	MCAM_RST_N	Primary Camera Reset (Active Low).
6	MCAM_PWDN	Primary Camera Power Down.
7	VCC	VCC_1V8
8	VCC	VCC_1V5
9	GND	Ground.
10	CSI1_MCLK	24MHz CSI Clock.
11	GND	Ground.
12	GND	Ground.
13	MIPI_DATA0_M	CSI Differential Data 0 Negative.
14	MIPI_CLK_P	CSI Differential CLK Positive.
15	MIPI_DATA0_P	CSI Differential Data 0 Positive.
16	MIPI_CLK_M	CSI Differential CLK Negative.
17	GND	Ground.
18	GND	Ground.
19	GND	Ground.
20	MIPI_DATA1_P	CSI Differential Data 1 Positive.
21	GND	Ground.
22	MIPI_DATA1_M	CSI Differential Data 1 Negative.
23	GND	Ground.
24	GND	Ground.

Table 17 : Camera Connector Pinouts

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15.3 Q410 SOM HDMI Bridge Board

This board is add-on accessory to Eragon410. This is designed to interface HDMI to Eragon410 boards. This board has mating Audio connector(J2) for HDMI audio connector (J44) of ERAGON410 board, MIPI DSI Connector(J1) for MIPI DSI Display connector(J10) of ERAGON410 and HDMI Type A connector(J3).It uses DSI to HDMI bridge IC to support HDMI output. The control and configuration mechanism uses I2C interface.

Figure 27 – HDMI Bridge Board

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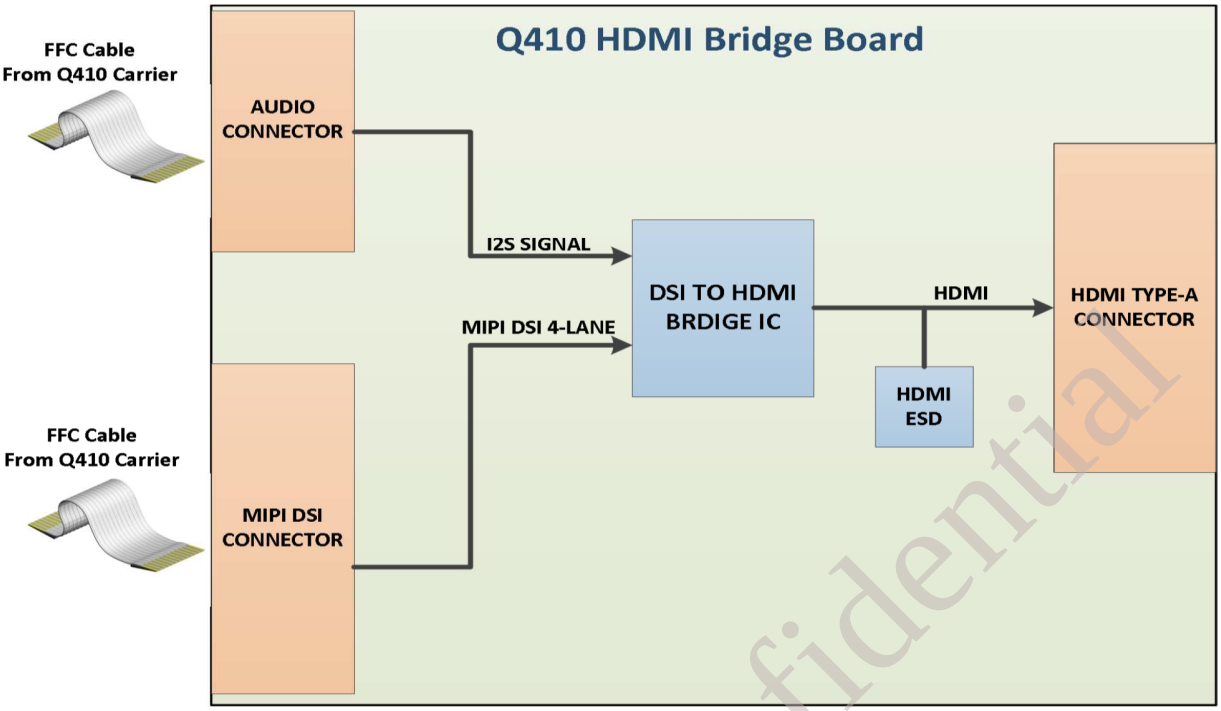

Figure 28 – Functional Block Diagram

The pin specification of the HDMI TYPE A connector(J3) is mentioned below:

Pin No.	Signal Name	Specification
1	HDMI_TMDS_TX2_P	Differential Data 2 Positive.
2	D2_SHIELD	HDMI Ground
3	HDMI_TMDS_TX2_M	Differential Data 2 Negative.
4	HDMI_TMDS_TX1_P	Differential Data 1 Positive.
5	D1_SHIELD	HDMI Ground
6	HDMI_TMDS_TX1_M	Differential Data 1 Negative.
7	HDMI_TMDS_TX0_P	Differential Data 0 Positive.
8	D0_SHIELD	HDMI Ground
9	HDMI_TMDS_TX0_M	Differential Data 0 Negative.
10	HDMI_TMDS_TXC_P	Differential Clock Positive.
11	CK_SHIELD	HDMI Ground
12	HDMI_TMDS_TXC_M	Differential Clock Negative.
13	HDMI_CEC	CEC I/O
14	NC	Not Connected.
15	HDMI_DDC_SCL	Serial Port Data Clock to RX

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16	HDMI_DDC_SDA	Serial Port Data I/O to RX
17	GND	Ground
18	VCC	SYS_5P0
19	HDMI_HPD	HDMI Hot Plug detect Pin.

Table 18 : Camera Connector Pinouts

15.4 Q410 SOM LCD Interface Board

This board is designed to integrate high resolution LCD and touch screen interface. The board supports 5.5" LCD from OSD displays. It is connected to MIPI interface of Eragon410. LCD control and configuration mechanism uses I2C interface. Touch screen is connected with Eragon410 using I2C interface. It has mating connector (J1) for MIPI Display connector (J10)of ERAGON 410 Board.

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Figure 29 – LCD Interface Board

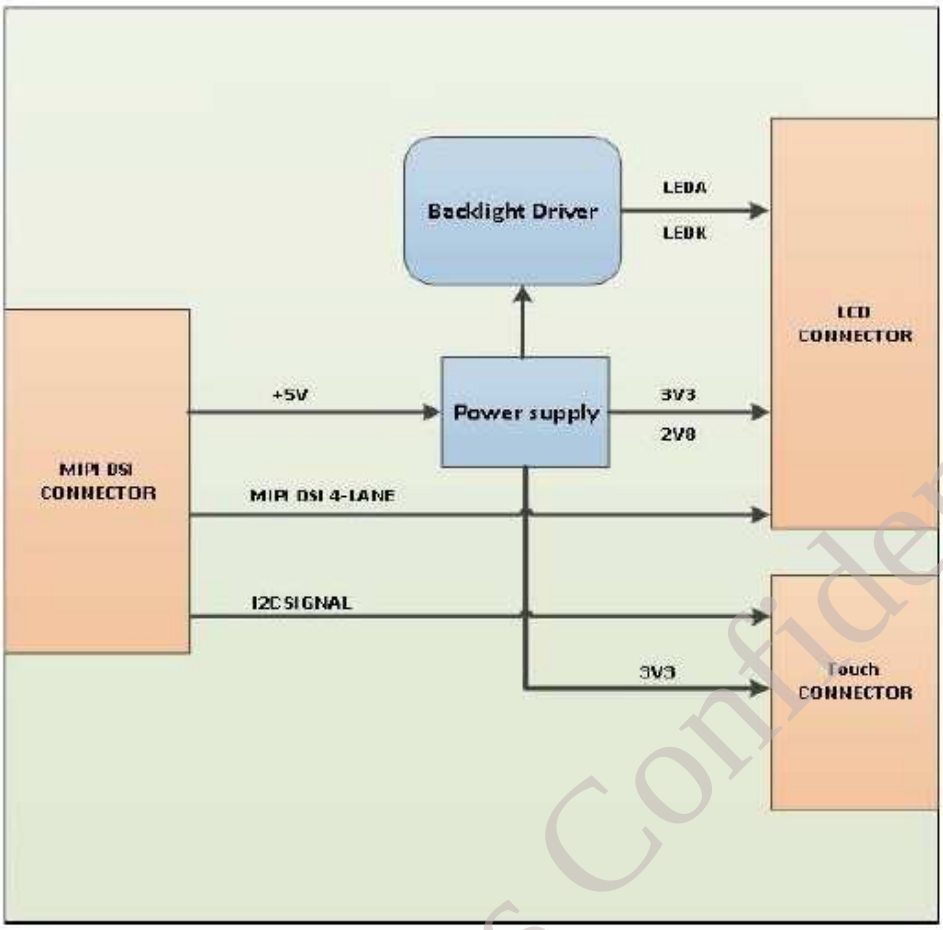

Figure 30 – Functional Block Diagram

The pin specification of the Display connector (J4)is mentioned below:

Pin No.	Signal Name	Specification
1	NC	
2	GND	Ground.
3	VCC	5V_POS
4	VCC	5V_NEG
5	GND	Ground.
6	GND	Ground.
7	MIPI_DSI0_DATA2_P_EXP_CONN	DSI Data2 Differential Positive.
8	MIPI_DSI0_DATA2_M_EXP_CONN	DSI Data2 Differential Negative.
9	GND	Ground.
10	MIPI_DSI0_DATA1_P_EXP_CONN	DSI Data1 Differential Positive.

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11	MIPI_DSI0_DATA1_M_EXP_CONN	DSI Data1 Differential Negative.
12	GND	Ground.
13	MIPI_DSI0_DATA0_P_EXP_CONN	DSI Data0 Differential Positive.
14	MIPI_DSI0_DATA0_M_EXP_CONN	DSI Data0 Differential Negative.
15	GND	Ground.
16	MIPI_DSI0_DATA3_P_EXP_CONN	DSI Data3 Differential Positive.
17	MIPI_DSI0_DATA3_M_EXP_CONN	DSI Data3 Differential Negative.
18	GND	Ground.
19	MIPI_DSI0_CLK_P_EXP_CONN	DSI CLK Differential Positive.
20	MIPI_DSI0_CLK_M_EXP_CONN	DSI CLK Differential Negative.
21	GND	Ground.
22	NC	
23	IOVCC	1V8
24	IOVCC	1V8
25	GND	Ground.
26	PWM_OUT	On Test point
27	NC	
28	LCD_RESET_N	LCD Reset(active low_3V3)
29	GND	Ground.
30	LEDA	BACKLIGHT LED Anode
31	LEDA	BACKLIGHT LED Anode
32	LEDK	BACKLIGHT LED Cathode
33	LEDK	BACKLIGHT LED Cathode

Table 19 : LCD Connector Pinouts

The pin specification of the Touch connector (J5)is mentioned below:

Pin No.	Signal Name	Specification
1	GND	Ground.
2	VCC	3V3
3	GND	Ground.
4	INT	LCD-Touch Interrupt
5	SDA	LCD I2C DATA
6	SCL	LCD I2C Clock
7	Reset	Reset(Active low)

Table 20 : Touch Connector Pinouts

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16 Appendix A (High Level BOM)

#	Description	Manufacturer	Manufacturer Part #
1	1.4 GHz quad-core Cortex-A53 Micro-Processor	Qualcomm	APQ8016
2	PMIC IC	Qualcomm	PM8916
3	eMCP - 8GB eMMC + 8Gb LPDDR3	Samsung/Hynix	KMQ72000SM-B316000(Samsung)/ H9TQ64A8GTMCUR(Hynix)
4	WiFi + BT Chip	Qualcomm	WCN3620
5	IC USB SWITCH SPDT DUAL 10UQFN	Toshiba Semiconductor and Storage	TC7USB40MU,LF
6	TRANS PREBIAS NPN 200MW SOT323	Diodes Incorporated	DDTC143ZUA-7-F
7	CRYSTAL 19.2000MHZ 7PF SMD	NDK	NX2520SG-19.2M-STD-CTX-1
8	Chip antenna for Wifi and BT	Fractus	FR05-S1-N-O-1004
9	CONN UMC JACK STR 50 OHM SMD	Hirose Electric Co Ltd	U.FL-R-SMT-1(01)
10	MOSFET N-CH 50V 0.2A 3VMT	ROHM	RUM002N05T2L
11	MOSFET P-CH 20V 1A SSOT3	Fairchild Semi.	NDS332P
12	TVS DIODE 10UQFN	Texas Instruments	TPD6E001RSER
13	TVS DIODE 5VWM 15VC SLP2510P8	Semtech	RCLAMP0524PATCT
14	3-PORT USB 2.0 HUB CTRLR 36VQFN	Microchip Technology	USB2513B-AEZC-TR
15	IC POWER DIST LOAD SW 4-WLCSP	Fairchild Semiconductor	FPF1203LUCX
16	IC USB-10/100/1K ETH CTRL 56QFN	Microchip Technology	LAN7500I-ABZJ
17	IC REG BUCK SYNC ADJ 0.8A 10SON	Texas Instruments	TPS62410DRCT
18	IC FILTER COMMON MODE ESD 10WDFN	ON Semiconductor	EMI4182MTTAG
19	GPS and Glonass RF Receiver	Qualcomm	WGR-7640-0-17WLNSP-TR-02-A
20	SAW FILTERS	AVX	SF14-1575M5UBA2

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21	GYRO/ACCEL/COMPASS/9-AXIS	InvenSense	MPU9250
22	IC REG BUCK SYNC ADJ 4A 16QFN	Texas Instruments	TPS54426RSAR
23	IC DRVR/RCVR RS232 1CH 16-TSSOP	Texas Instruments	MAX3221EIPWR
24	TXS0102 2-Bit Bidirectional Voltage-Level Translator	Texas Instruments	TXS0102DCTR
25	IC REG LDO ADJ 1A 6WSON	Texas Instruments	LP38692SD-ADJ
26	IC POWER DIST SWITCH ADJ 10SON	Texas Instruments	TPS2561DRCT
27	IC I/O EXPANDER I2C 16B 24WQFN	NXP Semiconductors	PCA6416AHF,128
28	IC REG BUCK ADJ 3A SYNC 16QFN	Texas Instruments	TPS62090RGTR
29	IC V-LEVEL TRANSL BI-DIR SC70-6	Texas Instruments	TXS0101DRLR
30	OSC XO 25.000MHZ CMOS SMD	ECS Inc	SG-310SCN 25.0000MJ3
31	Crystal 24.0000MHz 20ppm 18pF 50 Ohm -20°C - 70°C, 4-SMD	Abracon	ABM8-24.000MHZ-B2-T

Table 21 : High Level BOM

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17 Appendix B (Edge Castellation Connector (J42)Pins Description)

SOM Pin No.	Carrier Board Connector (J22) Pin Number	Signal Name	Default Pin Function	Voltage Level
EXP1	1	GND	Ground	-
EXP2	2	SPKR_OUT_M	Class-D speaker amp output	-
EXP3	3	SPKR_OUT_P	Class-D speaker amp + output	-
EXP4	4	CDC_MIC3_P	Secondary MIC	-
EXP5	5	CDC_MIC2_P	Headset MIC	-
EXP6	6	VCOIN_CELL	Supply for RTC (3V)	-
EXP7	7	CDC_EAR_P	Earpiece PA + output	-
EXP8	8	CDC_EAR_M	Earpiece PA output	-
EXP9	9	GND_CFILT	Ground reference for PMIC bias	-
EXP10	10	CDC_MIC1_P	Main MIC	-
EXP11	11	CDC_MIC_BIAS1	Microphone bias #1	-
EXP12	12	CDC_HS_DET	Headset detection	-
EXP13	13	PRE_BUCK_OUT	Battery voltage sense point	-
EXP14	14	PHONE_ON_N	Power on detect input	-
EXP15	15	USB_HUB_RESET_N_PM	PMIC GPIO (used to reset Hub in Q410 Carrier Board)	-
EXP16	16	VBATT_CONN	Battery Voltage Sense Pin	-
EXP17	17	USB_VBUS_IN	Input power from USB source	-
EXP18	18	VREG_L1_1P225	PMIC Linear regulator L1 output (By default 1.225Vset,can be used for GPS Chip WGR7640)	-
EXP19	19	CDC_HPH_L	Headphone PA left channel output	-
EXP20	20	CDC_HPH_REF	Headphone PA ground sensing	-
EXP21	21	CDC_HPH_R	Headphone PA right channel output	-
EXP22	22	BATT_THERM	Battery Thermistor Input	-
EXP23	23	GND	Ground	-
EXP24	24	BATT_ID	Battery ID	-

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SOM Pin No.	Carrier Board Connector (J22) Pin Number	Signal Name	Default Pin Function	Voltage Level
EXP25	25	USB_SW_SEL	USB Switch Control (High Signal on this pin will force USB data lines to switch on Host Line)	3.7V
EXP26	26	MI2S_1_WS	MI2S Word Select signal	1.8V
EXP27	27	MI2S_1_SCLK	MI2S SCLK signal	1.8V
EXP28	28	MI2S_1_DATA0	MI2S Data0 signal	1.8V
EXP29	29	MI2S_1_DATA1	MI2S Data1 signal	1.8V
EXP30	30	GND	Ground	-
EXP31	31	USB_HS_D_M_HUB	USB Data - Negative (For 410 Host Configuration)	-
EXP32	32	USB_HS_D_P_HUB	USB Data - positive (For 410 Host Configuration)	-
EXP33	33	GND	Ground	-
EXP34	34	USB_HS_D_P_DEVICE	USB Data - Positive (For 410 Device Configuration)	-
EXP35	35	USB_HS_D_M_DEVICE	USB Data - Negative (For 410 Device Configuration)	-
EXP36	36	GND	Ground	-
EXP37	37	DSI2HDMI_MI2S_SCK	MI2S SCLK signal	1.8V
EXP38	38	DSI2HDMI_MI2S_WS	MI2S Word Select signal	1.8V
EXP39	39	SSBI_GPS	SSBI 2 for RFIC 0	1.8V
EXP40	40	DSI2HDMI_MI2S_DATA0	MI2S Data0 signal	1.8V
EXP41	41	GND	Ground	-
EXP42	156	GND	Ground	-
EXP43	155	VPH_PWR	3.7V Supply for SOM (Battery/Input Power Supply)	-
EXP44	42	GND	Ground	-
EXP45	154	VPH_PWR	3.7V Supply for SOM (Battery/Input Power Supply)	-
EXP46	153	VPH_PWR	3.7V Supply for SOM (Battery/Input Power Supply)	-

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SOM Pin No.	Carrier Board Connector (J22) Pin Number	Signal Name	Default Pin Function	Voltage Level
EXP47	43	GND	Ground	-
EXP48	152	VPH_PWR	3.7V Supply for SOM (Battery/Input Power Supply)	-
EXP49	151	VPH_PWR	3.7V Supply for SOM (Battery/Input Power Supply)	-
EXP50	45	GND	Ground	-
EXP51	150	PMIC_MPP4_PWM	PWM control for external WLED driver	1.8V
EXP52	149	PM_RESIN_N	PMIC reset input	-
EXP53	44	GND	Ground	-
EXP54	148	PMIC_MPP3	Digital I/O (optional) (Digital input/output usage)	-
EXP55	147	PMIC_MPP2	Digital I/O (optional) (Digital input/output usage)	-
EXP56	46	GND	Ground	-
EXP57	146	VREG_L17_2P85	PMIC Linear regulator L17 output (By default 2.85V, can provide 450mA current max)	-
EXP58	47	BLSP4_I2C_SCL	BLSP 4 - I2C CLOCK	1.8V
EXP59	145	VREG_L17_2P85	PMIC Linear regulator L17 output (By default 2.85V , can provide 450mA current max)	-
EXP60	48	BLSP4_I2C_SDA	BLSP 4 - I2C DATA	1.8V
EXP61	144	JTAG_PS_HOLD	Power-supply hold control input	1.8V
EXP62	49	BLSP1_UART_RX	BLSP 1 - UART Receive Pin	1.8V
EXP63	143	GND	Ground	-
EXP64	50	BLSP1_UART_TX	UART Transmit for BLSP1	1.8V
EXP65	142	APQ_19.2MHZ_SYSCLK2	Baseband (low power) XO output 2 - 19.2 MHz Clock (From PMIC)	1.8V
EXP66	51	BLSP1_UART_RTS_N	BLSP1_UART_RTS_N (UART RTS (Request to Send) Signal)	1.8V

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SOM Pin No.	Carrier Board Connector (J22) Pin Number	Signal Name	Default Pin Function	Voltage Level
EXP67	141	GND	Ground	-
EXP68	52	BLSP1_UART_CTS_N	BLSP1_UART_CTS_N (UART CTS (Clear to Send) Signal)	1.8V
EXP69	140	GPS_19.2MHZ_RFCLK	19.2 MHz Clock	1.8V
EXP70	53	GND	Ground	-
EXP71	139	GND	Ground	-
EXP72	54	GNSS_BB_IP	GNSS receiver baseband input, in-phase plus	-
EXP73	138	USB_HS_ID	GPIO_121 (GPIO is used to detect USB Device connection)	1.8V
EXP74	55	GNSS_BB_IM	GNSS receiver baseband input, in-phase minus	-
EXP75	137	SD_CARD_DET_N	Secure digital card detection	1.8V
EXP76	56	GNSS_BB_QP	GNSS receiver baseband input, quadrature plus	-
EXP77	136	GYRO_ACCEL_INT_N	Interrupt Signal (Used for Gyro meter Interrupt)	1.8V
EXP78	57	GNSS_BB_QM	GNSS receiver baseband input, quadrature minus	-
EXP79	135	ALPS_INT_N	GPIO_107 (Configurable I/O)	1.8V
EXP80	58	GND	Ground	-
EXP81	134	TOUCH_INT	Interrupt Signal (Used for Touch Interrupt)	1.8V
EXP82	59	BLSP2_UART_TX	UART Transmit for BLSP2	1.8V
EXP83	133	GND	Ground	-
EXP84	60	BLSP6_I2C_SDA	I2C Data for BLSP6	1.8V
EXP85	132	BLSP5_SPI_CS_N	BLSP5_SPI_CS_N (Chip Select for BLSP5)	1.8V
EXP86	61	HDMI_HPD_N	GPIO_20 (Configurable I/O)	1.8V

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SOM Pin No.	Carrier Board Connector (J22) Pin Number	Signal Name	Default Pin Function	Voltage Level
EXP87	131	BLSP5_SPI_MOSI	SPI MOSI Pin for BLSP5	1.8V
EXP88	62	BOOT_CONFIG_1	Boot configuration control bit 1	1.8V
EXP89	130	BLSP3_SPI_MOSI	SPI MOSI Pin for BLSP3	1.8V
EXP90	63	FM_RX_ANT	Antenna Signal for FM	-
EXP91	129	BLSP5_SPI_MISO	SPI MISO Pin for BLSP5	1.8V
EXP92	64	BLSP2_I2C_SCL	I2C Clock for BLSP2	1.8V
EXP93	128	FORCED_USB_BOOT	Force USB boot control	1.8V
EXP94	65	BLSP2_I2C_SDA	I2C Data for BLSP2	1.8V
EXP95	127	BLSP5_SPI_CLK	SPI Clock for BLSP5	1.8V
EXP96	66	BLSP6_I2C_SCL	I2C Clock for BLSP6	1.8V
EXP97	126	CAM_I2C_SCL	Camera control interface I2C 0 serial Clock	1.8V
EXP98	67	BLSP2_UART_RX	UART Receive for BLSP2	1.8V
EXP99	125	CAM_I2C_SDA	Camera control interface I2C 0 serial data	1.8V
EXP100	68	VREG_L7_1P8	Linear regulator L7 output 1.8V	-
EXP101	124	BLSP3_SPI_MISO	SPI MISO Pin for BLSP3	1.8V
EXP102	69	VREG_L5_1P8	Linear regulator L5 output 1.8V	-
EXP103	123	SCAM_RST_N	Camera 1 (front camera) reset	1.8V
EXP104	70	VREG_L6_1P8	Linear regulator L6 output 1.8V	-
EXP105	122	GND	Ground	-
EXP106	71	GND	Ground	-
EXP107	121	GND	Ground	-
EXP108	120	BLSP3_SPI_CLK	SPI Clock for BLSP3	1.8V
EXP109	119	MCAM_RST_N	Camera 0 (rear camera) reset	1.8V
EXP110	118	BLSP3_SPI_CS_N	Chip Select for BLSP3	1.8V

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SOM Pin No.	Carrier Board Connector (J22) Pin Number	Signal Name	Default Pin Function	Voltage Level
EXP111	117	JTAG_TDO	JTAG data output	1.8V
EXP112	116	DSI2HDMI_INT_N	GPIO_31 (Configurable I/O)	1.8V
EXP113	115	JTAG_TRST_N	JTAG reset	1.8V
EXP114	114	JTAG_SRST_N	JTAG reset for debug	1.8V
EXP115	113	JTAG_TMS	JTAG mode-select input	1.8V
EXP116	112	JTAG_TCK	JTAG clock input	1.8V
EXP117	111	JTAG_TDI	JTAG data input	1.8V
EXP118	110	SDC2_DATA_1	Secure digital controller 2 data bit 1	2.95V
EXP119	109	SDC2_DATA_3	Secure digital controller 2 data bit 3	2.95V
EXP120	108	SDC2_DATA_0	Secure digital controller 2 data bit 0	2.95V
EXP121	107	SDC2_CMD	Secure digital controller 2 command	2.95V
EXP122	106	SDC2_DATA_2	Secure digital controller 2 data bit 2	2.95V
EXP123	105	SDC2_CLK	Secure digital controller 2 clock	2.95V
EXP124	104	GND	Ground	-
EXP125	103	CSI0_MCLK	Camera master clock 0	1.8V
EXP126	102	CSI1_MCLK	Camera master clock 1	1.8V
EXP127	101	GND	Ground	-
EXP128	100	MIPI_CSI0_DATA0_P	MIPI camera serial interface 0 lane 0 – positive	-
EXP129	99	MIPI_CSI0_DATA0_M	MIPI camera serial interface 0 lane 0 – negative	-
EXP130	98	MIPI_CSI0_DATA1_M	MIPI camera serial interface 0 lane 1 – negative	-
EXP131	97	MIPI_CSI0_DATA1_P	MIPI camera serial interface 0 lane 1 – positive	-
EXP132	96	MIPI_CSI0_CLK_P	MIPI camera serial interface 0 clock – positive	-

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SOM Pin No.	Carrier Board Connector (J22) Pin Number	Signal Name	Default Pin Function	Voltage Level
EXP133	95	MIPI_CSI0_CLK_M	MIPI camera serial interface 0 clock – negative	-
EXP134	94	MIPI_CSI0_DATA2_P	MIPI camera serial interface 0 lane 2 – positive	-
EXP135	93	MIPI_CSI0_DATA2_M	MIPI camera serial interface 0 lane 2 – negative	-
EXP136	92	MIPI_CSI0_DATA3_P	MIPI camera serial interface 0 lane 3 – positive	-
EXP137	91	MIPI_CSI0_DATA3_M	MIPI camera serial interface 0 lane 3 – negative	-
EXP138	90	GND	Ground	-
EXP139	89	MIPI_CSI1_DATA0_P	MIPI camera serial interface 1 lane 0 – positive	-
EXP140	88	MIPI_CSI1_DATA0_M	MIPI camera serial interface 1 lane 0 – negative	-
EXP141	87	MIPI_CSI1_CLK_P	MIPI camera serial interface 1 clock – positive	-
EXP142	86	MIPI_CSI1_CLK_M	MIPI camera serial interface 1 clock – negative	-
EXP143	85	MIPI_CSI1_DATA1_P	MIPI camera serial interface 1 lane 1 – positive	-
EXP144	84	MIPI_CSI1_DATA1_M	MIPI camera serial interface 1 lane 1 – negative	-
EXP145	83	GND	Ground	-
EXP146	82	MIPI_DSI0_DATA0_P	MIPI display serial interface 0 lane 0 – positive	-
EXP147	81	MIPI_DSI0_DATA0_M	MIPI display serial interface 0 lane 0 – positive	-
EXP148	80	MIPI_DSI0_DATA1_P	MIPI display serial interface 0 lane 1 – positive	-
EXP149	79	MIPI_DSI0_DATA1_M	MIPI display serial interface 0 lane 1 – negative	-
EXP150	78	MIPI_DSI0_CLK_P	MIPI display serial interface 0 clock – positive	-
EXP151	77	MIPI_DSI0_CLK_M	MIPI display serial interface 0 clock – negative	-
EXP152	76	MIPI_DSI0_DATA3_P	MIPI display serial interface 0 lane 3 – positive	-

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SOM Pin No.	Carrier Board Connector (J22) Pin Number	Signal Name	Default Pin Function	Voltage Level
EXP153	75	MIPI_DSI0_DATA3_M	MIPI display serial interface 0 lane 3 – negative	-
EXP154	74	MIPI_DSI0_DATA2_M	MIPI display serial interface 0 lane 2 – negative	-
EXP155	73	MIPI_DSI0_DATA2_P	MIPI display serial interface 0 lane 2 – positive	-
EXP156	72	GND	Ground	-

Note : "-" Indicates Not Recommended in PMIC 8916.

Table 22 : Edge castellation Connector Pinouts

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18 About eInfochips

eInfochips is a partner of choice for Fortune 500 companies for product innovation and hi-tech engineering consulting. Since 1994, eInfochips has provided solutions to key verticals like Aerospace & Defense, Consumer Electronics, Energy & Utilities, Healthcare, Home, Office, and Industrial Automation, Media & Broadcast, Medical Devices, Retail & e-Commerce, Security & Surveillance, Semiconductor, Software/ISV and Storage & Compute.

Covering every aspect of the product lifecycle, eInfochips draws from an experience of building 500+ products that have over 10 Million units deployed – to provide solutions on Product Design and Development, QA and Certifications, Reengineering, Sustenance and Volume Production. Being an innovation driven company, 5% of our revenues are earmarked for building reusable IPs that will accelerate product design cycles and reduce product risks.

About 80% of eInfochips business comes from companies with revenues over $1 Billion, and 60% of total business from building life and mission critical products. eInfochips has the experience, expertise and infrastructure to deliver complex, critical and connected products.

Today, more than 1400 chip mates operate from over 10 Design Centers and dozen Sales Offices spread across Asia, Europe and US.

Our clients have recognized our teams for commitment, teamwork and initiatives that we have brought forward, adding immense value to client processes and products. Chip mates have a strong growth path defined for them, with specific soft-skills training modules – Lagaan, Pegasus and Altius – to groom leaders for the future.

'At eInfochips we are determined that our growth should empower the ones in need. Every year we contribute 1% of our profits for development in education and healthcare'.

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