Evaluating the Impact of Increasing System Fault Currents on Protection

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Abstract — Every year the capacity of power systems is increasing, meaning that short circuit current levels are continuously going up. The ratings of instrument transformers at many existing substations that were designed many years ago are now becoming underrated with present fault current levels. Such a situation is obviously concerning to protection engineers who strive to ensure security and dependability of the protection is not jeopardized. Besides risks of trivial CT saturation, which affects the security of the protection system, the concern is if a particular relay is capable of processing such high current, while maintaining adequate accuracy to ensure protection security and dependability.

This paper first reviews the causes of increasing short circuit current level in power systems. Some historic and present fault current levels are described. Then, the impacts of increasing short current on protective relays are investigated in detail, in terms of signal processing algorithms, relay clamping level and CT saturation. A thought analysis is presented to examine the security and dependability of a specified transformer differential protection system. Some evaluation techniques and methods are introduced for the purpose of generalized analysis.

Index Terms — Increasing Short Circuit Current, Transformer Differential Relay, CT Saturation

I. INTRODUCTION

When a short circuit occurs on a power system, several things happen [1]:

- At the short circuit location, arcing and burning can occur.
- Short circuit current flows from the various sources to the short circuit location.
- All components carrying the short circuit currents are subject to thermal and mechanical stress.
- System voltage drops in proportion to the magnitude of the short circuit current.

The level of short circuit current is directly related to the size and capacity of the power sources and is independent of the load current of the circuit protected by the protective device. The larger the capacity of the power sources, the greater the short circuit current will be.

Basically, there are five power sources contributing to the short circuit current:

- Generators
- Synchronous Motors
- Induction Motors
- Electric Utility Systems
- Distribution Generations

Nowadays, the short circuit levels in power systems are continuously increasing compared to their historical levels.

A. Causes of increasing fault current in power systems

The major reasons that cause the incrementing of fault current are summarized as below:

- Installation of new transmission facilities, transformers and generation

  Due to the growth of power demand, more and more new transmission lines, transformers and generators are being installed in the power system. Equivalently in the circuit model, the Thevenin equivalent impedance seen at system buses is being reduced by these conditions. Consequently, the fault current level is increasing, simply according to the Ohm's law.

- Additions and changes to existing generators

  The upgrading of existing generators will increase the capacity of power sources, and therefore result in the larger fault currents.

- Reconfigurations of the bulk electric system (BES) network

  The short circuit, system stability, steady state power flow, and other types of analyses are required to be re-evaluated for reconfigurations or restructuring of the electrical generation resources, transmission lines, interconnections with neighboring systems, such as changes in interconnection location or increasing voltage level of a substation. These changes could result in larger fault currents.

- New distribution generation

  The renewable energy resources, such as solar, wind, biomass, geothermal etc. are growing fast and getting more stakes in the utility's energy portfolio. By the end of 2014, the total renewable power capacity exceeded 309 GW in North America, and 1,828 GW worldwide [2]. The connection of such distribution generations to the conventional power grids will increase the fault current levels since the total fault levels are now contributed by the combination of the upstream grid and the distribution generation.

The detailed short circuit current calculation methods can be found in the IEC standard 60909-0 [3], including the calculation of the contribution of wind power station units and power station units with full size converters to the short-circuit current. And some examples are also described in the IEC technical report 60865-2 [4]. More conveniently, the short circuit analysis programs, such as ETAP and ASPEN, can be used to model the specific power system and determine short circuit currents.

B. Historic and present fault levels

The Transmission System Code (TSC) published by the Ontario Energy Board (OEB) sets out the minimum standards that an electricity transmitter must meet in designing, constructing, managing and operating its transmission system [5]. The present and some historic values of the maximum allowable fault levels set out by the OEB are listed in Table 1. The values in the table do not mean that the power system would truly experience such fault current levels.

The maximum fault currents in some of main substations in the Hydro One network are summarized in Table 2. The requirements of circuit breaker interrupting capacity in the Hydro One are given in Table 3. It is estimated that the short circuit current level has increased by 27% in the Hydro One system in the last twenty years.

Table 1. Maximum allowable fault levels set out by OEB

Nominal Voltage (kV)	Maximum 3-Phase Fault (kA)	Maximum SLG fault (kA)
500	80 (usually limited to 63 kA)	80 (usually limited to 63 kA)
230	63	80 (usually limited to 63 kA)
115	50	50
44	20	19 (usually limited to 8 kA)
27.6 (4-wire)	17	12
27.6 (3-wire)	17	0.45
13.8	21	10

Table 2. Maximum fault levels in Hydro One network (2015)

Nominal Voltage (kV)	Fault Current (up to kA)
500	50.47
230	73
115	32.69

Table 3. Circuit breaker interrupting capacity requirement

Nominal Voltage (kV)	1990s (kA)	Present (kA)
500	40/63	63/80
230	40/50/63	50/63/80
115	40/50	40/50/63

C. Questions raised from protection engineers

The increased fault current causes the electrical devices to experience more thermal and mechanical stress. The protective relays are supposed to correctly operate to interrupt the fault current flowing through the protected equipment. However, relay misoperation, slow operation and failure to operate may be expected as the relay performance may be jeopardized in such scenarios.

Moreover, it can be predicted that the short circuit current level will further increase in the future. Considering the effects of the increasing fault current level on protective relays, protection engineers would ask the following questions:

- What will be the impact of increasing fault current on protection relays?
- Will relays be reliable or not under such situations?
- What are effects on the dependability and security of a relay?
- How to evaluate a specific system and relay under such circumstances?
- How to upgrade relay or adjust relay settings to increase dependability and security?

These questions will be discussed in the following sections, the examples will be analyzed, and the solutions will be provided and explained.

II. IMPACT OF INCREASING FAULT CURRENT ON PROTECTIVE RELAYS

A. Signal processing algorithms

The phasor and true root mean square (rms) value are the two most used quantities in relays. Normally, the true rms is calculated as the square root of the arithmetic mean of the squares of a set of raw samples in one cycle. The calculated rms value can truly represent the primary current regardless of the current level, if:

- the secondary current is not distorted by current transformer (CT) saturation or CT measurement error.
- the errors caused by analog-to-digital converter (ADC) quantization error, fixed point operations in relays, and anti-aliasing filter can be neglected.

The phasor estimation is used to calculate the fundamental magnitude and angle of the input signal. Two commonly used estimation techniques are Discrete Fourier Transform (DFT) and Cosine filter. Normally, a filtering technique is applied to remove DC decaying transients, which is prior to the phasor estimation by DFT. The above two techniques can be considered as a linear process such that the output is proportional to the input and the increased fault current level has no effect on the phasor estimation algorithms.

B. ADC range and clamping

Due to the conversion range of ADC, different relays normally have different clamping levels such that digital current samples will be clamped if they exceed levels. A simple example is shown below, where the clamping level is 10 pu and the current peak value is two times the clamping level.

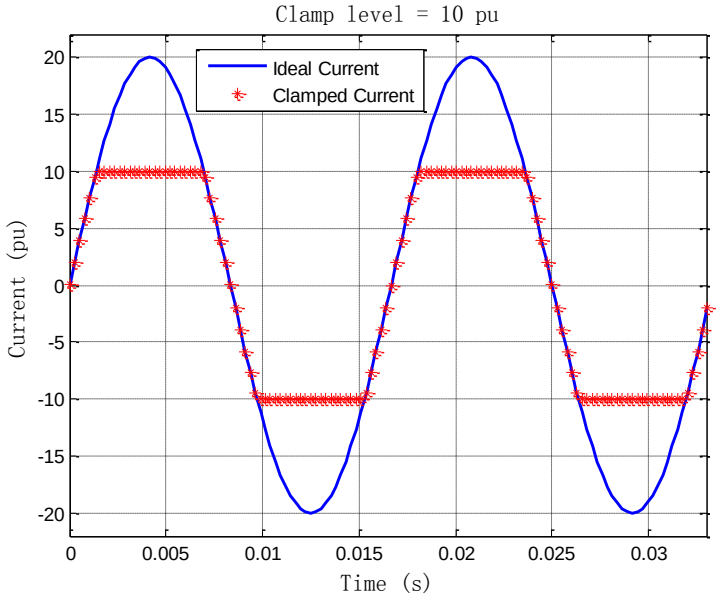

Figure 1. Example of clamped current

The digital samples clamped by ADC will not precisely express the secondary analog current, and they induce erroneous measurements and harmonics. The fundamental magnitude and rms values

of the clamped values are illustrated in Figure 2. Apparently, the lower clamp level results in the smaller magnitude and rms value. For example, if the clamp level is 50% of the peak value, the magnitude of the clamped current is 60.9% of ideal value, and rms is reduced to 62.5%. One more example, assuming that the clamp level is 28pu and the symmetrical fault current is 39.6pu (56pu for peak value), then the calculated magnitude will be 24.1pu, rather than the expected 39.6pu. It should be noted that the phase angle shift in the clamped currents is negligible.

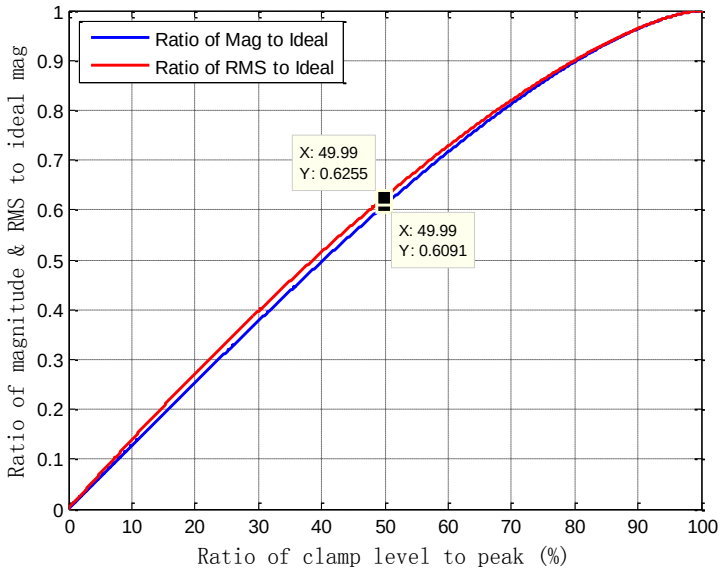

Figure 2. Magnitude and rms of clamped currents

The clamped currents induce the odd harmonics, but no even harmonics. The ratios of harmonics to the fundamental magnitude are shown in Figure 3. It should be mentioned that the fundamental magnitude here is calculated from the clamped current instead of the ideal current.

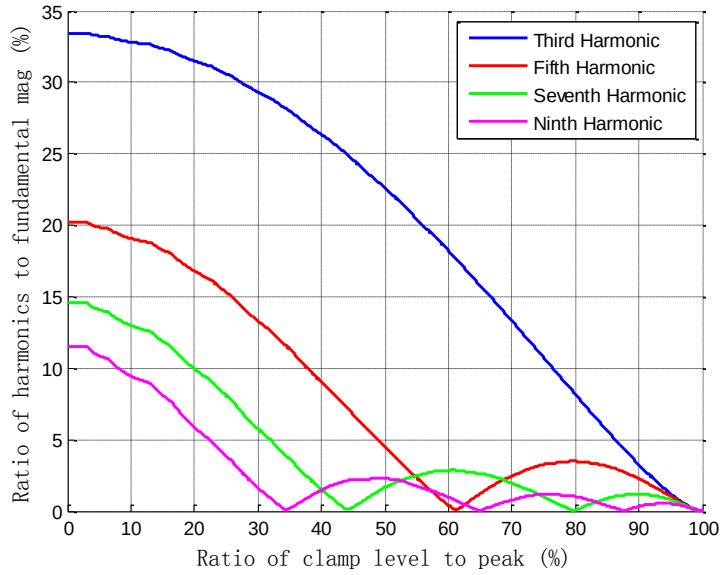

Figure 3. Ratio of harmonics to fundamental of clamped currents

It can be concluded that:

- The clamp level will reduce the current magnitude and rms values, which affects protection functions that are related to the current magnitude or rms values.
- The current phasor angle is not affected by the clamping mechanism.
- There is no erroneous even harmonics resulted from the clamping mechanism.
- However, erroneous odd harmonics are induced. For a constant clamp level and third harmonic, the larger fault current will result in the larger ratio of odd harmonics to fundamental magnitude if the current samples exceed the clamp level. Particularly, the ratio of the fifth harmonic to fundamental may be used to inhibit the transformer differential function during overexcitation conditions. Therefore, if the overexcitation inhibit mode is enabled, the transformer differential function may fail to operate on a severe fault due to the presence of the incorrect fifth harmonic induced by clamping. An instantaneous (unbiased/ unrestrained) differential function with a well-considered pickup setting is helpful to avoid such situation and increases the relay dependability.

C. CT saturation

Basically, there are five factors which contribute to CT saturation [6]:

- High primary fault current
- Low accuracy voltage class (due to improper CT selection/sizing)
- Excessive secondary burden
- Heavy DC offset in current
- Large percent remanence

The increase in primary fault current will increase secondary current, sequentially, increase exciting voltage, enter into the saturated region and significantly increase exciting current. As a result, the secondary current is greatly reduced and distorted.

When the CTs are selected with lower than required accuracy voltages or the low CT ratios are selected, the CT can go into saturation for the fault currents due to lower knee point voltage of the CT characteristics.

Larger CT burdens increase exciting voltage under the same fault current, and increase exciting current. Then CT is more likely to saturate.

The maximum DC component of a fault occurs when the instantaneous voltage is zero. Then the DC component starts decaying according to the time constant of the primary power system. The larger time constant will result in the longer decaying process, and then longer CT saturation period.

Remanence is the magnetic flux that is retained in the magnetic circuit after the removal of the excitation. Remanence may remain in either positive or negative direction. When the CT is subject to subsequent fault current again, the flux changes will start from the remanent value. Then the shifted remanence may worsen the transient response by pushing the core into deeper

saturation within a shorter time if the remanence and instantaneous flux have the same direction, or improve the transient response by keeping the core away from the deeper saturation if the remanence and instantaneous flux have the opposite direction.

The first factor (high primary fault current) in the above five factors will be discussed in this section. Due to the increased fault current, the existing CT may start saturating or experience the heavier saturation.

The CT secondary excitation characteristics curve is a practical way to represent the CT steady-state performance. This curve is normally provided by manufacturers and can be easily verified during field tests. The excitation curve maps the relationship between the root-mean-square (rms) value of the secondary exciting voltage and the rms value of the secondary exciting current. The Figure 4 shows an 800/5A CT excitation characteristic obtained during a field test.

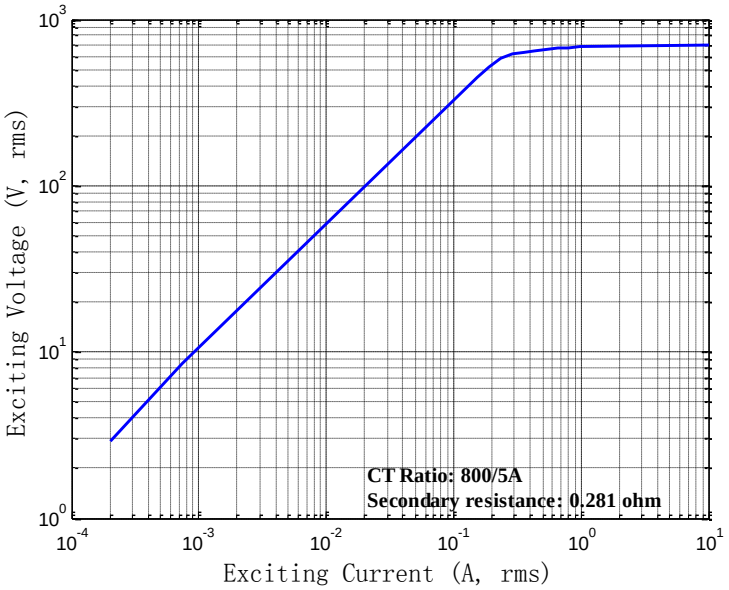

Figure 4. An 800/5A CT secondary excitation characteristics

In order to analyze the transient behavior of current transformers, this paper utilizes a simplified CT model proposed by the IEEE Power System Relaying Committee (PSRC) [7].

The AC saturation is caused by the symmetrical current with no DC component. A set of AC saturation examples is shown in Figure 5, which is generated by the PSRC model.

In order to avoid ac saturation [8], the secondary saturation voltage, V_X, must satisfy the following equation.

$$V_X > I_S \times Z_S \tag{1}$$

where, I_S is the primary current divided by the turns ratio, and Z_S is the total secondary burden (R_S + X_S + Z_B). It can be observed that the AC saturation may be caused by the higher primary current, lower ratio CT (such as ground CT), or a larger CT burden (long lead length, and/or small

AWG wire gage). Therefore, the AC saturation can be avoided by properly increasing the CT saturation voltage, CT ratio, or decreasing CT burden.

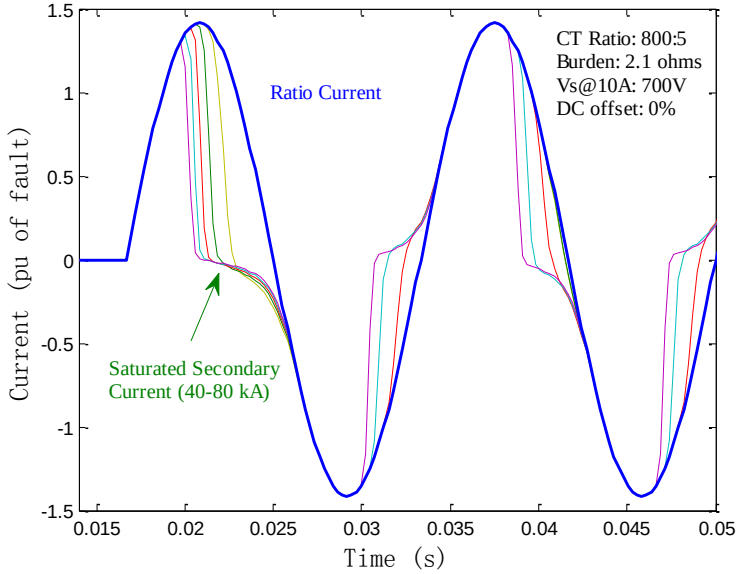

Figure 5. Examples of AC saturation

The DC saturation is commonly caused by the DC component in the fault current, unipolar half wave current or remnant flux in the CT. Once the transients decay enough or vanish so that the saturated region is not entered, the CT would get back to the steady state. A set of DC saturation examples caused by the fully DC offset is shown in Figure 6.

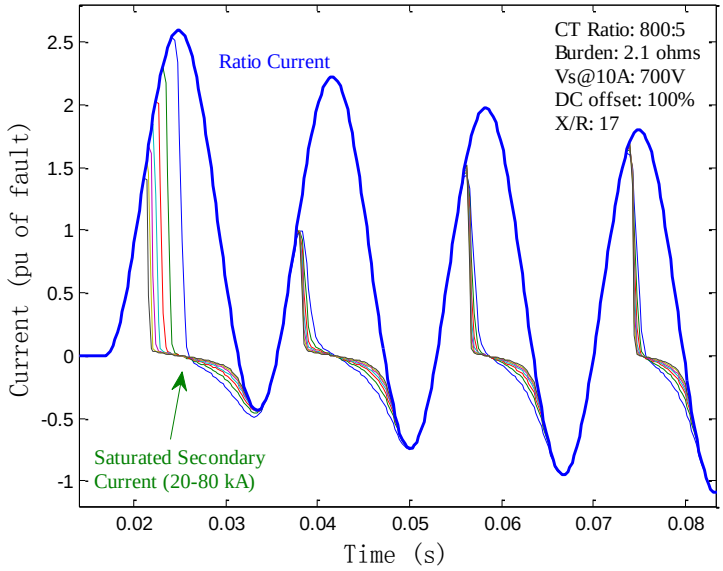

Figure 6. Examples of DC saturation

To avoid DC saturation (but ignoring effect of remanence), the required saturation voltage is given below,

$$V_X > I_S \times Z_S \times (1+\frac{X}{R}) \tag{2}$$

where *X/R* is the primary system X/R ratio. Comparing Eq. (1) with Eq. (2), it can be found that the knee point voltage to avoid DC saturation must be *(1+X/R)* times that required for avoiding AC saturation.

Taking AC saturation currents in Figure 5 as an example, the magnitude, rms, angle shift, and ratio of harmonics to fundamental are shown below.

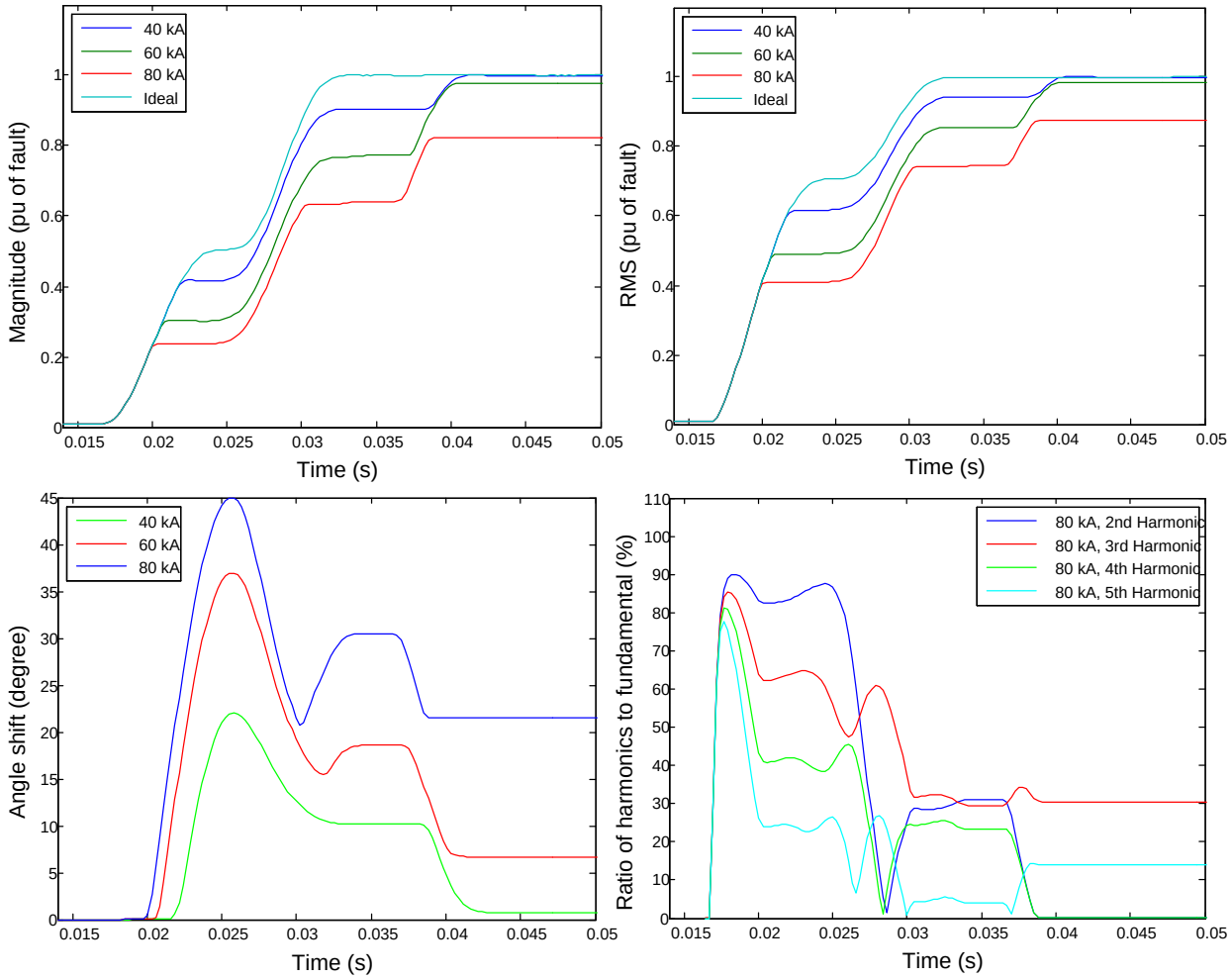

Figure 7. Magnitude, rms, angle shift and ratio of harmonics to fundamental (AC saturation)

It can be observed that:

- As expected, the deeper saturation will result in lower magnitude and rms value than the ideal values.
- The rms value is slightly higher than the corresponding magnitude since the waveform is distorted.

- The saturation will result in the leading angle. The deeper the saturation, the larger the leading angle will be.
- Taking the 80 kA fault current as an example, the ratios of even harmonics to fundamental will decay to zero less than 1.5 cycles after fault inception, but the ratios of odd harmonics to fundamental will reduce to a non-zero constant level. It should be noted that this decaying duration of 1.5 cycles is different from the decaying processing of the ratio of 2nd harmonic to fundamental in the transformer differential function, which takes quite longer time as described in Section IV-B.

Similarly, the relative analysis results of DC saturation currents in Figure 6 are shown below. The DC removal technique has been applied below to remove the DC decaying components in DC saturation waveforms.

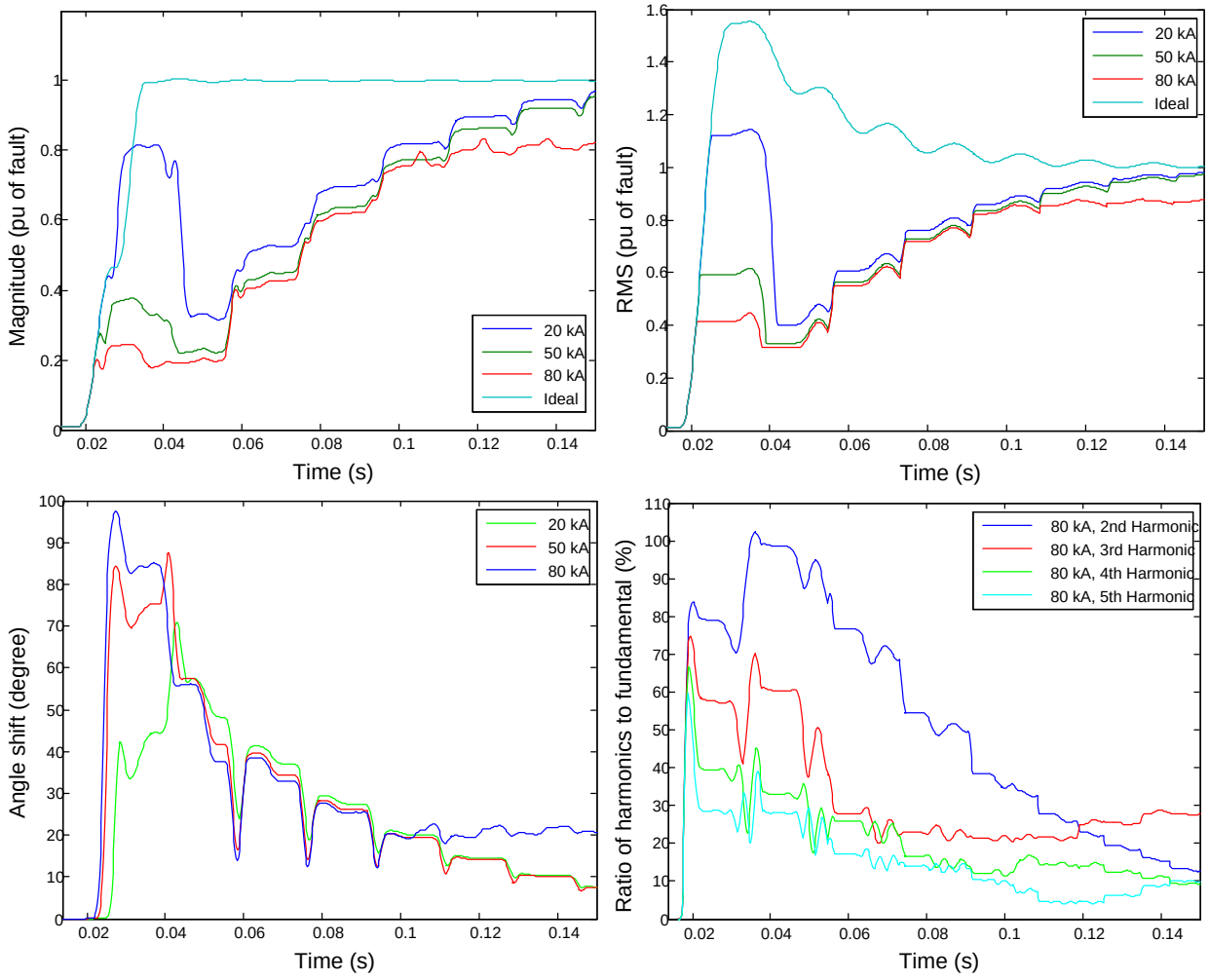

Figure 8. Magnitude, rms, angle shift and ratio of harmonics to fundamental (DC saturation)

It can be observed that:

- The deeper saturation will result in lower magnitude and rms value than the ideal values and take longer time to get stable.

- The rms value is higher than the corresponding magnitude since the waveform is distorted and the DC components are considered when calculating rms value.
- The saturation will result in the leading angle. The deeper the saturation, the larger the leading angle will be. Normally, the leading angle is less than 90 degree.
- Taking the 80 kA fault current as an example, the ratios of harmonics to fundamental will take a longer time to decay. Eventually, when the DC components decay enough or vanish, the CT will get into the stable state of AC saturation. Then, the ratios of even harmonics to fundamental are close to zero, but the ratios of odd harmonics to fundamental will reduce to the same level as shown in the bottom right figure in Figure 7.

It can be concluded that:

- The CT saturation will reduce the magnitude and rms values, which affects protection functions that are related to the current magnitude or rms values.
- The CT saturation will result in the leading angle, which may affect directional functions. DC saturation will cause more leading angle shift compared to AC saturation with the same symmetrical fault level.
- Due to the distortion in waveforms, the ratio of harmonics to fundamental magnitude increases.
    - Particularly, the ratio of the second harmonic to fundamental may be used to inhibit the transformer differential function during magnetizing inrush conditions. This ratio will decay to a lower level or zero after several cycles, which may cause the differential function to be slow to operate if the inrush inhibit mode is applied.
    - Similar to the explanation in Section II-B, the ratio of the fifth harmonic to fundamental may result in the transformer differential function failing to operate or being slow to operate on a severe fault if the overexcitation inhibit mode is enabled.

D. Combination of CT saturation and clamping level

As introduced before, the clamping level is used to flatten the high current input; however, the high fault current is subject to CT saturation. What happens if the saturated current is clamped?

Taking the three AC saturation current waveforms in Figure 5 as an example, two clamping levels, 32pu and 64pu, are applied separately, the magnitude, rms value, angle shift and 5^{th} harmonic ratio at the steady state are listed in the table below.

Table 4. Analysis of clamped currents with AC saturation (steady state)

	Fault Current (kA)	Clamping Level		
		No Clamping	32 pu	64 pu
Magnitude (pu of fault)	40	1.00	0.56	0.97
	60	0.98	0.37	0.70
	80	0.82	0.26	0.47
RMS (pu of fault)	40	1.00	0.57	0.97
	60	0.99	0.39	0.71
	80	0.87	0.26	0.48

Angle shift (leading, degree)	40	0.13	0.27	0.16
	60	6.69	14.04	9.22
	80	21.5	36.28	29.78
3rd Harmonic ratio (%)	40	0.16	24.49	3.07
	60	9.77	25.58	13.69
	80	30.51	10.72	11.66
5th Harmonic ratio (%)	40	0.12	6.65	2.17
	60	6.48	8.11	8.92
	80	14.04	13.97	17.95

It can be observed and concluded that:

- Doubtlessly, the higher the clamping level, the closer magnitude and rms values are to the non-clamping value.
- The higher the clamping level, the lesser the leading angle shift.
- Similar to Figure 7, the ratios of even harmonics to fundamental will decay to zero less than 1.5 cycles after fault inception regardless of the clamping level.
- However, the ratios of odd harmonics to fundamental will reduce to a stable non-zero level.
- It is interesting to find that the ratio of 5th harmonic to fundamental is becoming higher when the clamping level of 64pu is applied for the higher fault current. For example, the ratio of 5th harmonic to fundamental is increased from 13.97% to 17.95% if the clamping level is changed from 32pu to 64pu. This can be explained in Figure 3, as indicated by the red line. The ratio of 5th harmonic to fundamental at 80% of clamp to peak is larger than the one at 60%.

III. EVALUATION TECHNIQUES

This section presents some techniques and methods to explain how to evaluate the effect of the increased fault current on the dependability and security of a specific system and relay.

- Test in a high current laboratory: The advantage of the laboratory test is that the device is capable of generating as high fault current as the true fault in real power systems. Therefore, the relay experiences the very similar conditions as what happens in real faults. However, this method is costly and rarely available to most users. Besides the laboratory devices and relays, the other apparatus are also required, such as CTs.
- Test using a real time power system simulator: The simulator is able to model the power system, simulate different system and fault conditions in real time, generate analog signal which can be sent to a signal magnifier and then input to relays. Therefore, the relay performance and relay settings can be tested and verified. It should be noted that the capacity of the signal magnifier is a major concern for high level fault currents.
- Simulate in electromagnetic transient analysis software, such as EMTP or PSCAD/EMTDC: Except for outputting analog signals and simulating in real time, the functionality of the transient analysis software is similar to the real time simulator. Furthermore, different methods can be used to analyze the relay performance.
    - If the relay is already modeled in the software, the relay performance can be directly tested by simulating different system and fault conditions.

- If there is no relay model, the specific function in a relay can be modeled in the same transient software along with the power system.
- The simulated raw waveforms can be saved as a COMTRADE format file and injected to the relay by using a signal generator.
- Analysis software, such as MATLAB, can be programmed to load the raw waveforms, simulate the signal processing in the relay, model relay functions, and analyze the relay response.

If the second and forth methods are used, the signal processing and protection algorithms in the relay need to be investigated, understood and programmed.

- Playback recorded waveforms: In some cases the waveform of the actual events, which may have caused misoperations due to heavy faults, are existing. The COMTRADE files of these waveforms can be played back to the relay so that the relay performance and the corrective actions can be analyzed.
- Program in a simple Excel spreadsheet: If the above devices or tools are not available, a simple spreadsheet can be utilized. For example, once the maximum fault current level is determined and CT parameters are known, the PSRC CT saturation calculator can generate the secondary current with saturation or without it. By programming the signal processing and protection function in the spreadsheet, the relay function can be evaluated.

The two case studies in the next sections utilize the transient analysis software, PSCAD, to simulate different system and fault conditions, meanwhile saving the current waveforms as COMTRADE files. The mathematic tool, MATLAB, is then used to model the relay function algorithms, read recorded waveforms, and evaluate the performance the protection function.

IV. CASE ANALYSIS I

This section will analyze and evaluate the performance of a transformer differential relay in a 230/27.6kV substation.

A. System description and relay settings

A 215.5/28kV two-winding transformer is installed in a 230/27.6kV substation. The major parameters are listed below, which are obtained from field tests.

Table 1: Transformer parameters

Capacity	50/66.7/83.3 MVA
Cooling Type	ONAN/ODAN/ODAF
Primary Voltage	215.5 kV
Tap Voltage	215.5 kV ±16×1.16% steps (33 taps)
Secondary Voltage	28.0 kV
Windings	YNzn1, zigzag side grounded via 1.5 ohms resistance
No-load losses	28.847 kW at 100% rated voltage
Load losses	352.712 kW (83.3MVA, 85 ℃, Tap 17)
Impedance	12.43% (50MVA, 85 ℃)

The bushing CT at the high voltage side is an 800/5A CT, and its excitation curve is shown in Figure 4. The total CT burden is around 1.6 ohms. The bushing CT at the low voltage side is a 1600/5A CT and the total CT burden is around 1.73 ohms.

The settings of the percentage and unbiased transformer differential functions are illustrated in the following figure. The inrush mode inhibit is enabled, and the inhibit level is set as 15%. All settings are referred to the CT at the low voltage side. If not specified, all currents (per unit) in the following analysis are also referred to the low voltage side, where 1 pu current at the low voltage side is equal to 0.26 pu referred to the high voltage side.

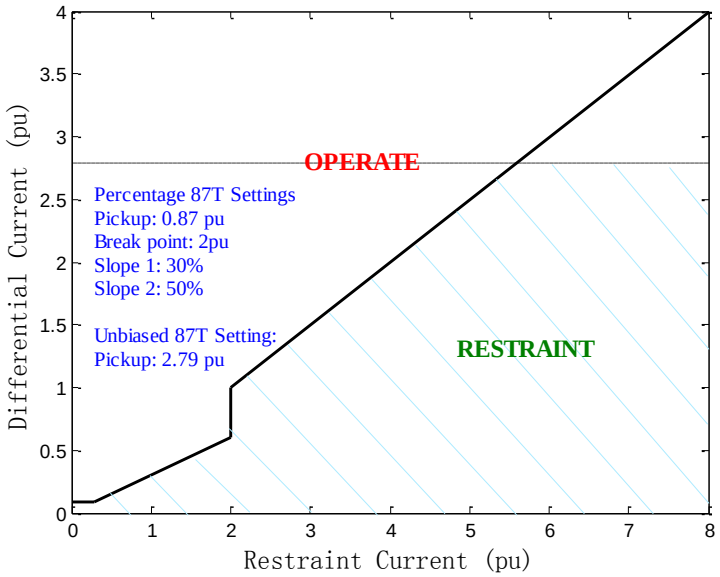

Figure 9. 87T settings

B. Analysis of increased fault current levels and CT saturation

Referred to the fault point F1 in Figure 10, two fault current levels are considered in this analysis: 60kA as the historic short circuit level and 73kA as the present short circuit level. According to Eq. (1), 60kA will not result in the AC saturation in the 800/5A CT, however, 73kA will cause light saturation. According to Eq. (2), any fault current greater than 3.5kA with full DC offset will result in the DC saturation in the same CT.

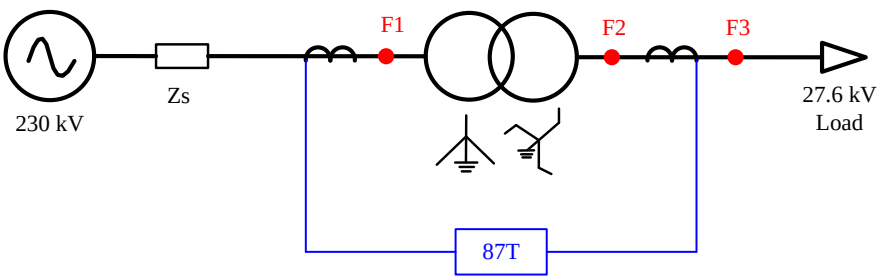

Figure 10. System diagram

In the following analysis in this section, the effect of clamping level in relays is not considered, which will be discussed in the next subsection. The combinations of the following scenarios have been simulated to examine the functionality of the transformer differential function.

- Three fault locations at F1, F2 and F3.
- Different fault types.
- Two different fault current levels, 60 and 73 kA (F1 point).
- Two fault inception angles, 0 and 90 degree (phase A voltage).

Generally, fault currents which cause light or zero CT saturation will not influence the dependability and security of the transformer differential relay if the appropriate settings are selected. However, faults inducing heavy CT saturation need to be studied carefully. Two examples are examined below.

The first case is a single-phase fault at F1, where phase A current at the high voltage side is heavily saturated with full DC offset as shown below.

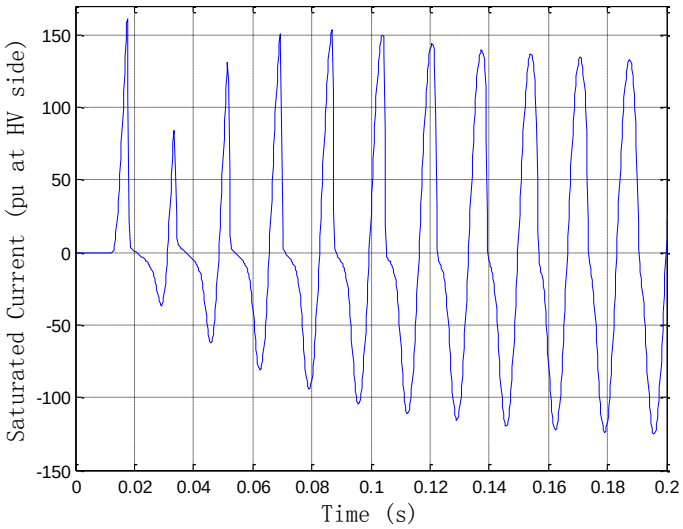

Figure 11. Example of saturated current (single-phase fault at F1)

The operating time sequence diagram of the transformer differential function is given below.

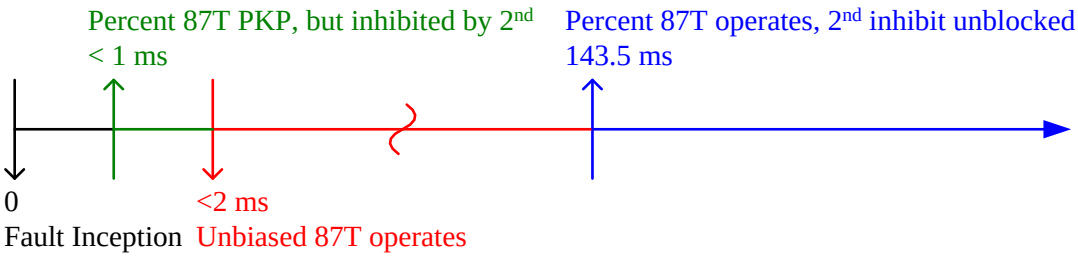

Figure 12. Operating time sequence diagram (single-phase fault at F1)

The second case is a 73kA three-phase fault at F1, where phase A current experiences slight AC saturation, and the other two phase currents are heavily saturated with DC offset.

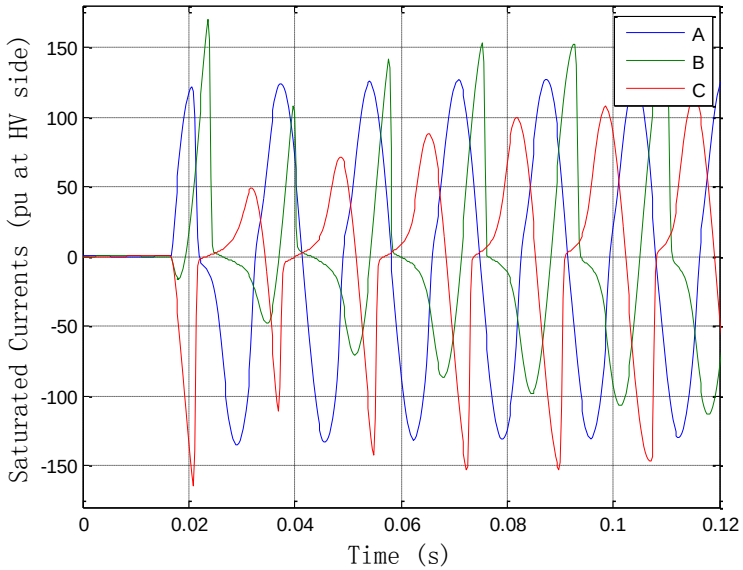

Figure 13. Example of saturated currents (three-phase fault at F1)

Similarly, the operating time sequence diagram of the transformer differential function is given below.

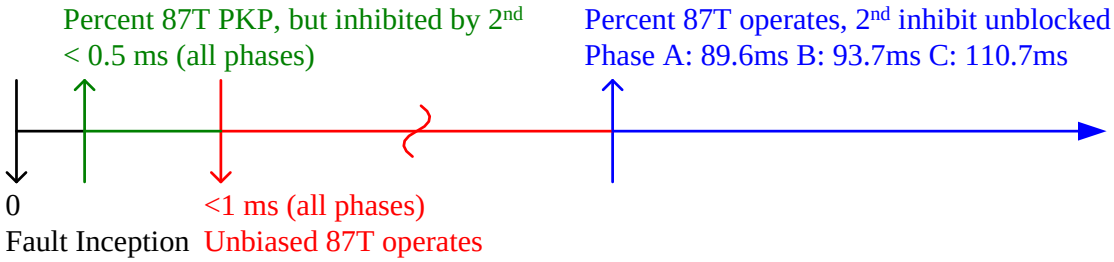

Figure 14. Operating time sequence diagram (three-phase fault at F1)

The simulations also indicate that,

- Faults at F2 and F3 do not cause CT saturation.
- The CT at the low voltage side does not experience CT saturation.
- Percentage differential function does not have failure to operate for internal faults or misoperations for external faults.

As observed from Figure 12 and Figure 14, it is important to point out that the instantaneous (unbiased) differential protection function should be enabled to avoid a slow operation if the percentage differential function is blocked by the second harmonic inhibit.

C. Analysis of different clamping levels

As mentioned in Section II-B, relays internally have the clamping level. In this section, two clamping levels are considered, 32pu and 64pu, where pu is based on the individual CT primary.

All fault cases in the previous section are studied with the two clamping levels considered. The results are summarized as below,

- Only fault currents at the point F1 experience clamping.
- The dependability and security of the unbiased differential function is not affected by the clamping level for the cases studied. The reason is that the fault current is high enough to trigger the unbiased 87T function. Meanwhile, a period free of saturation also allows the unbiased 87T to response fast.
- Regarding the percentage differential function, the dependability and security is not affected by the clamping level if the inrush inhibit is not enabled. However, if enabled, the cases with 64pu are faster by 0.66 cycles in average.

In the above analysis of the specific system, the unbiased 87T function is not affected by the application of clamping levels. However, the relay can be slow to operate for the 32pu clamping level in other situations. For example, if the total CT burden of the 800/5A CT is increased such that the first peak of the saturated current is between 32pu and 64pu as shown below, the operation time can be affected.

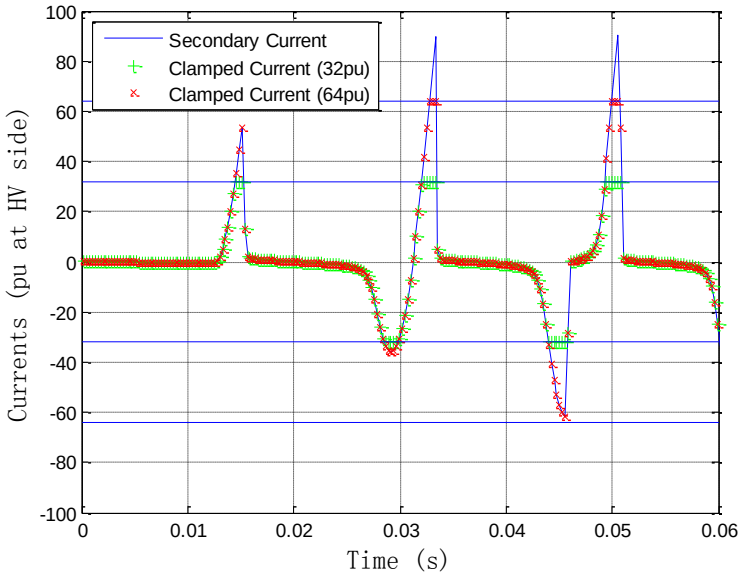

Figure 15. Clamped currents

If the pickup setting of the unbiased differential function is set larger than 8.5pu, a slow operation can be observed. For example as shown in the figure below, the unbiased 87T clamped by 32pu will be slower by 10.68ms if setting the pickup level to 10pu.

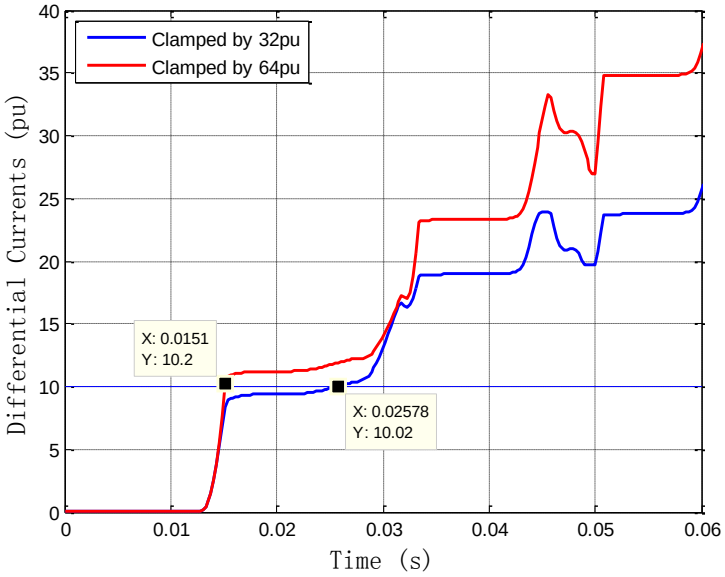

Figure 16. Magnitude of differential current

V. CASE ANALYSIS II

This case particularly demonstrates that the security of a transformer percentage differential function is affected by the increased fault current and clamping level. A 100MVA Yd11 transformer in a 138/19.5kV substation is studied. One external fault occurs at the low voltage side, which causes current saturation at the low voltage side. Similarly, two clamping levels, 32pu and 64pu, are applied. Two fault levels, 50kA and 65kA, are studied as well. The analysis and results are shown in Figure 17.

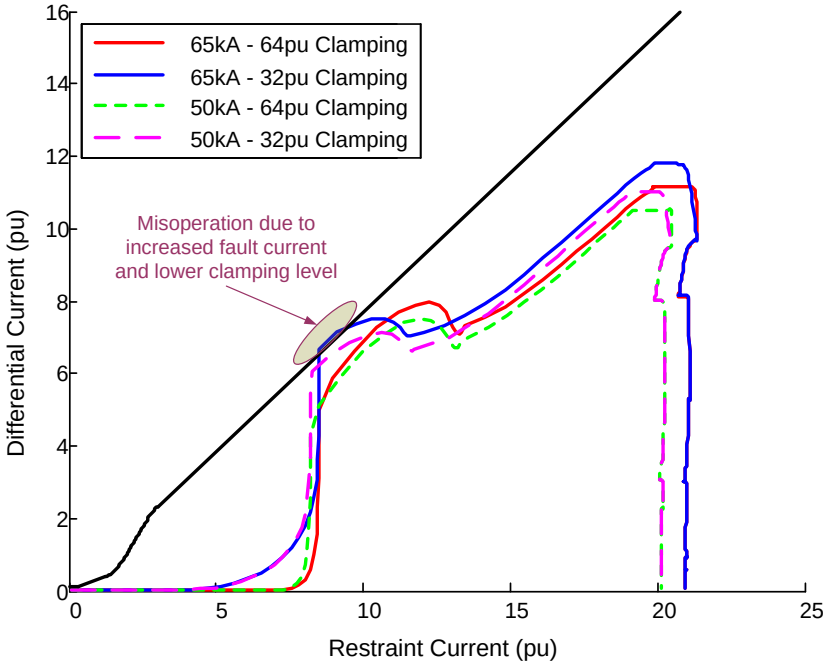

Figure 17. Example of misoperation due to increased fault current and lower clamping level

It can be observed from Figure 17 that:

- The increased fault current slightly drives the operating point closer to the operating boundary.
- The lower clamping level further pushes the operating point closer to the boundary, even entering the operating zone.
- Due to the effect of both increased fault current level and lower clamping level, a misoperation may occur.
- This misoperation can be blocked by applying the second harmonic inrush inhibit function, and/or increasing the slope setting.

VI. CONCLUSIONS

The increasing short circuit current level affects the protective relays in both external and internal aspects. Regarding the external impact, the higher fault current may cause or increase CT saturation. The CT saturation would reduce the fundamental magnitude and induce a leading phase angle shift, such that the performance of the current-based protection functions may be affected. As for internal effect of higher fault currents on relays, the relay internal clamping level limits the measurement range of the sampled waveforms. Therefore, the calculated magnitudes are decreased and erroneous harmonics result from higher fault currents exceeding the clamping levels.

Based on the analysis of the transformer differential function, it has been concluded that,

- It is better to enable the unbiased differential function for the sake of avoiding slow operation due to the inrush inhibit of the percentage differential function, thereby improving the relay dependability.
- The security of the percentage differential function may be jeopardized due to the increased fault current and lower clamping level. The security of the relay can be ensured by enabling the second harmonic inhibit function and/or increasing the differential settings.
- A transformer differential function with a larger clamping level is able to respond faster in some scenarios.

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VIII. BIOGRAPHIES

Zhihan Xu received the B.Sc. and M.Sc. degrees in power engineering from Sichuan University, the second M.Sc. degree in control systems from the University of Alberta, and a Ph.D. degree in power systems from the University of Western Ontario. He is a Lead Application Engineer with GE Grid Solution in Markham. His areas of interest include power system protection and control, fault analysis, modeling, simulation, and automation. He is a professional engineer registered in the province of Ontario.

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