Evaluation Board for AD9874

EVAL-AD9874EB

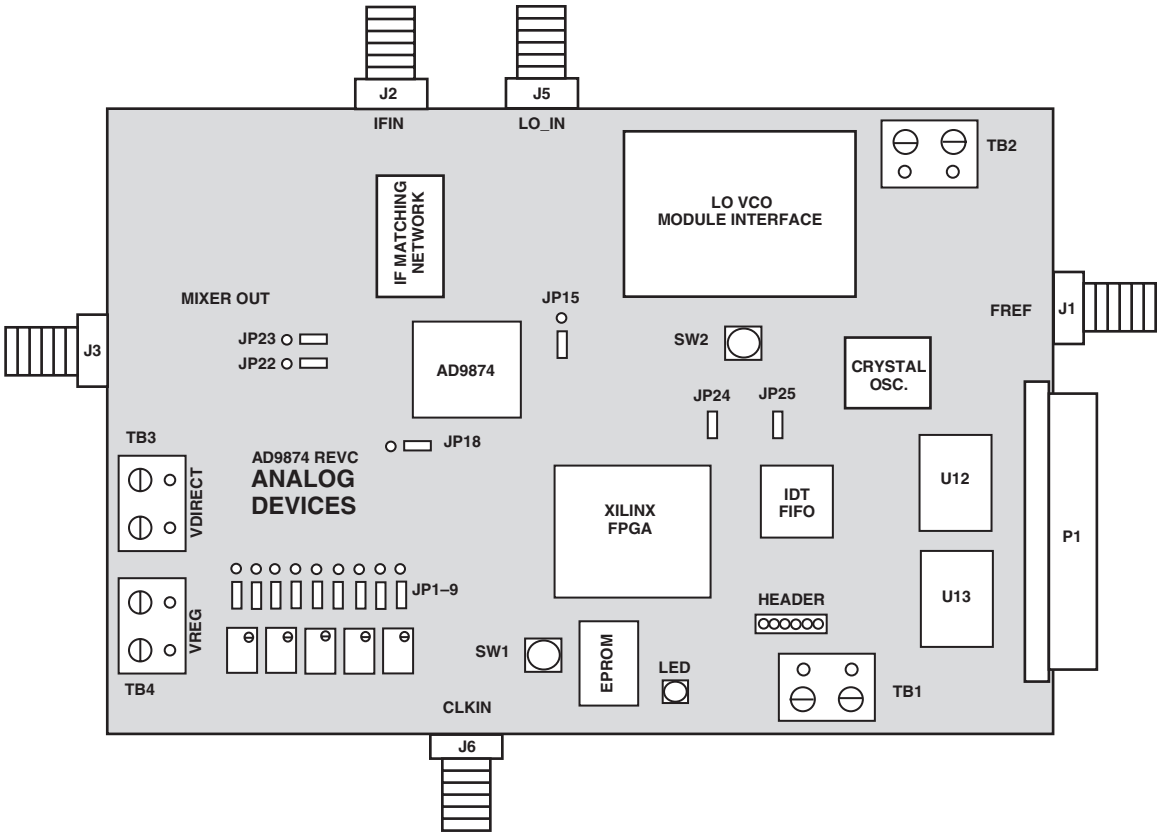
GENERAL DESCRIPTION

The evaluation board for the AD9874 and its accompanying software provide a simple means to evaluate this highly integrated IC. The AD9874 is a general-purpose IF subsystem that digitizes a low level 10 MHz–300 MHz IF input with signal bandwidths ranging from 6.8 kHz to 270 kHz. The signal chain within the IC consists of a low noise amplifier, a mixer, a variable gain amplifier, a band-pass Σ-Δ analog-to-digital converter, and a decimation filter with programmable decimation factor. Auxiliary blocks include clock and LO synthesizers as well as a serial peripheral interface (SPI) port.

The functional block diagram shows the major blocks of the evaluation board. The evaluation board is designed to be flexible, allowing the user to configure it for different potential applications. The power supply distribution block provides filtered, adjustable voltages to the various supply pins of the AD9874. In the IF input signal path, component pads are available to implement different IF impedance matching networks. The LO and CLK signals can be externally applied or internally derived from a user-supplied VCO module interface daughter board. The reference for the on-chip LO and CLK synthesizers can be applied via the external FREF input or an on-board crystal oscillator.

The evaluation board is designed to interface to a PC via a National Instruments NI 6533 series digital IO card. A XILINX FPGA formats the data between the AD9874 and digital I/O board. Software, developed using National Instruments' LabVIEW™ and provided as Windows® executable programs, is supplied for the configuration of the SPI port registers and analysis of the AD9874's output data. This software provides a convenient graphical user interface, allowing easy access to the various SPI port configuration registers along with real-time frequency and time domain analysis of its output data.

FUNCTIONAL BLOCK DIAGRAM



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SYSTEM REQUIREMENTS

A Pentium® 90 or greater PC

National Instruments' NI 6533 Series Digital I/O (i.e., PCI-DIO-32HS). Note: NI6534 series works with NIDAQ software version 6.9.2 or greater.

National Instruments' 64-Lead Shielded (SH68-68-D1) Interface Cable

High Quality RF Signal Generator(s) for the IF Input as well as LO and CLK Inputs (If the AD9874 LO and CLK Synthesizers Are Disabled)

VCO Module and Crystal Oscillator (or RF Signal Generator) if the LO and CLK Synthesizers Are Enabled

Two 5 V Power Supplies (Note, Additional Supply Required to Power VCO Module)

An AD9874 Evaluation Board with Software

HARDWARE DESCRIPTION

The following section describes the various sections pertaining to the AD9874 evaluation board. The functional block diagram on the previous page can be used to determine the location of the particular section being described. The relevant schematics are listed next to each section and can be found at the end of this document. The evaluation board's schematic, layout documentation, bill of materials, and software can be found at http://products.analog.com/products/info.asp?product=AD9874.

SMA Connector Description

There are five SMA connectors on the evaluation board. The functions of these connectors are outlined in Table I.

Table I. SMA Connector Description

No.	Name	Description
J1	FREF	Reference Frequency Input for LO and CLK Synthesizer
J2	IFIN	IF Input Signal
J3	MIXER OUT	Optional Mixer Output Signal
J5	LO_IN	Optional LO Input for Mixer
J6	CLKIN	Optional CLK Input for ADC

IF Matching Network (See Figure 6a)

The IF input signal path includes component pads such that a matching network can be implemented to match the AD9874's LNA input impedance to a nominal 50 Ω RF signal source. A 0.1 µF dc blocking capacitor, C83, is included in the signal path since the AD9874's LNA input is self-biasing. Table II lists the component values for several IF frequencies.

Table II. Matching Component Values for Various IFs

IF (MHz)	C30 (Ω)	C31 (pF)	C32	C34
73.35	0	18	220 nH	5 pF
109.65	0	19.5	120 nH	21.5 pF
240	0	5.7	4 pF	39 nH

The evaluation board is shipped with 0 Ω resistors inserted for C30 and C31 and a 57.6 Ω resistor inserted for R51. The addition of R51 (which is in parallel with the AD9874's input impedance) results in approximately a 50 Ω load for the external RF source and 8.1 dB of power loss for frequencies below 100 MHz. Also, since the IF signal path does not maintain a 50 Ω strip line impedance, care must be taken when developing a matching network for other IFs.

LO Input, Synthesizer, and VCO Module (See Figure 6b)

The LO input for the AD9874's mixer can be supplied by either an external RF generator via SMA connector J5, or a user-suppled VCO module. In either case, the LO signal can be passed on to the AD9874 as a single-ended signal (with R59 = R60 = Open and R62 = 0 Ω) or a differential signal via transformer T1 (with R59 = R60 = 0 Ω and R62 = Open).

The user can supply their own VCO module if the AD9874's LO synthesizer is to be enabled. The VCO module should be connected to the AD9874 Evaluation Board via *four* single row vertical 0.1 mil header and receptacle pairs (available from 3M, AMPS, Samtec). Use of the receptacle provides a solder-free connection that simplifies the evaluation of multiple VCO modules optimized for different LO frequencies. The user should populate the AD9874 evaluation board's VCO module interface with the receptacle and lay out their custom VCO module with the headers. Note, a solid ground connection is formed between the user-supplied VCO module and the AD9874 evaluation board's ground plane, since almost all of the receptacle/header pins (excluding the VCO module input and output) are dedicated ground pins.

The charge pump output current of the AD9874 can be directed to a resistor network consisting of R34 and R35 or to the synthesizer's loop filter via JP15. The former connection can be used to monitor the charge pump's performance independently, while the latter connection is used for normal synthesizer operation and closed-loop evaluation. Component pads consisting of C44, C66, C67, R36, and R37 are available to implement the application-specific loop filter.

CLK Input and Synthesizer (See Figure 6b)

The CLK signal for the AD9874 can be supplied via an external RF generator or derived from a VCO. In the former case, the external CLK signal is supplied via SMA connector J6 and ac-coupled (via C41, C42) as a single-ended or differential signal with R25 serving as a termination resistor. Note, the default configuration is for an external RF generator that is capacitively coupled to the AD9874's CLK input as a single-ended signal.

The AD9874 evaluation board also provides a means to evaluate the AD9874's on-chip CLK synthesizer and negative resistance oscillator. Component pads consisting of C62, C63, R30, and R31 are used to implement the application specific loop filter for the synthesizer. Varactor D5 (Toshiba 1SV2228, not included) in combination with C29, L12, and the AD9874's internal negative resistance core form a VCO that can be connected to the AD9874's CLK input via R3 and R4. Note, the component pads for varactor D5 accept SOT 23 packages, allowing other vendor varactors (i.e., Zetex) to be selected. R52 and C33 provide a filtered dc biasing point for the VCO circuit. Lastly, the charge pump output current from the AD9874 can be directed to a resistor network consisting of R32 and R33 for independent evaluation or to the CLK synthesizer's loop filter via JP18.

FREF Input (See Figure 6e)

An external reference frequency for the LO and CLK synthesizers can be supplied via SMA connector J1 or a crystal oscillator ("H" package, not included). The SMA input connector is terminated with a 50 Ω resistor, R5. Selection of the frequency

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reference source can be made by installing R7 or R8. Note, the crystal oscillator is locally decoupled and its supply tied to TB3 (VDIRECT).

FPGA, FIFO, and NIDAQ Interface (See Figures 6c and 6d)
The AD9874 evaluation board is designed to interface to a PC via a National Instruments NI 6533 (or NI6534) series digital IO (NIDAQ) card. The evaluation software that configures the AD9874 and analyzes its output data supports this interface. A XILINX FPGA (U3) and IDT FIFO (U11) are used to format the AD9874's serial output data and to control the interface between the AD9874 and NIDAQ card as shown in Figure 1. The interface supports normal data output modes of operation in which decimated 16- or 24-bit I and Q data (along with optional embedded AGC data) are provided within a frame. It also supports a mode that provides the undecimated digital output from the AD9874's Σ-Δ ADC.

For normal output data modes, the FPGA formats the AD9874's serial output (SSI) data within a frame into 16-bit parallel data for the FIFO and controls the interface timing between the FIFO and NIDAQ card. Line drivers (U12 and U13) are included to drive the NIDAQ card via a shielded cable (not included) with the 16-bit data. In the special interface mode, the FPGA provides the buffered undecimated output data directly to the NIDAQ card at the CLK rate.

The FPGA is also used to control the serial port interface (SPI) between the AD9874 and NIDAQ card. In this case, the FPGA buffers and conditions the 5 V logic input levels from the NIDAQ card. It also contains a bidirectional buffer that is used to control the data flow for SPI WRITE and READ operations. The FPGA is programmed via a serial EPROM (U4). A green LED illuminates when the FPGA is configured.

The evaluation board comes installed with a 68-lead male SCS1-11 type cable connector. The user is required to purchase a SH68-68-D1 shielded interface cable (National Instruments Part No. 183432-01) and NI 6533 digital I/O card (www.ni.com/pdf/products/us/2mhw332-333e.pdf).

Interfacing AD9874 Evaluation Board to a DSP (See Figure 6c)
The current AD9874 evaluation board unfortunately does not provide a simple and clean interface to a DSP evaluation board. However, only a minor board modification is required to enable such an interface. The SSI digital output interface is simple since the AD9874's output signals are buffered by the FPGA and made available from header J4. Note, the DGND test point next to J4 should be used to provide a digital ground return path between the two evaluation boards. The SPI interface is more complicated since there is no header provided for the PE, PC, and PD signals. The solution is to use the PE, PC, and PD test points located next to the FPGA and *lift* the corresponding FPGA pins (Pins 19, 20, and 21 of U3). These FPGA pins provide buffered output signals and can be disconnected to prevent bus contention.

Power Supply Interface (See Figure 6e and 6f)
The AD9874 evaluation board contains four power supply terminal blocks (TB) for external power supply connections. TB3 allows the user to *directly* apply power to any individual

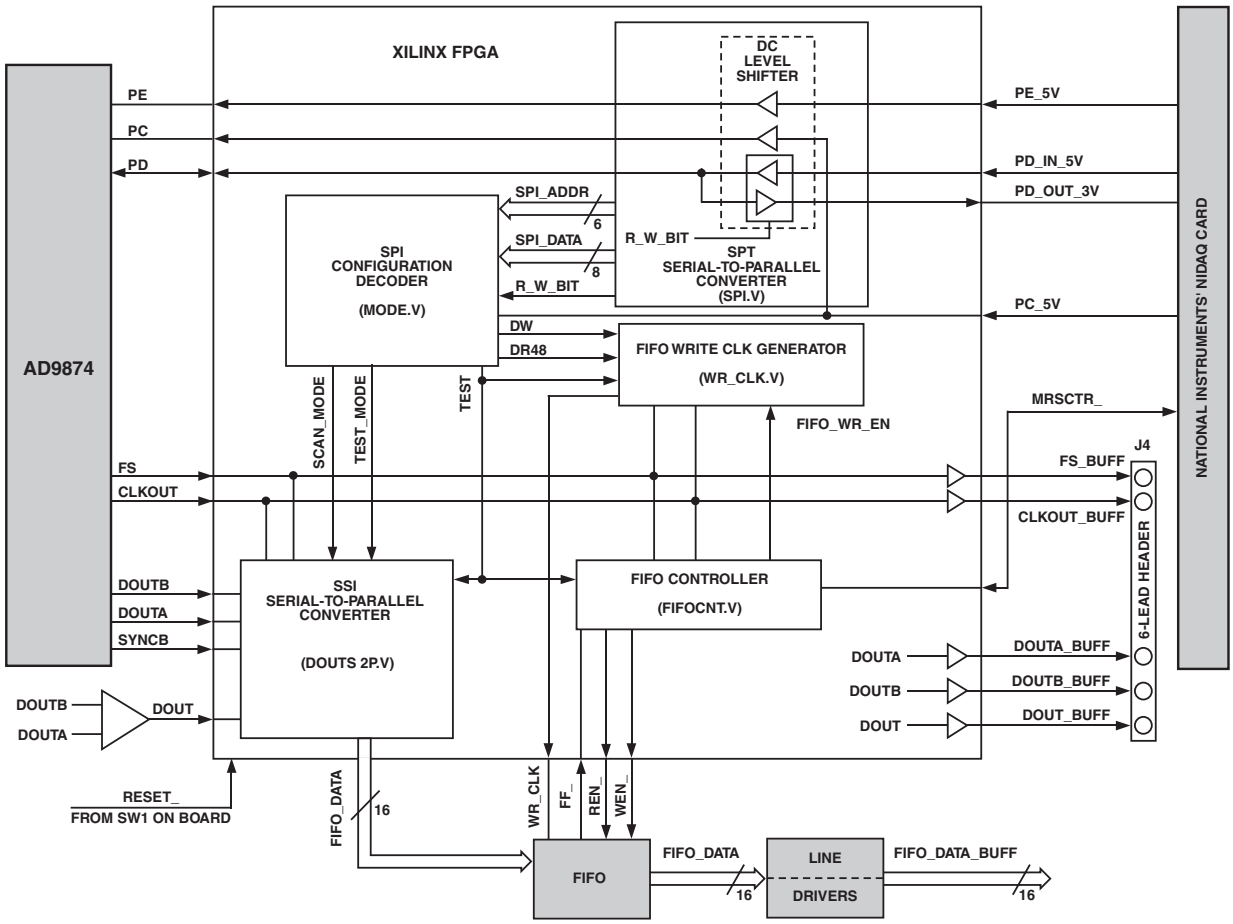


Figure 1. Block Diagram of XILINX FPGA and FIFO Used to Control Interface between AD9874 and NIDAQ Card

or group of AD9874 supply pins by proper configuration of jumpers JP1–JP9. This is useful for automated testing in which various supply voltages may be swept. Also, the individual supply currents can be monitored at these jumpers.

TB4 allows the user to apply an unregulated 5 V supply to five voltage regulators that provide regulated supplies to the AD9874 by proper configuration of JP1–JP9. The voltage of these regulators can be controlled over a 2.2 V to 3.8 V range via a potentiometer. TB1 provides an unregulated 5 V supply for the digital ICs, while TB2 provides a user-defined supply level for the LO VCO module (if installed).

Evaluation Board Setup Example

Figure 2 shows an example of a lab setup used to evaluate the AD9874. In this example, three RF generators are used to drive the IFIN, LO_IN, and CLKIN SMA connectors, since both the LO and CLK synthesizers of the AD9874 are disabled. All of the RF generators are phase locked to minimize the phase noise contribution and enable coherent sampling. Note, only a single RF generator would be required to supply the IFIN signal if the LO and CLK synthesizers were enabled with the necessary external components installed (i.e., crystal oscillator, PLL loop filter, VCO module, and so on).

Two 5 V supplies are connected to TB4 and TB1 with JP24 (or J25) installed to connect the grounds of the supplies together. Individual supplies to the AD9874 can be varied via the potentiometers. A shielded interface cable (National Instruments Part No. 183432-01) is used to connect the evaluation board to the NI 6533 digital I/O card.

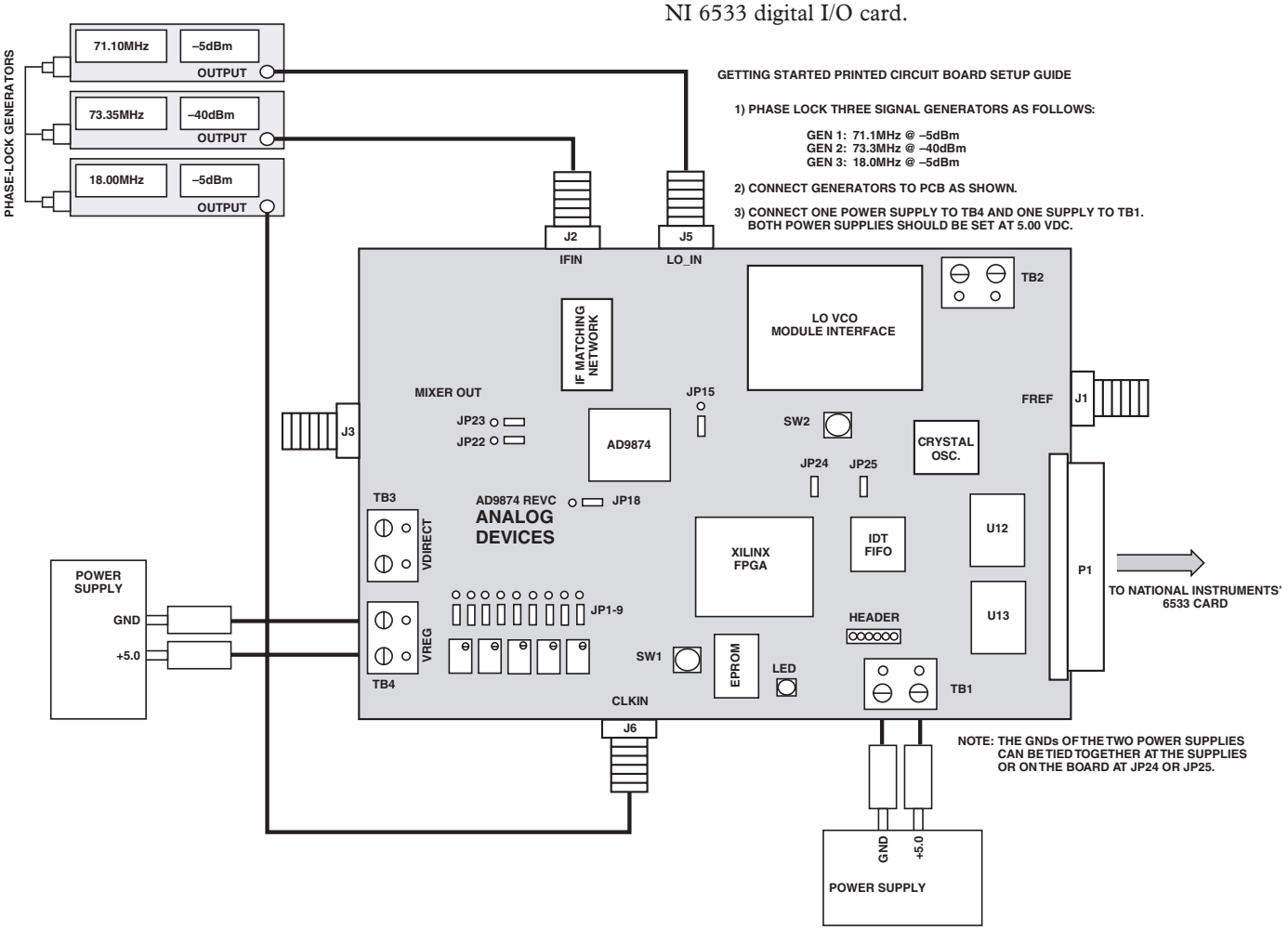


Figure 2. Typical AD9874 Evaluation Board Setup with the LO and CLK Synthesizers Disabled

SOFTWARE DESCRIPTION

Software Installation

The AD9874's evaluation board software and PCB board documentation comes on a CD-ROM titled, *AD9874 Evaluation Board Software/Documentation*. The contents of the CD are as follows and are placed in their associated folders:

- Readme File (Readme.txt)
- Eval Board Connectivity PDF File (interconnect_pcb.pdf)
- Layout PDF File (ad9874cpcb.pdf)
- Schematic PDF File (ad9874csch.pdf)
- LabVIEW Eval_ File (ad9874_eval.exe ver. 5.1.1)
- LabVIEW Eval_ Library File (ad9874_eval.llb ver. 5.1.1)
- Installer Setup File for LabVIEW Run-Time Engine (Setup.exe ver. 5.1.1)

The user has two options available in the installation and operation of the software. Before loading the software, the user should verify that the NI 6533 DIO card and associated software has been installed on to their PC. Option 1 is for users who currently have LabVIEW version 5.1.1 loaded on their computer, while Option 2 is for those who do not. Please select the appropriate option and follow the recommended guidelines below.

Option1: Running the VIs from the library files (.llb) in LabVIEW:

a. Launch the LabVIEW application
b. Choose File, Open, and select the ad9874_eval.llb file in the **Option1** subdirectory
c. From the File dialog box, choose the ad9874_Eval_SW_090402. vi and click OK

Note, Analog Devices does not support modifications to any of the VIs contained in the ad9874_eval library.

Option 2: Loading the run-time engine and running executable files (.exe)

a. From Windows desktop environment, select START, run, then browse to your cd drive, and execute the Setup.exe file found in <cd drive letter>:**Option2\Installer\disks** directory. Follow the instructions to load the run-time engine on your computer.
b. From Windows desktop environment, select Start, run, then browse to your cd drive and look for the ad9874_eval.exe files.
c. Hit Open to launch program.

Control Panel Description

Upon launching the AD9874_eval application, the control panel shown in Figure 3 should appear. This panel is used to:

- Configure and read back the various AD9874 SPI registers
- Initiate a self-tuning macro for the AD9874's ADC
- Set the National Instruments data acquisition device's number
- Access the demodulated complex I/Q signal or the ADC's undecimated data display windows.

The SPI registers are listed by their address and grouped according to their function within the AD9874. When applicable, the various control bits associated with some SPI register addresses are expanded to further simplify programming of the IC. Lastly, a Help button is available for each SPI register, providing a more detailed description of its function.

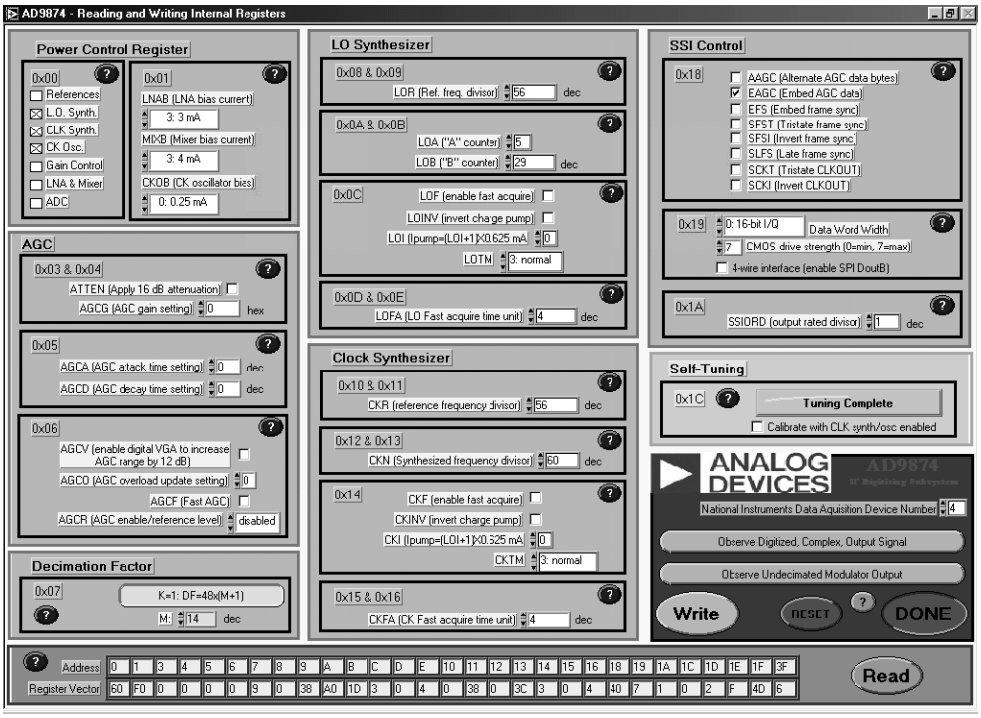


Figure 3. Control Panel for Programming and Tuning the AD9874 Prior to Observing Output Data

The bottom right corner of the control panel (next to the ADI logo) contains several buttons that are used to invoke various actions as described below in descending order. Positioning the pointer over the particular button followed by a left mouse click invokes a particular action.

Run Self-Tuning Macro—Clicking this button initiates a series of commands detailed in the HELP menu that automatically tunes the AD9874's Σ-Δ ADC. Note, tuning is required upon powering the AD9874 once the CLK frequency has stabilized. Tuning is also required if the CLK frequency is varied.

National Instruments Data Acquisition Device Number—One should ensure that the number entered in the box corresponds to the number used when installing the NIDAQ NI 6533 card software.

Observe Digitized, Complex Output Signal—Once the AD9874's SPI registers have been properly configured (and its Σ-Δ ADC tuned), clicking this button will open another display showing the complex I/Q output data in both the time and frequency domain.

Observe Undecimated Modulator Output—Once the AD9874's SPI registers have been properly configured (and its Σ-Δ ADC tuned), clicking this button opens another display in which the spectrum of the undecimated Σ-Δ ADC can be observed.

Write—Clicking this button causes all of the AD9874 SPI registers to be updated with the values programmed on the screen. Note, an automatic readback of the SPI registers occurs after the write command and the results are shown on the bottom of the control panel display.

Reset—Clicking this button "resets" the AD9874 to its default values as described in Table I of the AD9874 data sheet. Note, the default values will also appear on the bottom of the control panel display.

Done—Clicking this button closes the AD9874_eval application.

Read—Clicking this button reads back the contents of the AD9874's SPI registers and displays the values to the left of the button.

Digitized, Complex Output Signal Display Description
Figure 4 shows the display that will appear after clicking on the Observe Digitized, Complex Output Signal button. The displays show the Complex FFT of the I and Q data (normalized to its output data rate) as well as a time domain representation of the I/Q waveform and its constellation. The AD9874's attenuation setting, signal strength, and reset fields can also be observed graphically by changing the Embedded AGC Data_I/Q Constellation switch to the appropriate position (assuming the AD9874's SSI is configured properly). Note, upon entering this display, the control panel is rendered inactive while the display window remains active.

The horizontal and vertical axes of the displays can be modified by the following procedure: position cursor over the min (or max) axis setting, left click mouse, and type in new axis setting. Individual SPI registers can be updated by entering the designated register number and value in the boxes located in the display's bottom left corner followed by a left click on the WRITE button. The current status of the SPI registers can be observed in the lower portion of the display window.

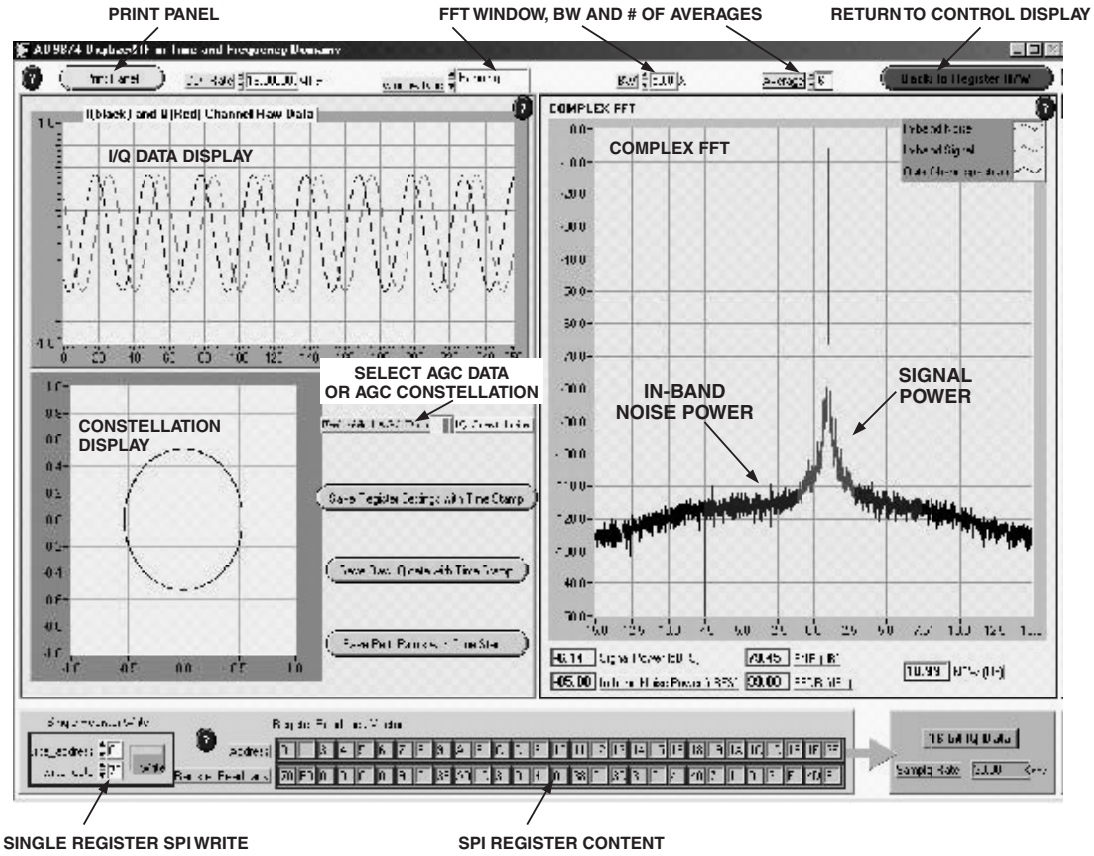


Figure 4. Complex Output Signal Display with I/Q Constellation

Parameters associated with the Complex FFT display can be modified by the user. They are highlighted in *yellow* across the top portion of the display window and include CLK rate, FFT Window type, BW, and FFT averages. BW sets the measurement bandwidth for which the following parameters are calculated: signal power, in-band noise power, SNR, SFDR, and NBW. The Complex FFT display highlights the signal power in *red*, the in-band noise power in *blue*, and the out-of-band region in *black*. Note, the signal power, SNR, and SFDR results are only applicable for unmodulated carriers located in FFT bins. The power of modulated carriers can be measured using the in-band noise power (*blue*) with the BW parameter set appropriately.

The display window also has the ability to data log the SPI register settings, the raw I/Q data, and the performance parameters. A left click over the appropriate Save button will prompt the user to specify a file name and location for the new data file. The data is saved into this file with a time stamp for further evaluation. Lastly, the display window can be printed to a file (or printer) using the PRINT PANEL button located in the upper left-hand corner.

Undecimated Modular Display Description

Figure 5 shows the display that will appear after clicking on the Observe Undecimated Modulator Output Signal button of the control panel. The displays show the FFT of the AD9874's Σ-Δ ADC's undecimated output data. The clock rate and FFT window type can be specified in the top right corner of the window. Note, the FFT display provides a clear demonstration of the noise-shaping inherent in the band-pass Σ-Δ ADC's output spectrum. Also, the peak signal level reported in the top right corner of the FFT display is useful in observing the amount of out-of-band rejection to signals falling outside its pass band prior to any digital filtering.

This display also provides the quantized output levels with the ability to write the data to a file. Single SPI register write capabilities are also included with the most current SPI register settings displayed on the lower portion of the window. A PRINT PANEL button is also provided on the display.

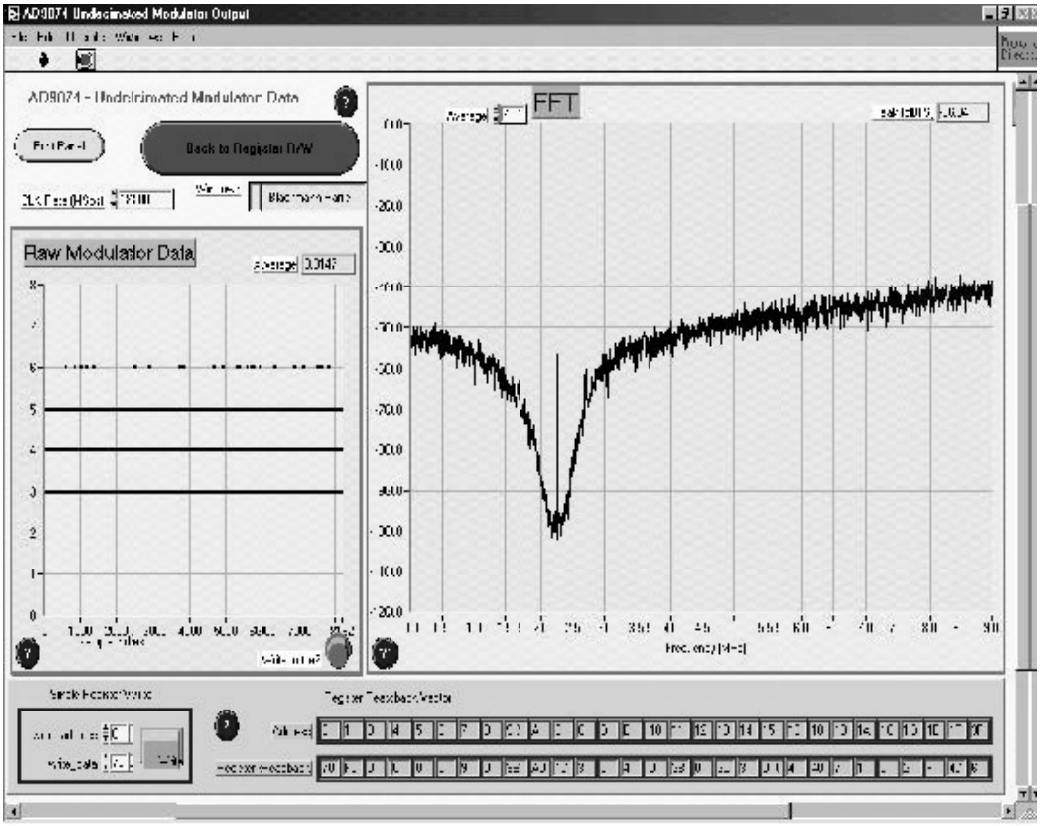


Figure 5. Complex Output Signal Display with I/Q Constellation

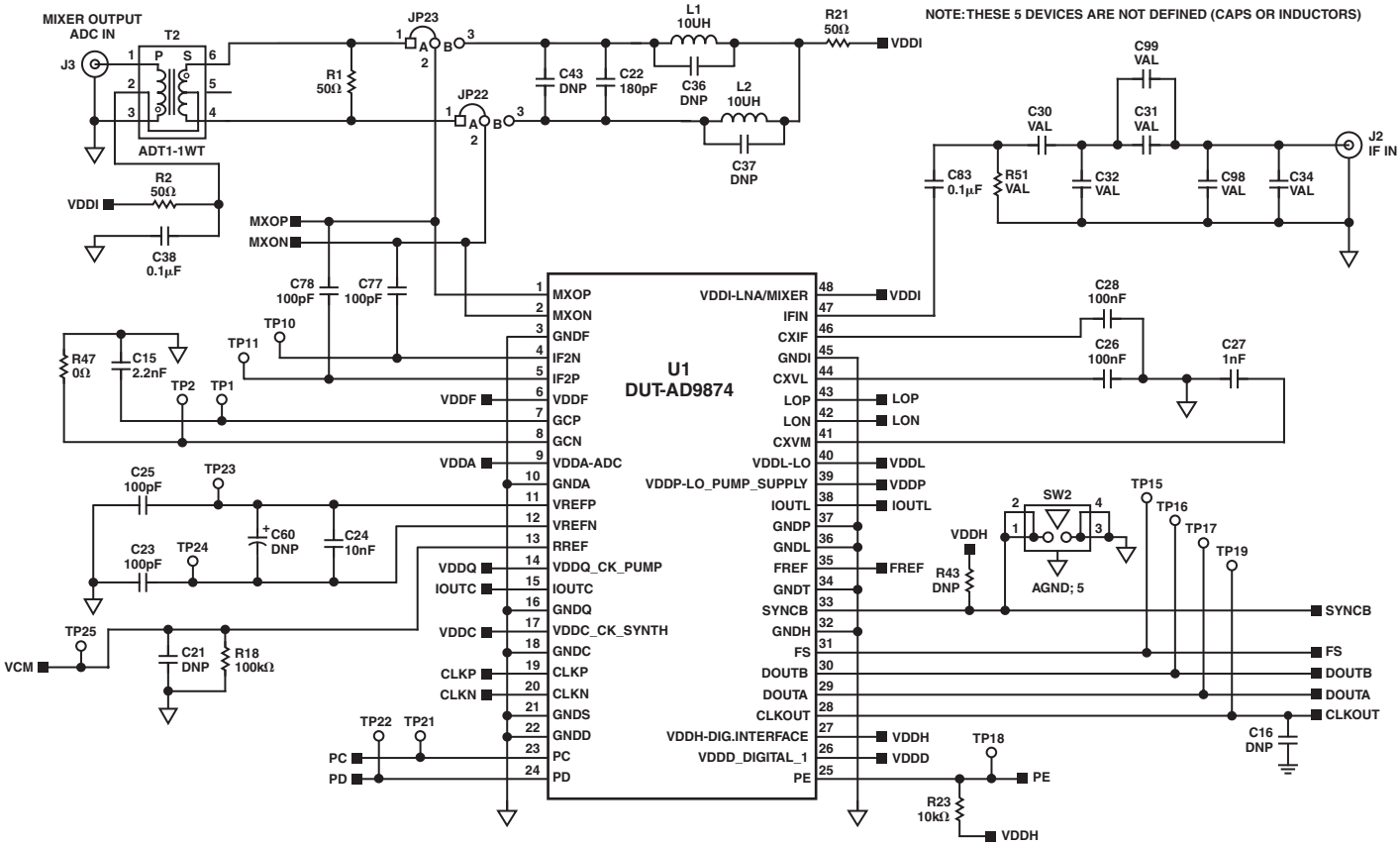
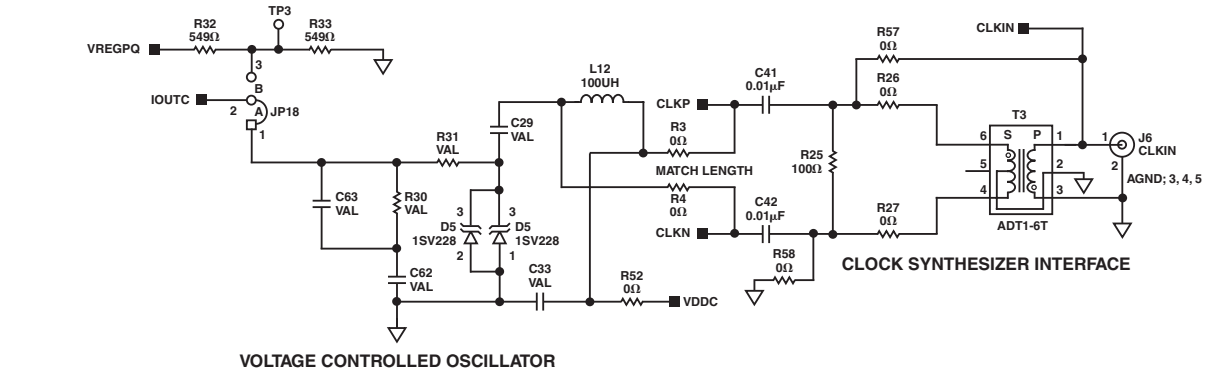


Figure 6a. AD9874 Interface



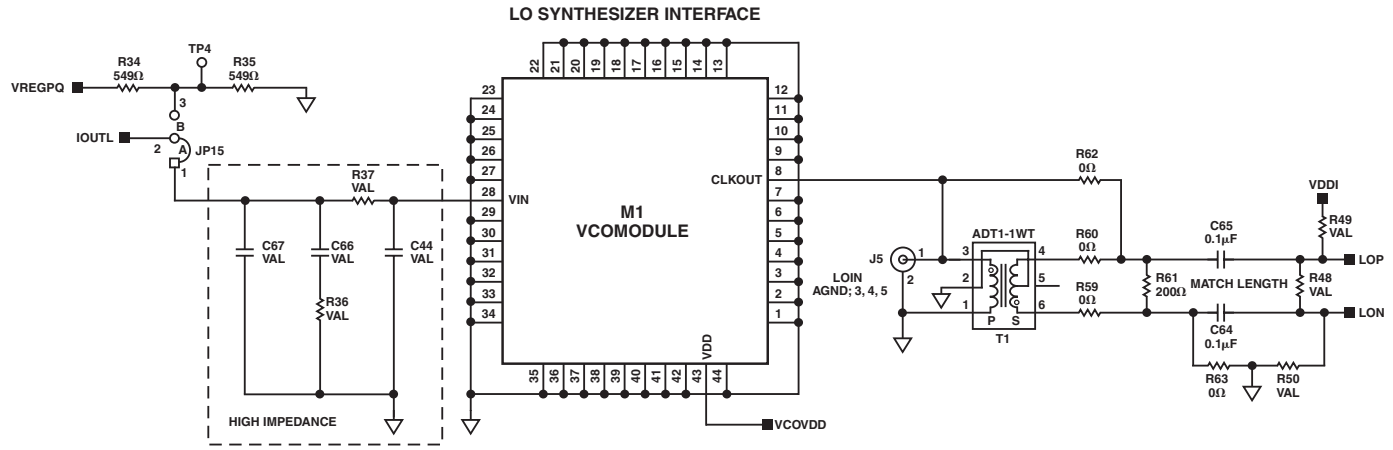


Figure 6b. CLK and LO Ext. Input/Synthesizer Interface

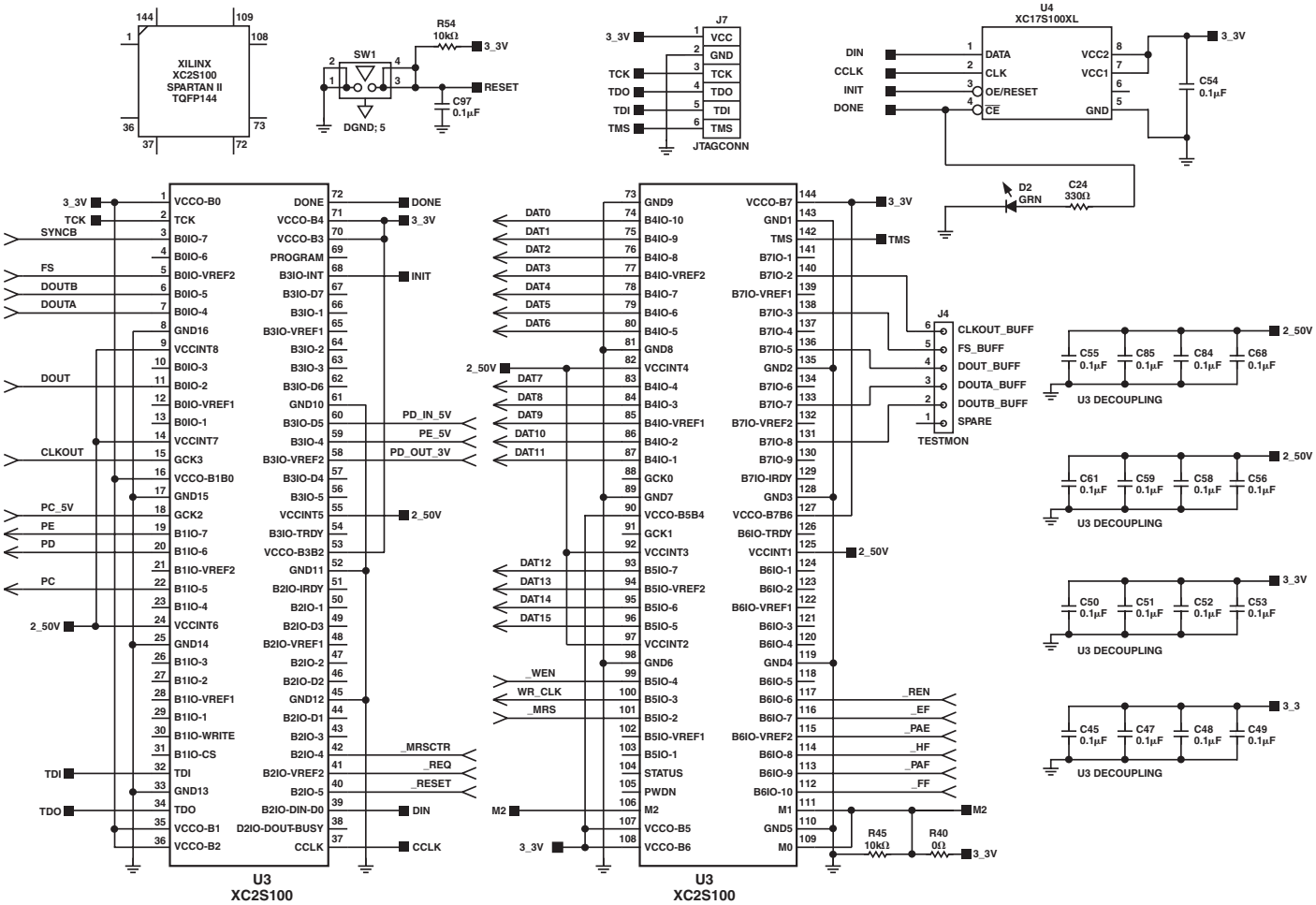


Figure 6c. FPGA

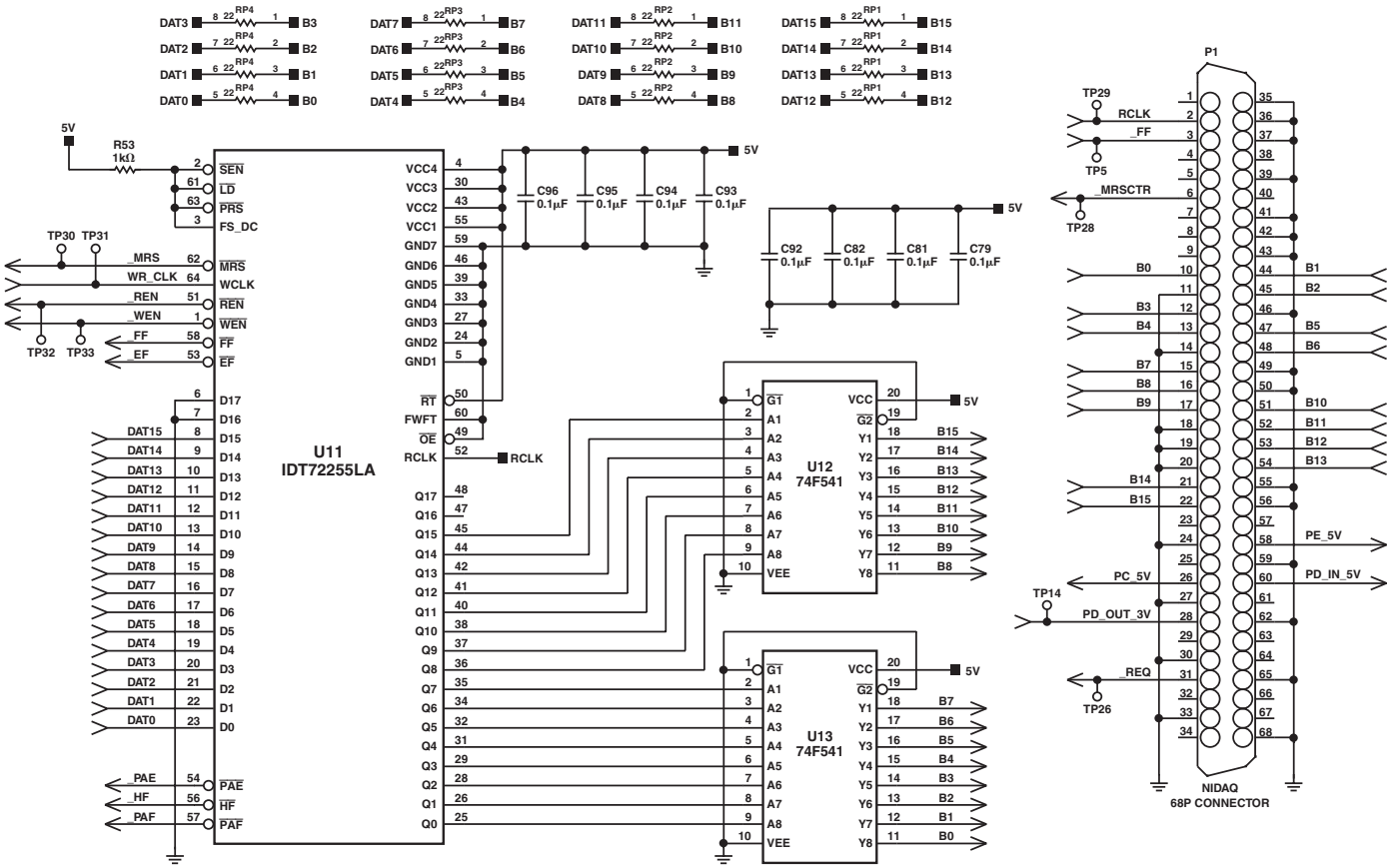


Figure 6d. FIFO, Line Drivers, and NIDAQ Connector

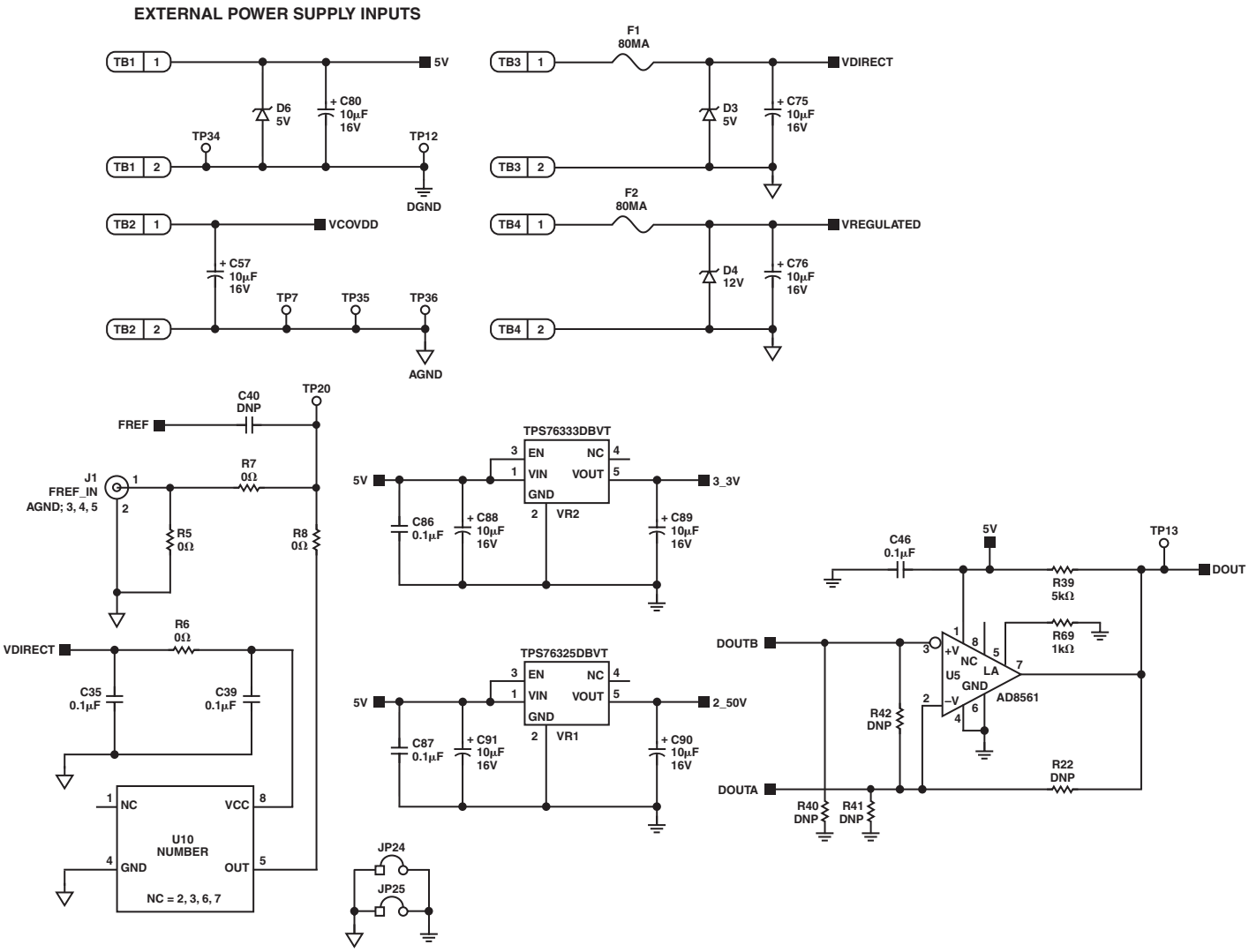


Figure 6e. Power Supply and FREF Inputs

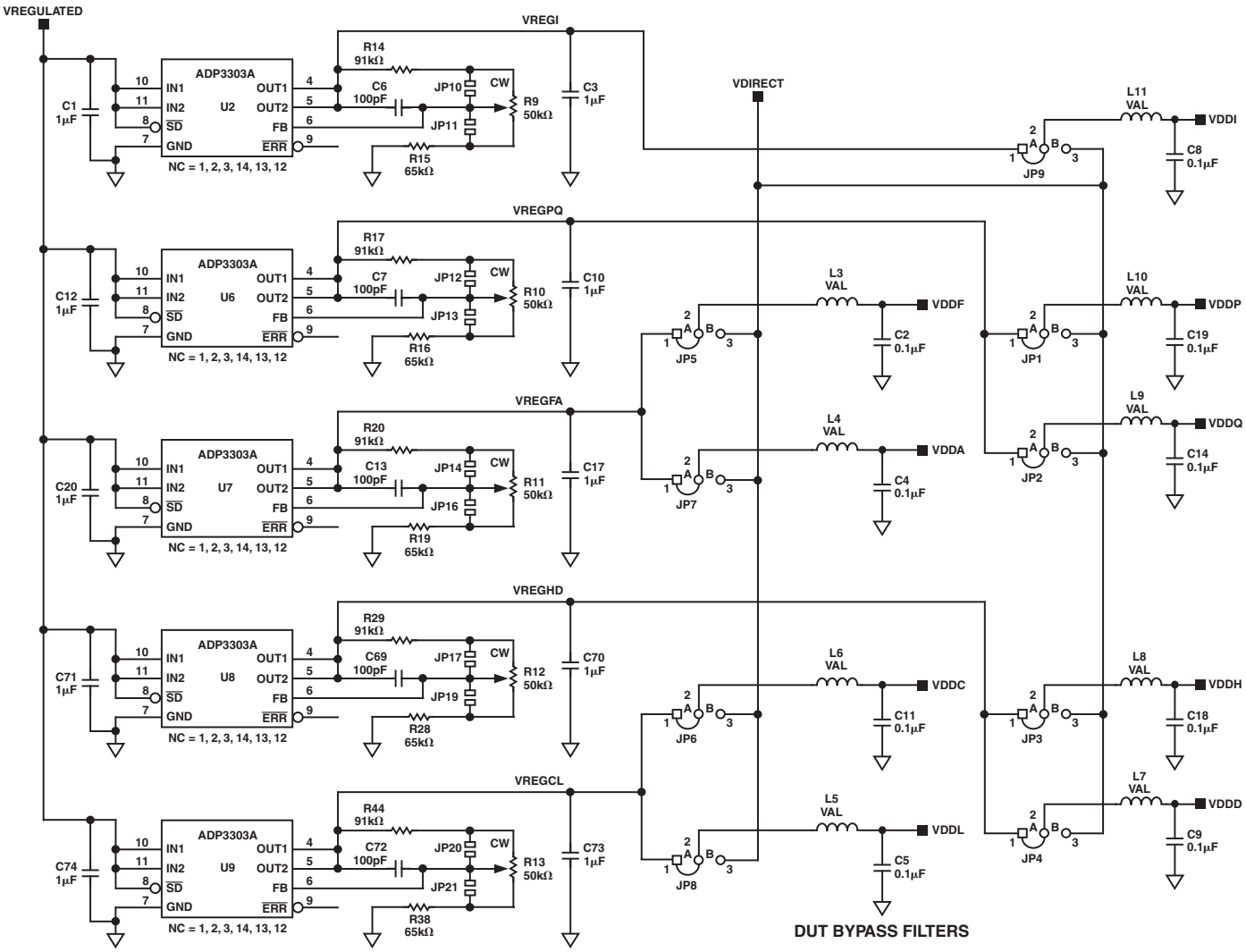


Figure 6f. AD9874 Power Supply Interface/Filtering

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